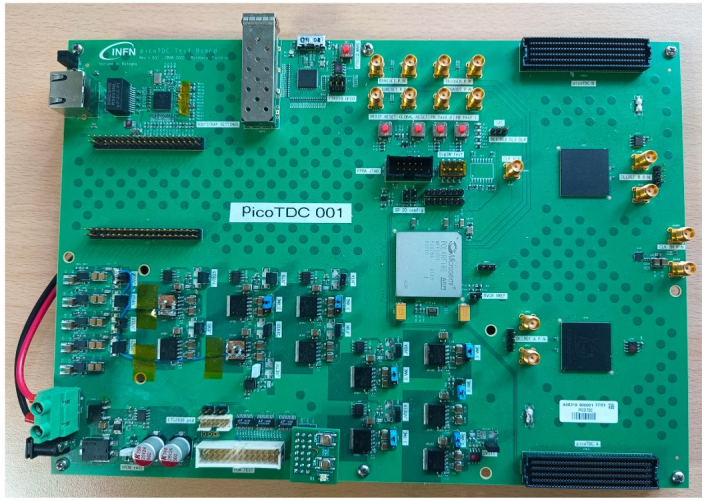
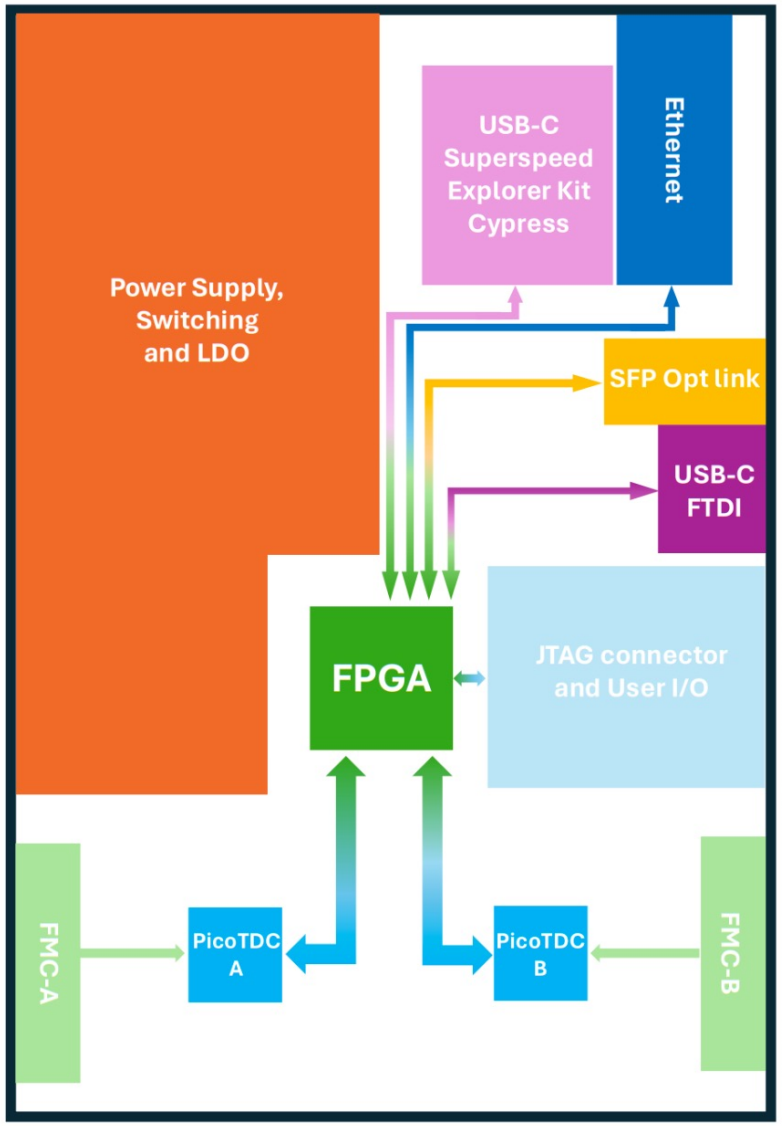
picoTDC Board (pBoard)

A reference DAQ for ALICE3 timing waiting for final electronics

P. Antonioli for the picoTeam (Casimiro, Davide, Marco, Jacopo, Sandro)



“open architecture” board



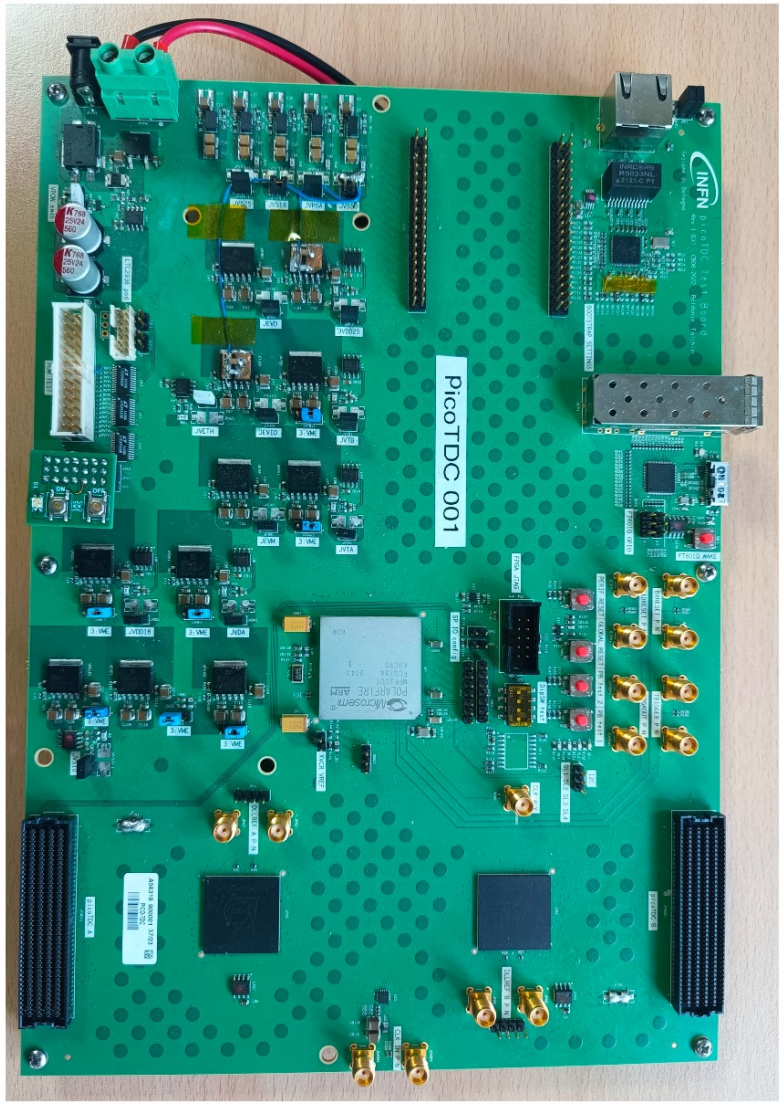


Figure 2: PicoTDC board designed at INFN Bologna. The Cypress Explorer Kit for

Design choices:

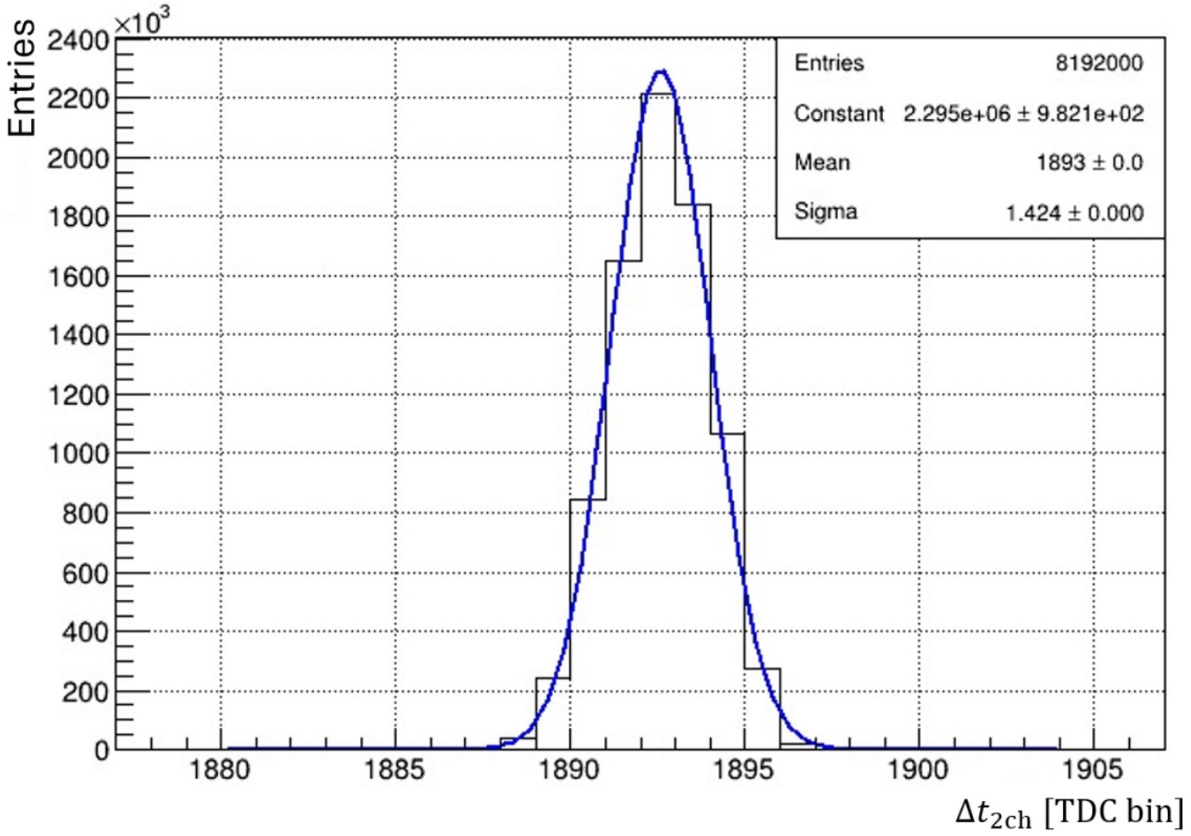
- test picoTDC choices towards ALICE TOF TRM2 design
- test PolarFire
- different interfaces (Eth, USB, SFP)
- exploit picoTDC resolution (3.05 ps LSB!)
- make no choice for pre-amp + discriminator (use for multiple applications) → FMC connector
- support 128 channels

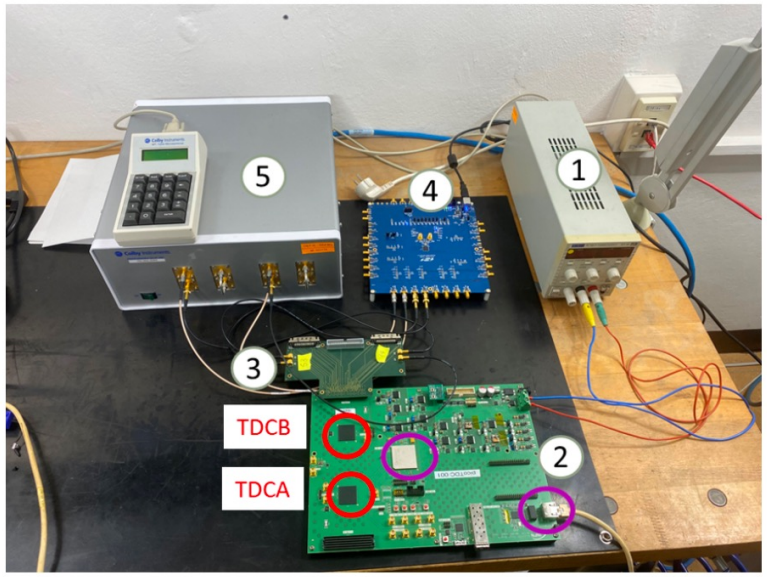
Currently implemented Eth interface using IPbus, USB is coming

Next test beam (June/July):
- use USB interface → Jacopo + Pietro/Davide

Lab tests of pBoard

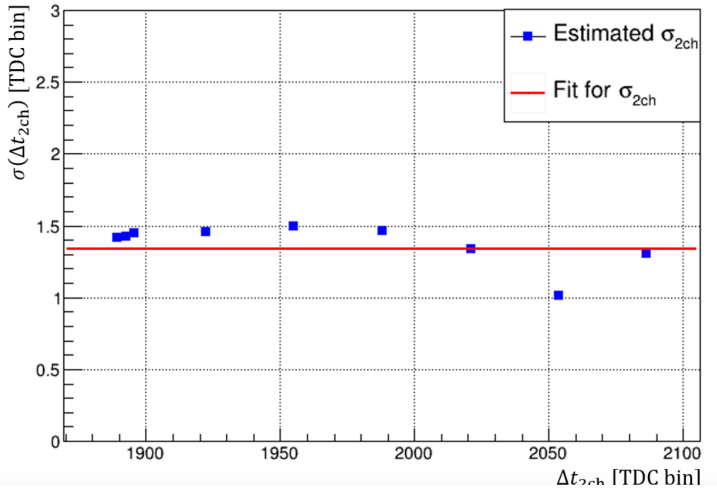
(arising from G. Zanasi bachelor thesis and S. Geminiani master thesis)





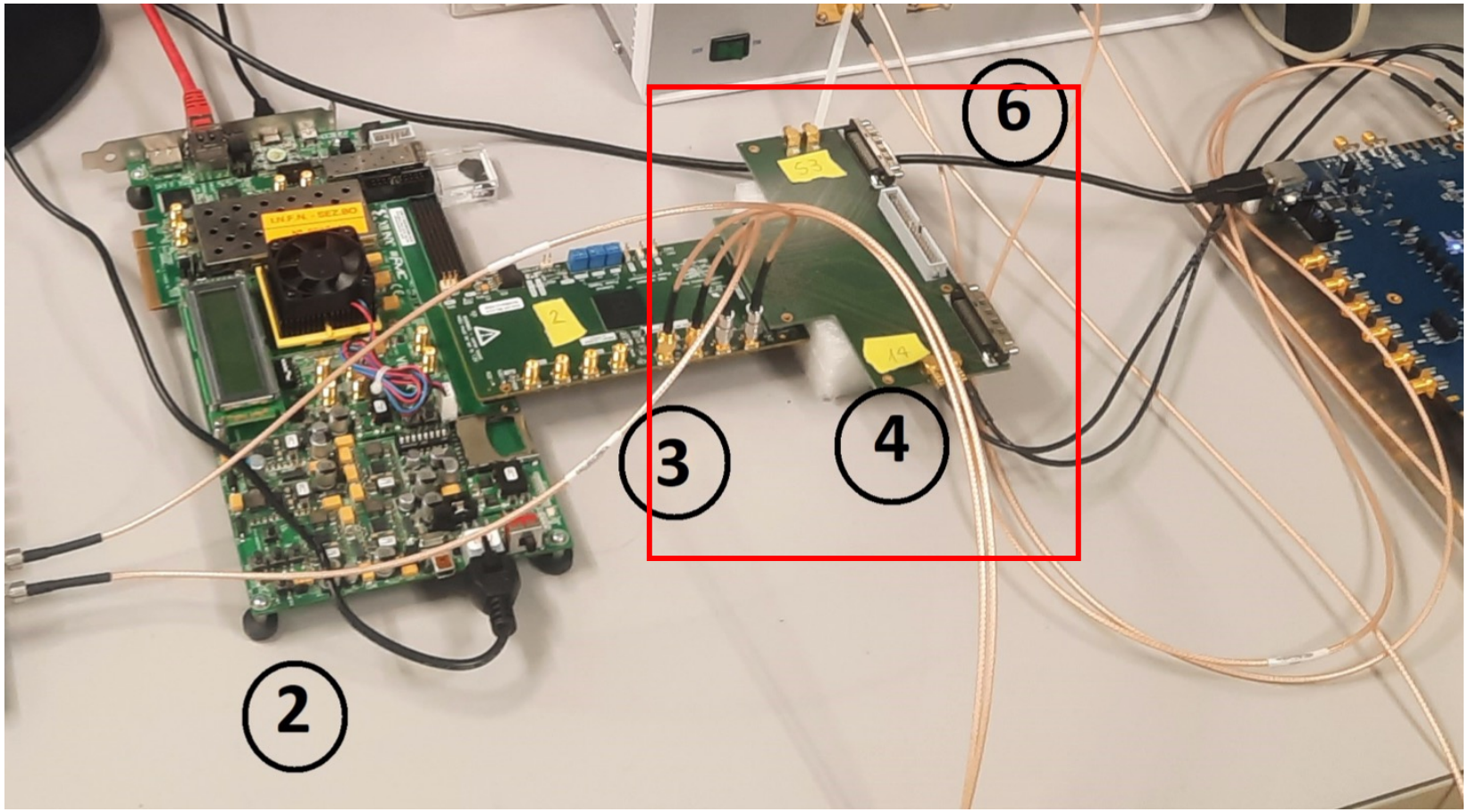
controlled delayed line with EM trombone

- Single channel resolution ~ 2.9 ps!
- All firmware done for I2C configuration, pTDC readout



PFEB-FMC concept

- PFEB: picoTDC Front End Board to house different adapters/amplifier/discriminator
- PFEB-FMC FMC form factor to get picoTDC inputs



First PFEB-FMC is just an adapter (**PFEB-A**):

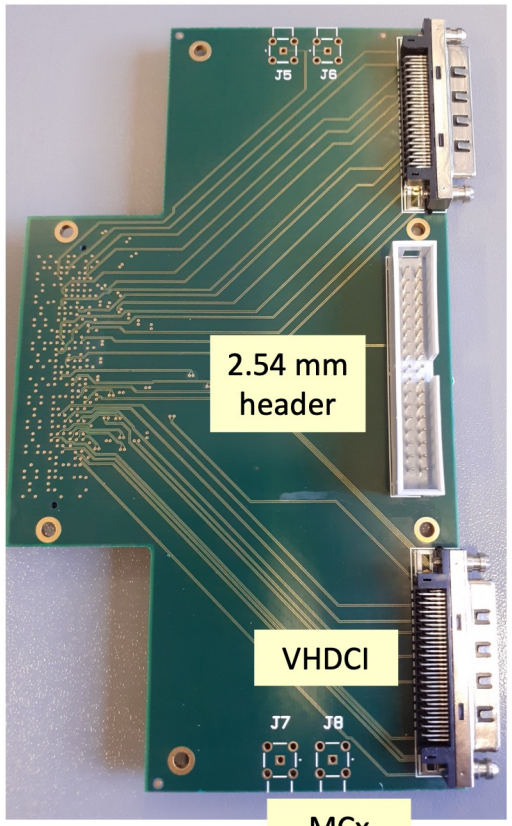
- 34 pins IDC connector
- 2 VHDCI connectors (for TOF use)
- 4 (2x2 diff. pairs) MCX connectors

It might be used to bring signals from MadPix to picoTDC but… we need sub-LVDS (see later on this)

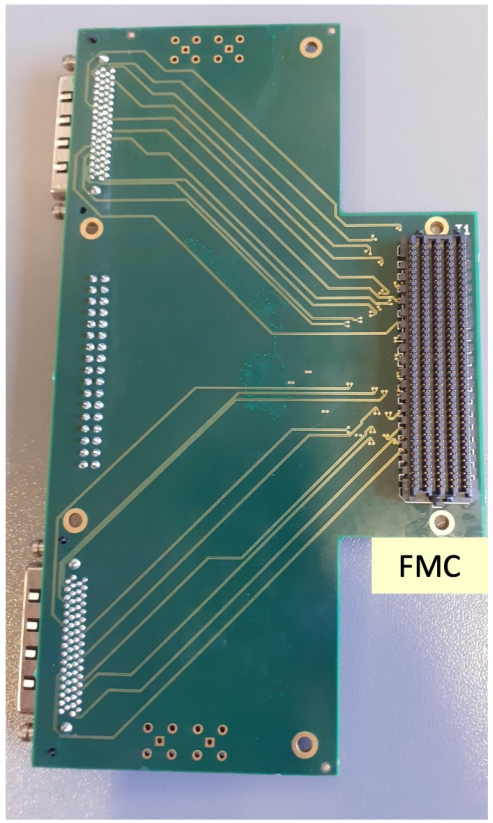
PFEB-FMC concept: PFEB-A

PicoTDC adapter board

top

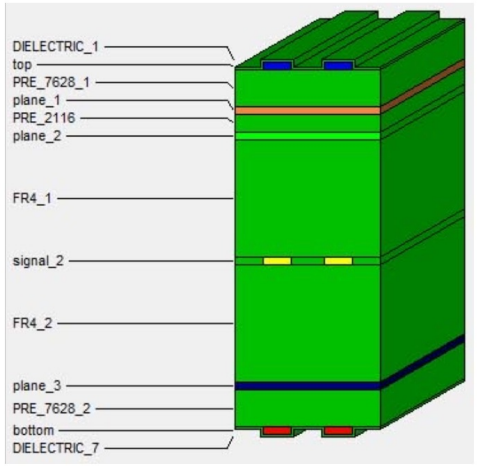


bottom



material: FR4
ε_r: 4.3
thickness: 1.6 mm

6 layers



FMC to VHDCI adapter board

PFEB-FMC concept: PFEB-L

- PFEB: picoTDC Front End Board to house different adapters/amplifier/discriminator
- PFEB-FMC FMC form factor to get picoTDC inputs

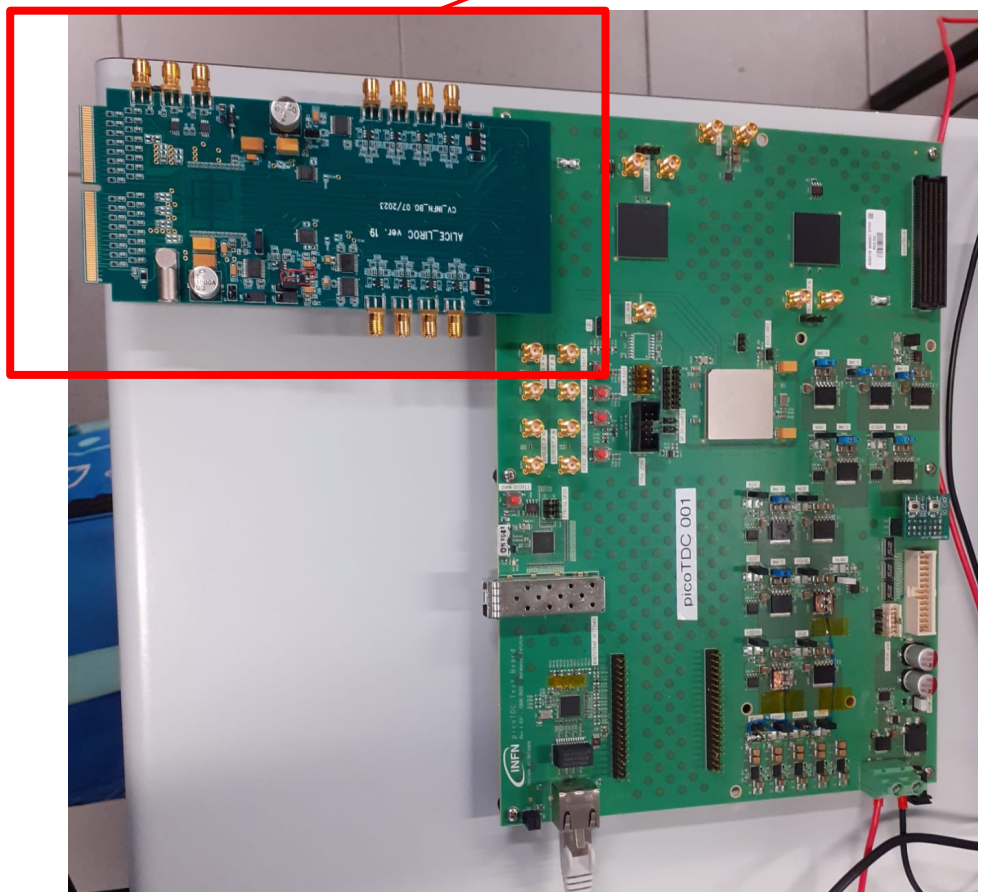
PFEB-L

LIROC PFEB-FMC

64 channels: 56 to picoTDC, 8 to scope

edge connector FERS (CAEN) compatible

Used @ April test beam



April test beam

This is a summary pBoard-oriented, not sensor-oriented

- Very minimal DAQ (TUI interface!), but proved robust
- Spill-oriented DAQ
- Trigger-oriented DAQ (latency/matching window)
- Plenty of space for improving interface for online analysis (Grafana, etc.) → not for June test beam
- QA already performing (kudos to Bianca/Sandro!)

DAQ operation documentation/mini-manual

Documentation for picoTDC board Test Beam operations

Login on alitopit0 host (DAQ machine)

Files for configuration of PicoTDC DAQ and data recording
LIROC Configuration (LIROC Server)
PicoTDC Configuration
How to manage the power cycle of the PicoTDC board every 4 hours

Run operations
- How to start a run
- Run monitoring utilities
  - spyLog
  - spyRun
  - spyPico
- How to stop a run

Run Data organization

Instructions for experts
- Start readout without starting a run
- Extreme DAQ reset
- Consolle monitor

QA Histograms and Root Tree

Network configurations

General info of the run

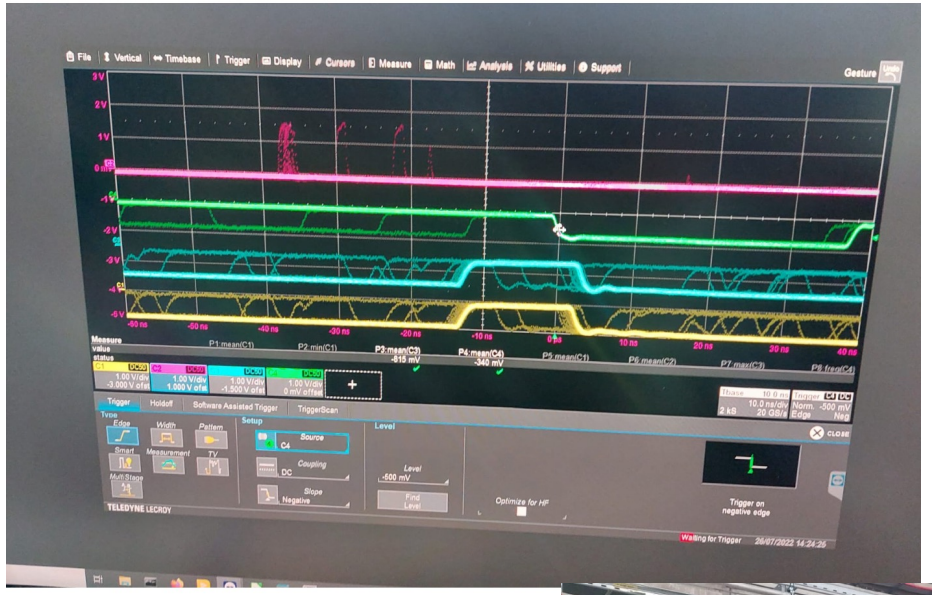
Info about stats collected during last spill

Info about stats collected during the whole run so far

```
------- PicoTDC Board Readout Status --- @ 27/04/2024-20:35:21
Run # 79 WAIT SPILL       SOR: 27/04/2024-20:33:45 EOR: 01/01/1970-01:00:00
Events | 00125607  | Buffers 00006812 | Ev/Buffer  18.4
Spill  | Uptime:  16.8 (s) | OFF | Off->On 007 | On->Off 007 |
Memory | Max FPGA buffer size  00007644 | Max hits/event 00000304
-- LAST Spill Stat --- Spill # 007 ----------------------------------------
Duration    2.40 (sec) Events: 18648 Ev. rate 2.400000 [KHz] |
PCI MEM 00320254 | FPGA MEM 000057 | Hit  0
[00] 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
[08] 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00011277
[16] 00000845 00000000 00000000 00000000 00000813 00000000 00000000 00000000
[24] 00000642 00000000 00000000 00002511 00009343 00008540 00003425 00005355
[32] 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00001695
[40] 00000000 00000000 00000000 00000000 00004960 00006825 00000000 00010975
[48] 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
[56] 00000000 00000000 00000000 00000000 00000000 00000000 00029272 00000000
-- All Run stat ----------------------------------------------------------
[00] 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
[08] 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00074911
[16] 00005147 00000000 00000000 00000000 00005187 00000000 00000000 00000000
[24] 00003908 00000000 00000000 00016065 00058101 00056496 00022125 00034597
[32] 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00010807
[40] 00000000 00000000 00000000 00000000 00031800 00044124 00000000 00072096
[48] 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
[56] 00000000 00000000 00000000 00000000 00000000 00000000 00199204 00000000
MULT:     0     1     2     3     4     5     6     7     8     9    10
     24099 33861 39415 20671 04208 00977 00719 00581 00288 00140 00120
```

from test beam…

trigger setup (LGAD in position L4)



- latency 650 ns
- matching window 250 ns
- spill window kept large (2.3 s) as per PS signal, can be optimized (down to 600 ms)

PFEB – FMC LIROC lessons learned

- LIROC is born for SIPM
- LGAD signals not easily handled by LIROC
- very difficult to operate LIROC with two different input polarity signals (SiPM and LGAD)
- performance of a system LIROC+pTDC ?
  - Weeroc measured 58 ps on a “similar” chain HPK 13360+LIROC+picoTDC (but this is SPTR) See T. Saleem at picoTDC Users meeting (”Combining picoTDC with Weeroc ASICs for space applications”)
  - eagerly waiting for analysis (but at TB we were able to be quickly down to 70 ps .. good start)

Next test beam (June/July):
- use 2 LIROC PFEB, one devoted to LGAD only, one for SiPM only
- second LIROC card needs reworking → Daniele
- software for configuration and data taking to be updated → Pietro/Daniele/Bianca

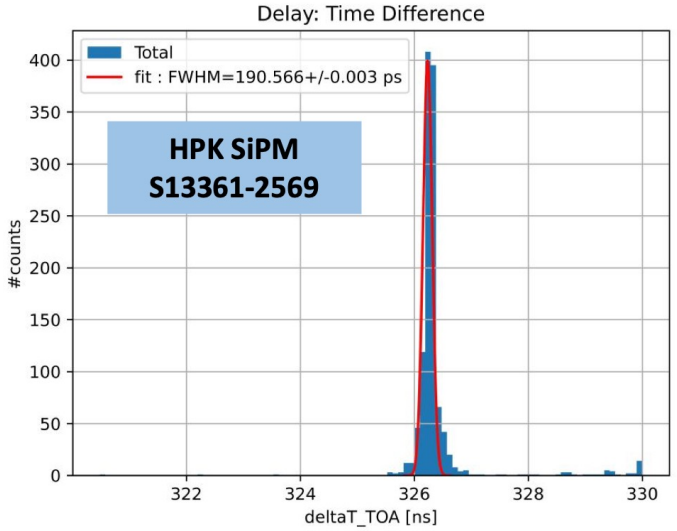
again on LIROC

Liroc-picoTDC system: Improved time resolution (SPTR)

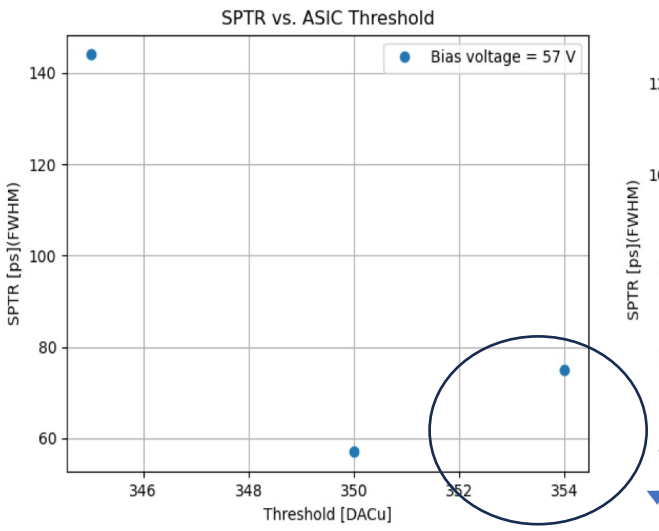
T. Saalem/WEEROC

HPK SiPM S13361-2050NE-08

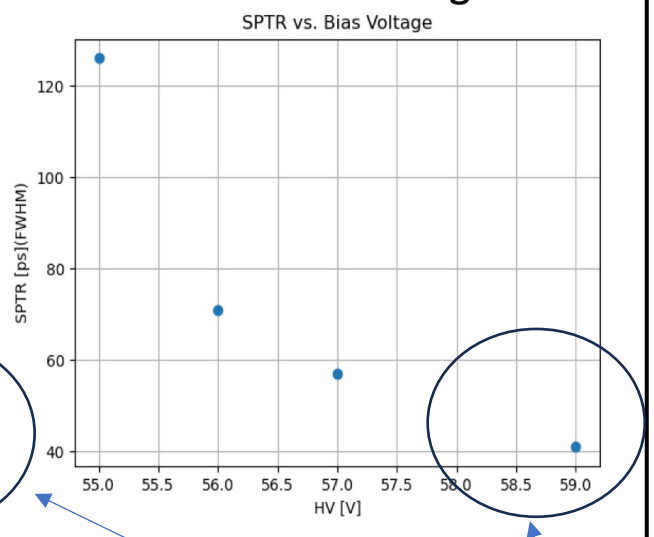
TOA Distribution



SPTR vs. Threshold

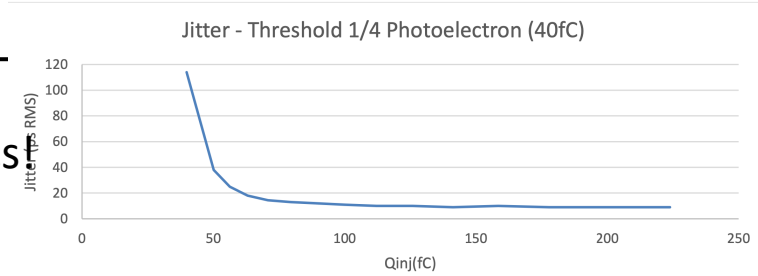


SPTR vs. Bias Voltage



→ TOA measurement: best SPTR HPK S13361-2569 is 191 ps (FWHM) at 57 V .

→ Improved SPTR for a standard HPK S13361-2050NE-08: 58 ps (picoTDC) compared to 167 ps.



we might stay here with thr>4 nphe…
close to 30 ps…

Remember LIROC specs:

PFEB – FMC: a generic discriminator for pBoard

main idea: have a PFEB capable to deal with analog (post-amplification) signal → **PFEB-D**

ANALOG DEVICES

Ultrafast 3.3 V/5 V Single-Supply SiGe Comparators

Data Sheet **ADCMP572/ADCMP573**

FEATURES

- 3.3 V/5.2 V single-supply operation
- 150 ps propagation delay
- 15 ps overdrive and slew rate dispersion
- 8 GHz equivalent input rise time bandwidth
- 80 ps minimum pulse width
- 35 ps typical output rise/fall
- 10 ps deterministic jitter (DJ)
- 200 fs random jitter (RJ)
- On-chip terminations at both input pins
- Robust inputs with no output phase reversal
- Resistor-programmable hysteresis
- Differential latch control
- Extended industrial −40°C to +125°C temperature range

FUNCTIONAL BLOCK DIAGRAM

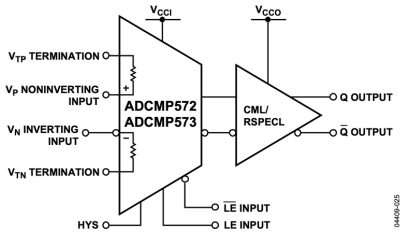
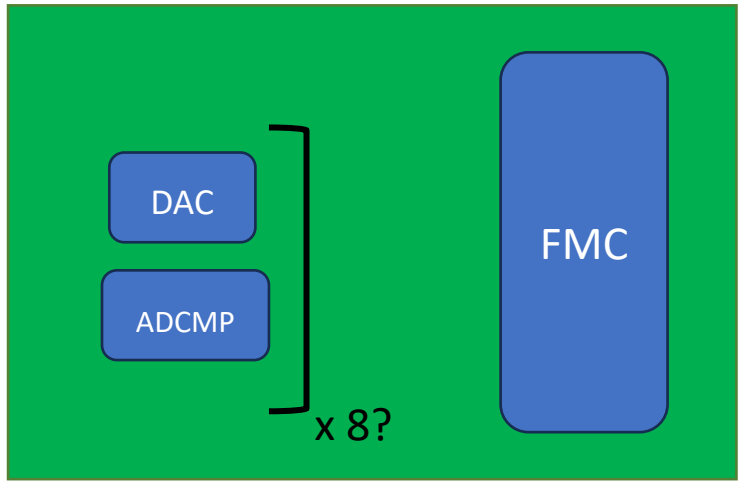


Figure 1.

target comparator: ADCMP573
PECL outputs → sub-LVDS
LFSCP package 3x3 mm
→ power consumption to be checked (not 64 channels…)
→ need to design carefully input stage
→ LGAD signal specs (post-amp) → Sofia
→ need to select a DAC (I2C or SPI controlled via picoBoard
→ TOT?

bottom



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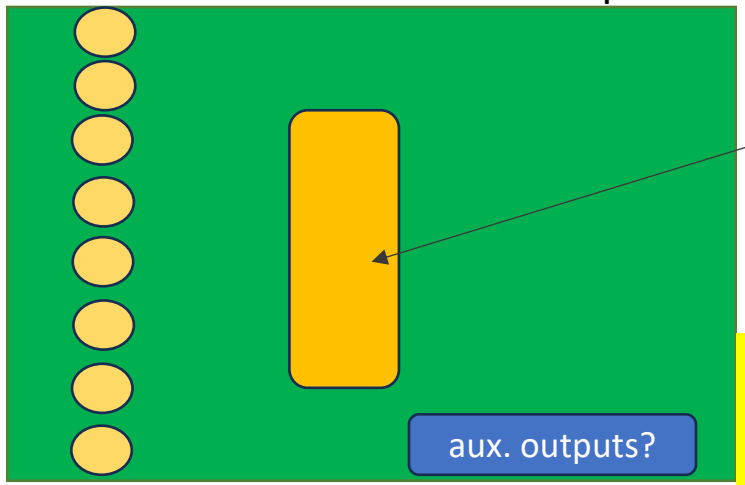


8 SMA connectors for analog input (single-ended)

- aux. diff. inputs to be routed to picoTDC directly (SMA/MCX/IDC?)
- we might have also some channels for LVDS-SLVDS adaptation
- aux. outputs for triggering

Asked resources at Electronic Workshop @BO
Unlikely but not impossible we can do it by October, if not… for next year.
It should replace “second Liroc card”, to be used with LGAD

Side note on CMOS-LGAD test with pBoard

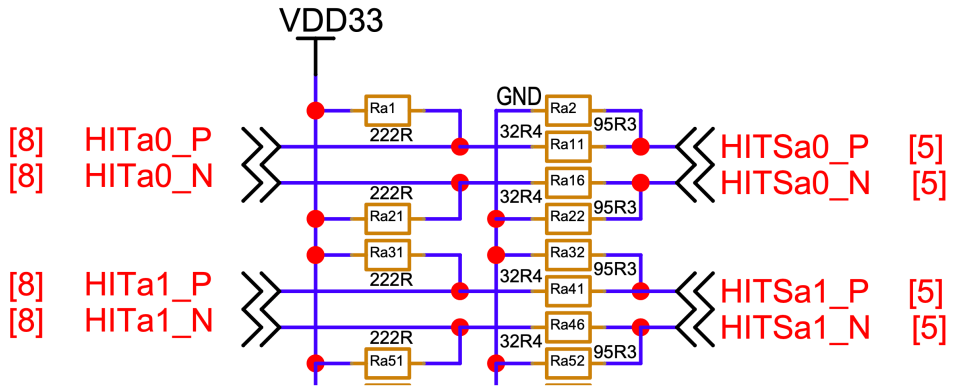
- Turin group provides CMOS-LGAD using MadPix board.

  Two outputs:

  ➢analog → can go to LIROC → can go to pBoard

  ➢digital → LVDS → need to be adapted to Sub-LVDS

Reference AN (from TI): Interfacing LVDS Driver With a Sub-LVDS Receiver



Input stage design for ALICE TOF TRM2 (tx Casimiro!)
Net resistors with 222, 32.4 and 95 Ω plus 3.3V/GND

If Turin group interested to use pBoard on CMOS-LGAD:
→ for analog we keep using LIROC card
→ for analog we could then use PFEB-D → specs!!!
→ for digital
a) make a PFEB just with resistors net (the closest point to picoTDC receivers
b) make the net between MadPix IDC output and IDC on PFEB-A (“accrocchio”)

Miscellanea & Outlook

- late in 2024 (or in 2025) we might consider an additional production (Rev2) of pBoard and PFEB-L fixing some mistakes. Some groups interested? [consider for INFN “preventivi”]
- pBoard might be good basis for ALICE3/timing TB until we have full-fledged CMOS-LGAD (good re-use of ALICE-TOF funding)
- need to agree plan for MadPix + CMOS-LGAD in June/July
- design additional PFEB need interaction with LGAD and CMOS-LGAD experts

the picoTeam is very happy to finally contribute to ALICE3!