dRICH: ALCOR ASIC

Fabio Cossio on behalf of the Torino group

Riunione EIC_NET - referee INFN

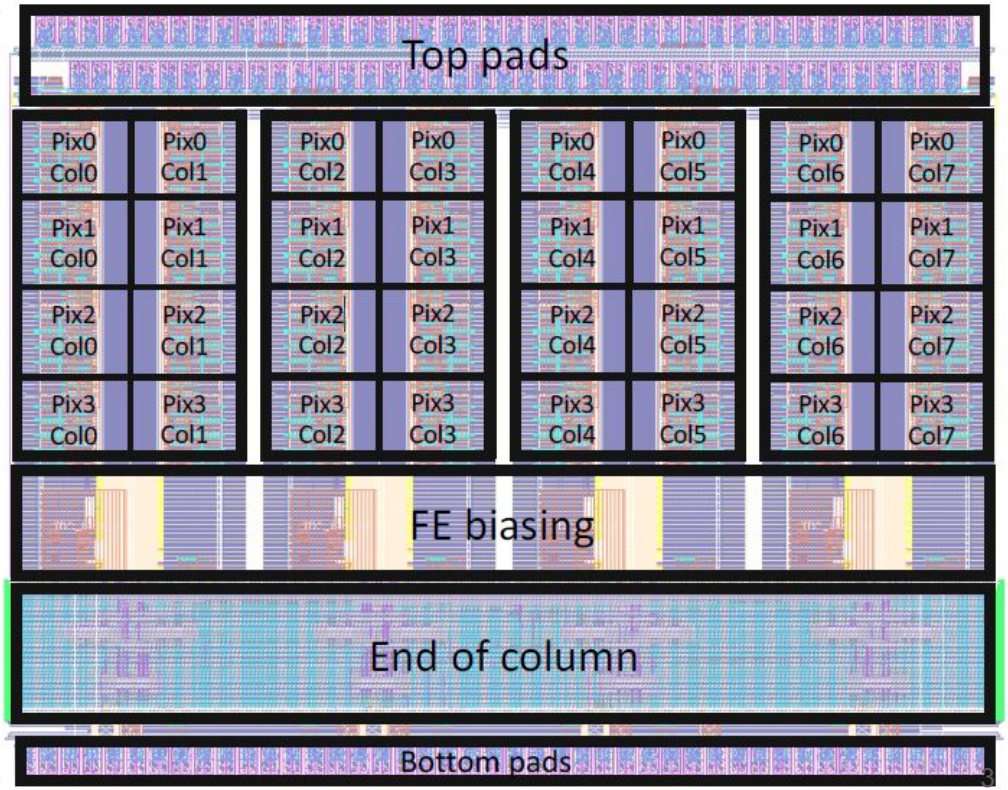
Bologna - 31.08.2023

Introduzione

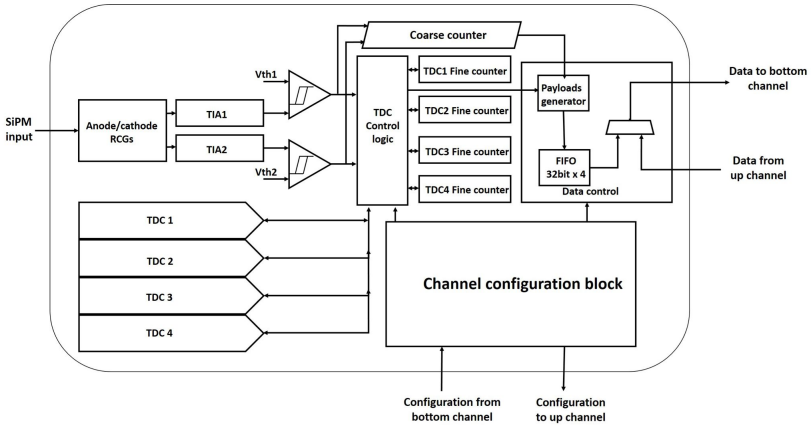
ALCOR (**A** **L**ow Power **C**hip for **O**ptical Sensor **R**eadout)

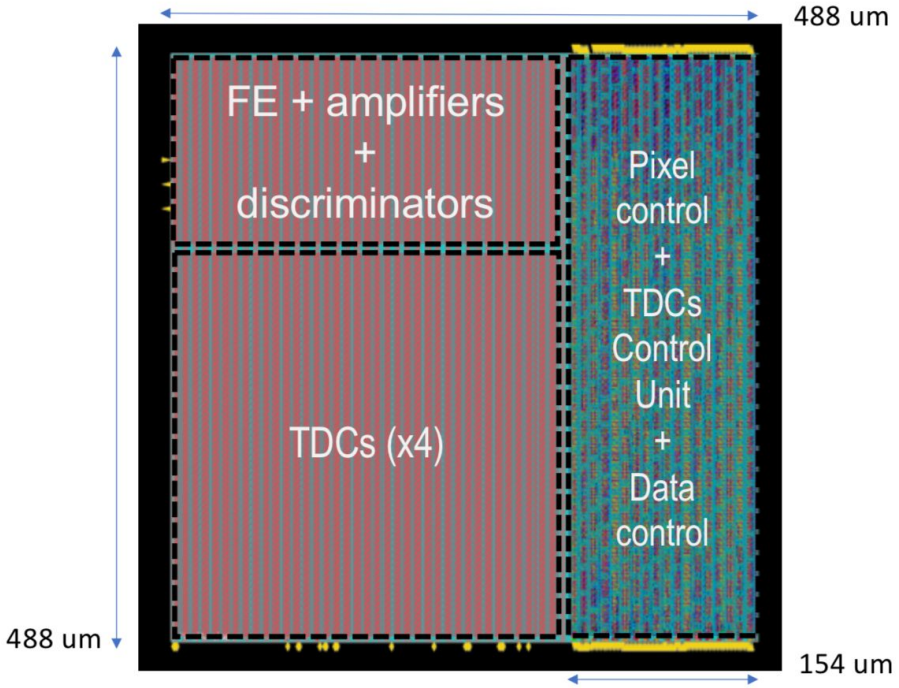
ASIC developed for the readout of the EIC dRICH SiPM sensors

- **32-pixel** matrix (8x4) mixed-signal ASIC
- **SiPM readout**: single-photon time tagging + Time-over-Threshold measurement
- 32-bit (64-bit in ToT mode) event word generated on-pixel and propagated down the column
- **Fully digital output**: 4 LVDS 320 MHz DDR Tx links



Pixel architecture



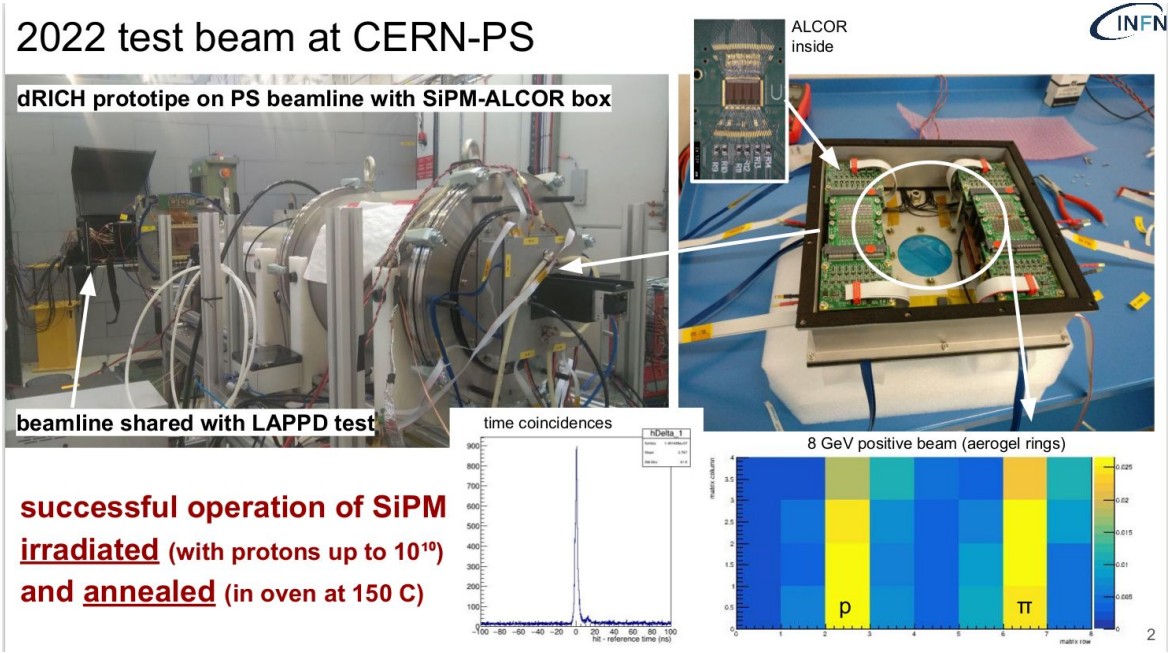


- TIA amplifier with RCG input stage
- 2 independent post-amp branches with 4 gain settings
- 2 leading edge discriminators with independent (and per pixel) threshold settings (6-bit DAC)
- 4 TDCs based on analogue interpolation with 25-50 ps time-bin (at 320 MHz clock frequency)
- Pixel control logic handles TDC operation, pixel configuration and data transmission

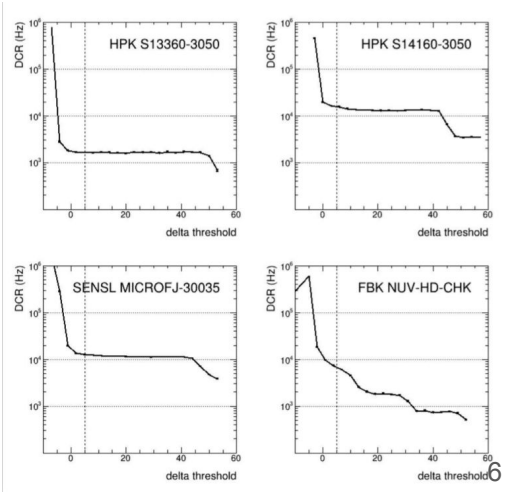
Attività
Settembre 2022 - Agosto 2023

ALCOR v1

- Developed for the readout of SiPMs at 77K, in the framework of Darkside (MPW, Dec 2019)
- Extensively used within the EIC dRICH Collaboration in the last 2 years



Slides from R. Preghenella



ALCOR v2

ALCOR v2

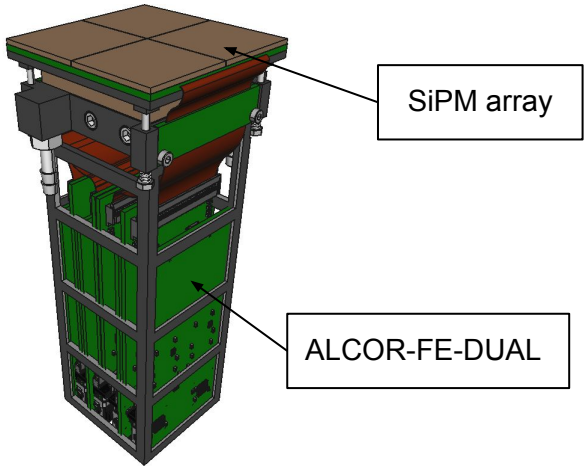
- MPW, submitted in Dec 2022
- 60 chips, received in June, promising results from preliminary tests
  - ✓ TDC logic critical error at high rates solved also for DCR rate at room temperature
  - ✓ New FE gain settings more suited for single photon applications
  - ✓ On-chip test-pulse also for EIC SiPM polarity
  - ✓ Special words from EoC (header, frame, CRC) ok also when status words are disabled

ALCOR v2.1

- INFN internal engineering run
- Submitted in Mar 2023, wafers delivered, dicing ongoing
- High number of chips will be available
- Removed TDC logic bugs (TFine-clock ambiguity, TOT orphans due to fake trigger at very low rates)

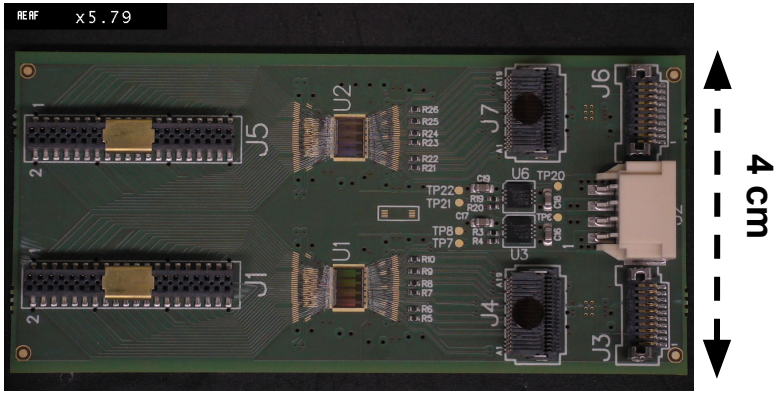
ALCOR 2023 readout system

Prototype photodetector unit (PDU)

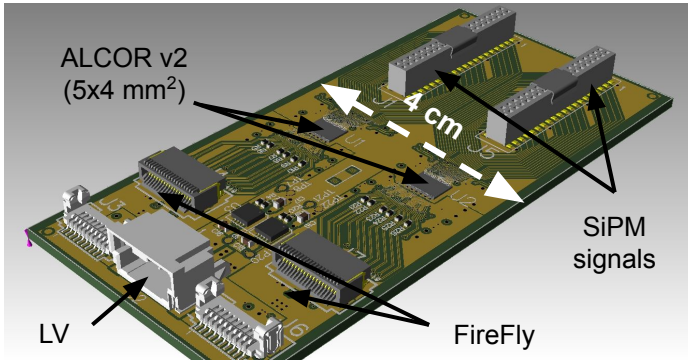


ALCOR-FE-DUAL

- Two **32-channel** ALCOR v2 ASICs **wire-bonded** on the PCB
- 4 ALCOR-FE-DUAL boards for each PDU
- This system will be used for 2023-2024 beam tests



designed by INFN Torino (Marco Mignone)



Attività e Richieste 2024

ALCOR v3

- **64-channel** version with shared digital signals and **BGA package** (~256 IO pins)
- Revise **ALCOR FE** design to improve time resolution and rate capability of the SiPM+ALCOR system
  - Studies on SiPM capacitance and optimal coupling with ALCOR (AC coupling inside ALCOR)
  - Increase amplifier bandwidth
  - Improve response for afterpulses and re-triggering (hysteresis discriminator)
- **Digital logic** bug fix and new features
  - TDC logic fix to remove orphans due to re-triggering of events very close in time
  - Increase EoC FIFO size to cope with higher data rates
  - **Digital shutter** for data reduction (EIC bunch crossing: 10 ns → 1-2 ns time window)
- Operation of ALCOR with multiple of EIC clock frequency (98.52 MHz): 295.56 MHz or **394.08 MHz**
  - First tests on ALCORv1 at 390 MHz look promising but more detailed tests and simulations are required, digital implementation must be re-done with new constraints

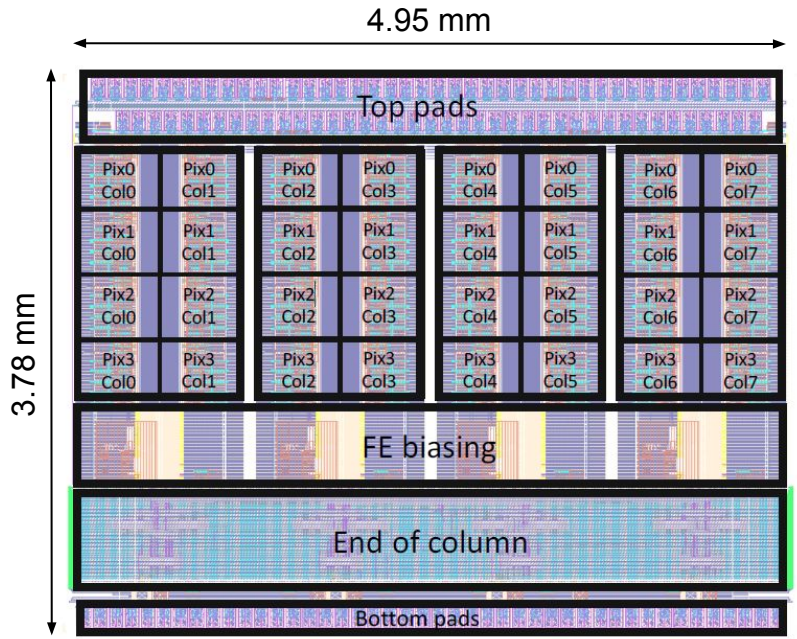
ALCOR I/Os

ANALOGUE (top, 44+38=82)

- 16 AVDD + 4 AVDD_IO
- 16 AGND + 4 AGND_IO
- 4 AVSS
- 32 inputs
- 4 debug outputs
- 2 bias Vref

DIGITAL (bottom, 20+24=44)

- 6 DVDD + 2 DVDD_IO
- 6 DGND + 2 DGND_IO
- 4 DVSS
- 2 clk, 2 reset, 2 test-pulse
- 8 Tx outputs
- 2 clk_out
- 8 SPI

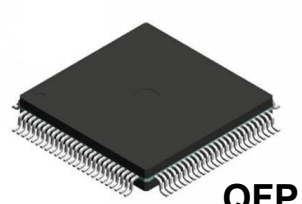


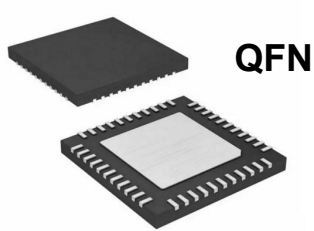
ALCOR current version has 32 channels and 126 I/Os

ALCOR v3: targeting a **64-channel** version with **~256 I/Os**
(Area: ~6.8 x 5 mm^2, MPW blocks are 5 x 5 mm^2)

ALCOR packaging

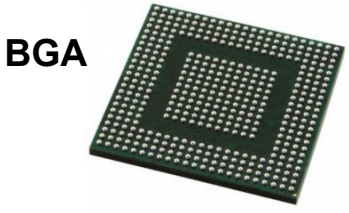
Standard packaging (QFP, QFN) is cheap but provides low number of pins and large area, which is not suitable for the implementation of the 64-channel ALCOR



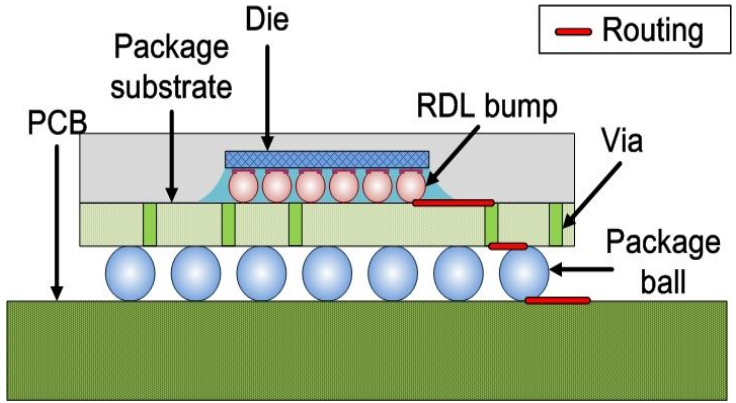


Ball grid array (BGA) package

Inside the package, the chip is flipped so that the active side of the device is bump-bonded to the package substrate



- The whole bottom surface of the device can be used, not just the perimeter
- More interconnection pins wrt QFP or QFN
- Shorter interconnections reduce inductance, allow high-speed signals and carry heat better



ALCOR packaging

Standard packaging (QFP, QFN) is cheap but provides low number of pins and large area, which is not suitable for the implementation of the 64-channel ALCOR

La definizione delle specifiche di ASIC e package è necessaria per portare avanti le discussioni con le aziende che forniscono i servizi di packaging

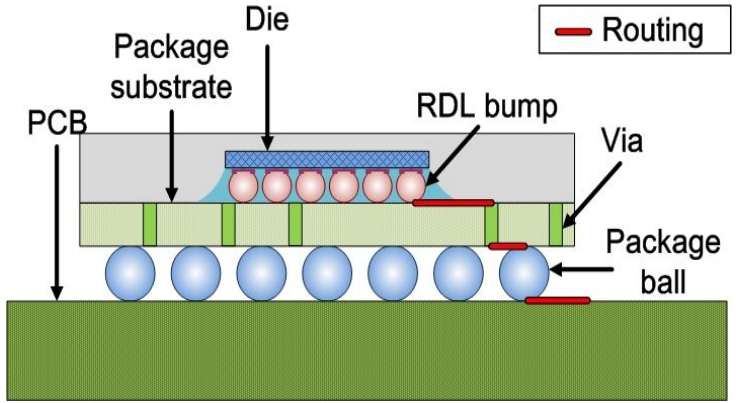
Ball grid array (BGA) package

Inside the package, the chi
side of the devi
substrate
age

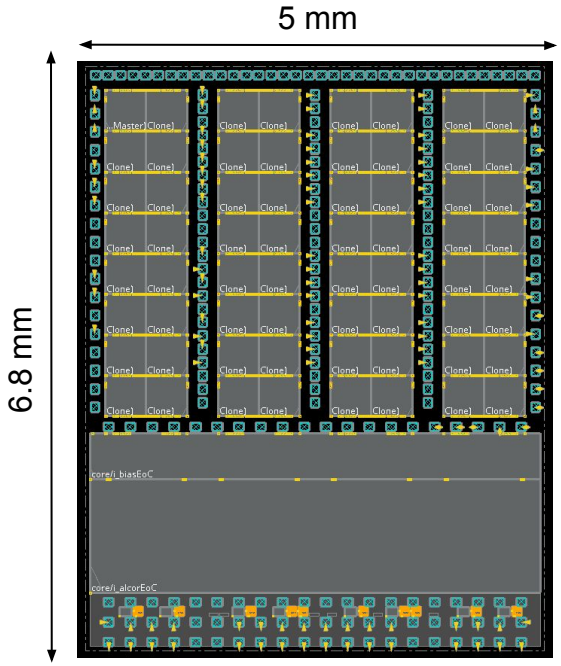
or the device can be used, not

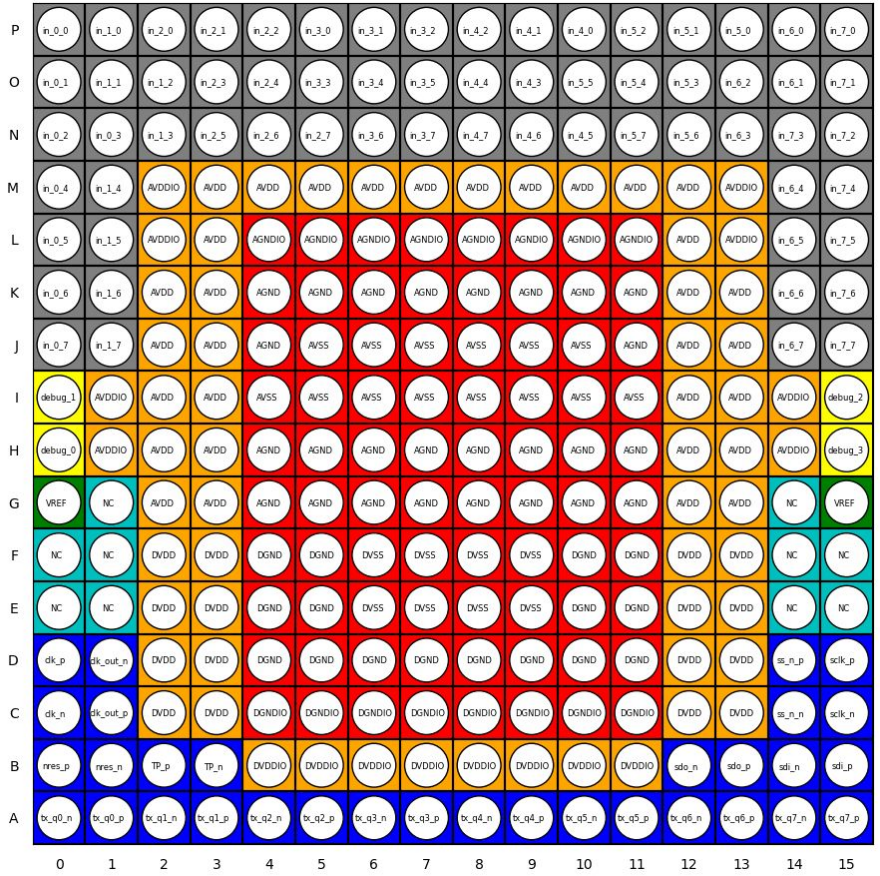
erconnection pins wrt QFP or QFN

Shorter interconnections reduce inductance, allow high-speed signals and carry heat better



ALCOR v3 floorplan





8x8 pixel matrix ASIC (64 channels)

- SiPM inputs bump pads between the pixel sectors
- Digital EoC in the bottom part

256 balls BGA package

- Power and ground on inner/mid contacts
- I/O on outer contacts

Richieste 2024 (Torino)

Descrizione	Richieste	SJ
Sottomissione Multi Project Wafer (MPW)		75
Packaging ALCOR-64		100
ALCOR Front End Board (FEB)	8	

Obiettivo: test beam nella prima metà del 2025 per testare sensori e elettronica nel layout finale

Necessario sviluppo per sottomissione MPW ALCOR v3 entro la metà del 2024. Concomitante alla sottomissione del MPW è la preparazione del package BGA e della scheda FEB (Front-End Board) dove montare i chip in package

ALCOR v3 MPW

UMC MPW Pricelist	Standard EUR / block	Discounted EUR / block
UMC L180 Logic GII, Mixed-Mode/RF	19,000 [1]	18,060 [1]
UMC L110AE Logic/Mixed-Mode/RF	34,800 [1]	33,060 [1]
UMC L65nm Logic, Mixed-Mode/ RF – LL/SP	50,600 [2]	48,080 [2]
UMC 55N Logic/Mixed-Mode/RF – SP	45,425 [2]	43,171 [2]
UMC 40N Logic/Mixed-Mode – LP	98,050 [2]	93,160 [2]
UMC 28N Logic/ Mixed-Mode – HPC	On request. Please, contact epumc@imec.be	

nel 2022 era 28,911

Important notes:

[1] Price = per block of 5mm x 5mm needed to fit the design in.

[2] Price = per block of 4mm x 4mm needed to fit the design in.

https://europractice-ic.com/schedules-prices-2023/

MPW da 6.8 x 5 mm^2 richiede 2 blocchi da 5 x 5 mm^2 → 33,060 EUR x 2 = 66,120 EUR + IVA = 80,666.4 EUR

RICHIESTA: 75k EUR SJ → richiesta sblocco alla finalizzazione del design di ALCOR v3 (metà 2024)

ALCOR v3 BGA package (offerta 1)

Offerta preliminare: contatti avviati a giugno per la definizione delle specifiche di base, necessario ulteriore tempo per soddisfare le loro richieste di informazioni per definire meglio l'offerta

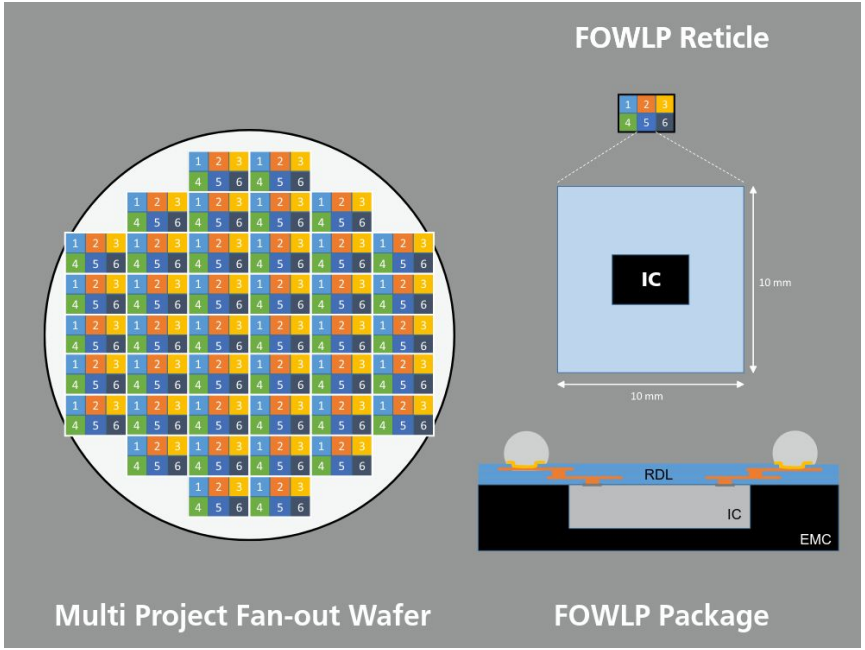
- **6 layer** per il substrato potrebbero essere non necessari
- Offerta per **80 pezzi**, la quotazione per il run della produzione di massa non ancora disponibile (necessaria prima la finalizzazione delle specifiche)

Preliminary

1. Design + simulation: USD 36,000.00
   * Substrate design: Up to 6 layers, 12 x 12 mm
   * Leadtime: 2 to 3 weeks
   * Simulation (5 to 6 weeks):
   * SI for digital pins, leadtime: 2 to 3 weeks
   * Electrical-Thermal, leadtime: 2 to 3 weeks
2. Substrate fabrication lot charge: USD 20,000.00
   * 6 layers substrate, 12 x 12 mm
   * Qty: 100 pcs
   * Include Open/Short test
   * Leadtime: 6 to 8 weeks
3. Assembly + packaging lot charge: USD 38,000.00
   * Qty: up to 80 pcs
   * Include assembly stencil, jig and fixture, open cavity mold, etc
   * Blind build
   * Deliver in single up pack in tray
   * Leadtime: 6 to 8 weeks
4. Total project cost: USD 94,000.00 (estimate 24 weeks)

ALCOR v3 BGA package (offerta 2)

MULTI-PROJECT FAN-OUT WAFER LEVEL PACKAGING: service provided by **Fraunhofer** and accessible for all **EUROPRACTICE** customers



- Die delivery: WafflePack, wafer, wheel
- Die size: 1.5 – 7 mm edge length
- Die thickness: 200 – 300 µm
- Package thickness: 450 µm
- Package size: 10x10 mm², smaller package size possible with extra effort
- Metal layers: 2
- Integration of e.g. antennas and passive structures in RDL
- Pin-out: BGA
  - Pitch: 500 µm
  - Ball size: 300 µm
  - Solder: SnAgCu
- Defined packaging materials

https://europractice-ic.com/services/system-integration/wafer-level-services/

ALCOR v3 BGA package (offerta 2)

MULTI-PROJECT FAN-OUT WAFER LEVEL PACKAGING: service provided by **Fraunhofer** and accessible for all **EUROPRACTICE** customers

Offerta preliminare:

- packaging del MPW di ALCOR: **25k EUR**
- packaging della produzione finale di ALCOR: **75k EUR**

Contatti in corso con Fraunhofer per **verificare se questa soluzione si adatta alle nostre richieste** e per **definire il costo finale**

- Die delivery: WafflePack, wafer, wheel
- Die size: 1.5 – 7 mm edge length
- Die thickness: 200 – 300 µm
- Package thickness: 450 µm
- Package size: 10x10 mm², smaller package size possible with extra effort
- Metal layers: 2
- Integration of e.g. antennas and passive structures in RDL
- Pin-out: BGA
  - Pitch: 500 µm
  - Ball size: 300 µm
  - Solder: SnAgCu
- Defined packaging materials

https://europractice-ic.com/services/system-integration/wafer-level-services/

ALCOR v3 BGA package

RICHIESTA: 100k EUR SJ

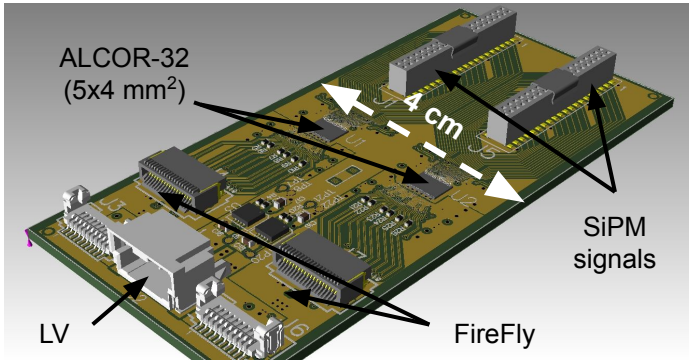
- Richiesta sblocco alla finalizzazione del design del package (metà 2024)
- Indagini di mercato in corso per trovare la soluzione migliore e possibilmente richiedere lo sblocco di una cifra inferiore
- 100k EUR inclusivi anche della scheda socket per testare chip in package pre-assemblaggio su FEB

ALCOR v3 board

Produzione schede Front-End Board (FEB) dove montare gli ALCOR v3 in package BGA

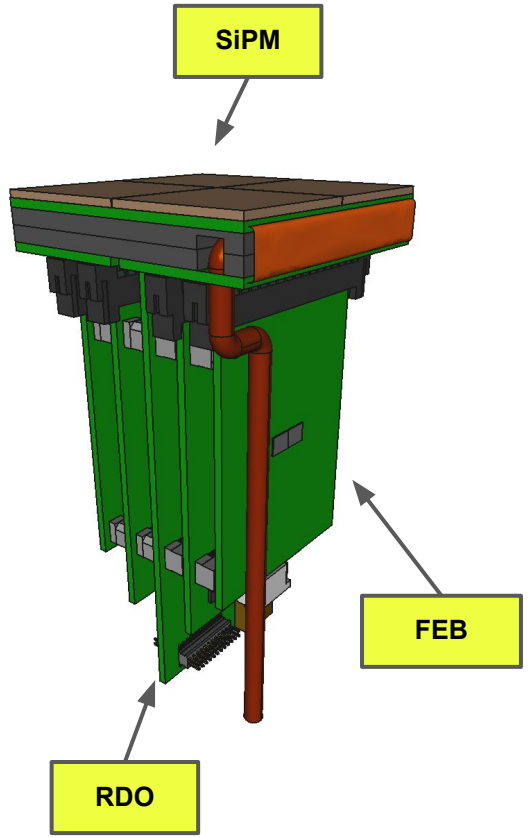
RICHIESTA: 8k EUR

ALCOR-FE-DUAL (versione attuale)



- 2 ALCOR a 32 canali (wire-bonded) sostituiti da 1 ALCOR a 64 canali (BGA)
- Connettori FireFly sostituiti da interfaccia verso RDO

Photodetector unit
(conceptual design
of final layout)

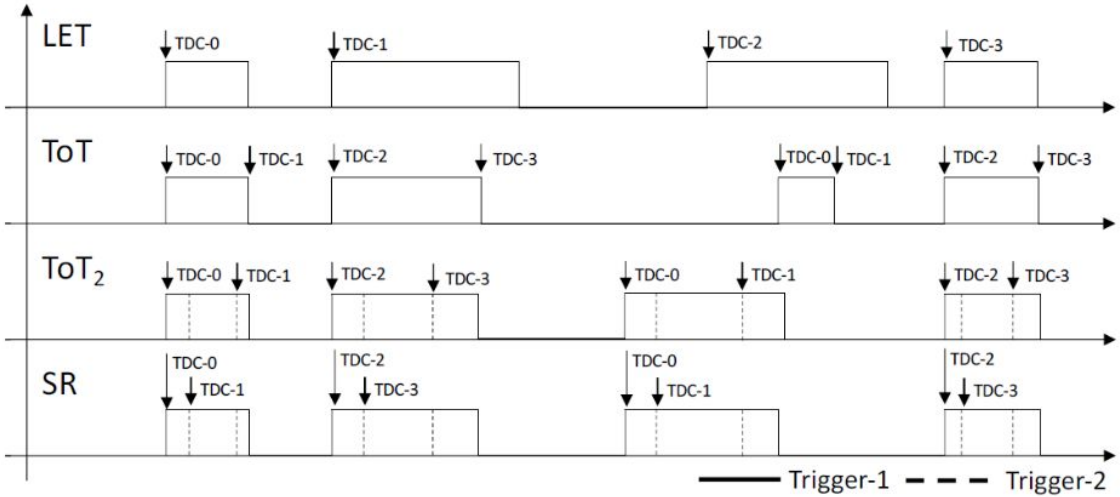


Istituto Nazionale di Fisica Nucleare
SEZIONE DI TORINO

M.Chiosso, F. Cossio, M. D. Da Rocha Rolo, G. Dellacasa,
M. Mignone, A. Rivetti, M. Ruspa, R. Wheadon

fcossio@to.infn.it

ALCOR pixel operating modes



4 operating modes:

- LET: leading edge measurement
- ToT: Time-over-Threshold measurement using the first discriminator for both edges
- ToT2: Time-over-Threshold measurement using both discriminators
- SR: slew-rate measurement

Each mode can be set to:

- FE: normal operation mode
- FE_TP: send test-pulse to analogue front-end
- TDC_TP: send test-pulse to pixel control logic to test and calibrate TDCs (bypass front-end)

Each pixel can also be disabled

ALCOR v2

- MPW, submitted in Dec 2022
- **~50-60 chips received mid June 2023, tests started 19th June 2023**

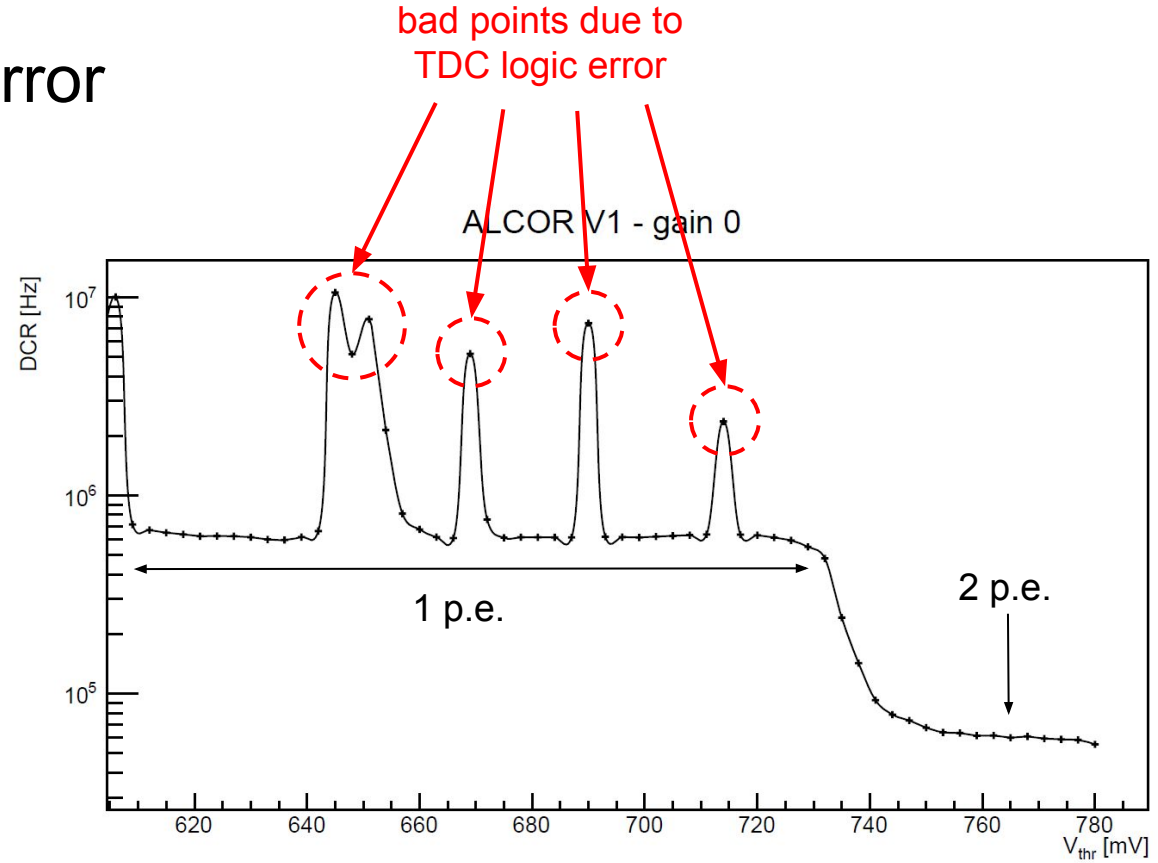
Bug fixes and new features:

1. Solve TDC logic critical error occurring at high rates
2. Generation of special words from EoC (header, frame, CRC) also when status words are disabled
3. New FE gain settings more suited for single photon applications
4. On-chip test-pulse also for EIC SiPMs polarity

1. TDC logic critical error

ALCORv1 TDC logic bug

- occurs at high rates (DCR > 500 kHz)
- generates corrupted data which saturates the ASIC output bandwidth
- requires a full reset to recover



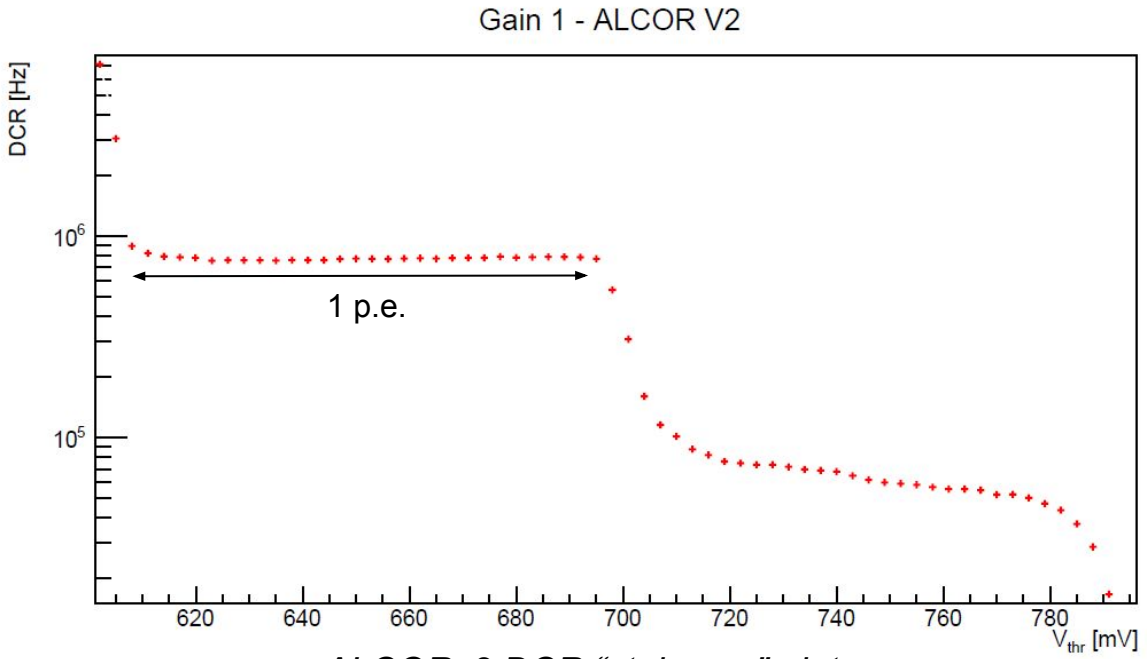
ALCORv1 DCR "staircase" plot

1. TDC logic critical error

ALCORv1 TDC logic bug

- occurs at high rates (DCR > 500 kHz)
- generates corrupted data which saturates the ASIC output bandwidth
- requires a full reset to recover

➢ **Solved in ALCORv2**



ALCORv2 DCR "staircase" plot

2. EoC special words

Header, *frame*, *CRC* and *status* words are added to *event* words to provide information for data clustering, synchronization and verification

ALCORv1 can operate in *raw-data mode* (only event words) or in *full mode* (all special words are included)

- ➢ **ALCORv2** can also operate in an intermediate mode where only ***status* words** are **disabled**
- ➢ This helps to reduce data throughput (status words are >50% of special words)

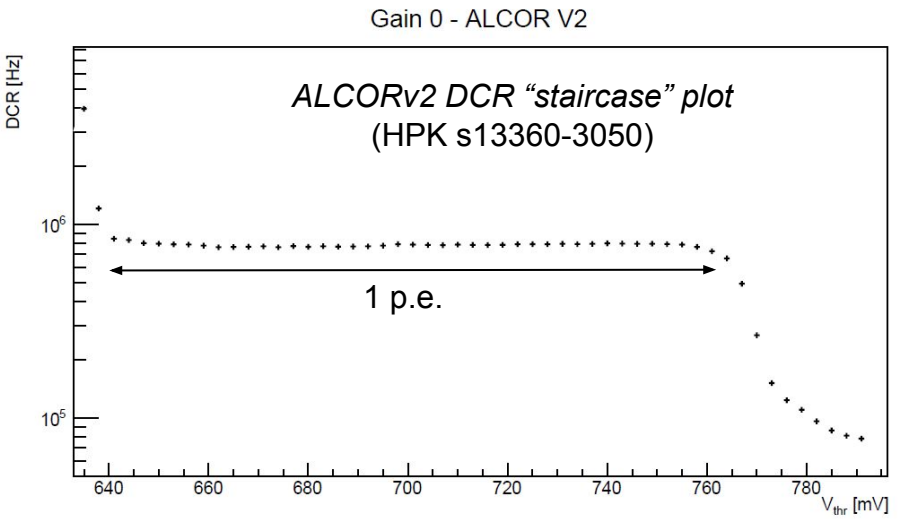
FIFO position	Data
1 (FPGA first received)	K28.0 (Frame header)
2	Frame number (16 bit)
3	Event words Column 0
..	Event words Column 1
n	K28.2 (Coarse Counter Rollover header)
n+1	K28.3 (Status header)
n+2	Status words Column 0 (x4)
n+6	Status words Column 1 (x4)
n+10	End of Column status word
n+11	K28.4 (Checksum header)
n+12	CRC value
n+13	K28.0 (New Frame header)

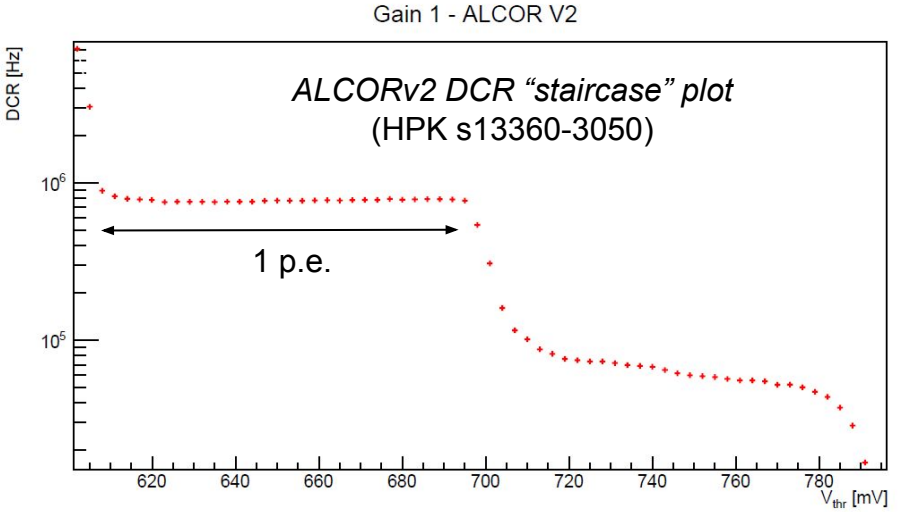
Table 5: Data stream with data events.

3. FE gain settings

ALCORv2 front-end implements two different gain settings best suited for single-photon applications

- ➢ to be tested with different SiPM models currently used within the EIC dRICH framework

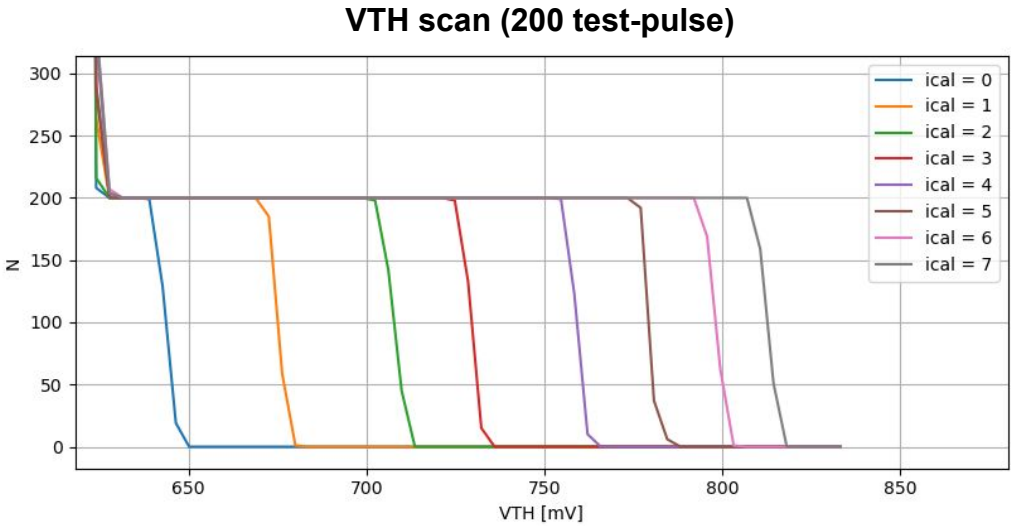




4. On-chip test-pulse

ALCOR can read both input signal polarities, but ALCORv1 internal test-pulse can only inject signals for negative polarity

➢ On-chip test-pulse generation included in **ALCORv2** also for EIC SiPMs signal polarity (positive)

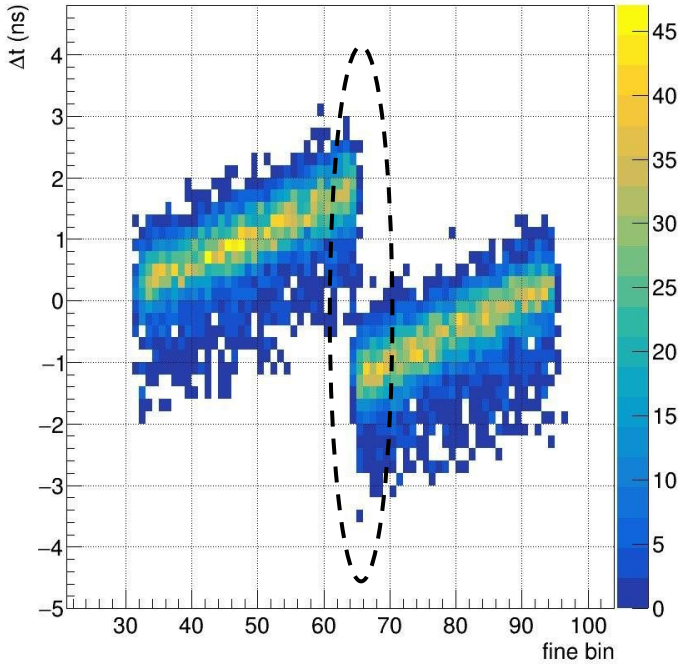


On-chip 3-bit DAC calibration circuit to define injected current magnitude

ALCOR v2.1

- INFN internal engineering run
- Submitted in Mar 2023, chips expected this Summer
- High number of chips will be available
- Corrected TDC logic bugs:
  - TFine-clock ambiguity
  - TOT orphans due to fake trigger at very low rates

R. Preghenella



Digital shutter

ALCOR test pulse can also act as **“inhibit”** of the pixel digital logic and this can help to reduce data throughput

- Successfully used in beam tests to reduce occurrence of ALCORv1 TDC logic critical errors
- In EIC: 10 ns bunch crossing, 250 ps bunch length
- Select 1-2 ns → **5-10x data reduction** before ALCOR TDCs

Current version of ALCOR cannot work with such short shutter time interval

- Inhibit signal is **synchronous** with clock
- Issues if leading/trailing edges of discriminator signal are across the time window

Logic for asynchronous digital shutter implemented in ALCORv3

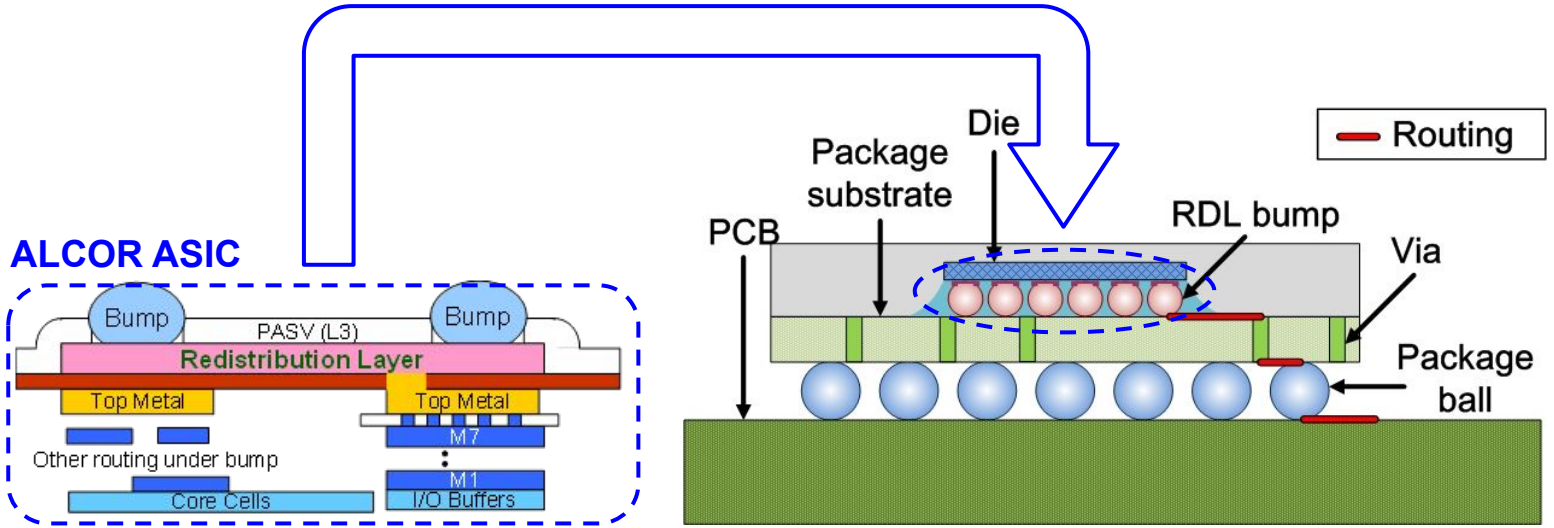
- Studies ongoing to define **delays** needed to guarantee same time window for all the channels
- Need to evaluate effect due to **time-walk** and **thresholds dispersion**


1
42
43
82
ALCOR
version 1
4.95 mm × 3.78 mm
(before optical scaling: 5.4942 mm x 4.1944 mm)
http://personalpages.to.infn.it/~fcossio/projects/ALCOR/ALCOR_user_guide.pdf
83
126

Flip-chip BGA packaging

Inside the package, the chip is flipped so that the active side of the device faces the package substrate to which it can be bump-bonded

→ Each pixel can be directly connected to the outside

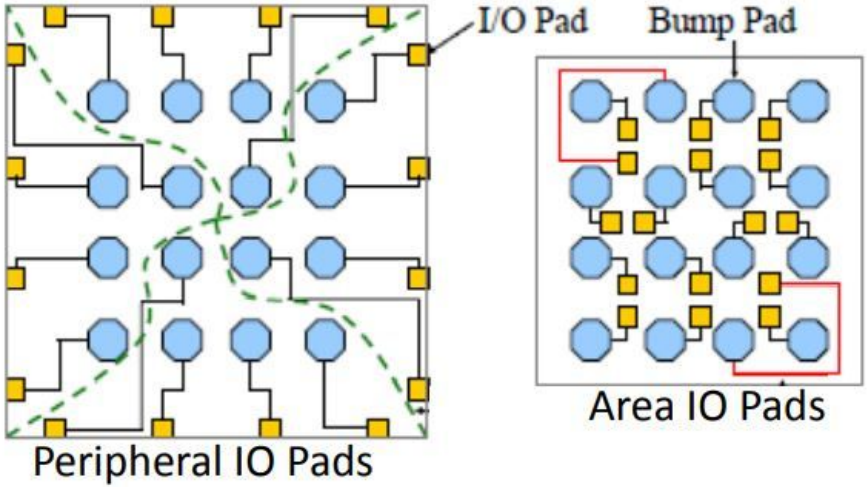


Flip-chip BGA packaging

Bump pads: pads to be connected to package interposer, usually placed in a grid pattern

IO pads: pads providing connection to core cells of the chip, provide also ESD protection, geometry can be *peripheral* (wire-bond like) or *area*

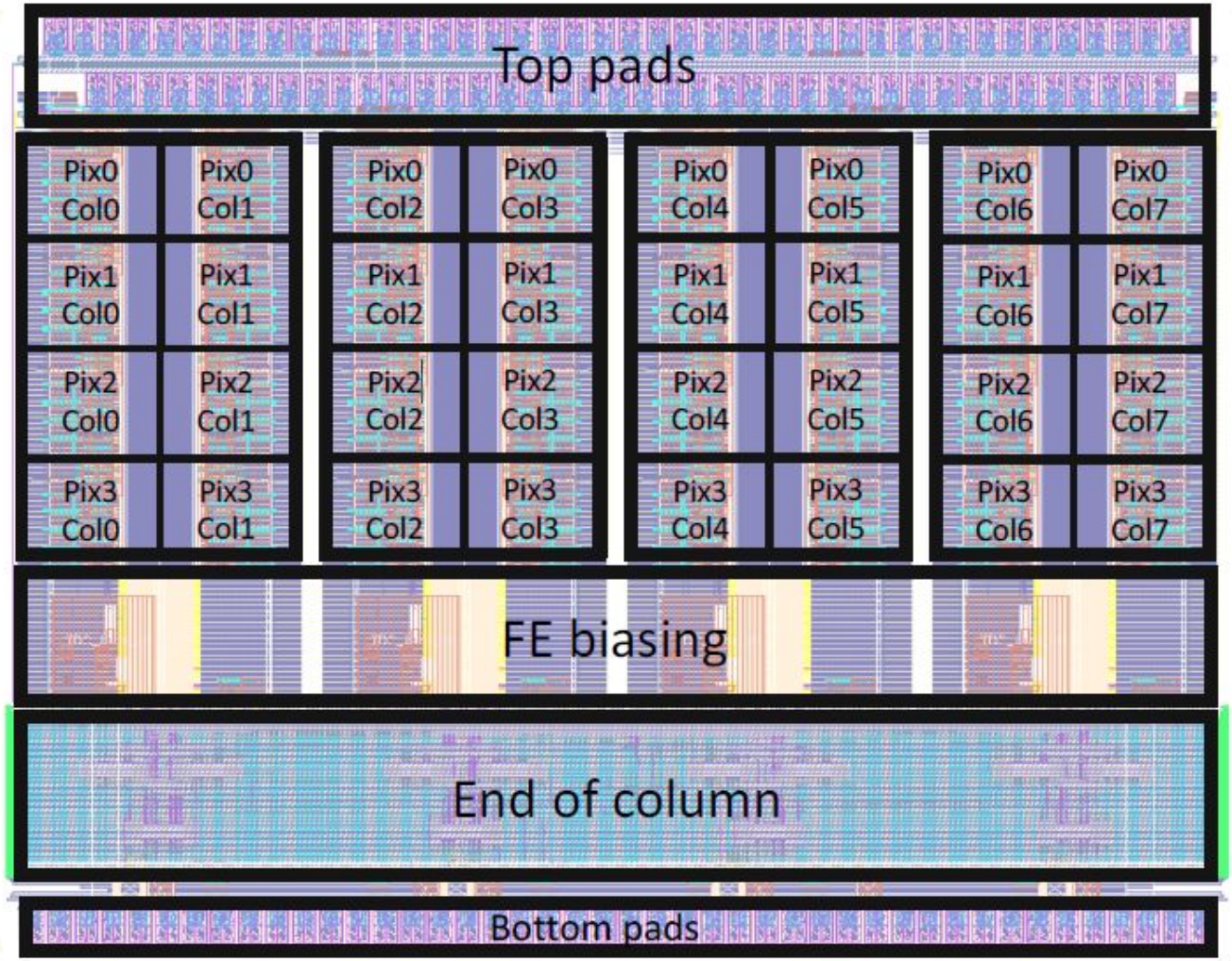
RDL (redistribution layer): extra metal layer connecting IO pads and bump pads



Support to RDL stopped by UMC, only METAL8 can be used to do the redistribution (no special layer)

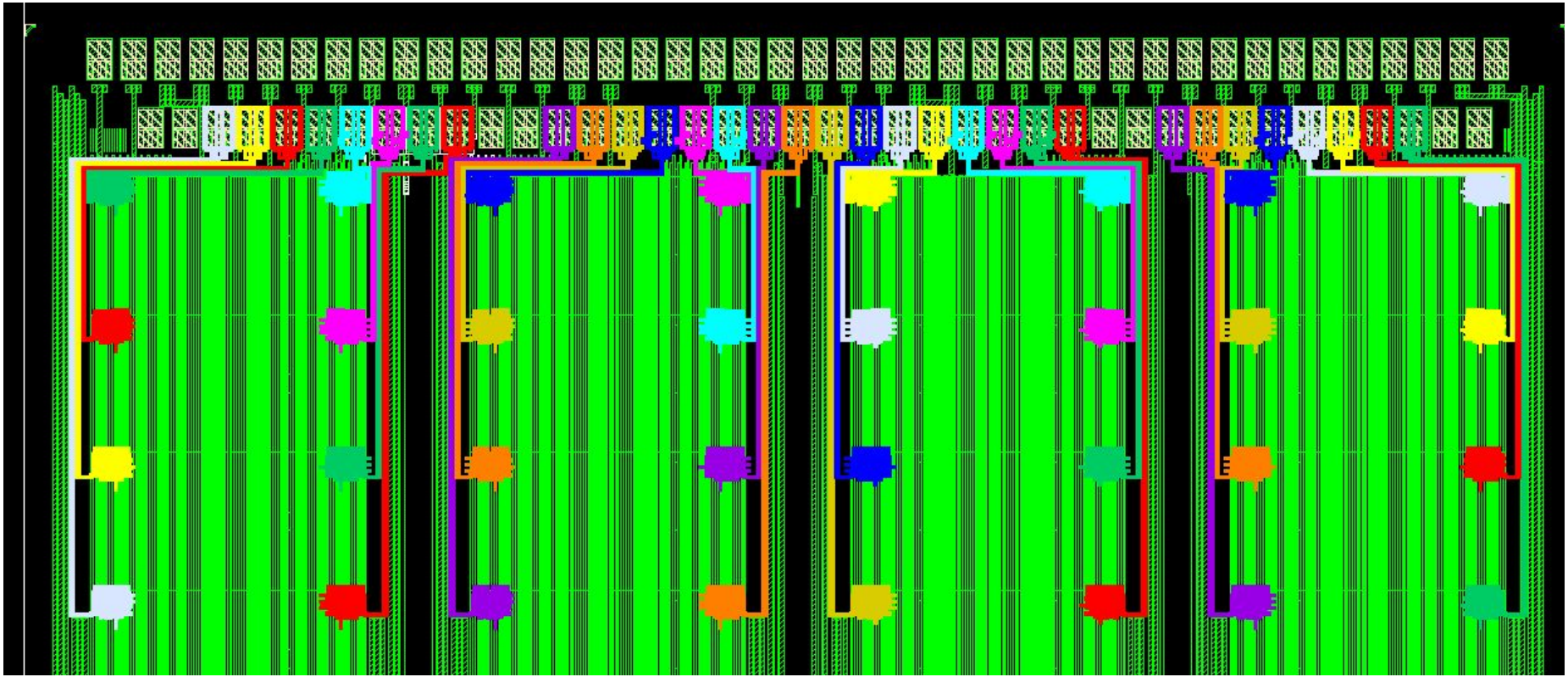
ALCOR-32

Space between each sector is used to route the pixels input to the Top pads and for decap capacitance



ALCOR-32

In ALCOR-32 the space between each sector is used to route the pixels input to the Top pads (going to the SiPMs)



ALCOR-64 I/Os

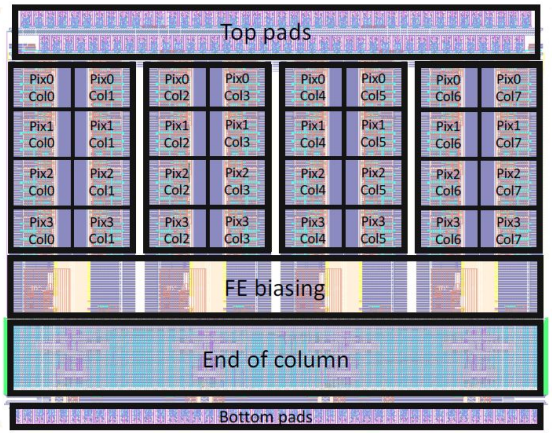
ANALOGUE (top)

- 32 AVDD + 8 AVDD_IO
- 32 AGND + 8 AGND_IO
- 8 AVSS

- 64 inputs
- 4 debug outputs
- 2 bias Vref

TOTAL = 88 + 70 = 158

2x



DIGITAL (bottom)

- 12 DVDD + 4 DVDD_IO
- 12 DGND + 4 DGND_IO
- 8 DVSS

- 16 Tx outputs
- 2 clk, 2 reset, 2 test-pulse
- 8 SPI
- 2 clk_out

TOTAL = 40 + 32 = 72

ALCORv3 64-channel version with 230 I/Os

ALCOR v1 FE

PM5: input transistor (CG)

PM4: CG bias

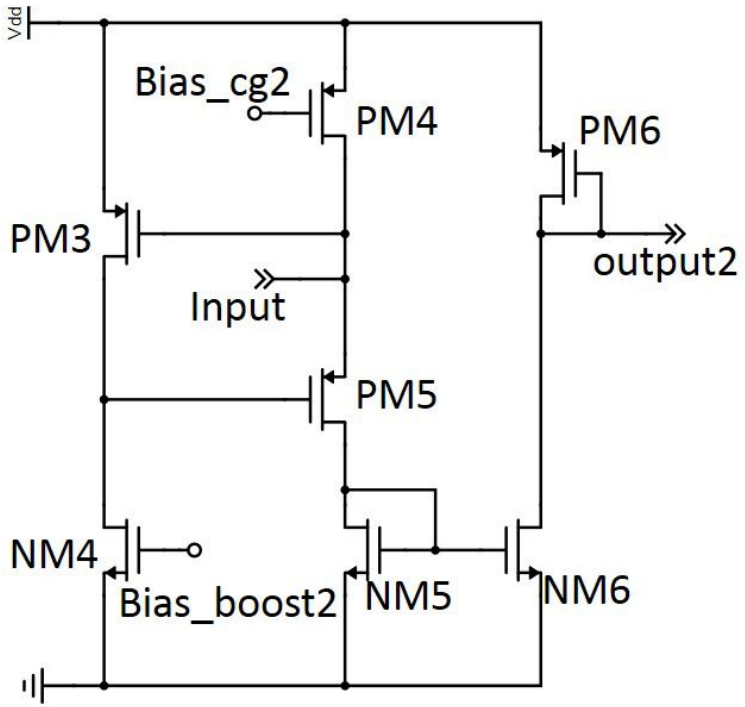
PM3: boost transistor

NM4: boost bias

PM3 + NM4 = CS amplifier

$A = gm_{PM3} \cdot R_p$

$Zin \simeq 1 / (A * gm_{PM5})$



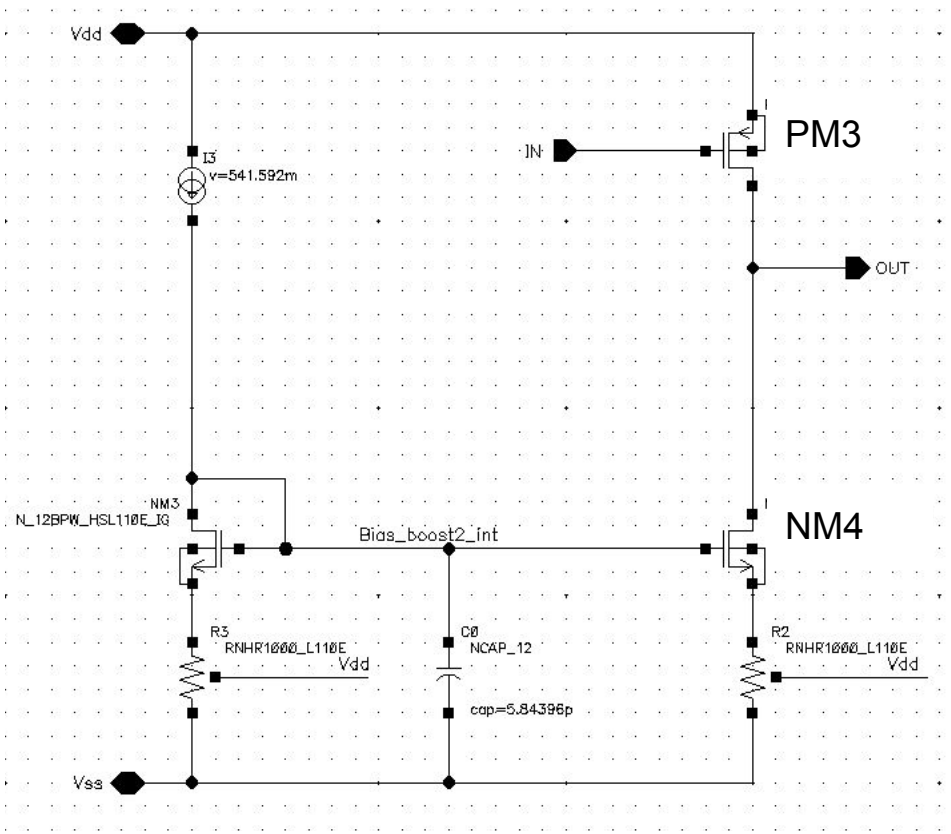
New FE (CS boost stage)

Boost bias transistor (NM4) with source degeneration to reduce its contribution to noise and increase output resistance

Zin ≃ 1 / (A * gm_{PM5})

$A = gm_{PM3} \cdot R_p$

Attention must be paid to small mismatches in the resistors and to the decreased voltage headroom

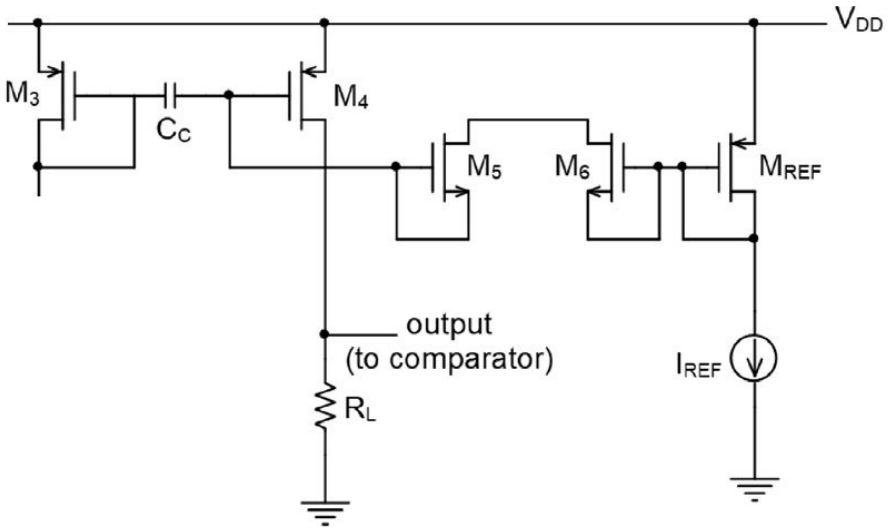


Internal AC-coupling

Input and output stages of ALCOR amplifier are AC-coupled via Cc

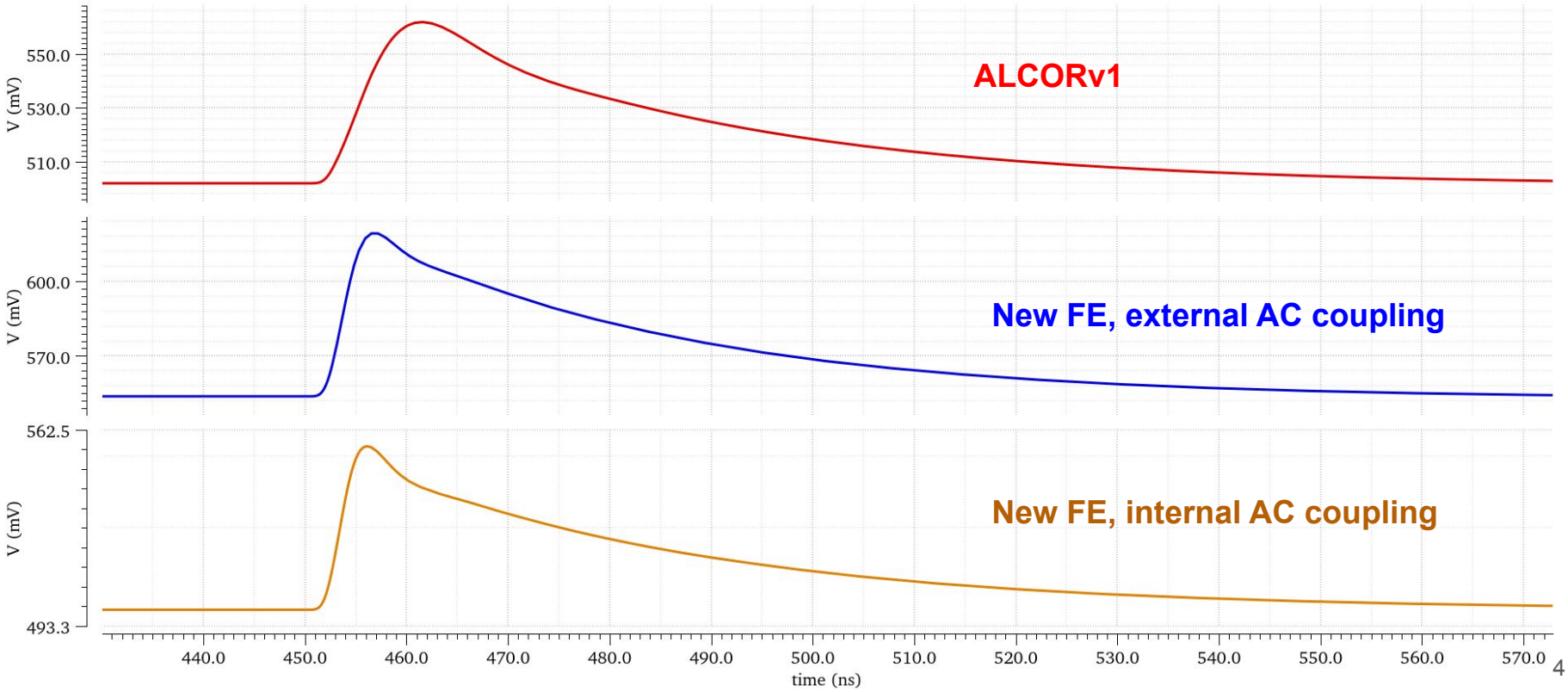
IREF and MREF set DC operating point of M4 via M5 and M6: back-to-back cut-off MOSFETS providing equivalent large resistor (~GΩ)

Baseline can be controlled using I_{REF}, using a simpler architecture w.r.t. the one implemented in ALCOR v1 with DC-coupled output stage

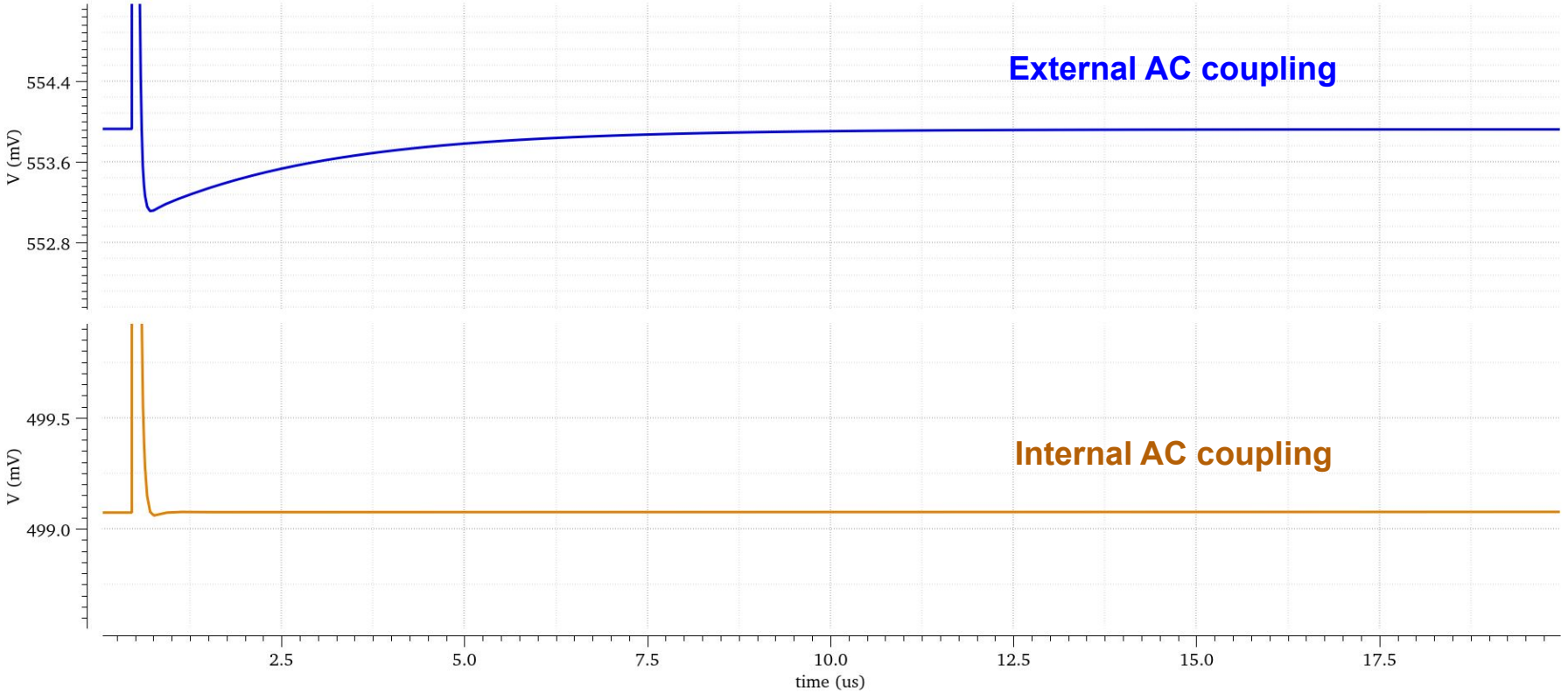


Input stage can be in principle DC-coupled to the SiPM → need to study interplay with annealing MOSFETs and SiPMs HV trim DACs

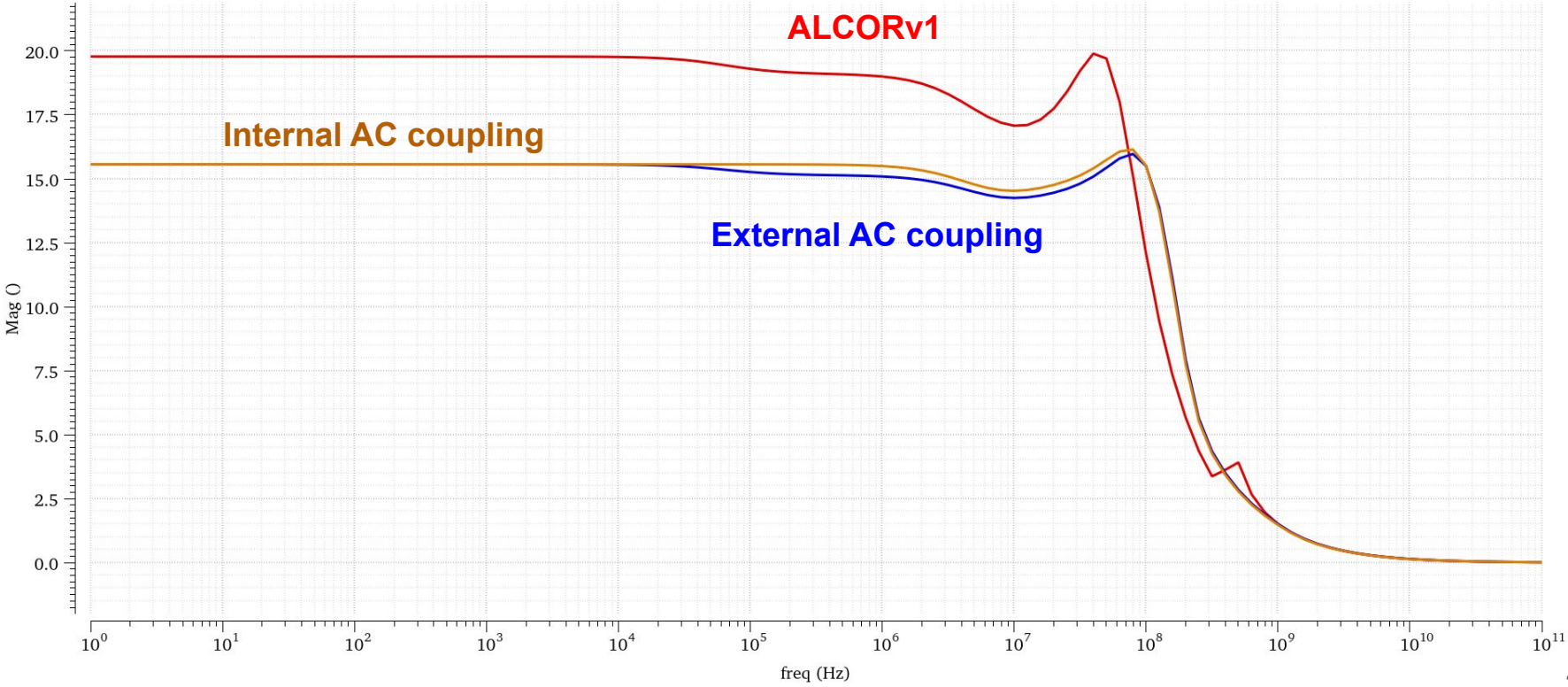
Transient simulation



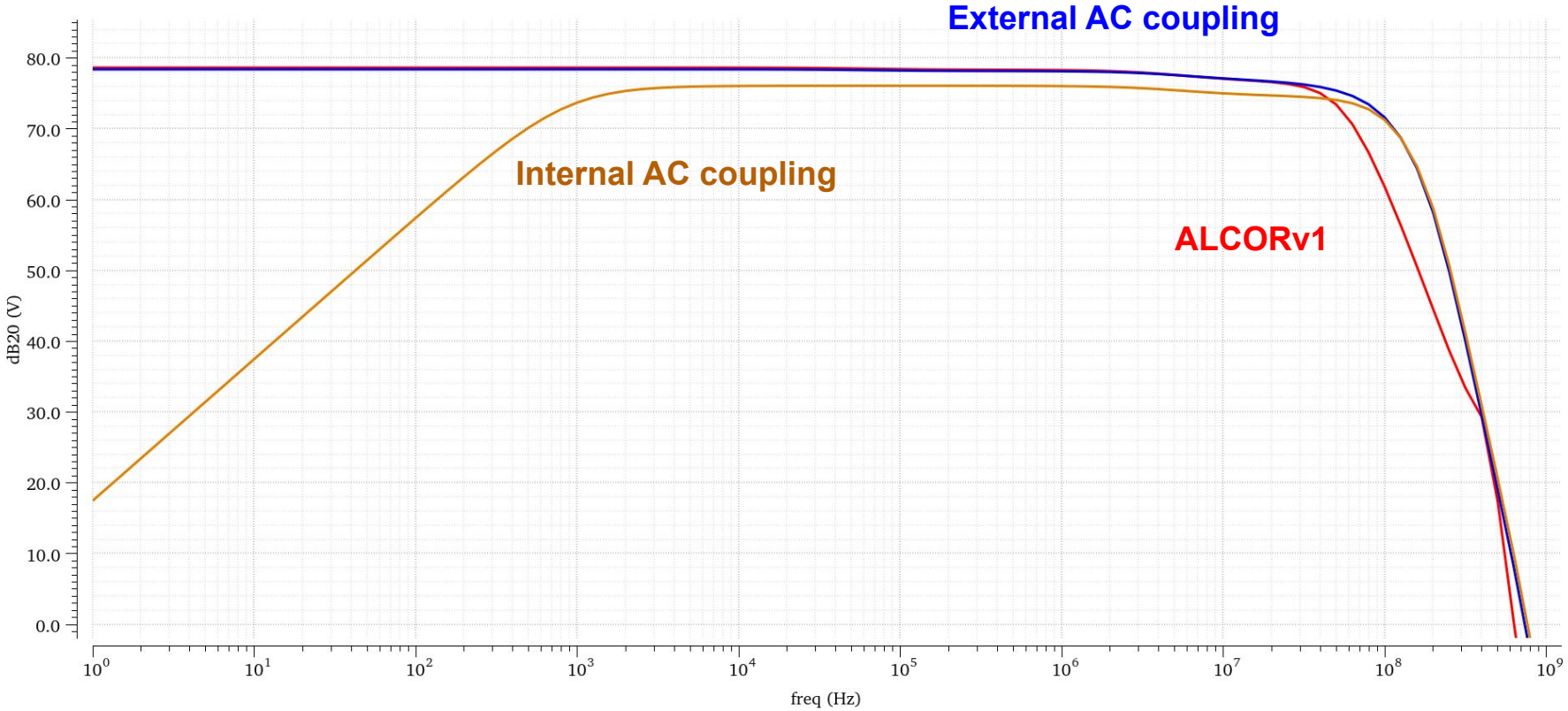
Return to baseline



Input impedance



Frequency response



Specs comparison

Schematic simulations with SiPM model: Hamamatsu S131360-3050, OV = 3 V

ALCORv1	
RMSnoise	1.43 mV
SR	9.72 MV/s
jitter	147 ps
gain	221.4 mV/pC
SNR	41.9
rise_time	10.4 ns
Zin_DC	19.8 Ω

External AC coupling	
RMSnoise	1.65 mV
SR	20 MV/s
jitter	82.6 ps
gain	243.5 mV/pC
SNR	39.7
rise_time	5.61 ns
Zin_DC	15.6 Ω

Internal AC coupling	
RMSnoise	1.54 mV
SR	19.74 MV/s
jitter	77.9 ps
gain	198.9 mV/pC
SNR	37.5
rise_time	5.17 ns
Zin_DC	15.6 Ω