High-Speed Serial Data Transmission - 1

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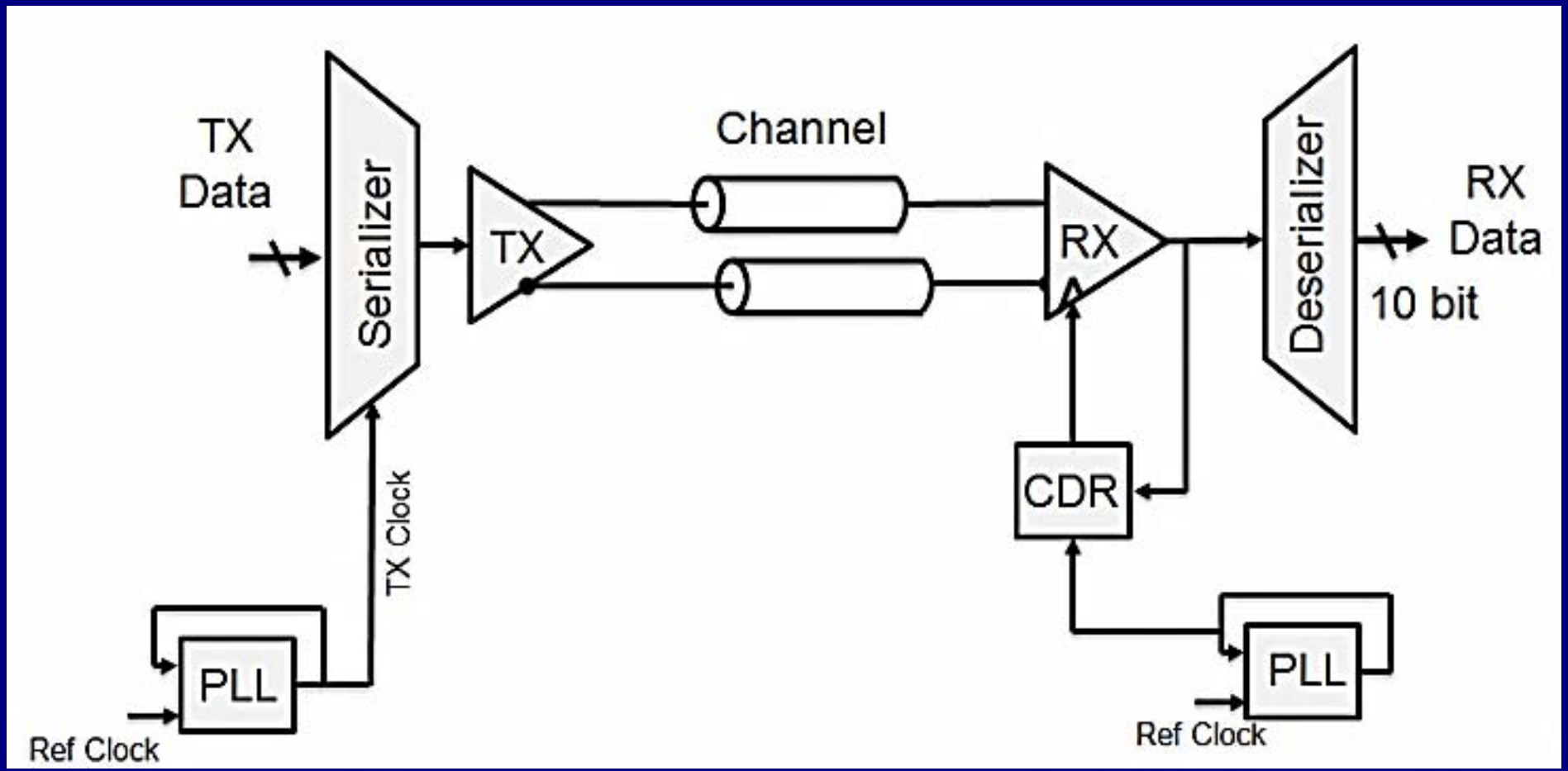
Motivations

Why high speed serial links are required in HEP experiments :

- "Dramatic" increase in the amount of data to be transmitted, due to :
  - Increased luminosity
  - Increased detector granularity (both in space and in time)
  - Triggerless readout schemes
- Impact of cabling in the material budget

Typical application is more demanding in the downstream channel

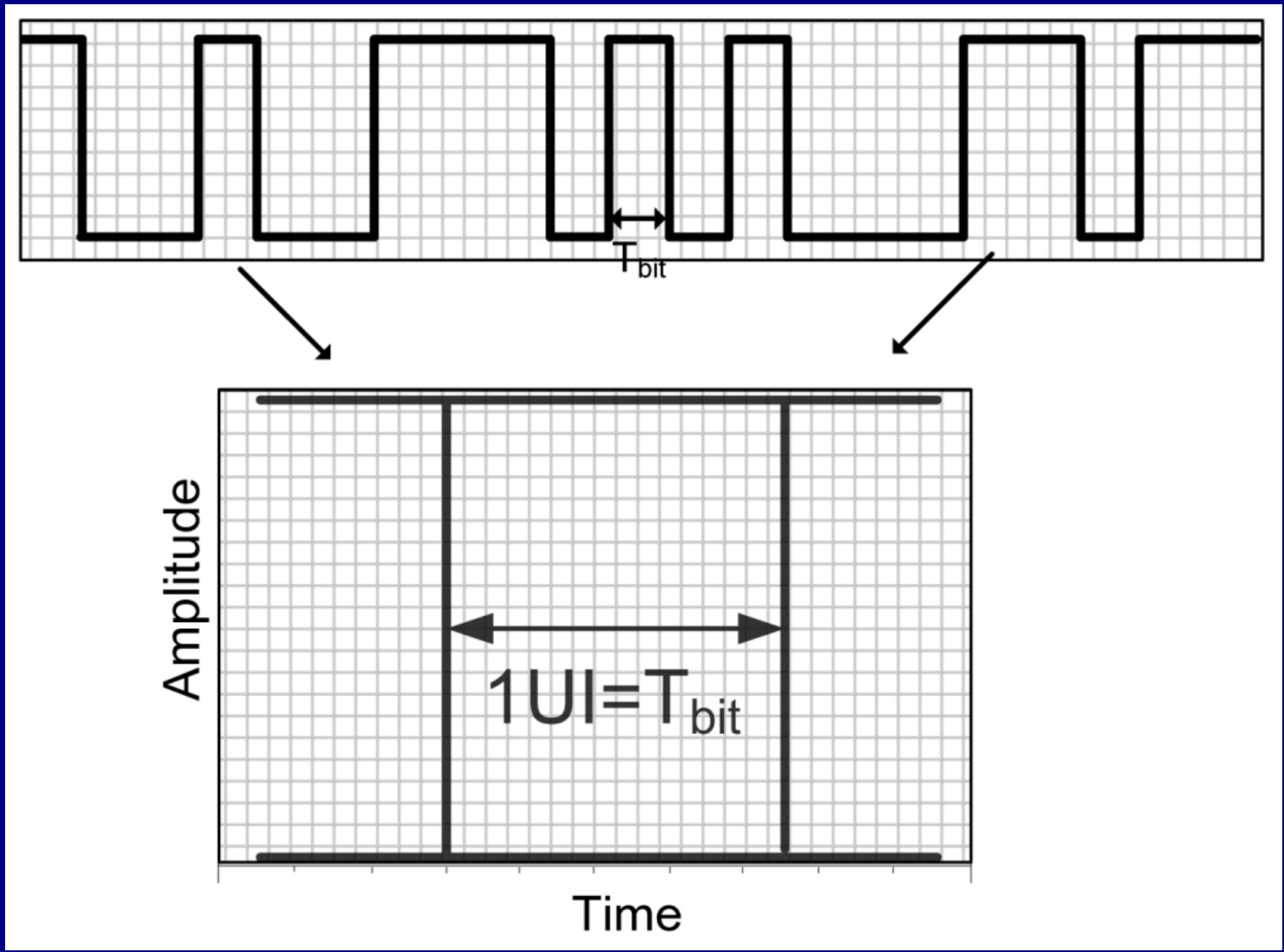
Serial link


TX
Data
Serializer
TX
Channel
RX
Deserializer
RX
Data
10 bit
CDR
TX Clock
PLL
Ref Clock
PLL
Ref Clock

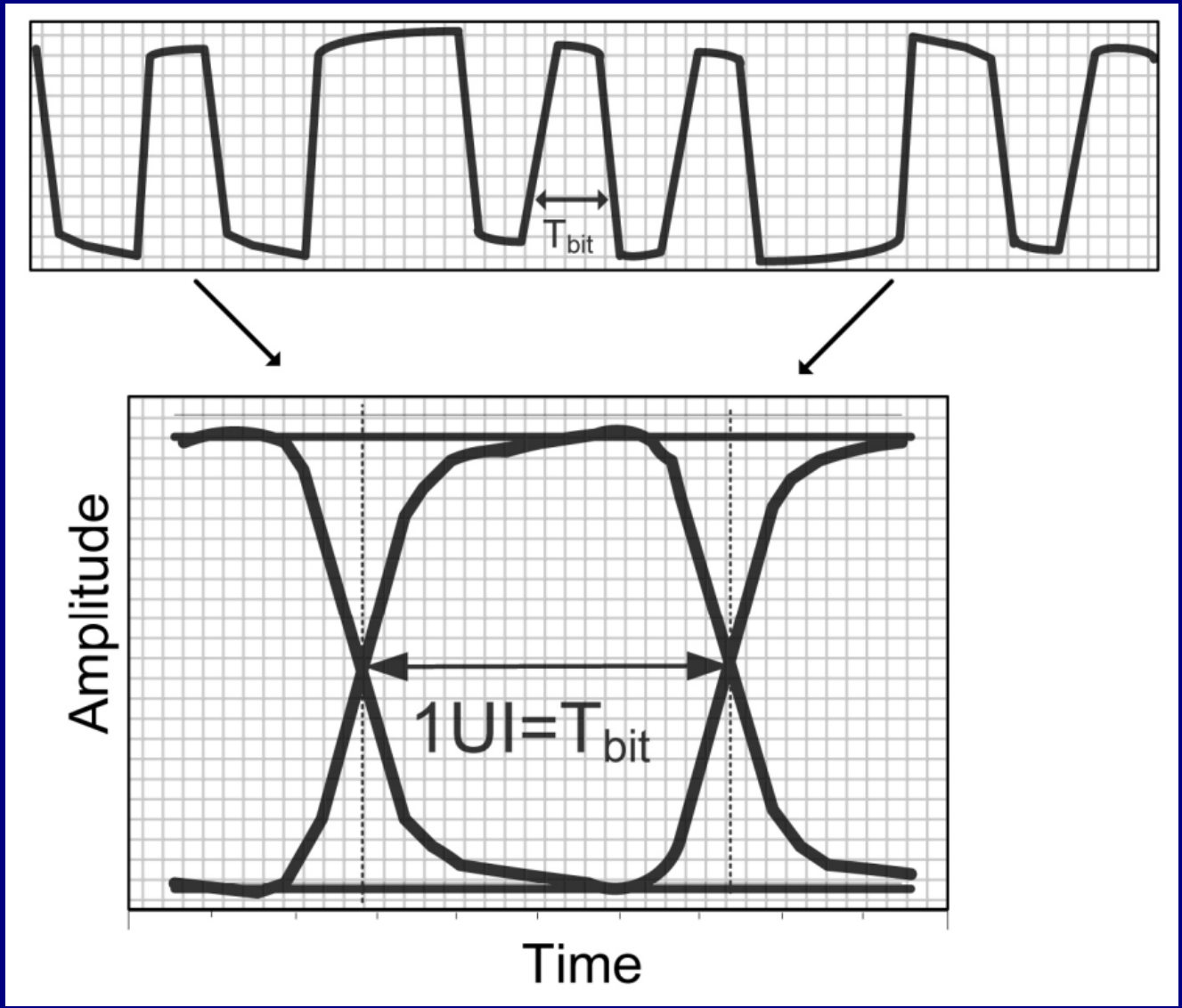
Ingredients

- Clock multiplication PLLs
- Clock and Data Recovery (CDR) circuit
- High-speed serializers
- Laser or cable drivers

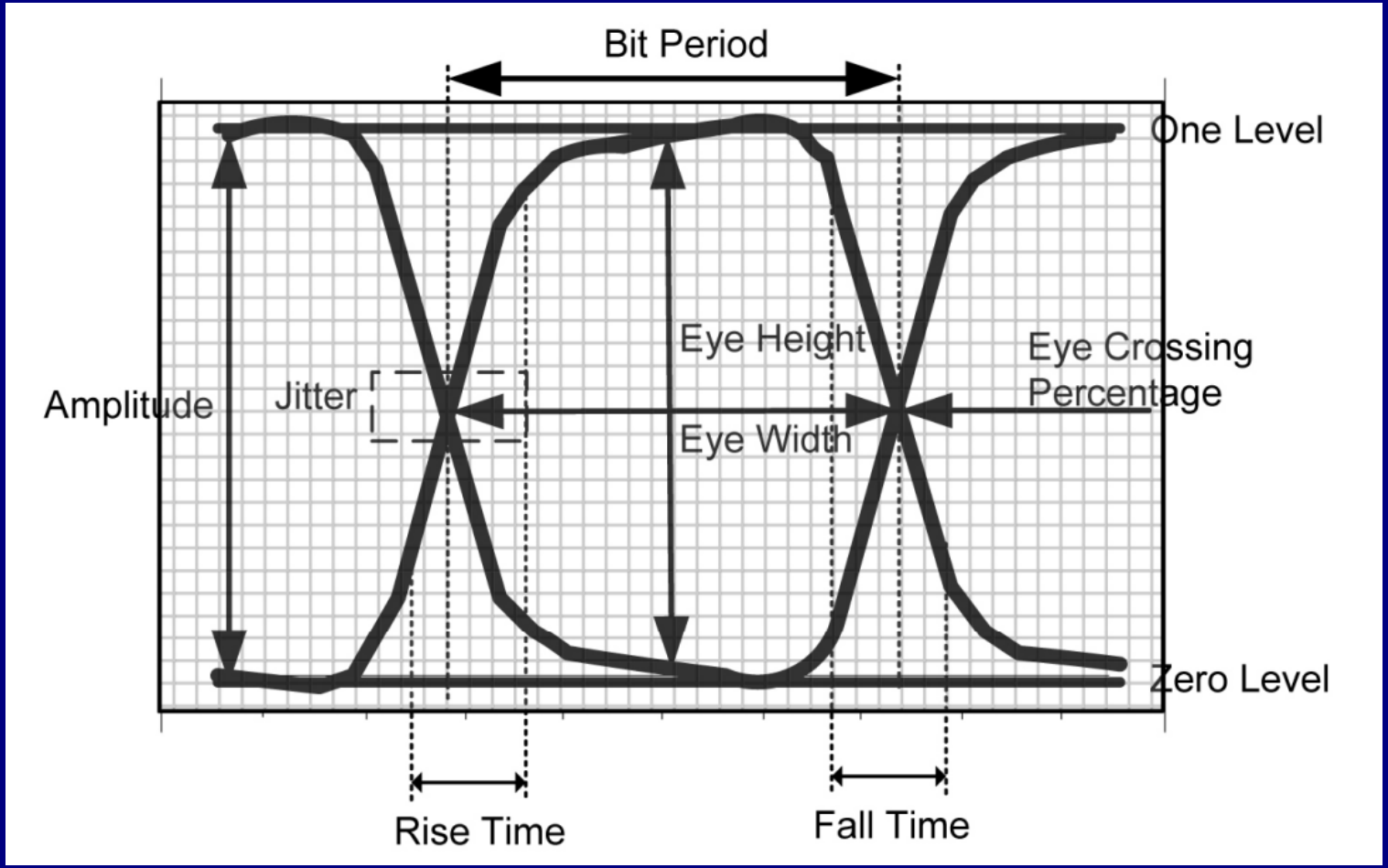
Eye diagram - ideal



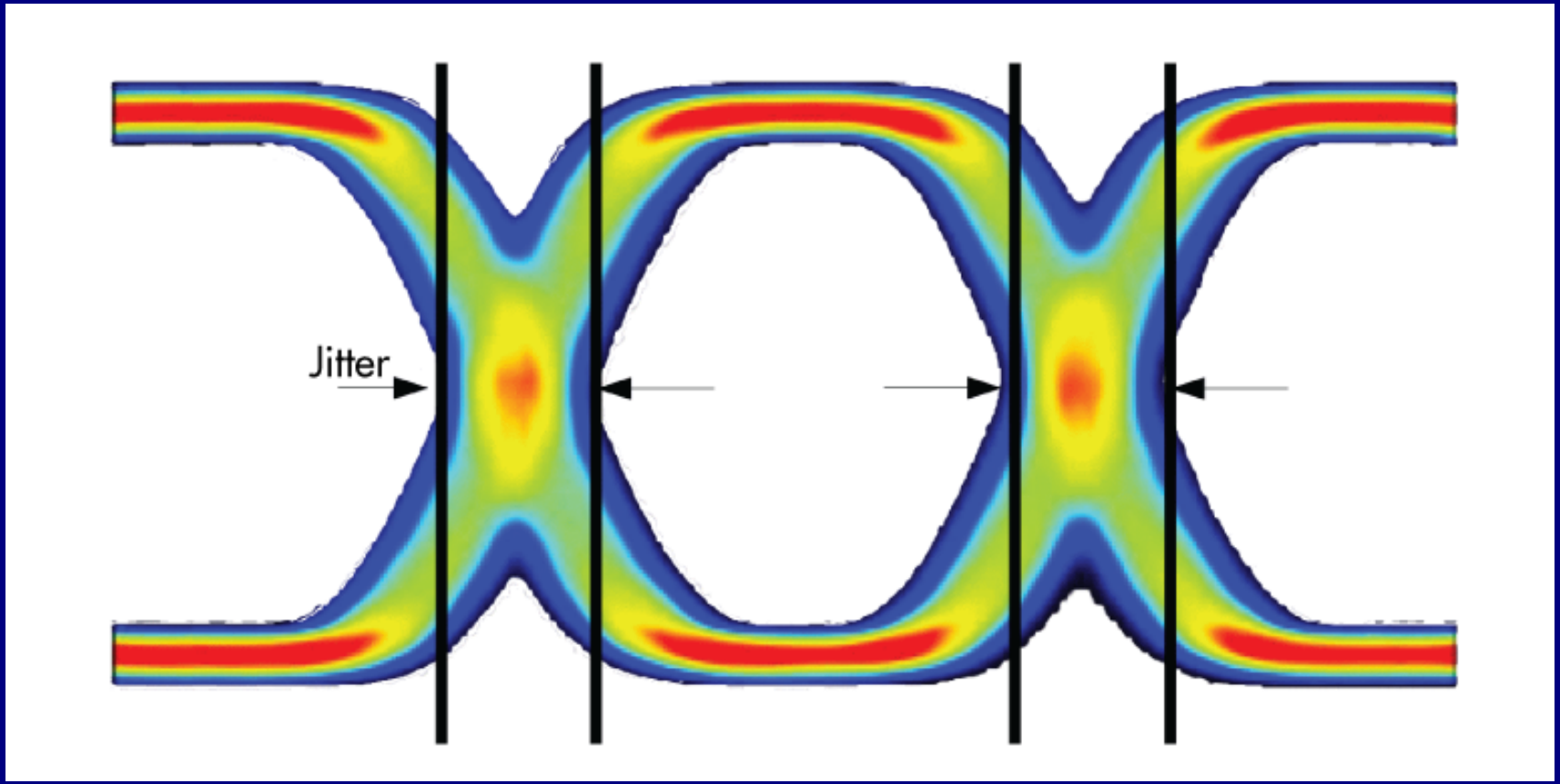
Eye diagram - bandwidth limitation



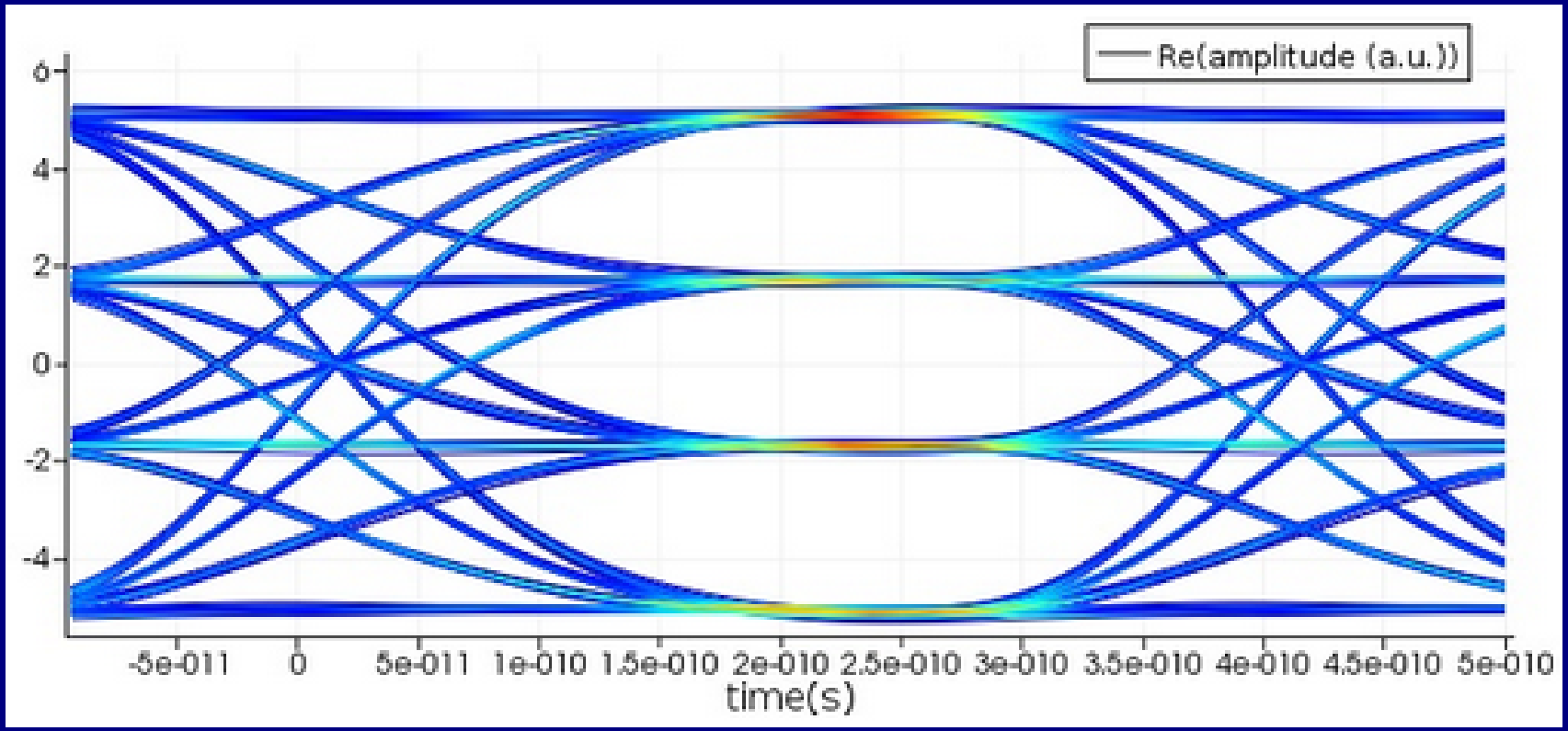
Eye diagram - metrics



Eye diagram - real



Eye diagram - multi level



Bit Error Rate (BER)

The Bit Error Rate is the ratio between the number of errors and the number of bits transmitted.

$$BER = \frac{N_{errors}}{N_{bits}} \tag{1}$$

The confidence level is the percentage of tests that the systems true BER is less than the specified BER. Since we cannot measure an infinite number of bits and it is impossible to predict with certainty when errors will occur, the confidence level will never reach 100

$$C_L = 1 - e^{-N_{bits} BER} \tag{2}$$

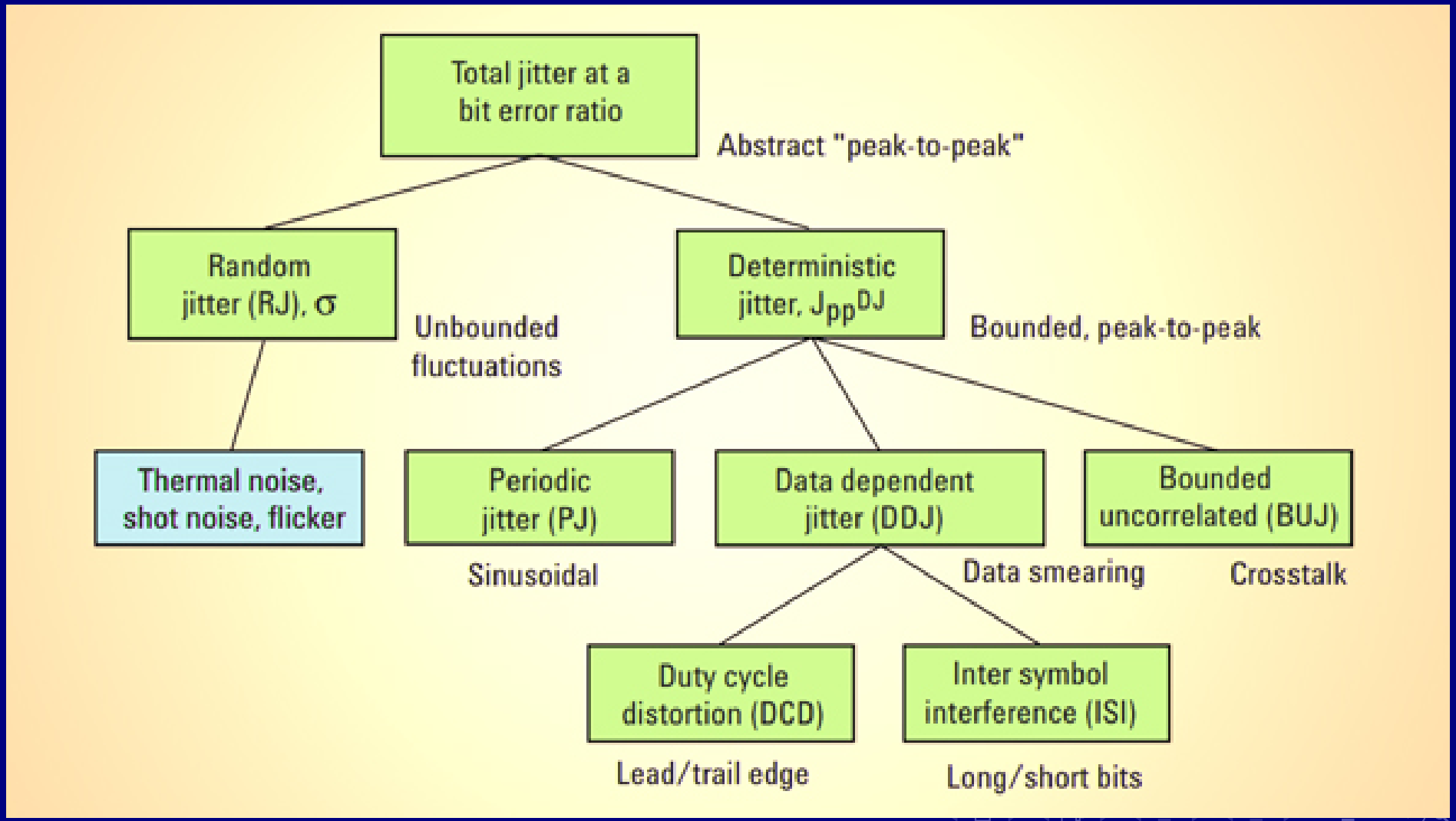
$$Time(s) = \frac{-ln(1 - C_L)}{f \cdot BER} \tag{3}$$

Test times

	STM-256/OC-768 39.81312 GHz	STM-264/OC-192 9.95328 GHz	STM-16/OC-48 2.48832 GHz	STM-4/OC-12 622.08 MHz	STM-1/OC-3 155.52 MHz
10^{-11}	≈7.5 s	≈30 s	≈2 m	≈8 m	≈32 m
10^{-12}	≈1.3 m	≈5 m	≈20 m	≈80 m	≈5.25 h
10^{-13}	≈12.5 m	≈50 m	≈3.3 h	≈13 h	≈2.2 d
10^{-14}	≈2.1 h	≈8.4 h	≈1.4 d	≈5.6 d	≈22.4 d
10^{-15}	≈21 h	≈35 d	≈14 d	≈42 d	≈224 d
10^{-16}	≈8.7 d	≈35 d	≈139 d	≈2 y	≈8.4 y

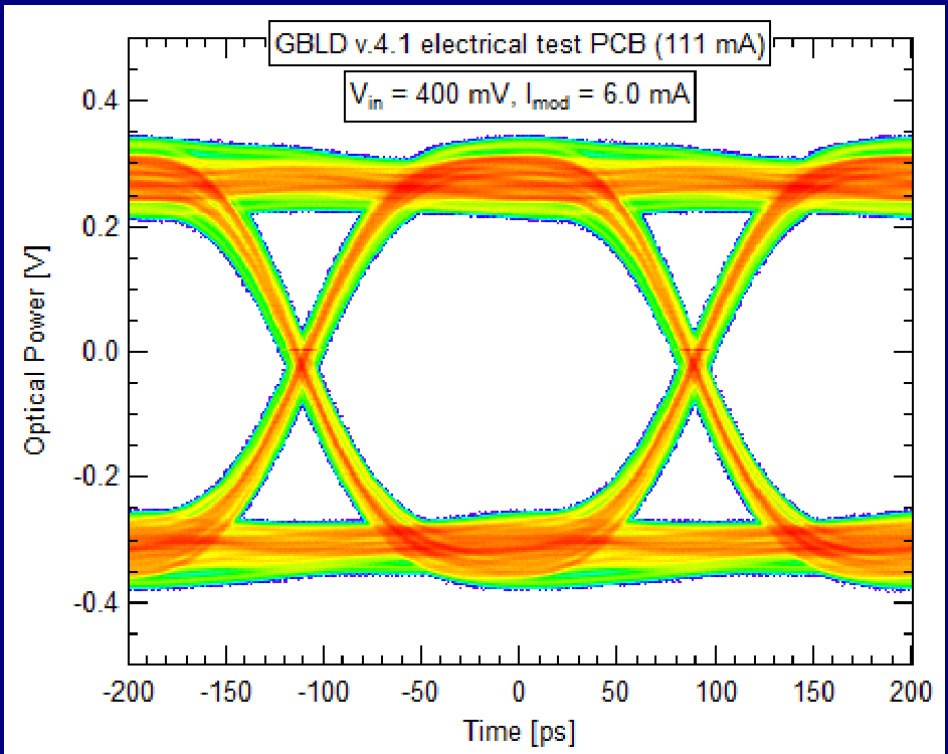
Jitter

Jitter is the deviation from true periodicity of a presumably periodic signal, often in relation to a reference clock signal

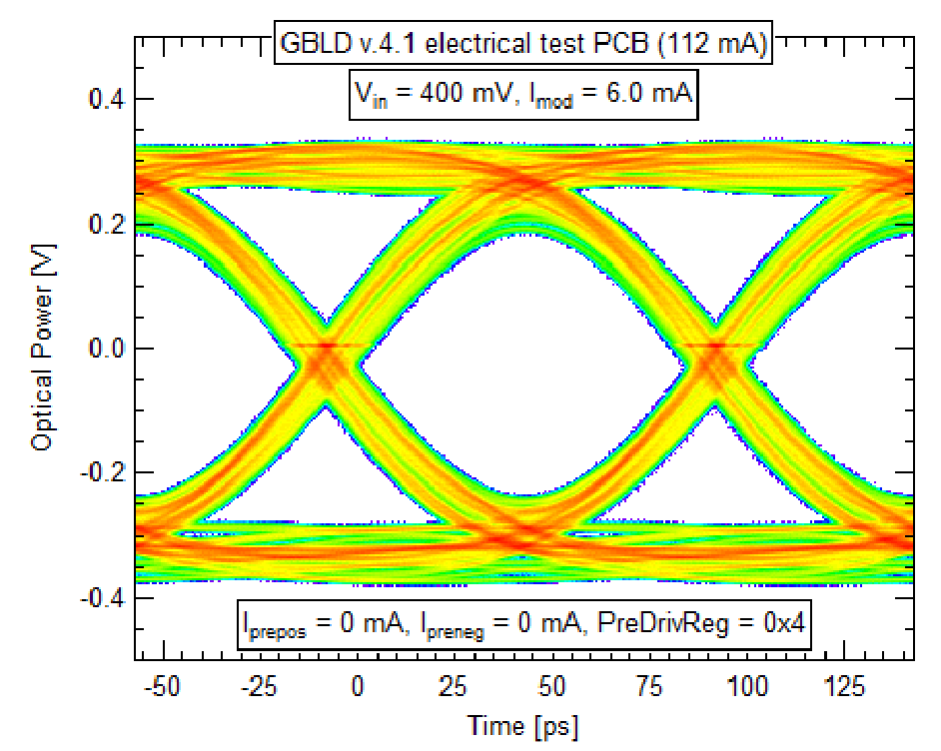


Inter-Symbolic Interference (ISI)

Effect of limited driver or line bandwidth.



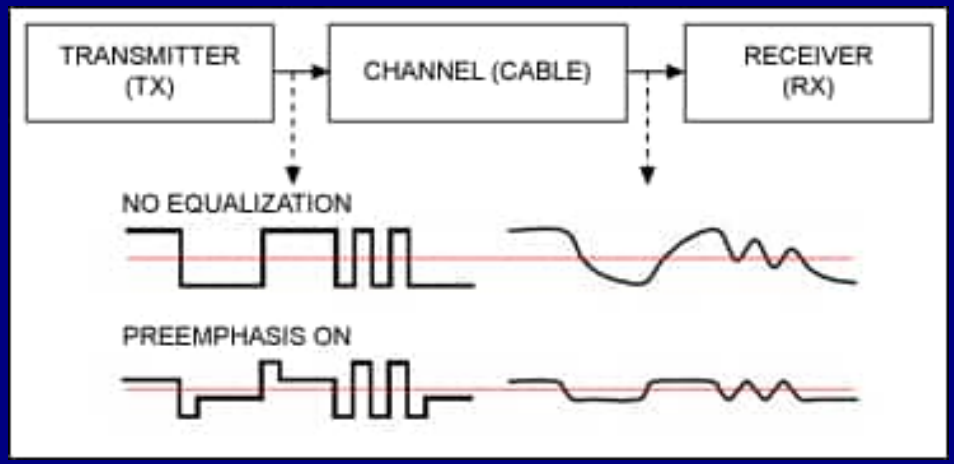
Data rate : 5 Gb/s

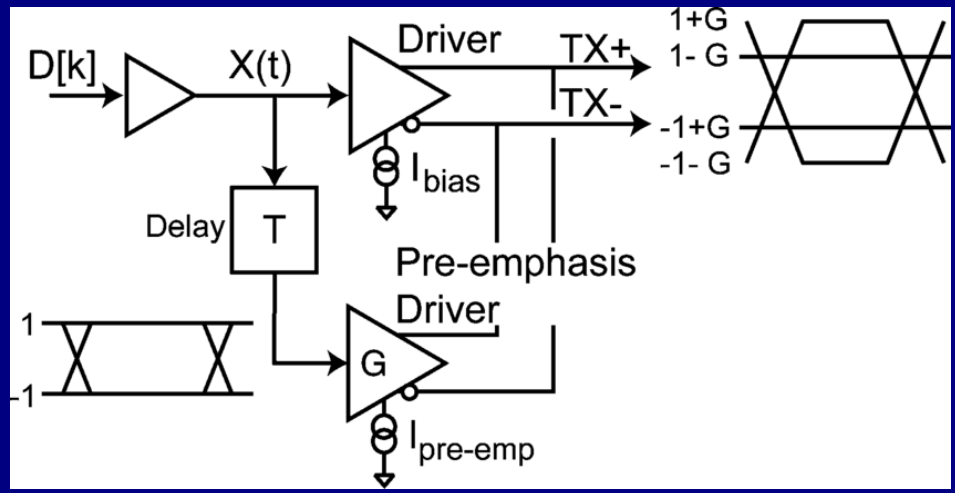


Data rate : 10 Gb/s

Pre emphasis

Signal amplitude is artificially increased during transition





Step forward : FIR equalization filter.

Total jitter

Random jitter is unbounded (Gaussian), while Data Dependent jitter is bounded. How they combine ?

$$Tj = \alpha Rj + DDj \tag{4}$$

BER	pk-pk Rj
10^{-10}	$12.7\times\sigma$
10^{-11}	$13.4\times\sigma$
10^{-12}	$14.1\times\sigma$
10^{-13}	$14.7\times\sigma$
10^{-14}	$15.3\times\sigma$

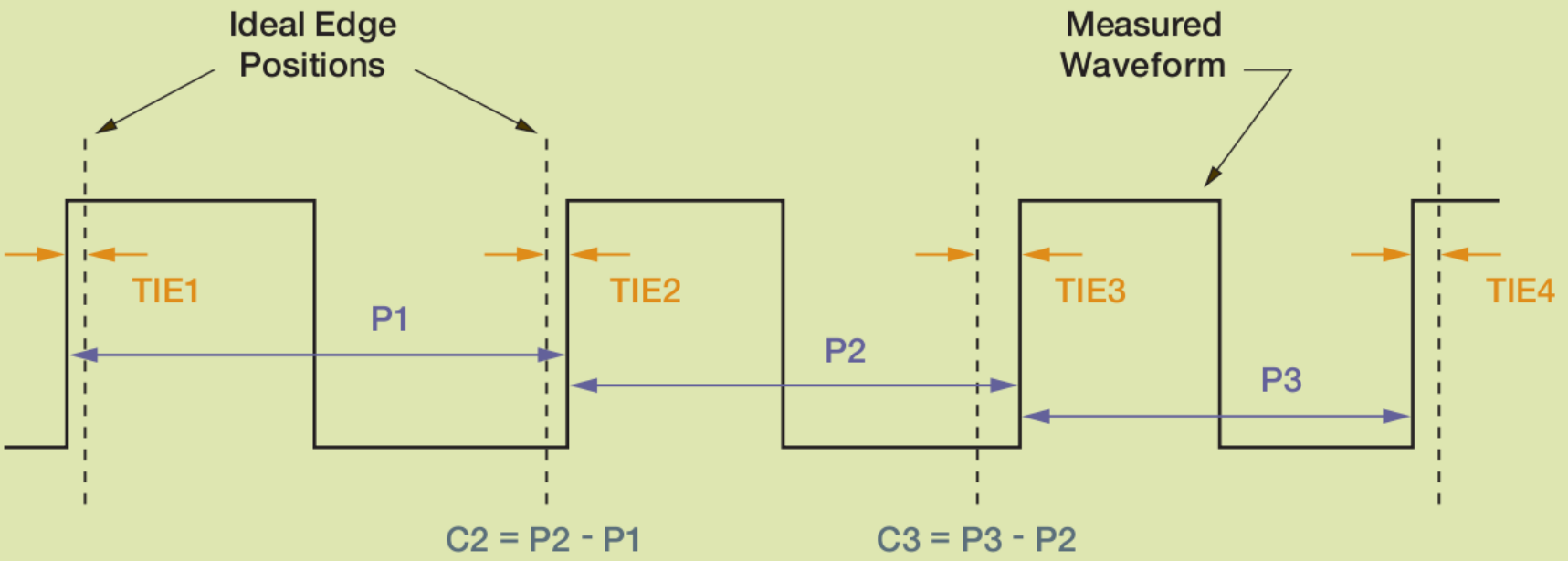
Jitter measurement - 1

Measures typically provided by a scope :

- Period jitter : variation of the measured period for each clock cycle
- Cycle-to-cycle jitter : change of period between two consecutive clock cycles
- N-Cycle-to-cycle jitter : change of period between two clock cycles at distance N
- TIE jitter : how far each active edge of the clock varies from its ideal position.

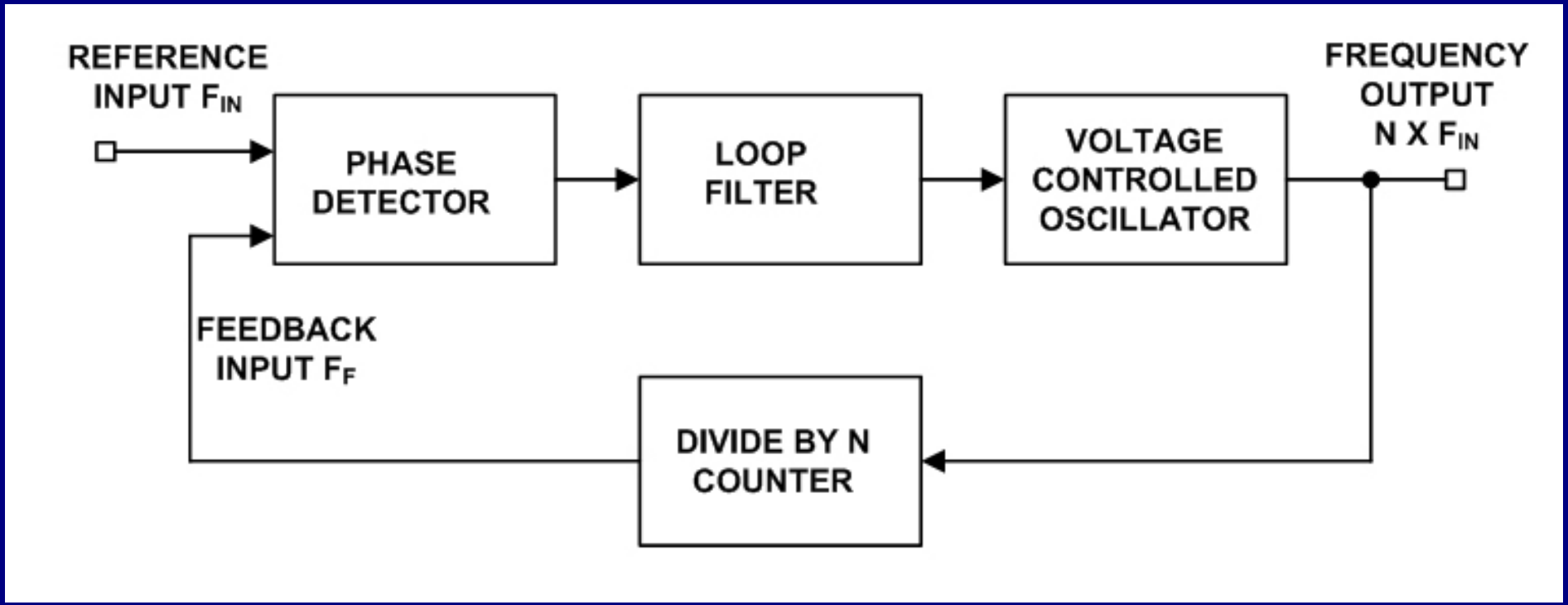
Jitter analysis requires additional DSP packages in the scope.

Jitter measurement - 2

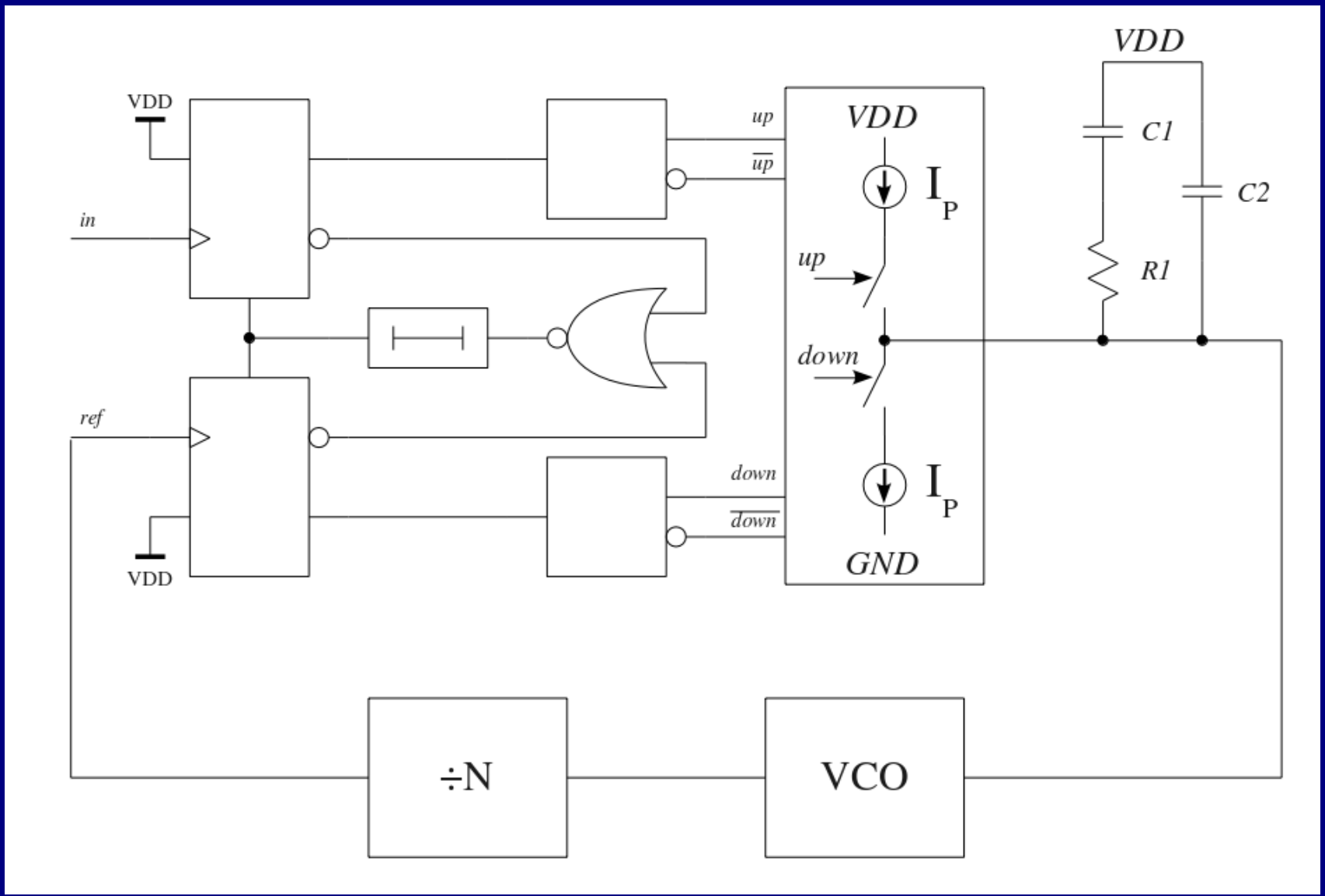


Clock multiplication Phase Locked Loop

Data transmission requires high frequency clock that can be either transmitted to the FE ASIC or generated internally via a clock multiplication PLL.



Charge Pump Phase Locked Loop



Types of VCOs

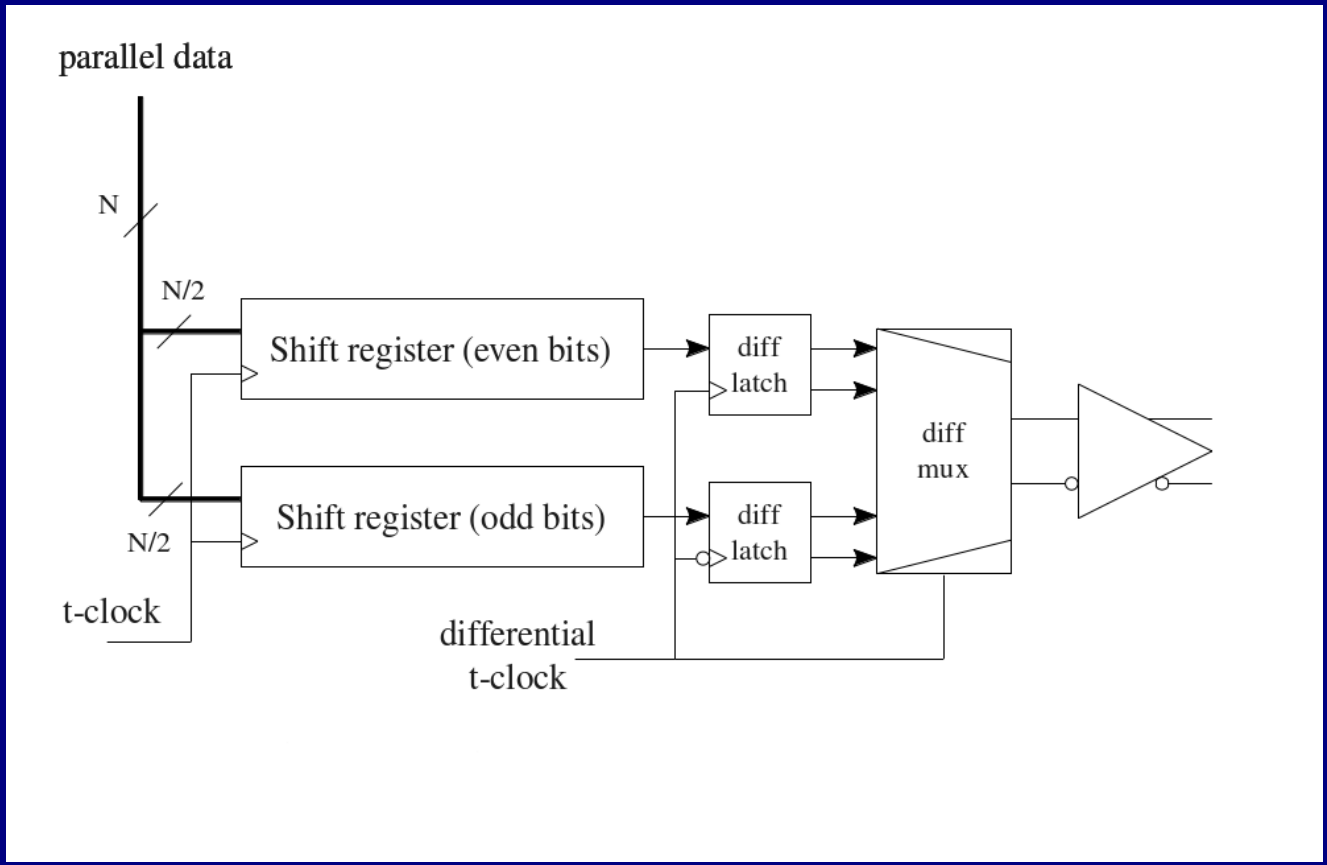
- Ring oscillator VCO
  - Based on a controlled delay chain
  - Medium jitter
  - Compact size
  - Large lock range
- LC VCO
  - Based on a LC resonant circuit
  - Low jitter
  - Large size (due to the inductor)
  - Small lock range

PLL bandwidth

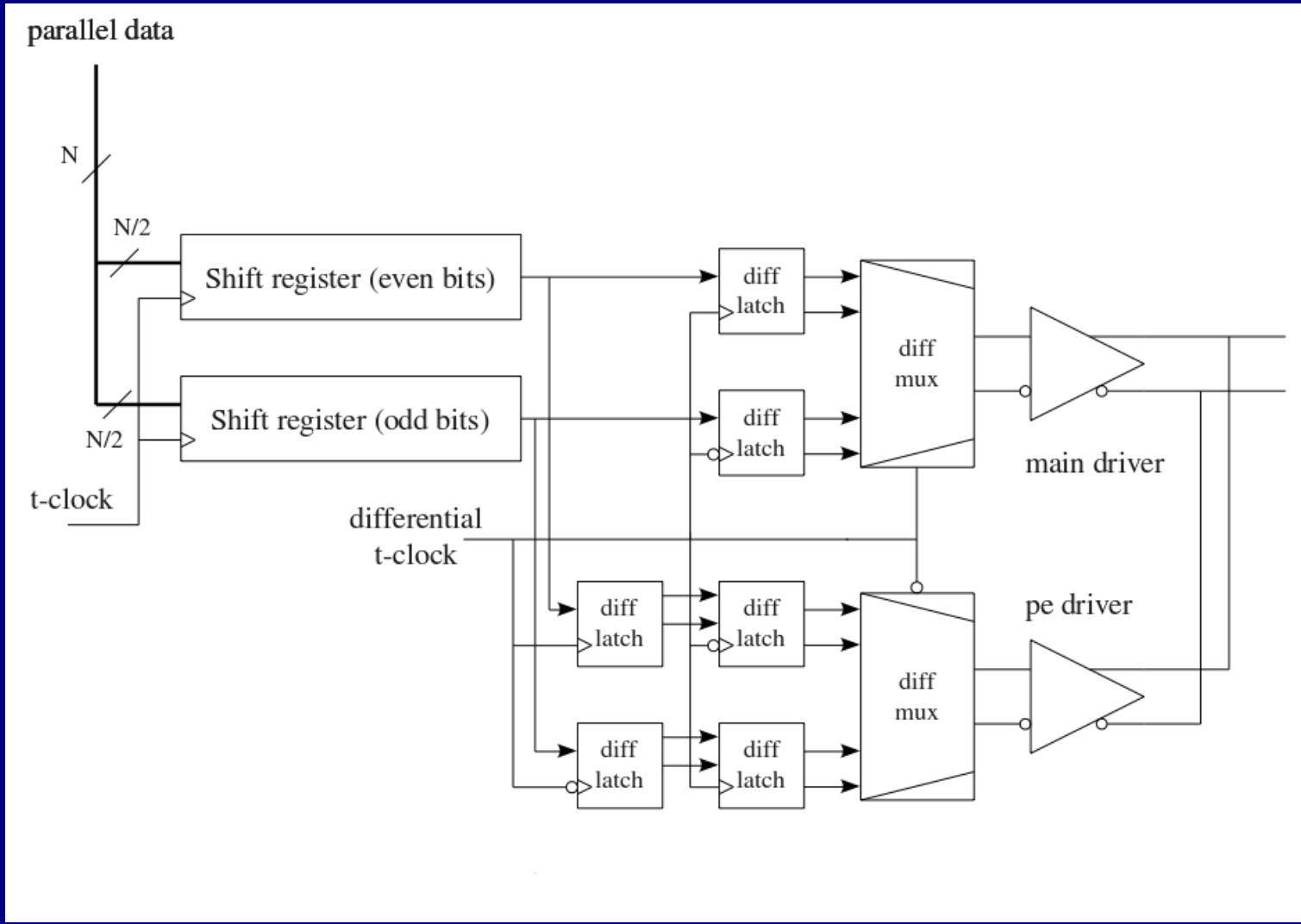
- Set mainly by the loop filter
- Related items :
  - Lock time
  - Input frequency tracking performances
  - Input jitter rejection
- *Optimum value strongly depends on the application*

Serializer

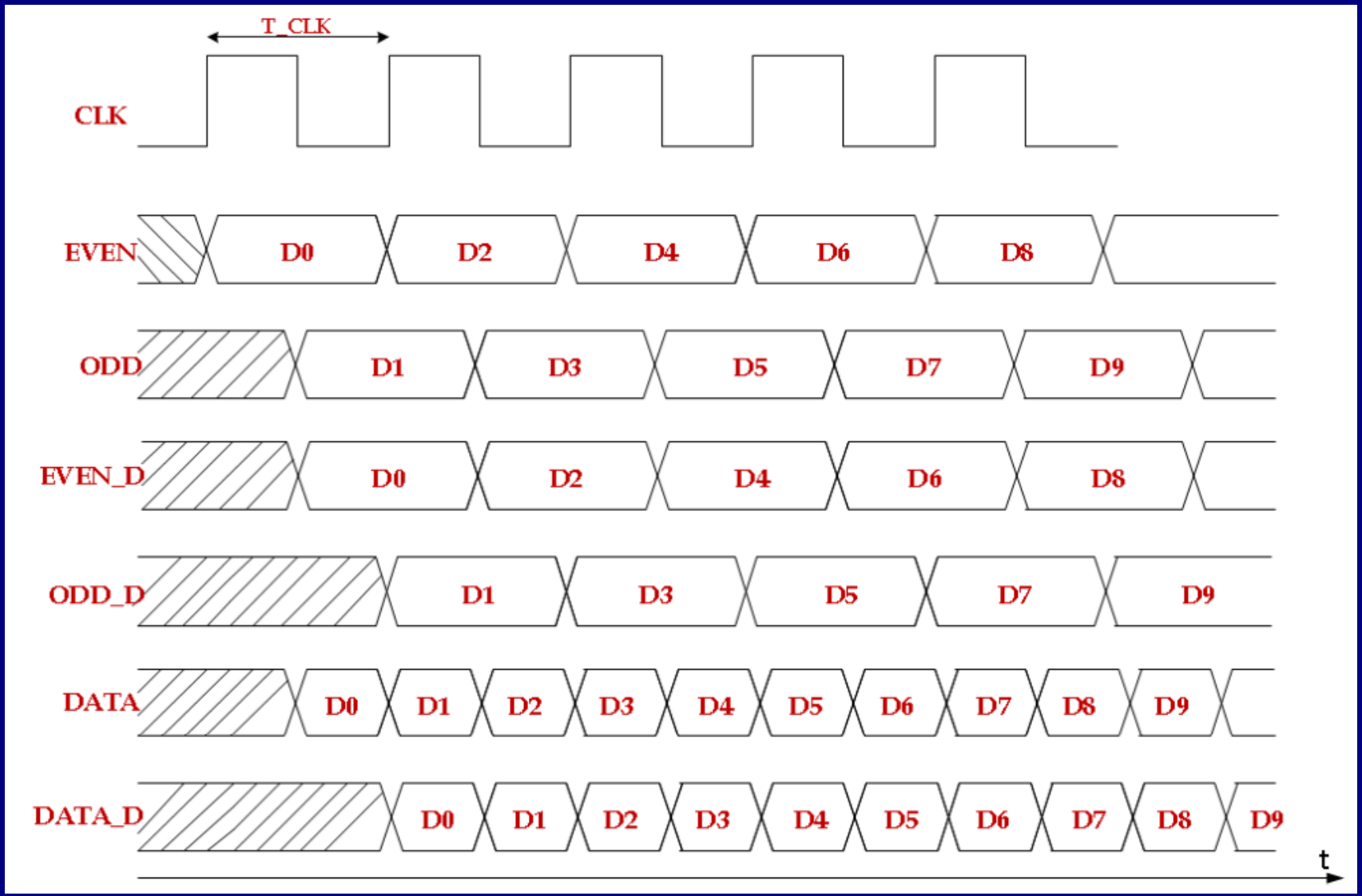
- Usually based on SC shift register in deep submicron technology
- Double Data Rate as a technique to double the data rate with the same clock
- Single Event Upset issues



DDR Serializer with pre-emphasis

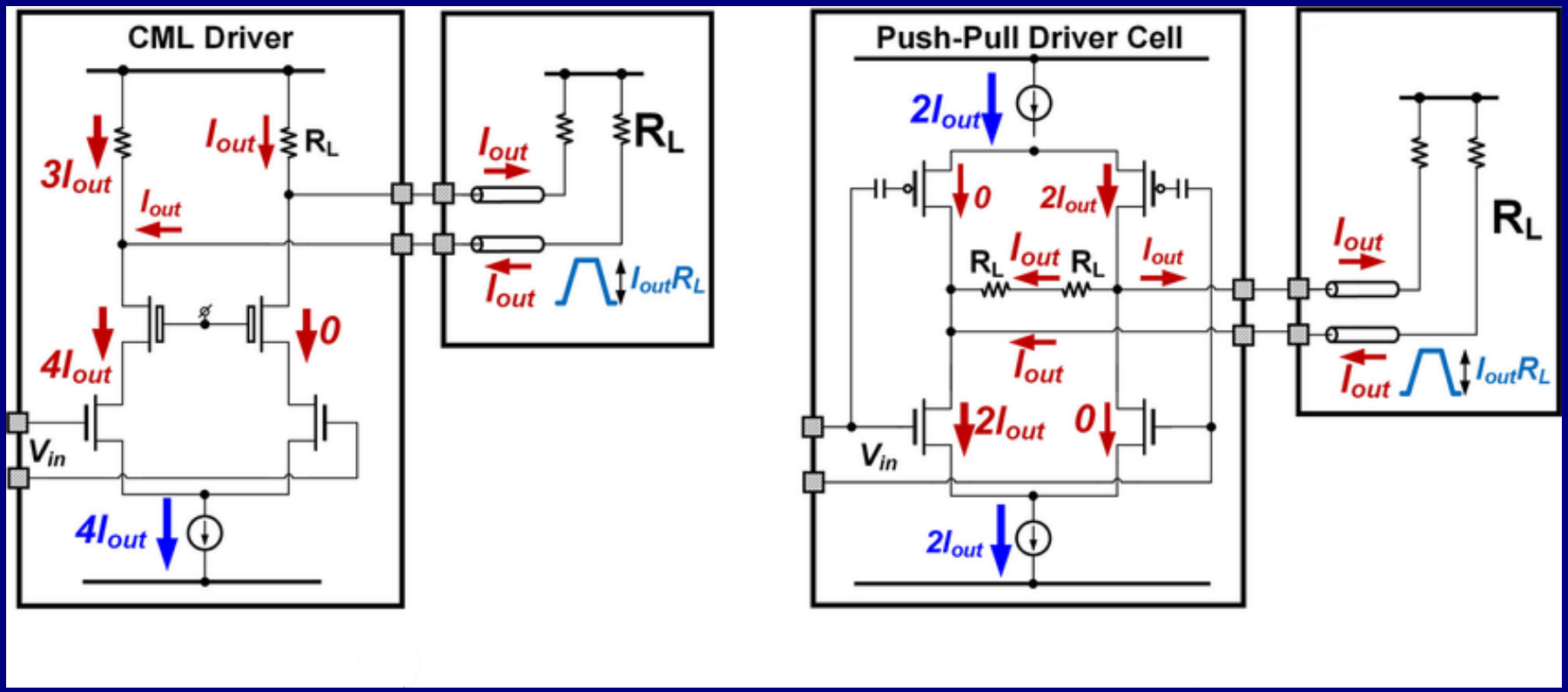


DDR Serializer timing



Differential driver architectures

- CML
- Push-pull (LVDS-SLVS)



Drivers : critical points

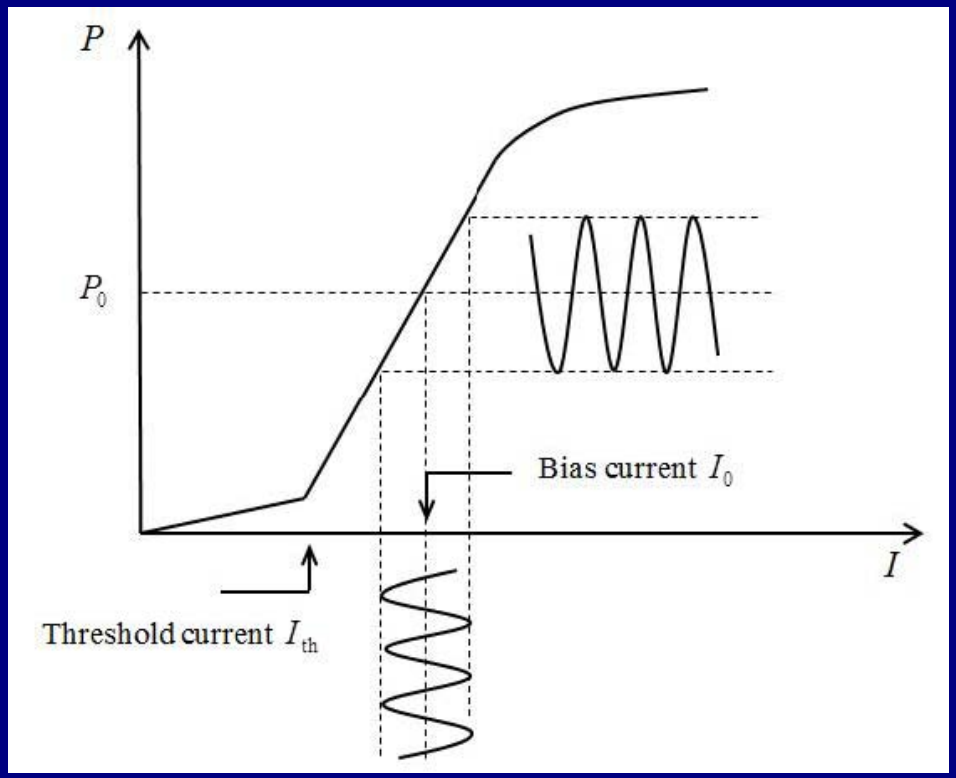
- Input termination
  - Termination efficiency *vs* power consumption
- AC connection
  - V_{CM} independence *vs* output stage bias
- Load termination

Laser diodes

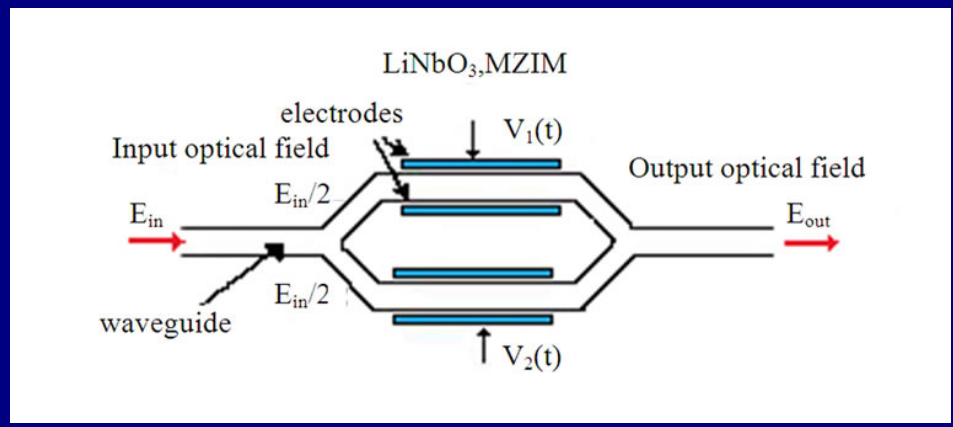
- Edge emitting lasers
  - Bias and modulation currents : tens of mA
  - Dynamic impedance : $\approx \Omega$
- Vertical Cavity Surface Emitting Lasers
  - Bias and modulation currents : mA
  - Dynamic impedance : $\approx$ tens of Ω
- Modulation :
  - On-off modulation : hundreds of MHz
  - Over threshold modulation : up 10 10-20 GHz
  - Mach Zender modulation : above 20 GHz

Laser modulation

Direct modulation



Mach Zender modulation



Laser driver issues

- High speed
- High driving current
- High voltage swing (problems with deep submicron technologies)
- Radiation issues (radiation-induced threshold current increase)