Front-end electronics for large arrays of macro-bolometers

P. Carniti[a] on behalf of the CUORE and CUPID collaborations

a - INFN and University of Milano Bicocca, Piazza della Scienza 3, I-20126, Milan (Italy) - paolo.carniti@mib.infn.it

The search of neutrinoless double beta decay with macro-bolometers

Underground bolometric experiments offer unique opportunities for the study of neutrinoless double beta decay and other rare decays.

Among the current generation experiments, CUORE is the first one reaching the 1-ton scale, thanks to an array of 988 TeO_2 crystals. Detector optimization phase is currently on-going and data taking will follow.

CUORE update, CUPID, will enhance the concept of large scale bolometers adding particle identification by detecting the light produced in the interactions, greatly improving the background rejection and thus increasing the sensitivity. The first demonstrator, CUPID-0 is also finishing pre-operation phase.

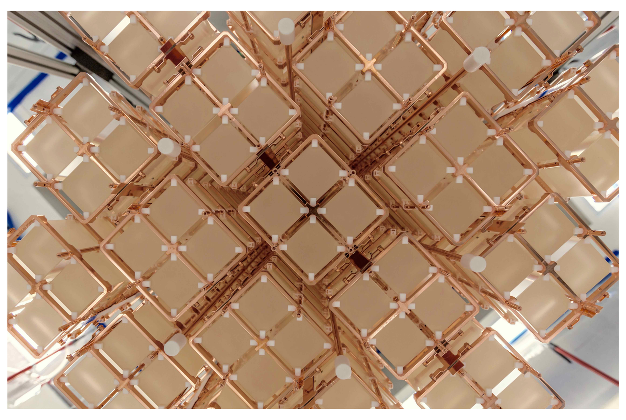

Figure 1: CUORE towers from below

Figure 2: CUPID-0 detector detail

Bolometer readout

Bolometers detect any energy deposition in the absorber by producing a small temperature rise, typically few hundreths of μK per MeV.

In order to read out this signal, a temperature sensor is glued to the absorbers. CUORE and CUPID-0 adopt Germanium NTD thermistors for this purpose.

When biased with a constant and stable current, the change of resistance due to the temperature rise is converted to a voltage signal smaller than 1 mV for a typical 2.6 MeV event.

The electronic readout system has to amplify this signal while maintaining adequate signal-to-noise ratio and high stability over time.

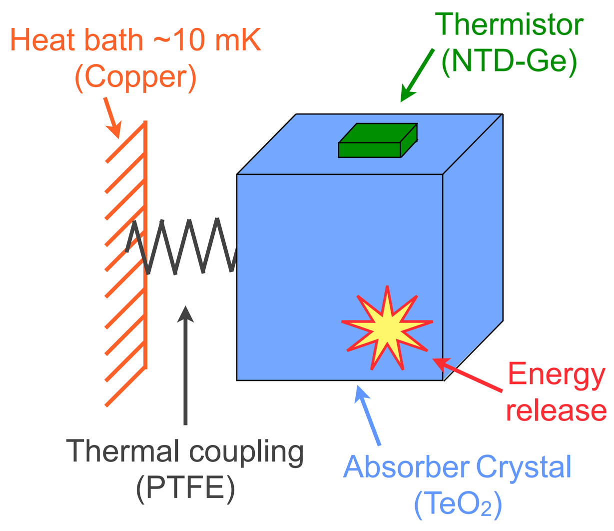

Figure 3: Schematic picture of a bolometric detector

Preamplifier

The fully differential voltage preamplifier is responsible of the first stage of the voltage signal amplification.

It is based on a JFET-input pair with selected components for fulfilling the low noise requirements in the bandwidth of the signal (0.1-10 Hz region).

Offset, drift and common-mode rejection are automatically adjusted or calibrated by the maiboard hosting the preamplifiers.

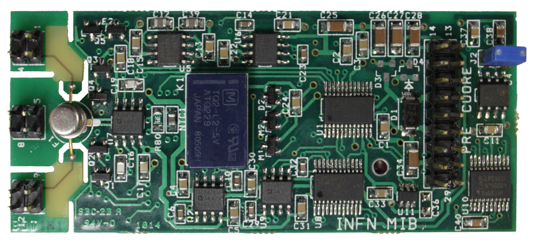

Figure 5: Photograph of the preamplifier

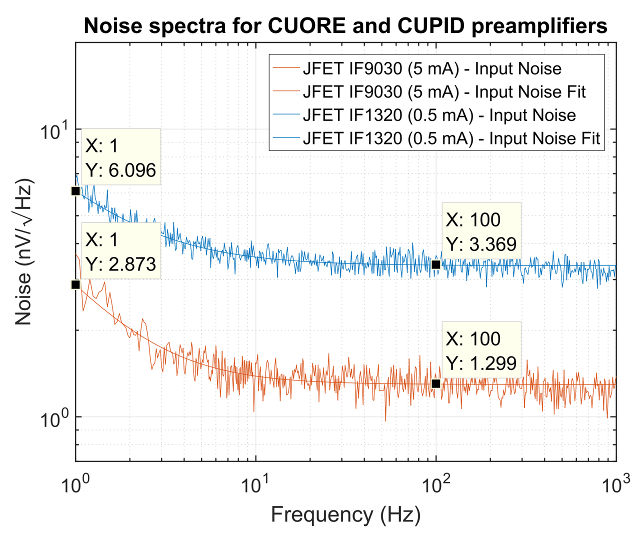

Figure 6: Input voltage noise of CUORE (blue) and CUPID (red) preamplifiers

Mainboard

The mainboard hosts 6 pramplifiers and is responsible of the second stage programmable gain and detector biasing, plus offset, drift and common-mode rejection adjustments.

Precise and low noise voltage references are provided by a linear power supply installed in the mainboard card cage.

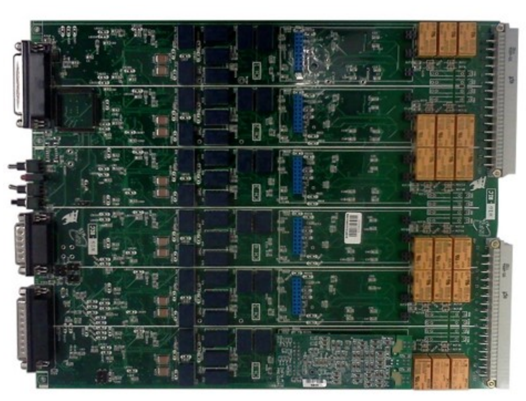

Figure 9: Photo of the mainboard

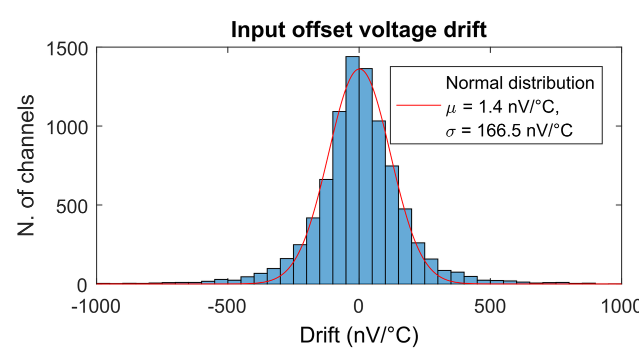

Figure 10: Input offset voltage drift for all channels

Antialiasing filter

Before being digitized by the 18-bit DAQ, signals are filtered by an active 6-pole Bessel-Thomson filter to suppress high frequency noise and avoid aliasing.

The filter has 4 programmable cut-off frequencies for detector optimization (15, 35, 100 and 120 Hz).

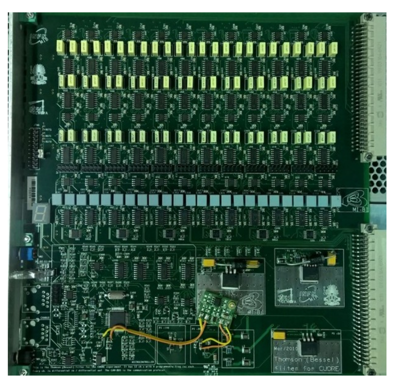

Figure 11: The Bessel filter

Electronic readout scheme

Several topologies were evaluated (cold/warm preamplifier, AC/DC readout, etc).

The final scheme is shown in Figure 4 and the main features are summarised here.

- *Room temperature preamplifier:* simpler and more flexible solution. The increased stray capacitance is not critical due to the low bandwidth of the signals (0.1-10 Hz range).
- *Differential readout:* best suppression of common mode and microphonic noise.
- *DC readout:* expected NTD working point is around 100-200 MΩ for CUORE, giving an intrinsic NTD series noise of about 10 nV/√Hz at 10 mK. This makes DC reading at room tempreature feasible with an accurate design of the preamplifier and selection of the input JFET. Parallel noise is minimized selecting high value load resistors (60 GΩ). For CUPID, lower NTD resistances are expected, thus lowering preamplifier series noise with a larger JFET biased with higher current is beneficial.

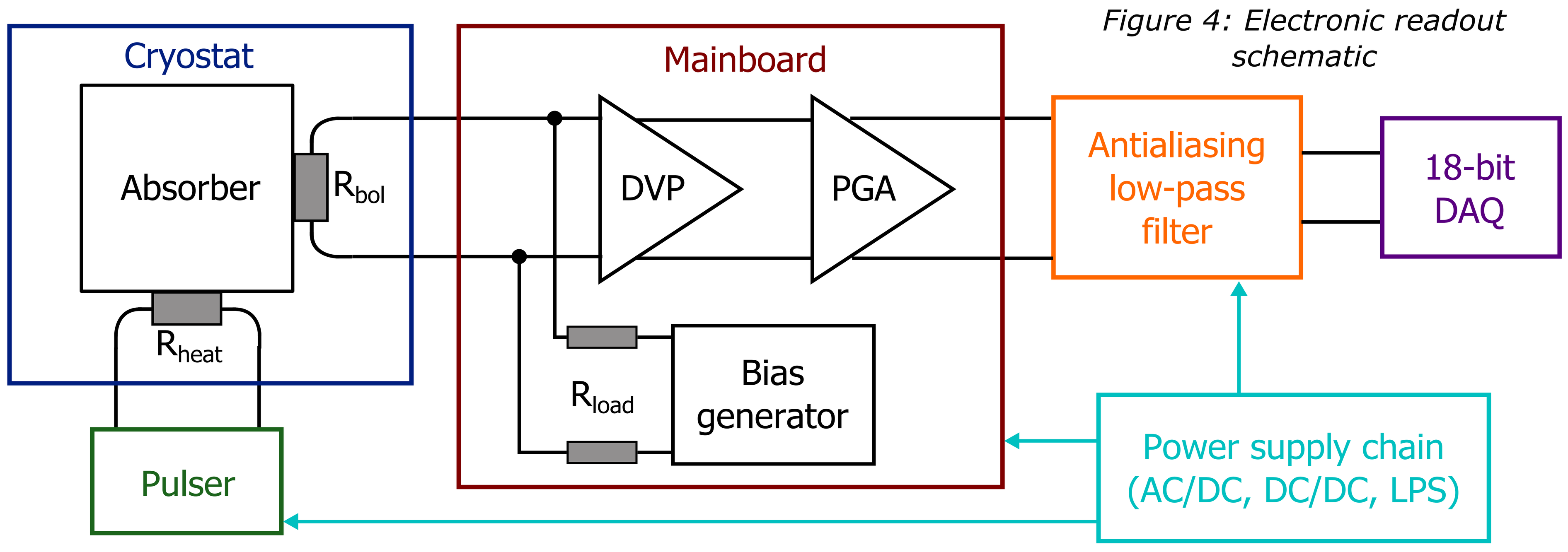

Figure 4: Electronic readout schematic

Calibration pulser

The detector response is periodically calibrated injecting voltage pulses through a heater resistance glued to the crystal.

These pulses are generated by a low noise, low jitter and high stability pulser board. Pulse width jitter is below 1 ppm, while pulse amplitude thermal drift is <0.3 ppm/°C.

A dedicated pulser board is also responsible of the stabilization of the cryostat temperature with a PID algorithm.

Figure 7: Photograph of a 4 channel pulser board. Each channel is connected to several heaters in parallel

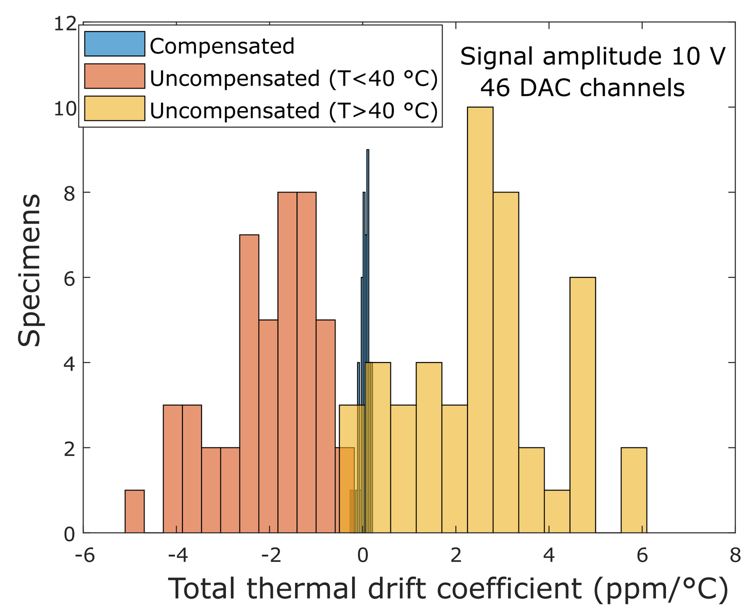

Figure 8: Pulse amplitude thermal drift coefficient before and after calibration

Power supply

The power supply chain consists of 3 stages. A commercial AC/DC converter generates the 48V DC voltages fed into the next stage, a custom low noise and insulated DC/DC converter. For noise-critical boards (mainboard and pulser) a further linear power supply provides even better filtered and stabilized voltages.

Figure 12: Power supply racks

First pulses

The electronic readout systems for CUORE and CUPID-0 detectors already passed successfully the commissioning phase and they are both fully operational.

The first pulses were recorded and detectors are approaching the data taking phase.

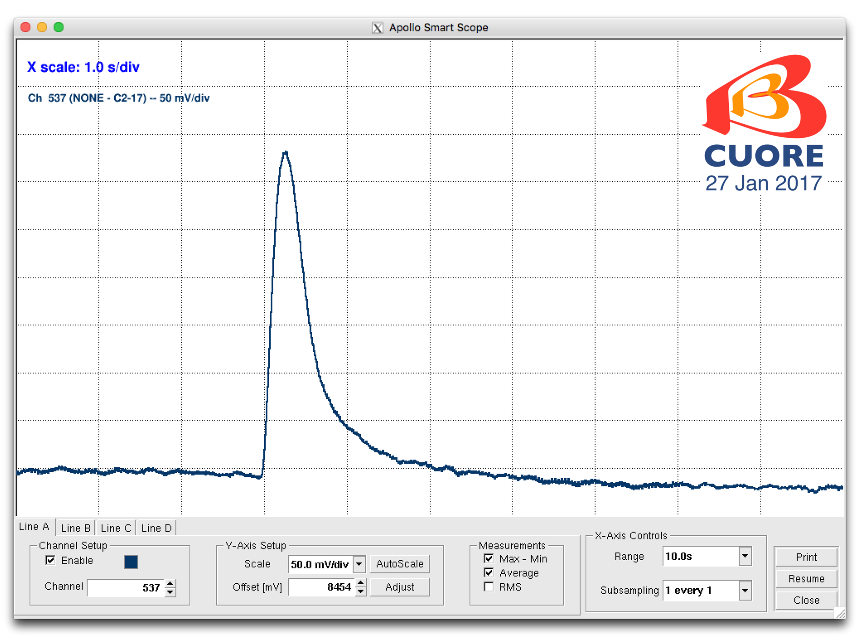

Figure 13: CUORE first pulse

NeuTel 2017 - XVII International Workshop on Neutrino Telescopes   Palazzo Franchetti, Venice (Italy), 13-17 March 2017