Total Dose Effects in Electronic Devices and Circuits

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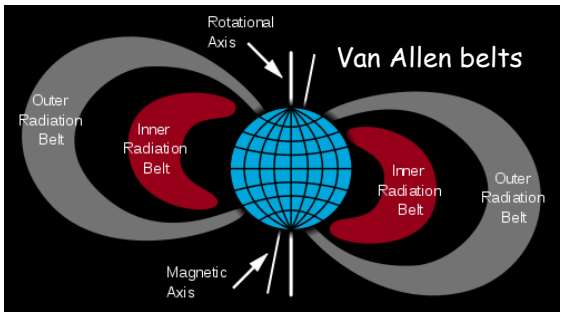
Outline

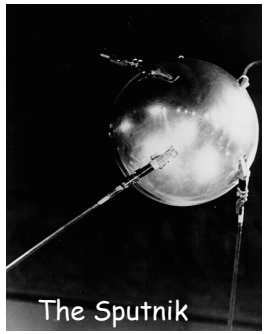
- Introduction
- Radiation environments
- Radiation effects in electronic devices
- Radiation-resistant technologies and hardening techniques

Introduction

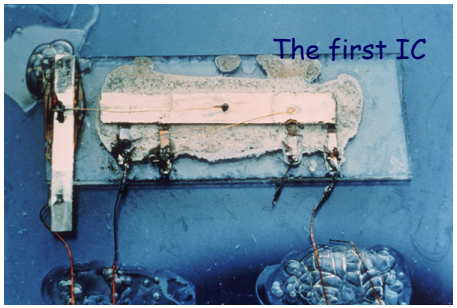
- From a historical standpoint, the study of radiation effects in electronic circuits started in the early 60's mainly as a response to two concerns:
  1. the increasing demand for hardened electronics that could survive the impact of a nuclear explosion (nuclear arms race was in full swing at the time)
  2. the discovery of radiation belts by Van Allen and Vernov and the resulting need for protection from them (in the wake of early space exploration)



- The first steps of electronics can be dated back to about the same period: the first satellite (Sputnik 1, 1957) appeared at the same time as the first integrated circuit in germanium (1958); the metal-oxide-semiconductor (MOS) transistor was born in 1960, just the same year as the first interplanetary space probe Pioneer; the Apollo program was a contemporary of the first 256-bit computer memory



- The advance in the microelectronics field, at a pace that has never abated since its debut, has made the use of electronic devices ever more attractive, even for applications in hostile environments



Introduction

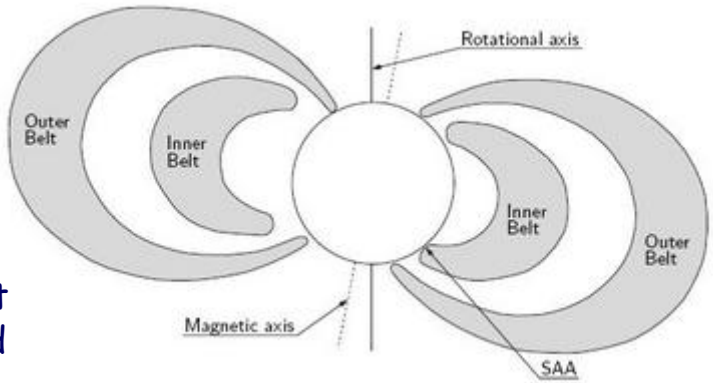
- Electronic circuits are used in several fields where a more or less high degree of radiation tolerance is required: space and avionic applications, high energy physics experiments, nuclear and (still experimental) thermonuclear power plants, medical diagnostic imaging and therapy, industrial imaging and material processing
- When operated in these environments, solid-state devices and integrated circuits may be directly struck by photons, electrons, protons or heavier particles; alteration of their electrical properties may cause an electronic subsystem to fail
- Depending on the type and characteristics of the impinging radiation, different effects, either irreversible or (partially or totally) reversible, may arise
- Knowledge of the mechanisms underlying the radiation response of electronic devices is of paramount importance for
  1. devising hardness assurance methodologies to guarantee that the tested devices can work reliably in the target environment
  2. developing rad-hard circuits and design techniques to improve the tolerance of electronic circuits to specific effects of radiation in some specific applications

Radiation environments

Semiconductor devices and integrated circuits are nowadays operated in a number of hostile environments

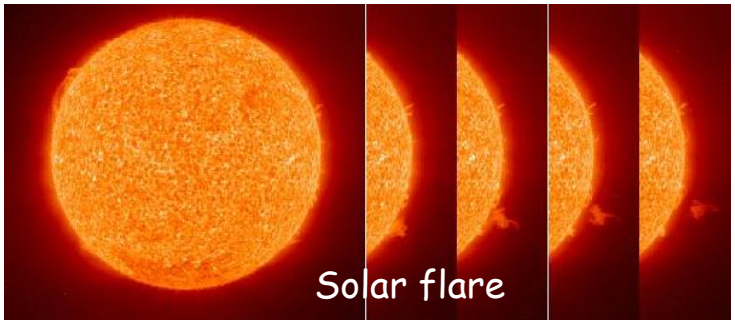
Space environment

- The Earth and its immediate surroundings are protected by the atmosphere, which acts as a semi-permeable shield letting through light and heat while stopping radiation and UV's; because no such protection is available in space, human beings and electronics (onboard Earth orbiting satellites, space shuttles, space probes) must be able to cope with the resulting set of constraints
- **Radiation belts**: the idea that particles trapped stably in the geomagnetic field formed "belts" (geometrically speaking, taking the form of a torus) of intense radiation was first advanced in 1958 by Van Allen in US and Vernov in the Soviet Union
  - Particle trapping in the inner belt (consisting mainly of energetic protons, 800 to 6000 km above the Earth surface) is caused by neutron decay resulting from the interaction of heavy ions or protons with the Earth atmosphere; in the outer belt (mainly including electrons, 2500 to 36000 km above the Earth surface), particles are trapped directly from the solar wind
  - Energy can reach 30 MeV in the case of trapped electrons, about 400 MeV in the case of protons; the flux, both for electrons and protons, is a function of the altitude and energy and can get as high as 10^{10} $cm^{-2}s^{-1}$



Space environment

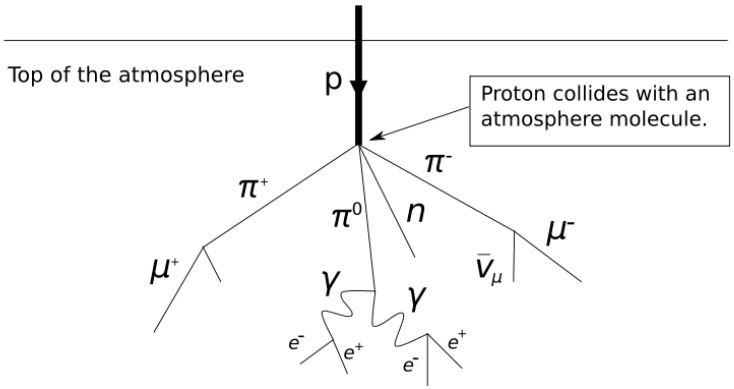
- **Solar activity**: since the launching of artificial satellites, solar activity, featuring an 11 year (sun spot) cycle modulated by an 80 year (Gleissberg) one, has been correlated with particle fluence level
- Two main event categories:
  - **coronal mass ejections**: emit mainly protons with energy up to several hundred MeV
  - **impulsive events (e.g., solar flares)**: involve large emissions of heavy ions, with energies up to hundreds of GeV per nucleon



- **Cosmic rays**: their true nature being still under investigation, cosmic rays consist of protons, He nuclei, electrons and heavy ions, with energies as high as 10^{21} eV
- **Solar wind**: consists of a radial flow of solar gas from the Sun arising from evaporation of the coronal plasma; the solar corona temperature reaches several million of degrees, resulting in its electrons escaping the Sun gravity; the consequent charge imbalance leads to flights of protons and ions into interplanetary space, at a speed of about 400 km/s (corresponding to 1 eV for electrons and a few keV for protons)

Earth environment

- As early as 1984, it was predicted that **atmospheric neutrons** would cause single event upsets in electronic devices; the first in-flight upset was actually observed in 1992 and, after that, several hundreds have been recorded
- Cosmic rays cover a large spectrum of energies, with a comparatively high flux in the 100 MeV to 10 GeV range and a peak around 500 MeV; cosmic particles collide with the nuclei of atoms making up the Earth atmosphere and initiate the so-called air showers, producing particles such as neutrons, protons, muons, pions, electrons and gamma-rays



- Analysis of particle flux as a function of the distance from the Earth surface shows a predominance of neutrons at the altitude where the aircraft flights take place
- Atmospheric protons play a minor role while, on the other hand, the impact of heavy ions is strongly mitigated by the atmosphere

Military environment

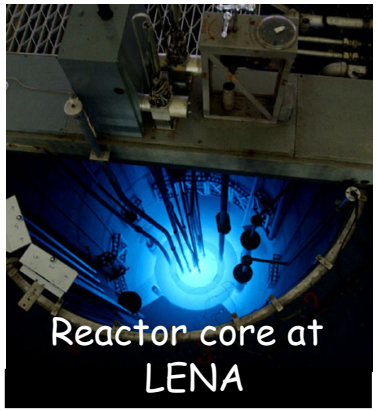
- The huge amount of energy released by a fission (atomic) weapon or a fusion (hydrogen or thermonuclear) weapon, is the result of nuclear rather than chemical reactions
- A significant portion of the weapon energy is released as X-ray, another part goes into plasma kinetic energy (the temperature achieved during nuclear reactions is of the order of a hundred million degrees) and a small amount is carried by neutrons and fission gamma-rays.
- In case of an explosion occurring above the Earth atmosphere, two possible scenarios may be considered
  - Aerospace systems operating at altitudes higher than 50-100 km will be directly submitted to the radiation emitted by the weapon; hard X-rays, gamma-rays and neutrons all have a significant impact on the electronic systems onboard satellites
  - The main indirect effect to be considered is that related to trapping by the Earth magnetic field lines of electrons from fission debris, resulting in the formation of highly stable, artificial radiation belts which can deliver much higher radiation doses to satellites than natural belts; the first satellite failure due to radiation effects dates back to 1963, to the Starfish test (a 1.4 Mton thermonuclear bomb detonated at an altitude of 400 km); the test produced an intense radiation belt destroying seven satellites over seven months, primarily because of dose effects on their solar panels; the TELSTAR satellite, launched on July 10, 1962, broke down in February 1963

Military environment

- A nuclear explosion in the Earth atmosphere, besides a variety of mechanical effects, is responsible for different purely radioactive effects, which can be split into two main categories
  - Initial nuclear radiation (INR) is that released within less than a minute after detonation; X-rays are quickly stopped (at about 500 m above sea) so that gamma-rays (responsible for ionizing dose effects) and neutrons remain
  - Residual nuclear radiation (RNR) features several radiation sources; fission products, radioactivity of debris (neutron-activated weapon materials), that of unfissioned uranium and/or plutonium and activation of the environment; a further distinction can be made between local fallout, occurring less than 24 hours after explosion, with a resulting significant level of ground radiation, and worldwide fallout, which can take place at significant distances from the place of explosion

Commercial nuclear industry and power plants

- In today commercial nuclear industry, there is a growing demand for remote handling and inspection equipment for operation in radiation environments; such environments are associated with nuclear power generation in fission and (still experimental) fusion reactors
- **Fission-based nuclear power** has undergone spectacular development since the oil crisis in the 1970s; the relevant radiation environments are associated with the various stages in the nuclear power cycle:
  - **fuel fabrication plants**: relatively low energy (several tens to several hundreds of keV) photon radiation, with doses below the sensitivity levels of electronic devices
  - **fission reactors**: mainly gamma-rays and neutrons, with dose rates (up to 1 Grad/h) and fluxes (up to 10^{13} 1Mev neutrons $cm^{-2}s^{-1}$) strongly dependent on the distance from the core and on the operation of the reactor
  - **spent fuel reprocessing facilities**: take care of activities like handling of spent fuel, mechanical cutting and washing, chemical treatment, separation of waste and fission products, packaging and storage or waste removal; dose rates may range from those of background radiation to just behind the values recorded in the core of a working reactor (1 Grad/h)
  - **radioactive waste storage**: permanent storage of very high level, solidified waste implies complex shielding, surveillance and teleoperated devices; vitrified waste management involves active elements in concentrated form and dose rates of up to 1 Mrad/y
  - **power plant dismantling and decommissioning**: old nuclear power plants need to be revamped or dismantled; robots and other teleoperated systems involved in such activities may have to withstand doses as high as 1 Mrad


Reactor core at LENA

Commercial nuclear industry and power plants

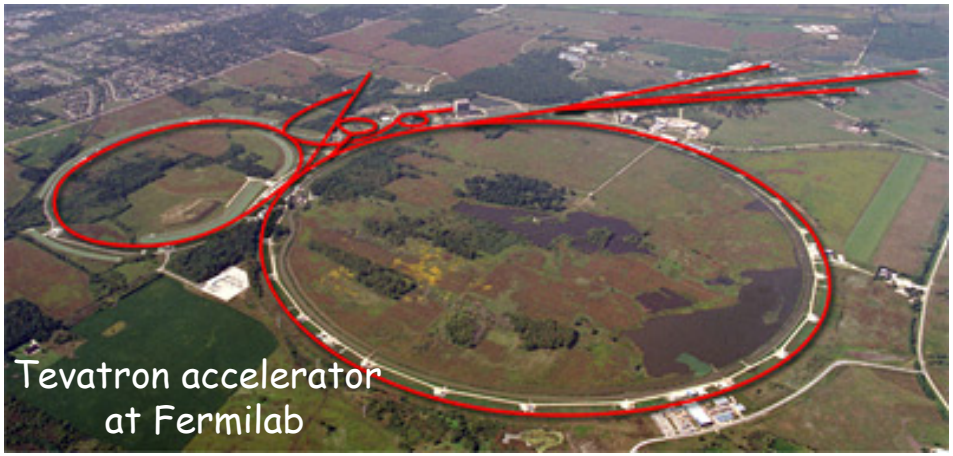
- **Controlled thermonuclear fusion** is still at the experimental stage; two approaches to this technique are currently being explored:
  - **magnetic confinement fusion**: typical radiation levels for a TOKAMAK reactor goes from 100 Mrad/h for gamma-rays and 3×10^{14} 1MeV neutrons $cm^{-2}s^{-1}$ for neutrons inside the reactor to about 1 rad/s and 10^5 1MeV neutrons $cm^{-2}s^{-1}$ on the external surface of the shield; in the design of the remote manipulators for the ITER (international thermonuclear experimental reactor) project, a total dose of 10 Grad was credited
  - **inertial confinement fusion**: in an inertial confinement experiment, a deuterium-tritium target is made to implode by means of extremely powerful laser beams; since the energy is released in a very short time (~100 ps), the radiation environment features extremely high dose rates, $\sim 5 \times 10^{11}$ rad/s for neutrons and 3×10^{10} rad/s for gammas, which must be taken into account in designing measurement devices for plasma diagnostic

Model of the ITER vacuum vessel

High energy physics research environment

- Particle accelerators were developed in the first half of the XX century (thanks to the pioneering work of Van de Graaf, Cockroft, Walton and Lawrence) as a way to overcome the limitations of natural radiation sources and produce artificial particles

- In the most recently fabricated machines (like the Tevatron at Fermilab, USA, and the LHC in Geneva, Europe), particles can be made to smash into each other with energies in the TeV scale

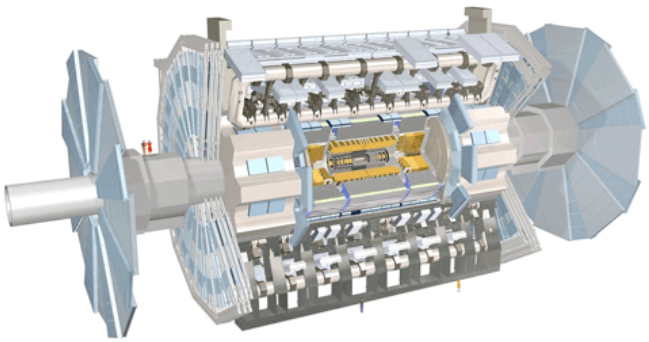

Tevatron accelerator at Fermilab

- Used in fundamental physics research, modern large accelerators can afford such high intensities to produce many types of radiation with potential damage for electronic components and surrounding materials

- Detectors and the relevant readout electronics located close to the interaction points have to survive the hostile environment preserving acceptable sensitivity performance over the entire experiment duration or for a significant part of it before being replaced

High energy physics research environment

- **Circular electron colliders**: electron colliders (like the LEP, the large electron positron collider, used at CERN until 2000) generate intense synchrotron radiation from which protection is required; the yearly absorbed dose for electronics may be at most of the order of 100 krad
- **Hadron colliders**: accelerate protons and heavy ions and feature negligible synchrotron radiation; beam losses (due to interaction with residual gas and/or machine components) are the main source of radiation, with maximum yearly absorbed dose values of 1 krad for the auxiliary electronics
- **Detector environments**: large detectors for high energy physics experiments consist of huge cylinders placed at selected beam interaction points, at whose centers the desired collisions take place; for instance, the zoo of secondary particles from proton collisions at the LHC gives rise to a severe radiation environment for detectors and the associated electronics, yielding a radiation level of 2.5 Mrad/y, in terms of dose equivalent, and of 8×10^{13} 1MeV neutrons $cm^{-2}y^{-1}$ in terms of displacement equivalent



ATLAS detector at the LHC

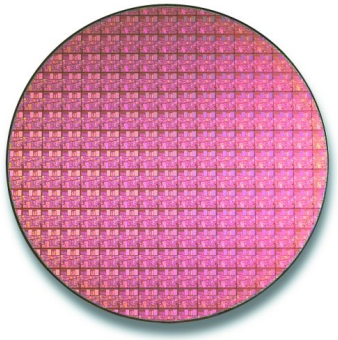
Medical and industrial applications

- Radiation sources are widely used for diagnostic instrumentation, both for medical and industrial applications, and for medical treatment; also many industrial processes involve some kind of material irradiation
- **Protontherapy and hadrontherapy**: hadrontherapy centers are more and more being included in existing hospital facilities; by taking advantage of the so called Bragg peak, hadrontherapy machines can deliver dose more selectively to a given region of the body; proton therapy makes use of beams with high intensities (up to several hundreds of nanoamperes) and energy ranging from 60 to 250 MeV; electronic equipment is exposed to several tens of krad per year of ionizing radiation and to single event upsets (SEU) induced by scattered protons and neutrons (featuring a much larger flux than in the case of atmospheric neutrons)

Proton treatment of a patient at the Loma Linda center

Medical and industrial applications

- Other industrial sectors use irradiation treatment
  - **food irradiation** (e.g., fruit, vegetables)
  - **medical irradiation** (sterilization of instruments and equipment)
  - **waste and water treatment**
  - **radiation-assisted polymerisation**
  - **microelectronic processing** (e.g., ionic implantation)



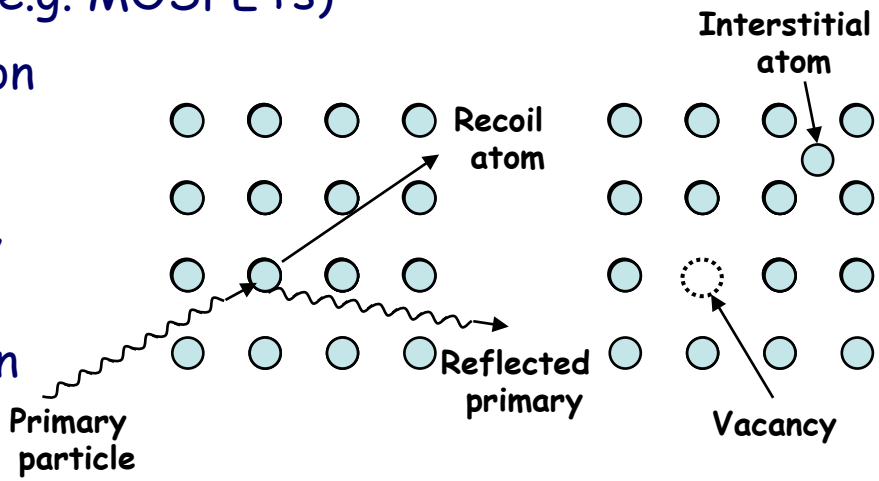
Silicon wafer

Radiation effects in electronic devices

Effects of radiation may change depending on the particular operating principle of the considered electronic device

Basic damage mechanisms in semiconductor devices

- Despite the complexity of the interaction processes and their dependence on the properties of the incident particle and of the target material, two are the basic radiation damage mechanisms affecting semiconductor devices
- **Ionization damage**: takes place when energy deposited in a semiconductor or in insulating layers, chiefly SiO_2, frees charge carriers (electron-hole pairs), which diffuse or drift to other locations where they may get trapped, leading to unintended concentrations of charge and parasitic fields; this kind of damage is the primary effect of exposure to X- and γ-rays and charged particles; it affects mainly devices based on surface conduction (e.g. MOSFETs)
- **Displacement damage (DD)**: incident radiation dislodges atoms from their lattice site, the resulting defects altering the electronic properties of the crystal; this is the primary mechanism of device degradation for high energy neutron irradiation, although a certain amount of atomic displacement may be determined by charged particles (including Compton secondary electrons); DD mainly affects devices based on bulk conduction (e.g. BJTs, diodes, JFETs)



Displacement effect in a bidimensional crystal

Basic effects of radiation damage

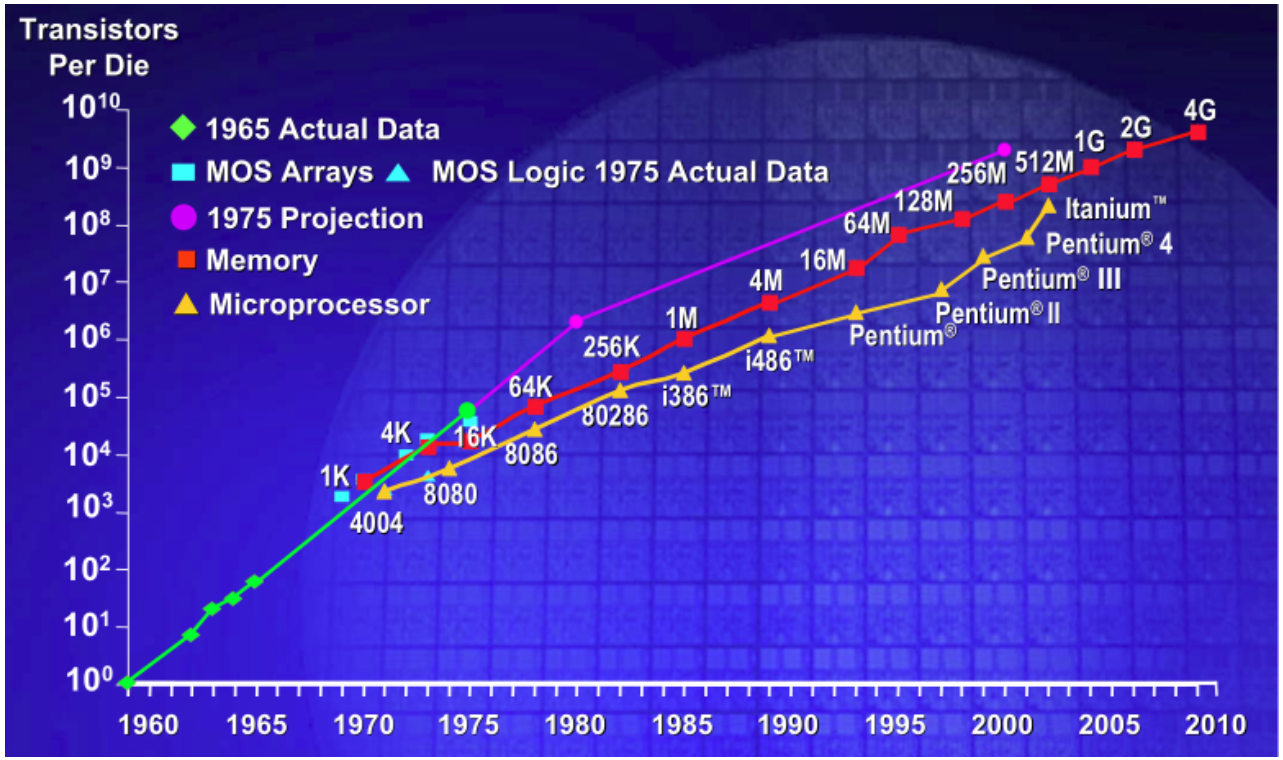
- Effects of radiation in semiconductor devices can be included in one of two broad classes
- **Total dose (TD) effects**: are due to the progressive build-up of trapped charge in insulating layers or at the Si/SiO_2 interface (as a consequence of ionization phenomena) or of defects in the bulk of the devices (originating from accumulation of displacement events)
- **Single event effects (SEE)**: are due to charge deposition induced by a single particle that crosses a sensitive device region; the effects may lead to destructive or non-destructive damage of the device
  - SEEs occur stochastically, while TD is cumulative and may become visible after the device has been exposed to radiation for some time
  - TD is usually related to long term response of devices, whereas SEE is concerned with short time response
  - Only a tiny part of the device is affected by SEE, corresponding to the position of the particle strike, while TD uniformly affects the whole device, because it results from the effect of several particles randomly hitting the device
  - As far as SEE is concerned, the most important figure is the rate of occurrence; TD is characterized by the maximum drift of the main device parameters

Radiation effects in MOSFETs

Metal oxide semiconductor field-effect transistor (MOSFET) technology has become dominant in the fabrication of integrated circuits (in particular digital) because it enables the design of very high density, low power systems

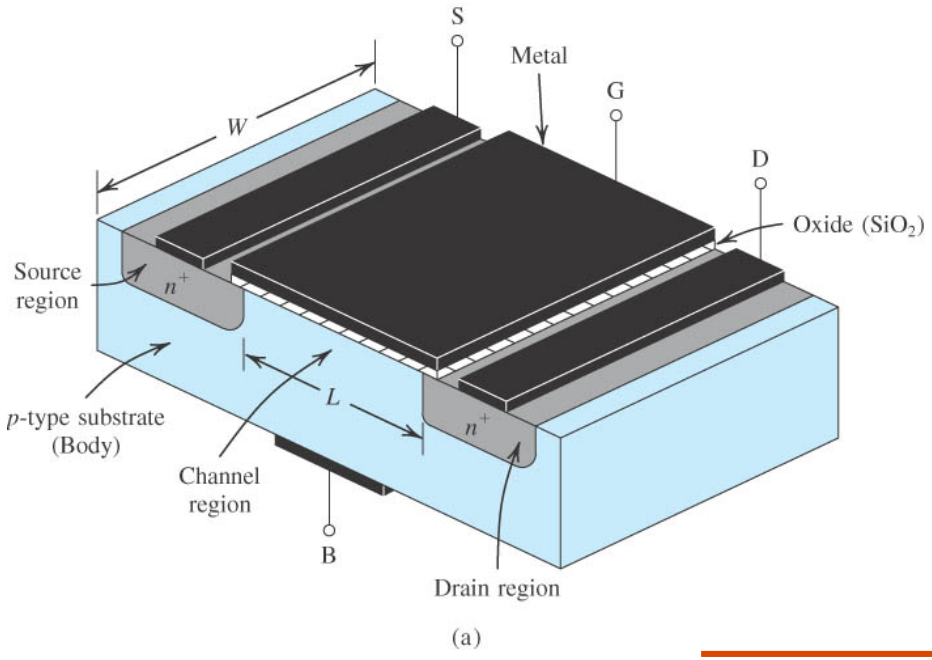
CMOS technologies

- CMOS (complementary MOS) technologies have become dominant in the area of digital integrated circuits because they enable the design of very high density and low power systems
- The development of CMOS processes has been driven by the fast growth of the computer and communication market (ICT, information and communication technology)
- For example, the number of transistors integrated in a microprocessor has increased in the past years at an exponential pace not so far from Moore's prediction, who said that the number of transistors on a chip would double every two years

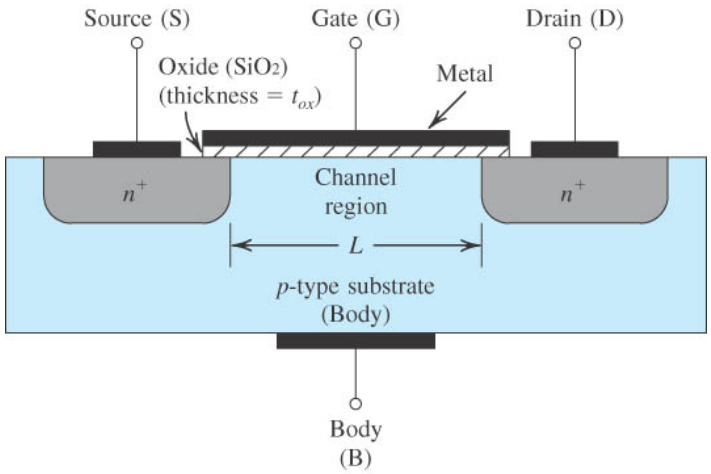


The MOSFET transistor

- MOS transistors come in two flavors, N-type (using electrons as carriers) and P-type (where the current flowing in the device channel is made of holes)
- Fabrication of CMOS transistors requires a sequence of processing steps, performed on a silicon wafer (generally less than 1 mm thick and 30 cm in diameter) including ion implantation, thermal cycling for diffusion and damage annealing, deposition of oxides, metal strips and masking layers and selective attack of the wafer surface (etching)



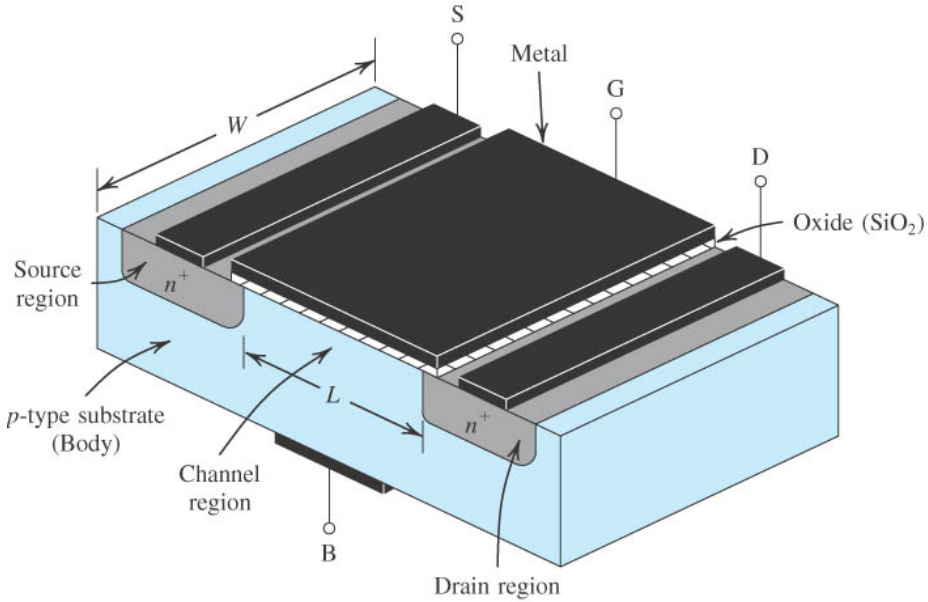
(a)

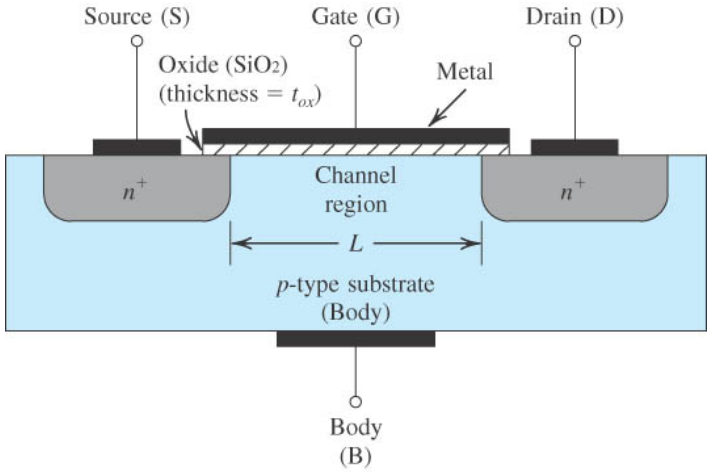


(b)

Operation of the MOSFET transistor

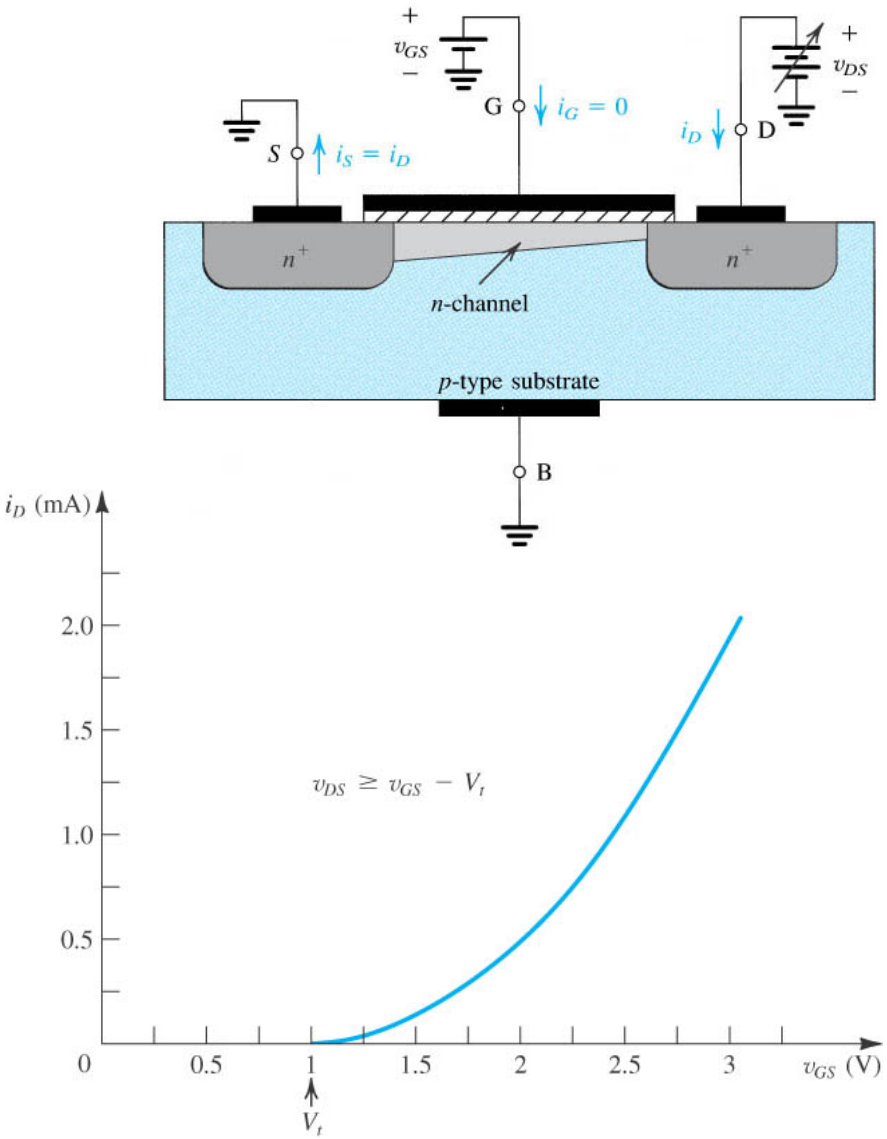
- In an enhancement mode NMOS device
  - heavily doped N-type source and drain regions, at the two ends of the device channel, are fabricated in a P-type substrate (often called the body)
  - a thin layer of silicon dioxide is grown over the substrate material and a conductive gate material (metal or polycrystalline silicon) covers the oxide between source and drain; during device operation, the gate-to-source voltage is used to control the current flowing between source and drain; this control can be used to provide gain in analog circuits and switching characteristics in the case of digital circuits
  - in general, the minimum value of the channel length L which can be achieved in a given technology is used to provide a measure of the lithographic limitations of the fabrication process





Operation of the MOSFET transistor

- In an enhancement mode NMOS device
  - if a positive voltage is applied to the gate terminal, at first free holes will be repelled from the region of the substrate under the gate, leaving behind a depleted region populated with bound negative charges (ionized acceptor atoms)
  - if the gate voltage is further increased, electrons from the n+ source and drain regions are attracted into the channel region; when a sufficient number of electrons has accumulated near the surface of the substrate under the gate, an N region is created, connecting the source and drain regions
  - if a voltage is applied between the drain and source, a current flows through this induced N region (also called inversion layer), carried by mobile electrons
  - the value of V_{GS} at which a sufficient number of mobile electrons accumulates to form a conducting channel is called **threshold voltage** and is usually denoted V_t



Total dose effects in MOSFET structures

- An MOS device exposed to an ionizing radiation environment typically suffers degradation in one or more of its parameters (threshold voltage, gate voltage to drain current gain, or transconductance, and channel leakage); changes may not be constant with time after irradiation and may depend on the dose rate

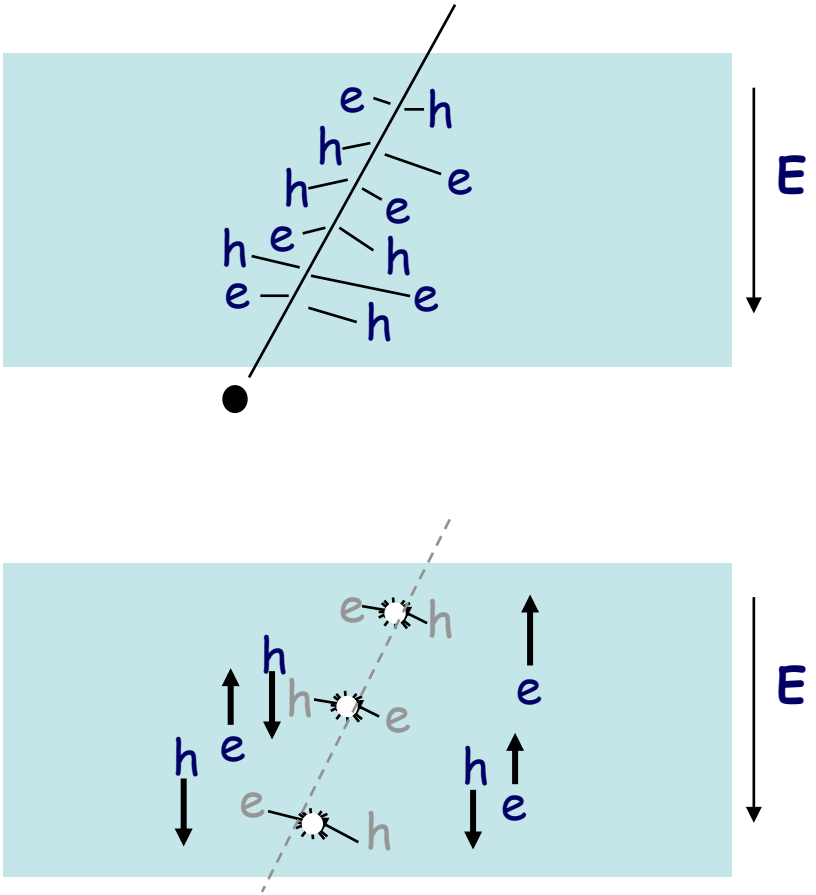
- An integrated CMOS circuit may slow down, show higher leakage (parasitic) currents, or even cease functioning properly (catastrophic failure)

- Damage responsible for these total dose effects occurs in the insulator layers (SiO_2) of the device structures and at the interface between the silicon substrate of the device and the oxide, and consists of three components:

  1. buildup of (positive) charge trapped in the oxide (the gate oxide and/or the field oxide, used to isolate devices from each other)
  2. increase in the number of interface traps
  3. increase in the number of traps in the oxide bulk

Carrier generation and transport in the oxide

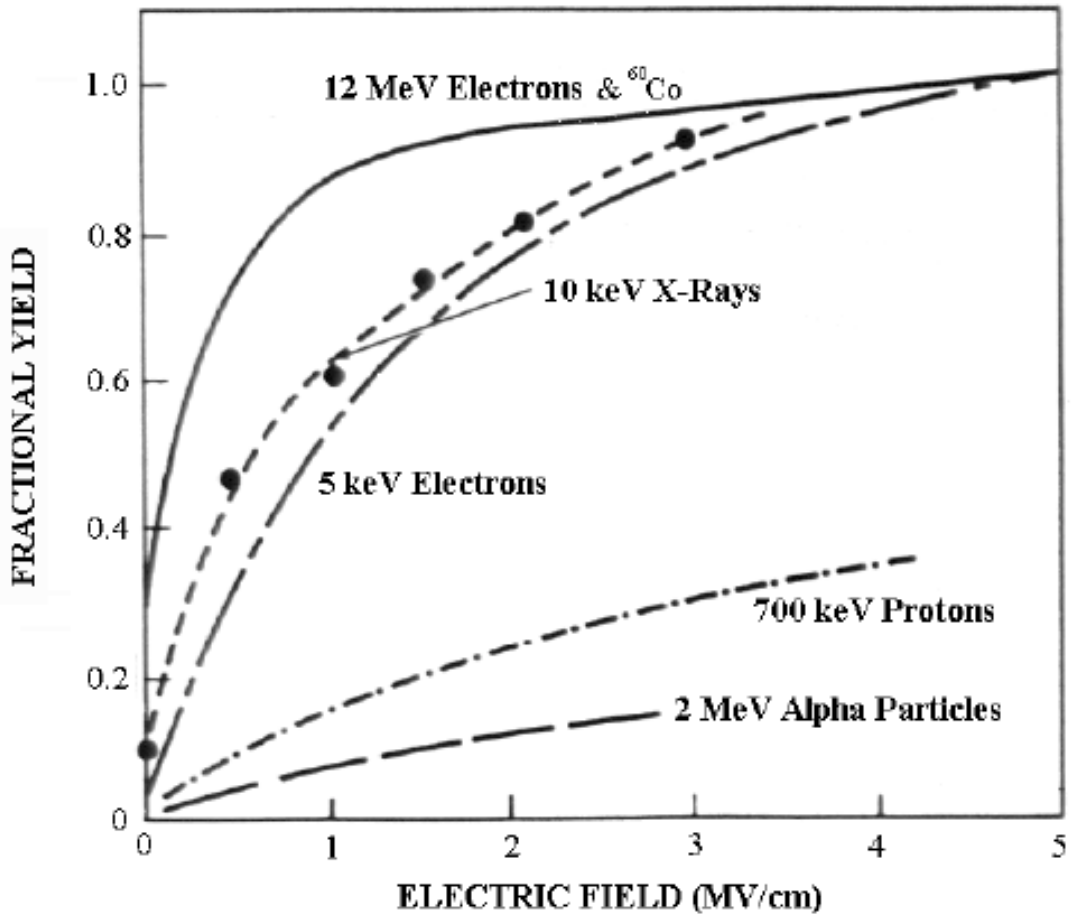
- When a particle passes through the MOS structure, it ionizes the lattice atoms, leaving behind free electron-hole pairs along its track
- In the gate oxide, part of the pairs recombines; the remaining electrons and holes are separated by the applied electric field; in the case of an NMOS device, assuming that a positive voltage is applied to the gate terminal,
  - **electrons** move towards the gate; electrons are very mobile in SiO_2 (μ_n=20 $cm^2V^{-1}s^{-1}$) and quickly get out of it through the gate contact
  - **holes** move towards the Si/SiO_2 interface; holes have a very low effective mobility (between 10^{-4} and 10^{-11} $cm^2V^{-1}s^{-1}$) and transfer via a complicated, stochastic trap-hopping mechanism



- Since the number of e-h pairs is proportional to the deposited energy, the total damage is also roughly proportional to the total absorbed dose

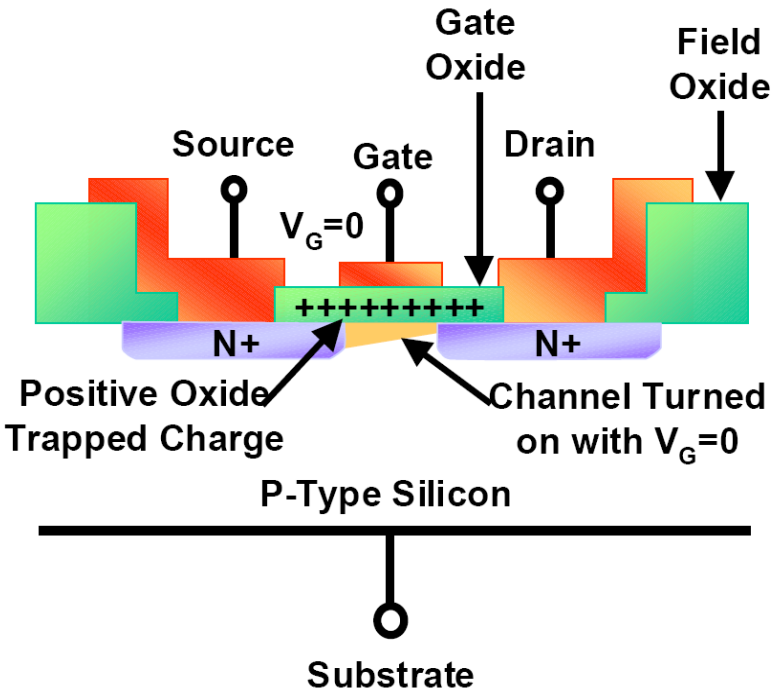
Fractional yield

- The amount of recombination depends on the fractional charge yield, which is a function of the applied electric field and on the type and energy of the incident radiation; the results shown in the figure are well established for thermally grown silicon dioxide, while much less is known for other dielectrics, like SiN, which are largely used in the microelectronic industry



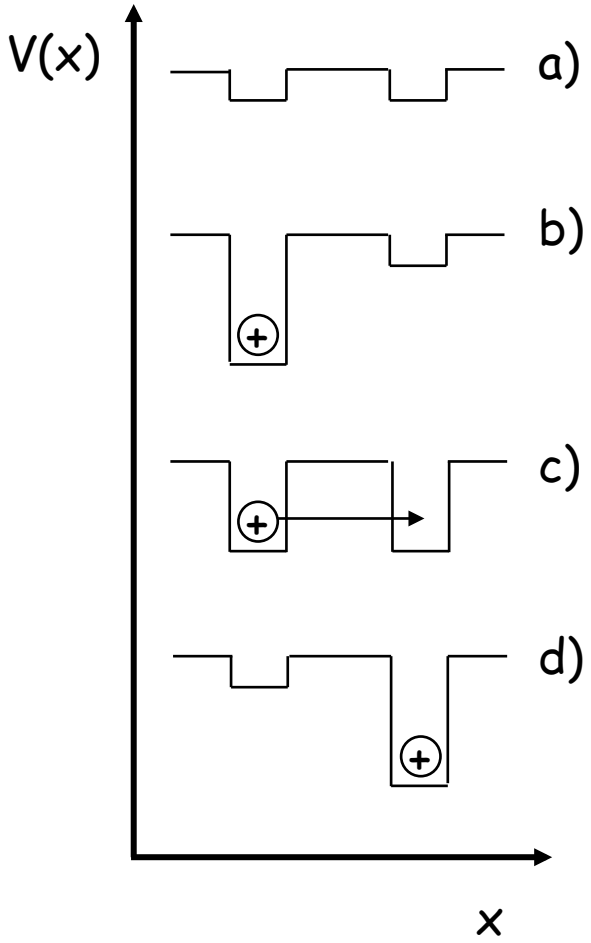
Carrier transport in the oxide

- Some of the holes may be trapped within the oxide, leading to a net positive charge (the ratio between trapped holes and trapped electrons is somewhere between 10^3 and 10^6); others may move to the Si/SiO_2 interface, where they can create an interface trap by capturing electrons
- Along with the electron-hole generation and/or hole transport processes, chemical bonds in the oxide structure may be broken; in particular, bonds associated with hydrogen and hydroxyl groups may release hydrogen ions (protons), which may migrate to the Si/SiO_2 interface and undergo a reaction resulting in the creation of interface traps; also defects created in the oxide bulk can migrate and form interface traps
- Generally, interface traps can trap both holes and electrons by capturing them from the device channel; their state depends on the bias conditions and type of the device



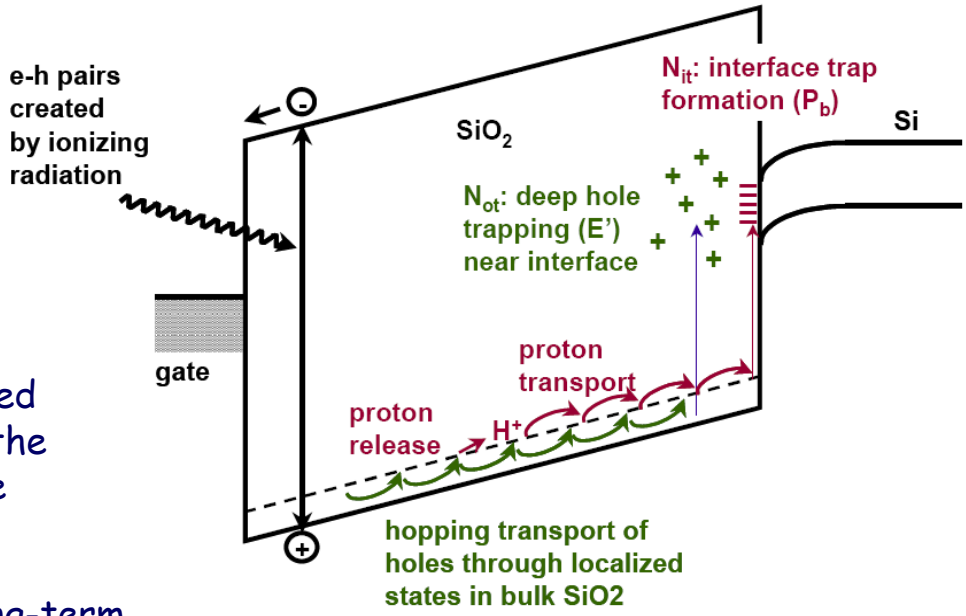
Hole transport mechanism (polaron hopping)

- Let us start with an initially empty localized trap a); when a hole, while moving through the oxide, gets stuck in it, the total energy of the system is lowered by a distortion of the lattice around the trap site b); the hole digs a potential well for itself, i.e. is self-trapped
- The transition of the trap between two nearby sites occurs via an intermediate thermally activated state c), for which thermal fluctuations of the system momentarily bring the electronic energy levels very close to each other; the hole tunnels from the first to the second site
- In the final state of the process, the hole resides in the second site d), the transition probability depending on the tunneling transition probability and on the probability that the intermediate state in c) is created



Hole trapping and interface state formation

- To summarize, in the oxide of an MOS structure
  - electron-hole pairs are created along the track of the impinging particle
  - the electric field quickly sweeps electrons out of the oxide, while holes migrate to the Si/SiO_2 interface with a peculiar hopping mechanism
  - under the effect of the field, also protons (released as a consequence of the generation process or of the hole motion in the lattice) may reach the interface and create traps there
  - holes get trapped in the oxide, some of them in long-term trapping sites close to the interface (a region relatively rich of lattice imperfections), building up a net positive charge



- While the net charge trapped in the oxide (oxide trapped charge) is always positive, charge balance at the interface (interface trapped charge) depends on the type of MOSFET, whether it is an N- or a PMOS; when the channel is formed (➔ gate-to-source voltage > threshold voltage) interface traps are mostly positively charged in PMOS, negatively in NMOS

Oxide trapped charge

- Oxide trapped charge is responsible for a negative variation ΔV_{OT} in the threshold voltage

$$\Delta V_{OT} = -\frac{q}{C_{OX}}\Delta N_{OT} = -\frac{q}{\varepsilon_{OX}} t_{OX}\Delta N_{OT}$$

- q=elementary charge (1.6×10^{-19} C)
- $C_{OX}=\varepsilon_{OX}/t_{OX}$ is the specific capacitance of the MOS capacitor (to be measured in F/m^2)
- t_{OX}=gate oxide thickness
- ε_{OX}=dielectric constant
- ΔN_{OT}=density of oxide trapped holes per area unit (to be measured in m^{-2})

- According to a very simple model, ΔV_{OT} is proportional to t^2_{OX}, ΔN_{OT} being proportional to t_{OX}; actually, the trapped hole concentration generally peaks close to the Si/SiO_2 interface

- If n_{ht} is the local density of trapped holes and x the coordinate along the direction perpendicular to the Si/SiO_2 interface (n_{ht} is assumed to be constant in any plane parallel to the interface)

$$\Delta N_{OT} = \int_0^{t_{OX}} n_{ht}(x)dx$$

Interface trapped charge

- The net charge residing in interface traps can either be positive, neutral or negative; based on their allowable charge states, interface traps are classified as either donors or acceptors
  - a donor trap level is in a neutral charge state when it is below the Fermi level, and becomes positive by donating an electron when it moves above the Fermi level
  - an acceptor trap level is in neutral charge state when it is above the Fermi level, and becomes negative by accepting an electron when it moves below Fermi level
- When a voltage is applied to the gate of an MOS device, the interface trap levels move up or down relative to the Fermi level; experimental data show that interface traps in NMOS are predominantly acceptor-like (can be neutral or negatively charged), predominantly donor-like (neutral or positively charged) in PMOS
- Depending on the device bias condition, interface trap charge is responsible for a change ΔV_{IT} in the threshold voltage, given by

$$\Delta V_{IT} = -\frac{\Delta Q_{IT}}{C_{OX}}$$

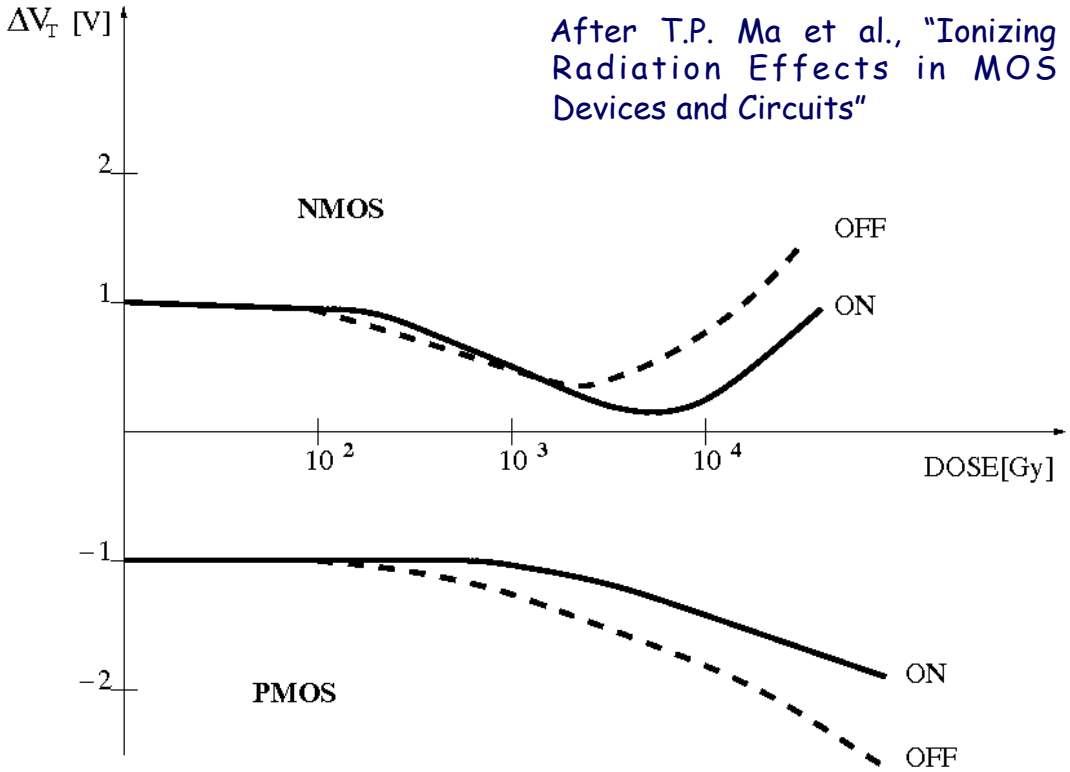
where ΔQ_{IT} is the interface trapped charge

Threshold shift

- The overall effect of oxide trapped charge and interface trapped charge can be written as

$$\Delta V_t = \Delta V_{OT} + \Delta V_{IT} = -\frac{1}{C_{OX}}\left(\Delta Q_{OT} + \Delta Q_{IT}\right)$$

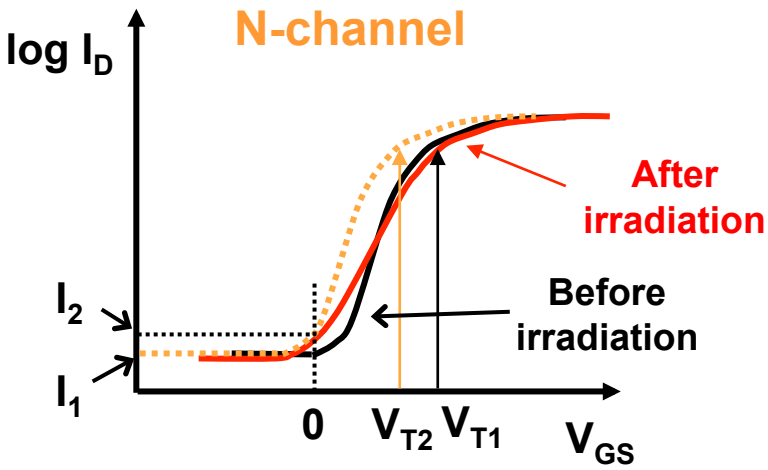
- In NMOS transistors
  - at low doses, V_t decreases since its behavior is dominated by positive charge trapping in the oxide
  - at high doses, V_t increases since its behavior is dominated by negative charge trapping at the Si/SiO_2 interface
- In PMOS transistors
  - both at low and high doses, V_t decreases as both oxide and interface traps can only be positively charged (or neutral, if not charged)

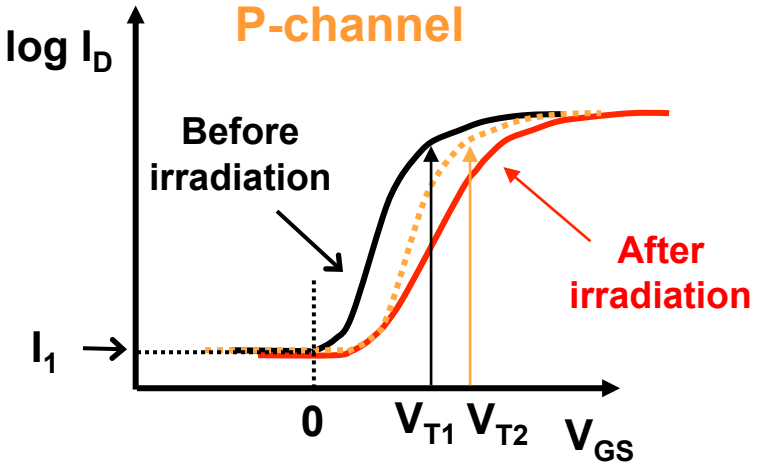


After T.P. Ma et al., "Ionizing Radiation Effects in MOS Devices and Circuits"

Subthreshold current change

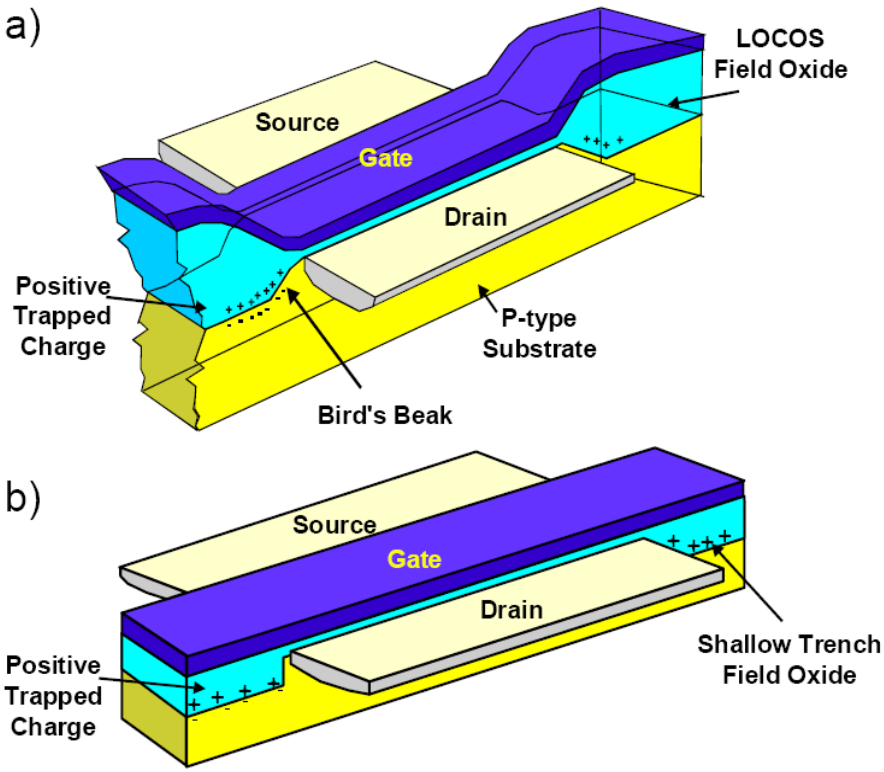
- Oxide charge trapping and interface trap buildup induced by ionizing radiation also are responsible for a remarkable change in the I_D-V_{GS} curves in MOSFETs
- Two different effects can be distinguished:
  - a shift of the curve along the voltage axes (towards negative values for NMOS, towards positive values for PMOS transistors) due to threshold voltage shift
  - a decrease in the subthreshold curve slope (curve stretch-out) for both device types, which was experimentally found to be correlated to interface trap buildup
- As a consequence of these effects, a net increase in the NMOS drain current is observed at V_{GS}=0, while no increase (if not a decrease) can be detected in the PMOS





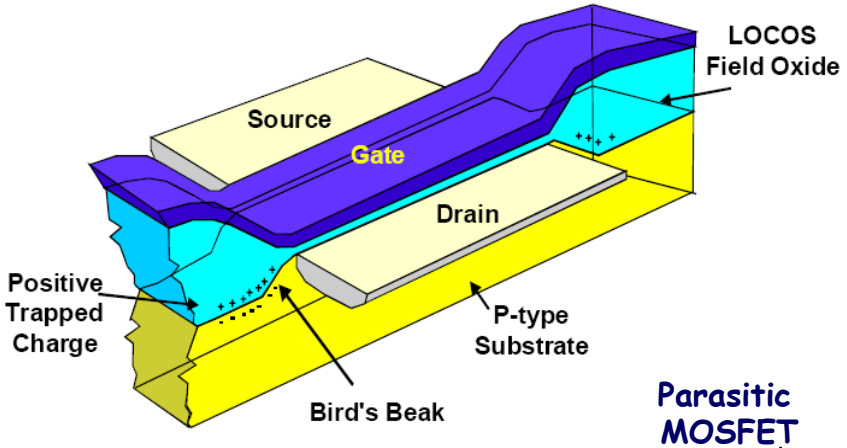
Leakage currents due to field oxides

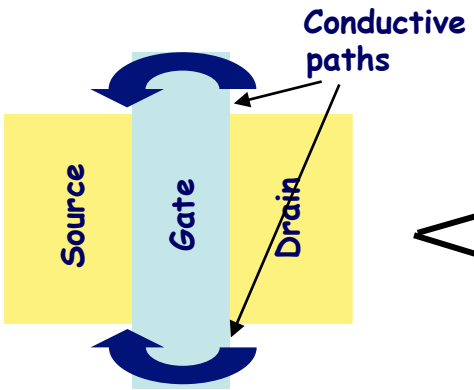
- The trend to device scaling in the modern microelectronic industry has brought along a progressive reduction of the gate oxide (2 nm in 130 nm CMOS technology) and an ever higher degree of tolerance to ionizing radiation
- On the other hand, the field oxide used to electrically isolate devices from each other features a thickness ranging between 100 and 1000 nm
- Two different kinds of isolating oxides are used in CMOS processes
  - a) LOCOS, local oxidation of silicon (actually progressively abandoned in modern CMOS technologies)
  - b) STI, shallow trench isolation
- In an NMOS device, positive charge trapping in the field oxide due to ionizing radiation can invert the underlying P doped region and form an N-type conducting channel between the source and drain terminals, therefore increasing the drain leakage current

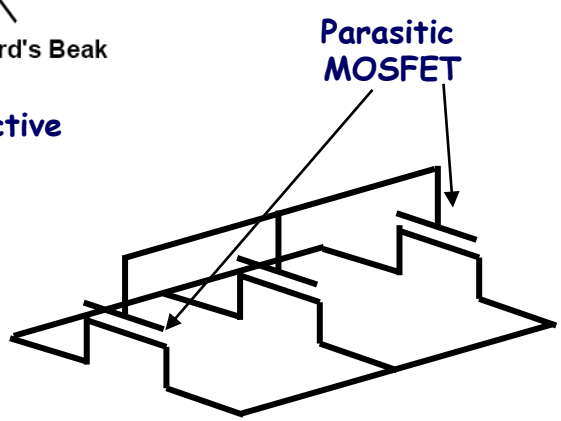


Leakage currents due to field oxides

- Positive charge trapped in the field oxide may create a parasitic channel between the source and drain terminals under the bird's beak region
- The oxide thickness in the bird's beak region is larger than in the gate oxide and the accumulated positive charge can be such that the underlying P substrate is inverted and an N-type channel is created
- The radiation induced channel can be modeled with a parasitic transistor in parallel with the main device and featuring a different width W but the same length L
- This effect can be observed only in NMOS transistors, since in PMOS devices the charge in the channel is carried by holes and the N-type substrate cannot be inverted by the positive trapped charge



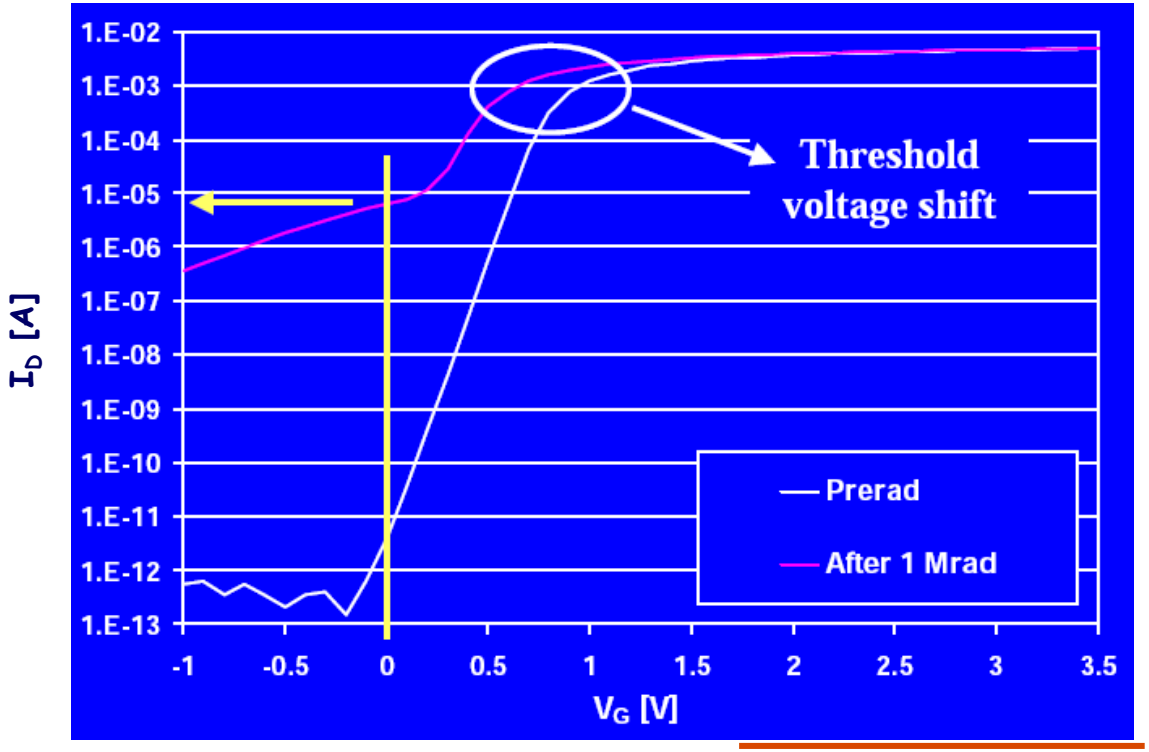


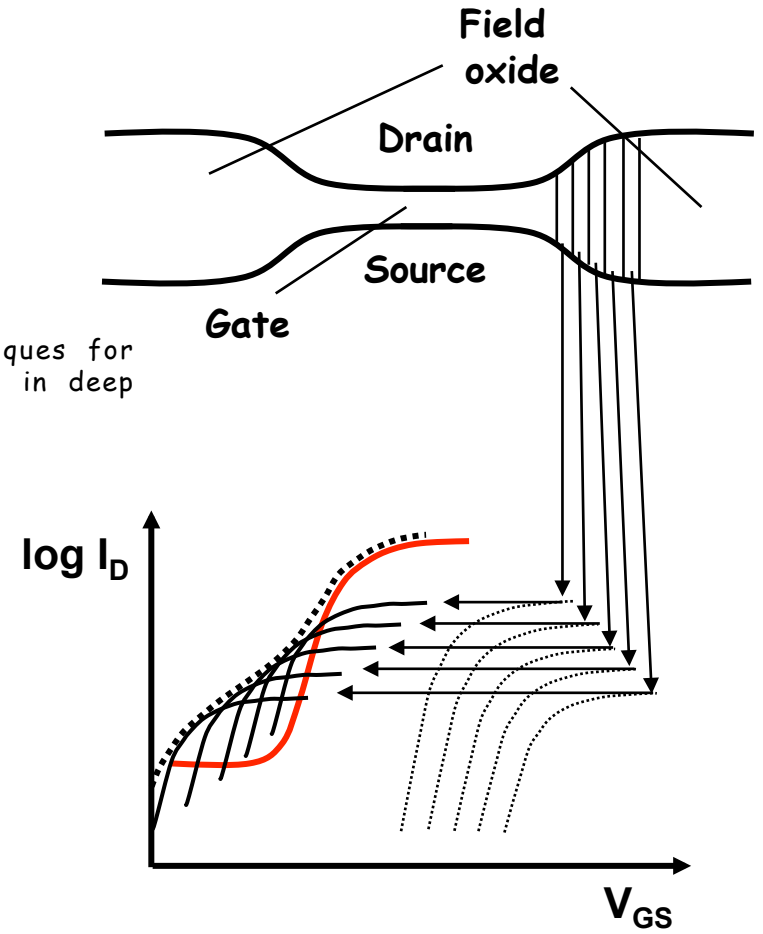


Leakage currents due to field oxides

- The radiation induced increase in the drain current results from the superposition of the current contributions from several, small parasitic transistors in parallel; subthreshold current may increase of several orders of magnitude after irradiation

After G. Anelli, "Techniques for radiation tolerant design in deep submicron CMOS technology"





Radiation effects on an NMOS transistor from a 0.7 μm CMOS process (t_{OX}=17 nm)

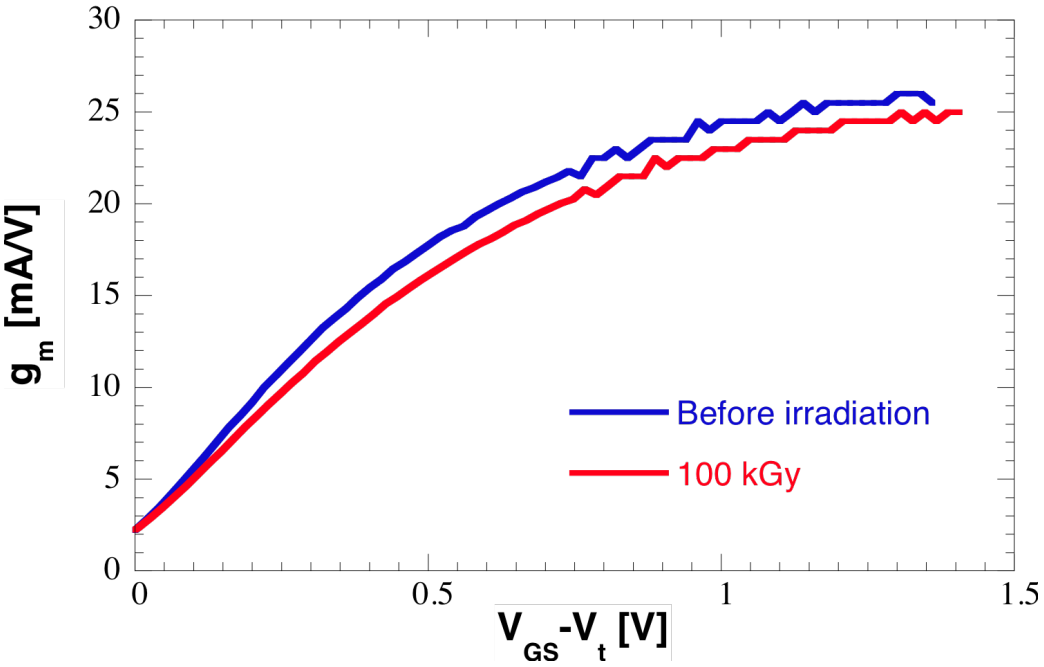
Mobility degradation

- Increase of interface traps is also responsible for a degradation in the carrier mobility **μ** according to the following relationship

$$\mu = \frac{\mu_0}{1 + \alpha \cdot \Delta N_{IT}}$$

- μ_0=pre-irradiation mobility
- α=mobility degradation parameter ($\approx 10^{-12}$ cm^2)
- ΔN_{IT}=interface trap increase

- The change in the mobility has a direct effect on the device transconductance (defined as the derivative of the drain current with respect to the gate-to-source voltage)



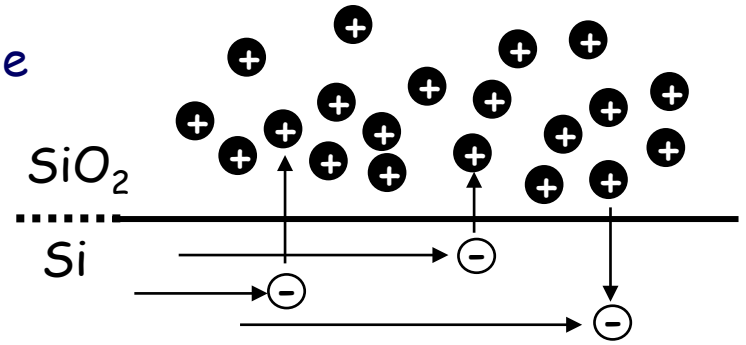
Transconductance g_m in an NMOS device with W/L=200 μm/0.7 μm, from a 0.35 μm process before and after exposure to ^{60}Co γ-rays

Annealing

- Holes trapped in the SiO_2 of an MOS structure are not truly permanently trapped; actually, they are observed to disappear from the oxide over times from milliseconds to years; this discharge of the hole traps, commonly observed near room temperature, is the major contributor to the so-called long-term annealing of radiation damage in MOS devices
- Annealing of trapped holes has two manifestations, which may reflect different hole removal processes
- A slow bias-dependent recovery of ΔV_{OT} typically observed at normal device operating temperatures (-55° to 125°C); such a process has been described through a **tunneling** model
- A relatively rapid and strong temperature-dependent removal or recombination of the holes observed when MOS structures are deliberately subjected to thermal annealing cycles at elevated temperature (150° to 350°C); this process has been described through a **thermal detrapping** model

Tunnel annealing

- The tunneling model assume that electrons from the silicon tunnel to and recombine with the trapped holes in the distribution of traps near the SiO_2 interface (or holes tunnel from the traps to the silicon valence band)



- As a consequence of the exponential decay of the tunneling probability with the distance into the SiO_2, at a given time **t** the hole traps are emptying at a depth $X_m(t)$ from the silicon according to the following equation, valid under the assumption of uniform trap distribution in the oxide

$$X_m(t) = \left(\frac{1}{2\beta}\right)\ln\left(\frac{t}{t_0}\right)$$

- β=tunneling barrier height parameter
- t_0=time scale parameter

- It was experimentally observed that applying a positive (with a higher potential on the metal side in the MOS structure) electric field has the effect of increasing the annealing rate; this can be explained by the fact that a positive electric field lowers the barrier to tunneling

Thermal annealing

- Electrons in SiO_2 valence band can acquire enough energy to jump into the conduction band and recombine with trapped holes; this process can be modeled with an emission probability $\mathbf{p_{em}}$ of an electron from the valence band of the silicon dioxide to the traps where holes are located

$$p_{em}(T) = AT^2 \cdot \exp\left(-\frac{q\varphi}{k_B T}\right)$$

- A=constant depending on trap cross section
- T=absolute temperature
- φ=energy difference between the trap level and the valence band

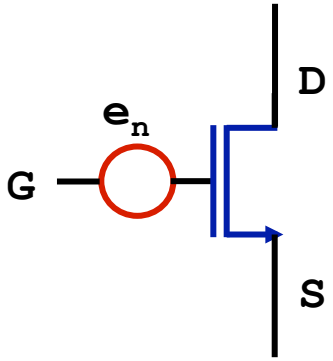
- The emission probability is strongly temperature dependent
- A couple of different annealing techniques are used to study the nature and distribution of SiO_2 bulk traps
  - In **isochronal annealing** tests, the device is subjected to temperature increments and parameter measurements at regular time intervals
  - In **isothermal annealing** tests, the sample is heated at a constant temperature for a given duration of time

Electronic noise

- The word ``noise'' is used to indicate spontaneous fluctuations of electric variables taking place in passive and active electronic devices
- Electronic noise originates from the fundamental physical phenomena which underlay the operation of electronic components (e.g., thermal agitation of charge carriers, granularity of electric charge); such phenomena cannot be eliminated without denying fundamental physical laws
- Noise has a different nature from that of other disturbances coming from the environment (e.g., 50/60 Hz harmonics from the power supply, electromagnetic induction from other circuits), which, at least theoretically, can be suppressed by shielding or filtering techniques.
- Noise may impair the capability of a circuit to accurately measure the amplitude of a signal and represents the unavoidable, final limitation to an electronic system performance
- Since noise is a random process, its properties can be described only through statistical tools and quantities (e.g. mean square value, root mean square, or rms, value, power spectral density)

Noise in field-effect transistors

- Noise in a MOSFET can be circuitally described by means of a voltage source e_n in series to the gate terminal of the device; this source, formally represented by means of its power spectral density, includes two terms
  - a frequency independent one (S_W), dominated by the channel thermal noise, which originates from thermal agitation of carriers in the device channel (the white noise component may include contributions from parasitic resistors, not considered here)
  - a term which is inversely proportional to the frequency, also called 1/f or flicker noise, which arises from continuous, random capture and release of carriers by border (very close to the Si/SiO_2 interface) traps in the oxide



$$\frac{\overline{de_n^2}}{df} = S_w + \frac{A_f}{f}$$

$$S_w = \frac{4k_B T\Gamma}{g_m}$$

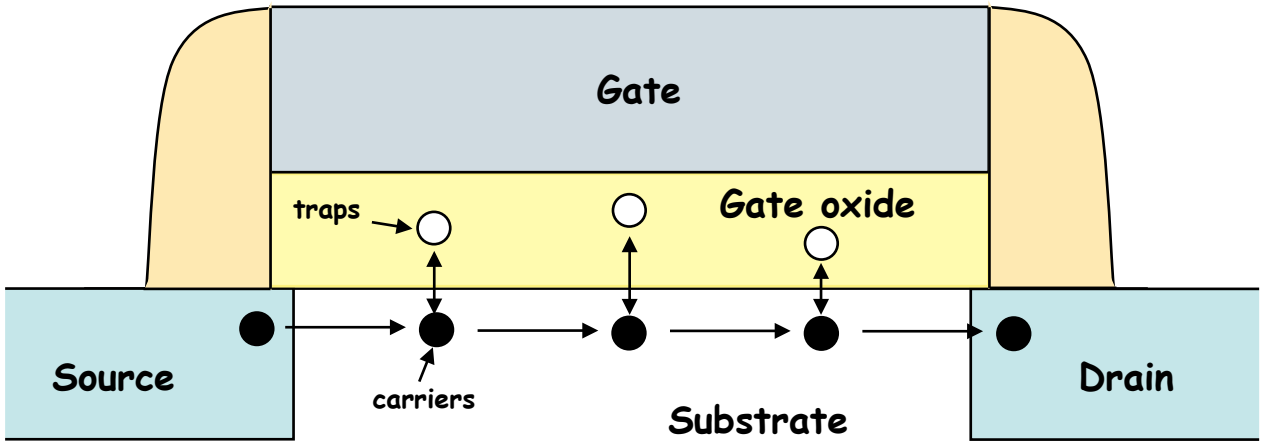
$$A_f = \frac{K_f}{C_{OX}WL}$$

- k_B=Boltzmann's constant
- T=absolute temperature
- Γ=channel thermal noise coefficient
- g_m=channel transconductance
- K_f=1/f noise parameter
- W, L=channel width and length
- f=frequency

- The same equation holds for junction field-effect transistors (JFET), where 1/f noise arises from continuous carrier exchange between the device channel and localized traps in the gate-channel depletion region

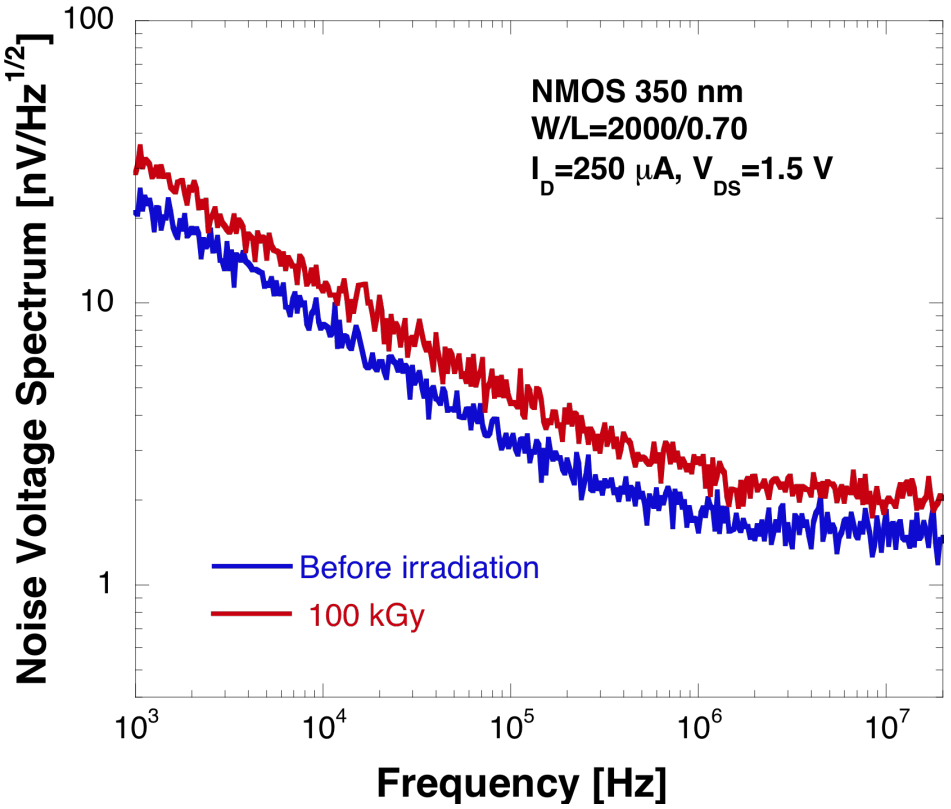
1/f noise in MOSFETs

- In MOSFET devices, 1/f noise is due to the interaction between carriers in the channel and traps in the gate oxide; the process of random capture and emission of carriers is responsible for a fluctuation in the number and mobility of carriers, resulting in a stochastic fluctuation of the drain current
- Experimental investigations show that 1/f noise is almost entirely due to the so-called border traps, traps in the oxide located within 3 nm of the Si/SiO_2 interface, which can exchange charge with the underlying channel with characteristic times of the same order of an electrical measurement
- Border traps exchange charge with the channel with a probability exponentially decreasing with the trap distance from the Si/SiO_2 interface
- The definition of a trap as a border trap depends also on the operating conditions (in particular on the gate-to-source voltage, V_{GS})



Noise increase in irradiated MOSFETs

- Exposure to ionizing radiation also affects the noise performance in MOSFET devices
- As far as white noise is concerned, the gate referred power spectral density (the noise voltage spectrum is the square root of the power spectral density) increases due to the radiation induced reduction of the channel transconductance g_m
- Flicker noise increase is correlated with the increase in positive trapped charge close to the interface and with the increase in the number of border traps



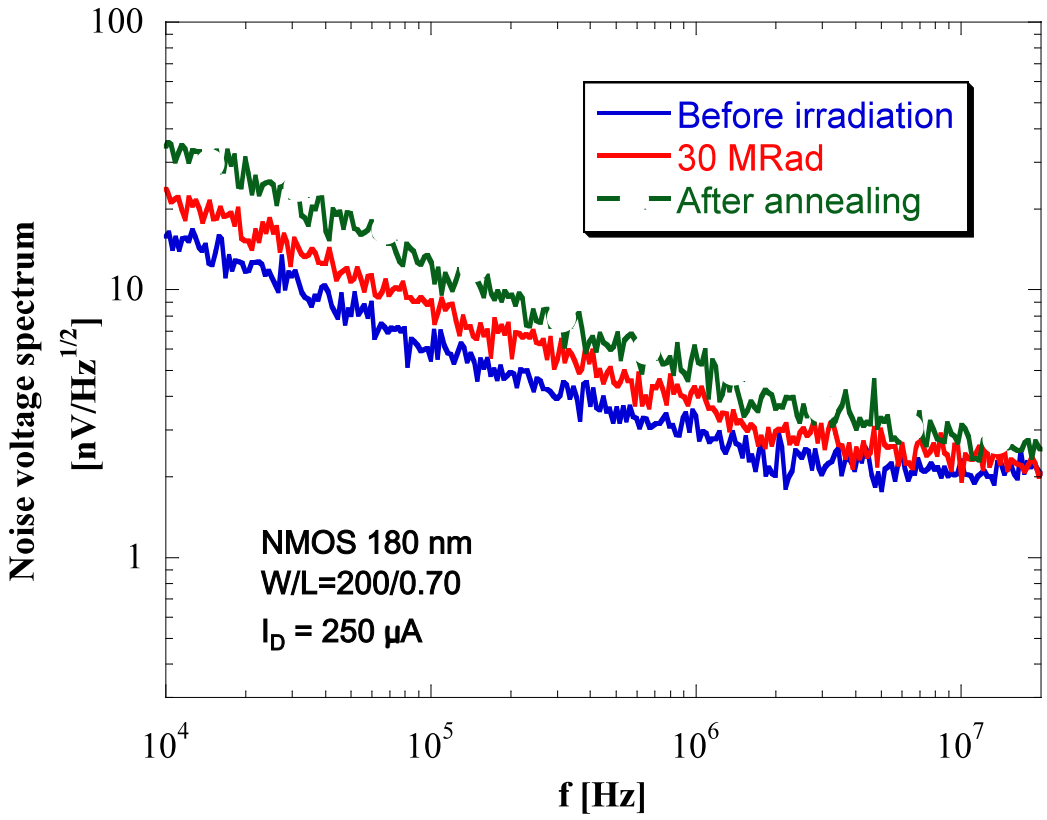
Gate referred noise voltage spectrum in an NMOS device with W/L=2000 μm/0.7 μm, from a 0.35 μm process before and after exposure to ^{60}Co γ-rays

Effects of bias conditions during annealing

- Going from 350 nm to 180 nm minimum channel length, CMOS technologies have become radiation-harder from the standpoint of channel thermal noise; this trend is preserved in the subsequent CMOS generations and is correlated to technology scaling (more on the subject in the following); a sizable degradation in flicker noise can still be detected

- Further degradation is detected after annealing with all the device terminals grounded (no field across the oxide); this effect has been correlated with an increase in the oxide trapped charge

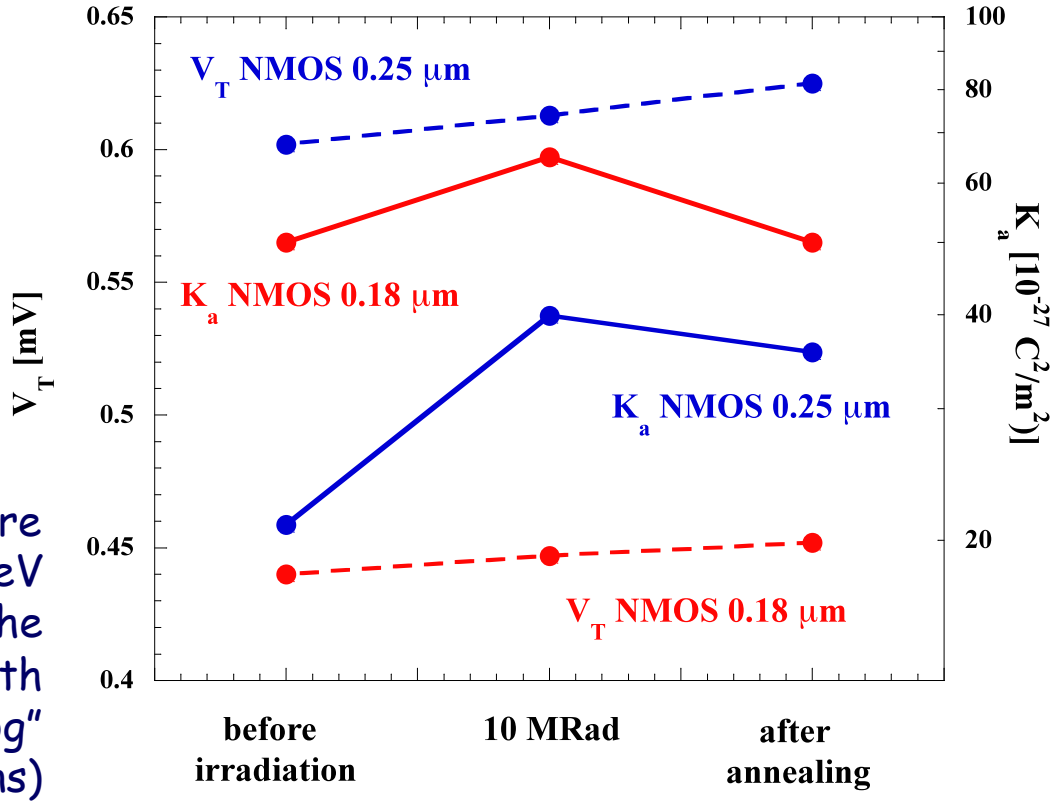
Gate referred noise voltage spectrum in an NMOS with W/L=200 μm/0.70 μm, from a 180 nm process before and after exposure to ^{60}Co γ-rays under worst case bias conditions (V_G=1.8 V, all other terminals grounded) and after annealing with all terminals grounded



Effects of bias conditions during annealing

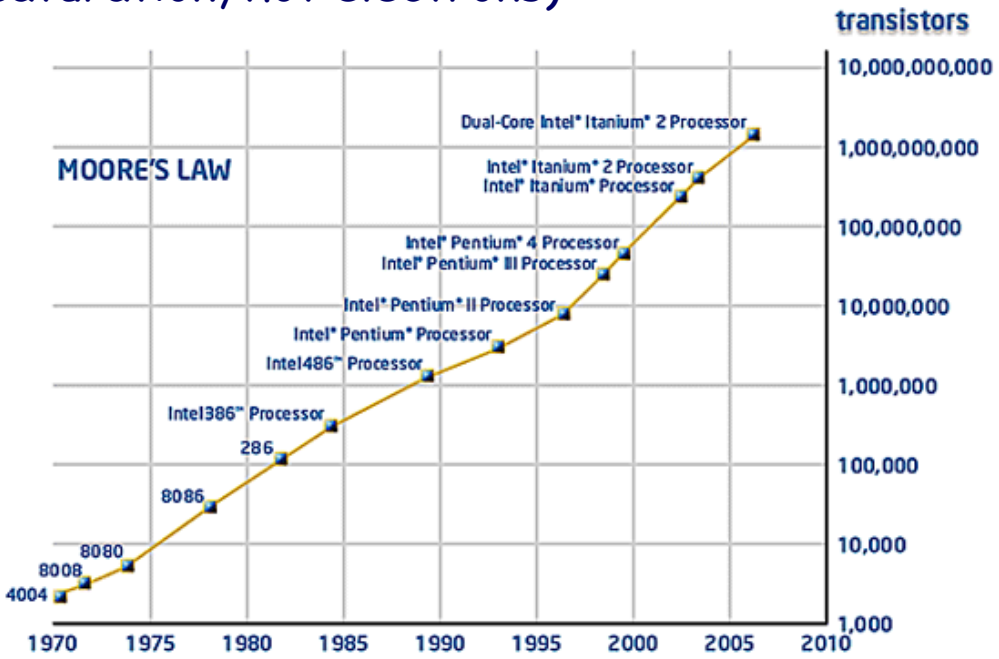
- Different results are obtained when annealing is performed under "analog" bias conditions (i.e., the devices are biased in the same condition as in analog circuits, e.g., V_S=0, V_G=0.5 V, V_D=1 V, with a positive field applied to the oxide); a partial recovery is detected in flicker noise, whereas threshold voltage can be observed to increase both after irradiation and after annealing
- In this case, 1/f noise recovery after annealing has been correlated to decrease in oxide trapped charge
- 1/f noise behavior also depends on the device polarity (not shown here)

Threshold voltage and 1/f noise variation before irradiation, after exposure to a 10 Mrad 10keV X-ray dose and after annealing for NMOS in the 180 nm process and in the 250 nm process (both irradiation and annealing performed in "analog" conditions)



CMOS roadmap

- While fundamental physical processes of radiation damage remain the same, CMOS processes, following Moore's law, are rapidly evolving yielding ever larger scale of integration and processing speed
- Power and speed performance optimization is obtained by progressively reducing the bias voltage (VDD) and the horizontal device dimensions (i.e., the device channel length); this leads to the so-called short channel effects, which may result in a deviation from the expected behavior of the transistor (e.g., excess high frequency noise, carrier mobility saturation, hot electrons)
- In order to alleviate short channel effects, also vertical dimensions of the device (gate oxide thickness, source and drain junction depth) are reduced

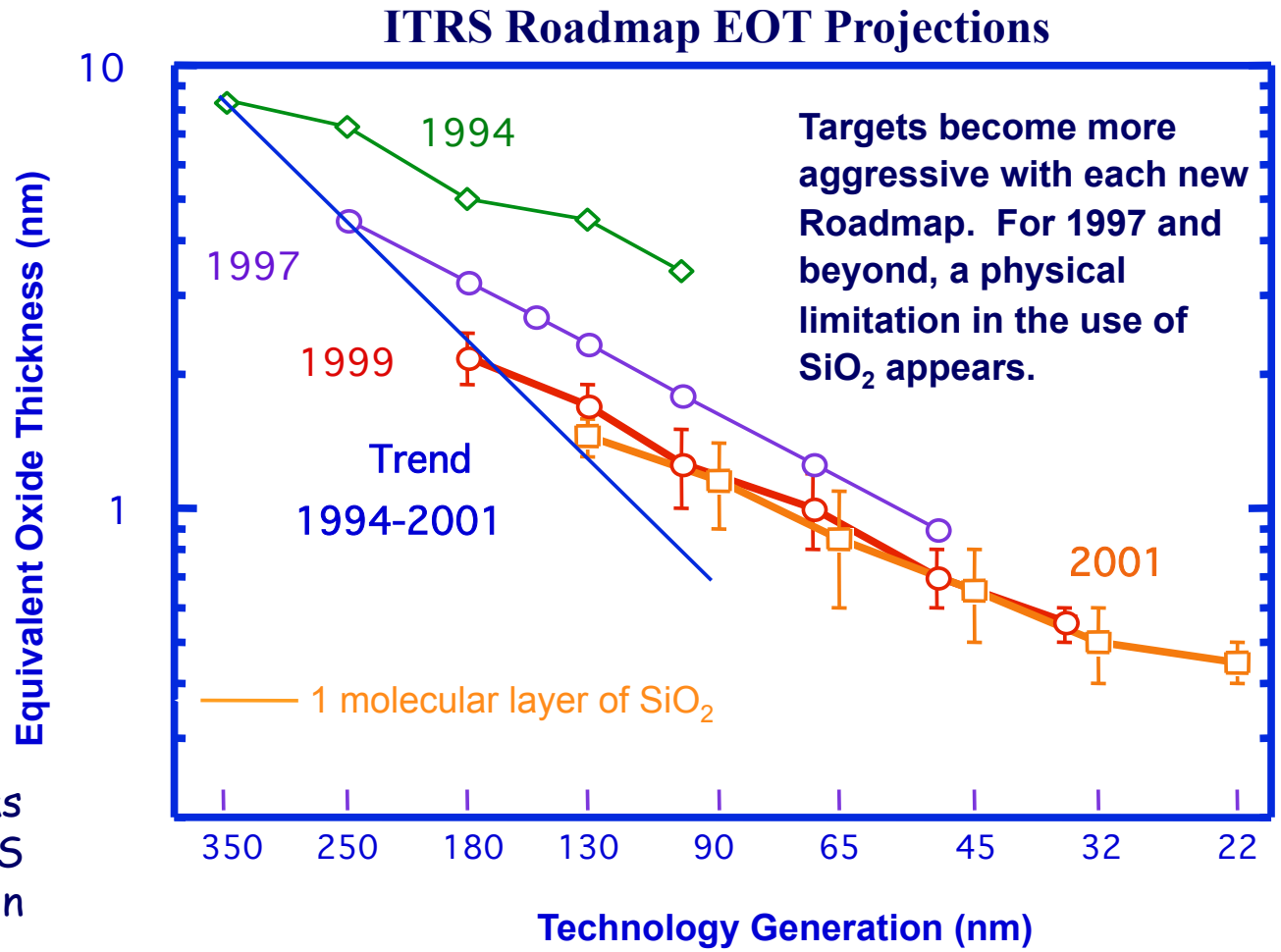


CMOS roadmap

Oxide scaling and radiation effects

- Device scaling (increase in speed and circuit complexity per unit of chip area) requires decreasing the oxide thickness

- Change in the geometrical features of the transistor may result (and actually does result) in a change of the impact of radiation damage processes on the devices fabricated with the new technologies

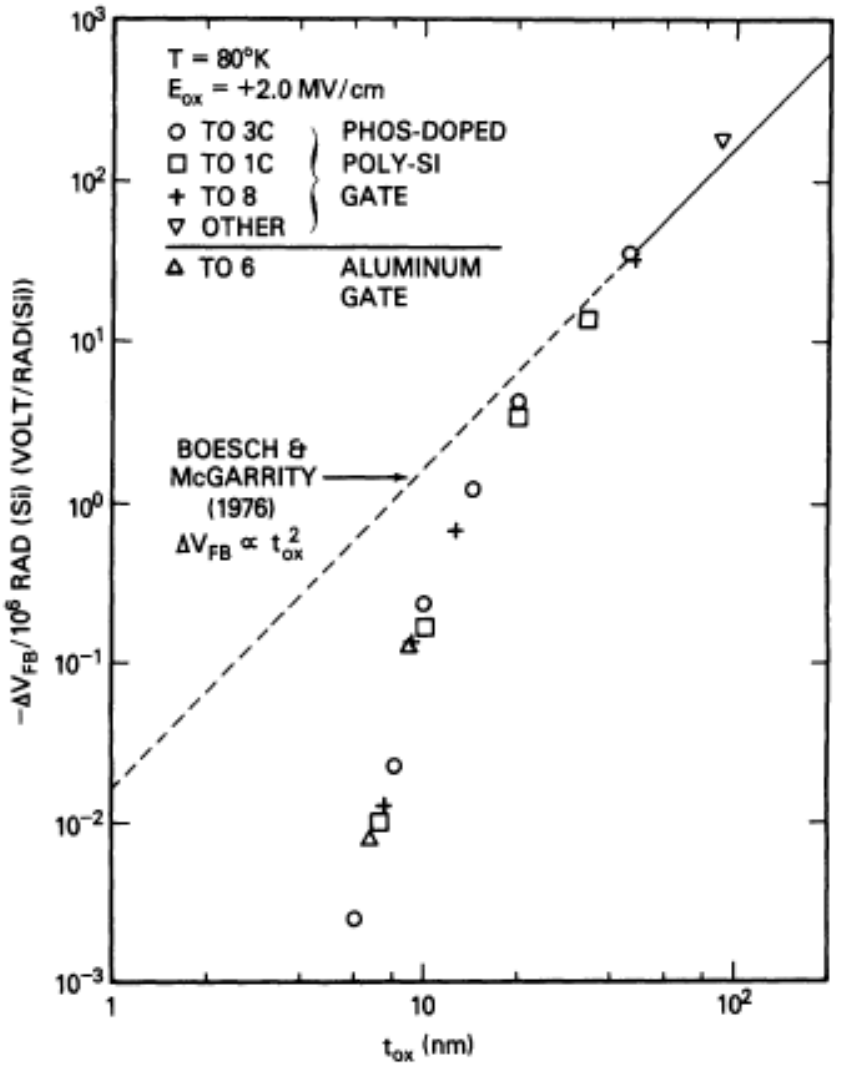


Trend of the oxide thickness as a function of the CMOS generation

Oxide scaling and radiation effects

- For t_{OX} values above 30 nm, as t_{OX} decreases, variation of flat-band voltage in ^{60}Co irradiated MOS capacitors is found to decrease with the square of the oxide thickness, in good agreement with the theoretical behavior; for t_{OX}<20 nm considerable discrepancy between experimental data and expected behavior is observed; these results were found to be independent of the way the oxide was processed

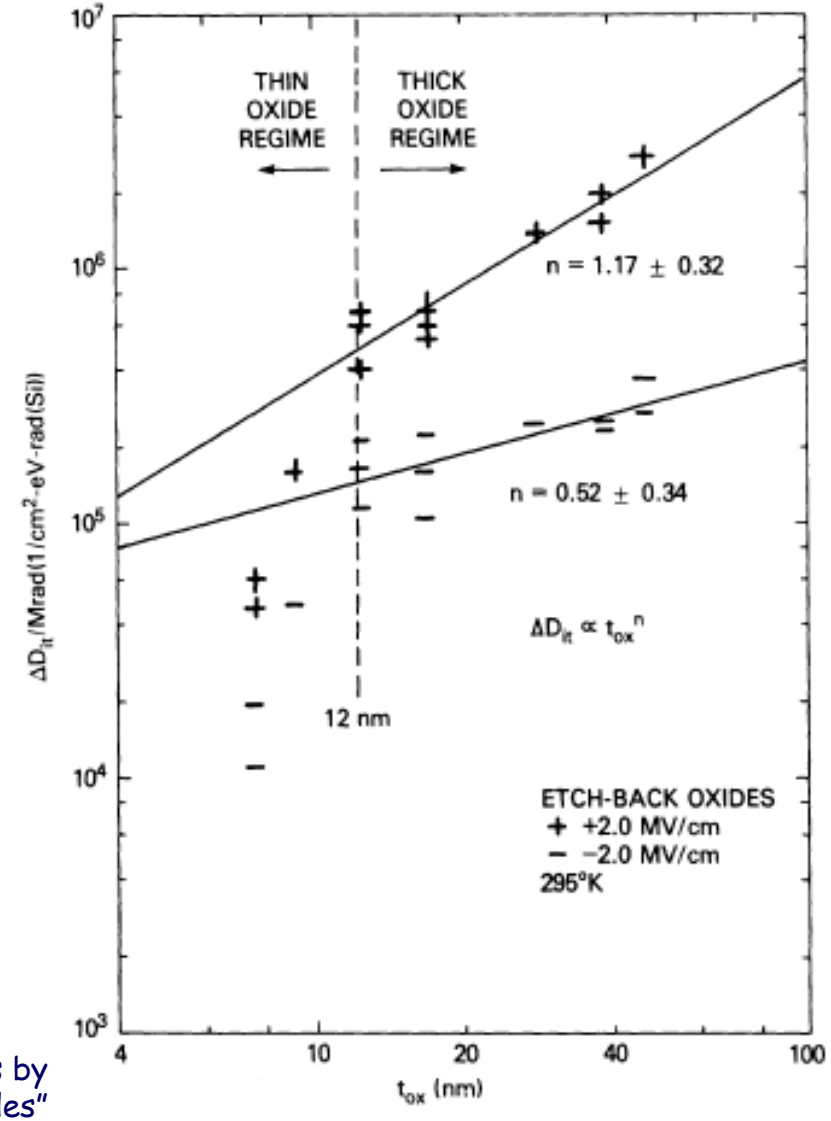
After N.S. Saks et al., "Radiation effects in MOS capacitors with very thin oxides at 80°K"



Flat-band voltage variation per Mrad dose (^{60}Co) for MOS capacitors, biased with a 2MV/cm field, as a function of oxide thickness; the plot also shows the anticipated proportionality to t^2_{OX}

Oxide scaling and radiation effects

- As t_{OX} decreases, the density of radiation-induced interface traps, D_{it}, in MOS structures tends to decrease with a given power **n** of the oxide thickness; however, for thin oxides (t_{OX}<12 nm), the rate of decrease of D_{it} is much larger than extrapolated from the power law behavior for thicker oxides

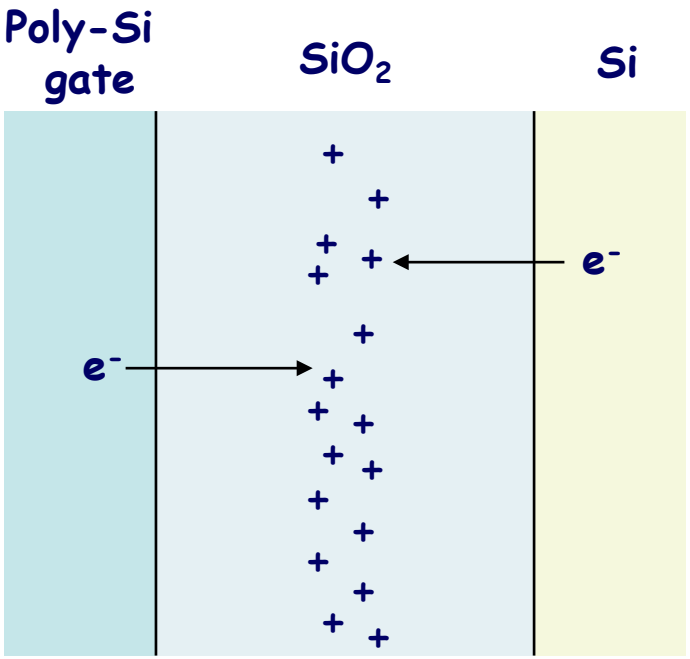


Dependence of interface trap density (D_{it}) on the oxide thickness in etchback oxides

After N.S. Saks et al., "Generation of interface states by ionizing radiation in very thin MOS oxides"

Oxide scaling and radiation effects

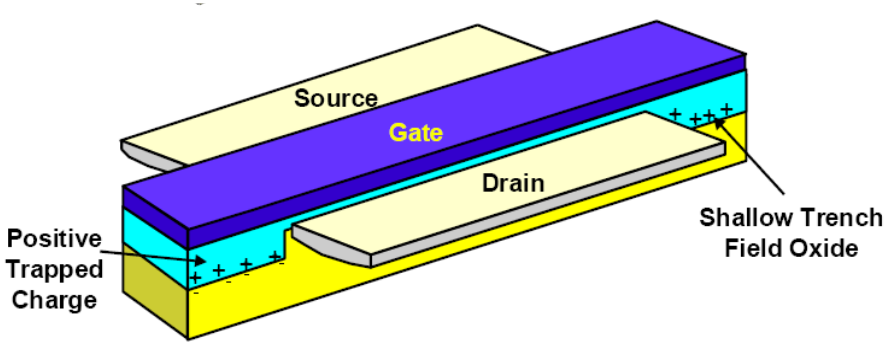
- Hole removal from the gate oxide proceeds via a "tunneling front" which moves into the oxide with a "velocity" of about 0.2 nm per decade in time
- The time-dependent tunneling distance $X_m(t)$ lies in the range from 2 to 4 nm for practical time of interest, say from 1 ms to 10^6 s; hence, for oxides less than 10 nm in thickness, one could expect enhanced hole removal to occur by electrons tunneling into the oxide also from the gate electrode
- Device scaling brings about an improved radiation-tolerance due to the enhanced recovery by trapped hole recombination with tunneling electrons from both the gate and the transistor channel

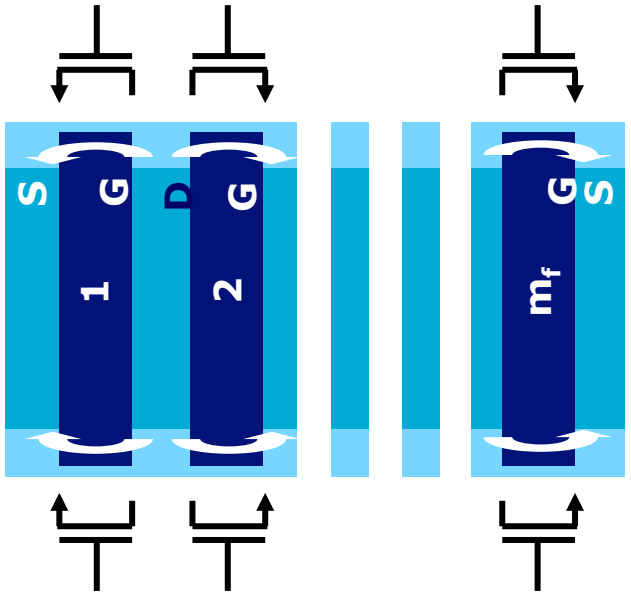


MOS structure and trapped charge tunnel annealing

Deep submicron and nanoscale technologies

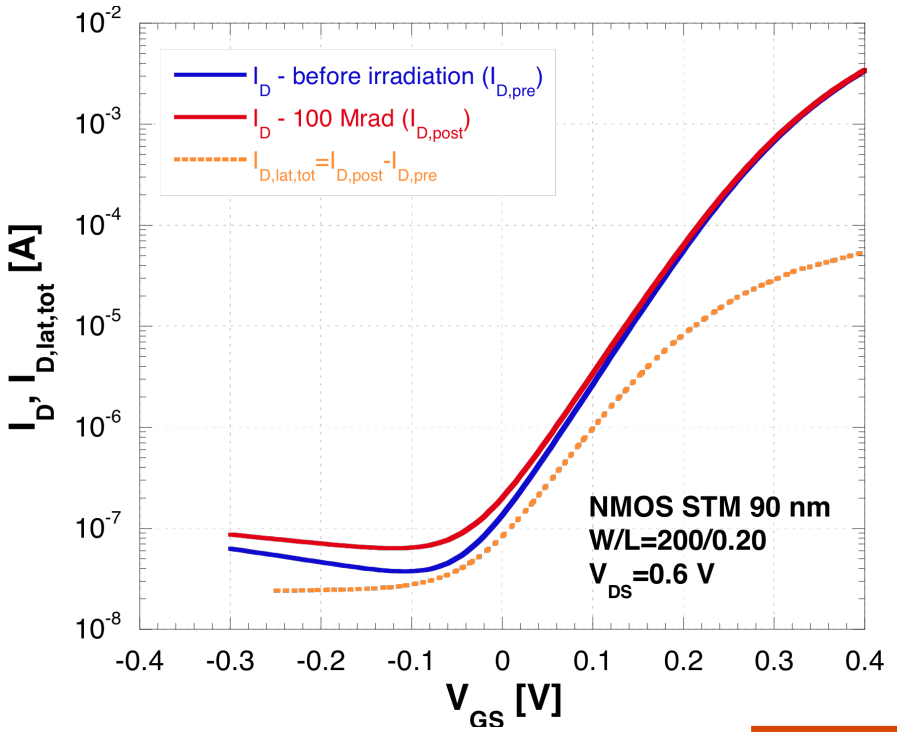
- At smaller integration scales (starting from the 130 nm process) the parasitic devices switched on by charge accumulation in the shallow trench isolation oxides (STI) affects electronic noise and static properties of NMOS transistors
- In a stacked NMOSFET including $\mathbf{m_f}$ fingers, radiation may create 2 x m_f theoretically identical parasitic transistors sharing the same channel length **L** with the main device
- Each parasitic device turned on by charge build-up in the STI oxide contributes to the overall noise of the transistor, particularly in the low frequency range and at low current densities (i.e., low I_D/W)

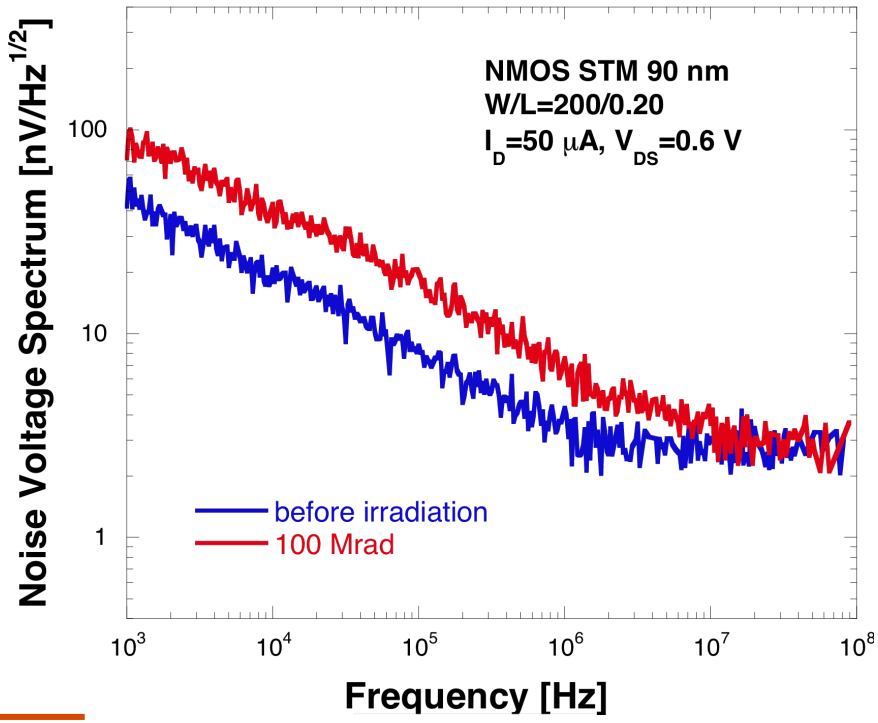




STI effects on static and noise properties

- Due to radiation-induced charge accumulation in the STI field oxide
  - a small change in the drain current, relatively high at small drain current values, can be detected
  - a significant change in low frequency (1/f) noise can be observed, in particular at low current densities
- No significant changes, even at extremely high doses, can be detected in the threshold voltage of wide channel devices (confirming the high degree of radiation-tolerance of the gate oxide)

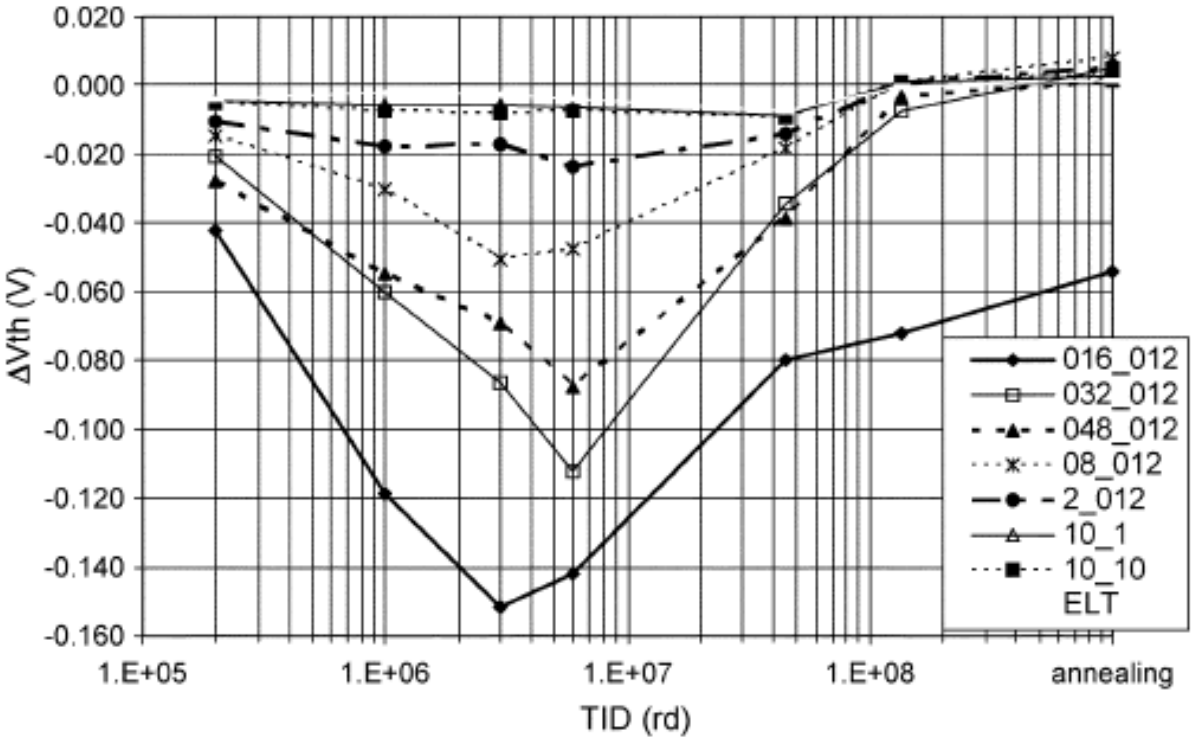




Radiation induced narrow channel effect (RINCE)

- While no change in the threshold voltage can be detected in MOSFET devices with large channel width, narrow channel devices were found to feature a peculiar behavior
- Positive charge trapped in the lateral STI oxide influences the electric field in the main transistor (narrow channel effect); it decreases the threshold of sufficiently narrow NMOS transistors, whilst they increase it (in absolute value) for PMOS transistors
- Also drain leakage current is affected by radiation-induced narrow channel effect

After F. Faccio et al., "Radiation-induced edge effects in deep submicron CMOS transistors"



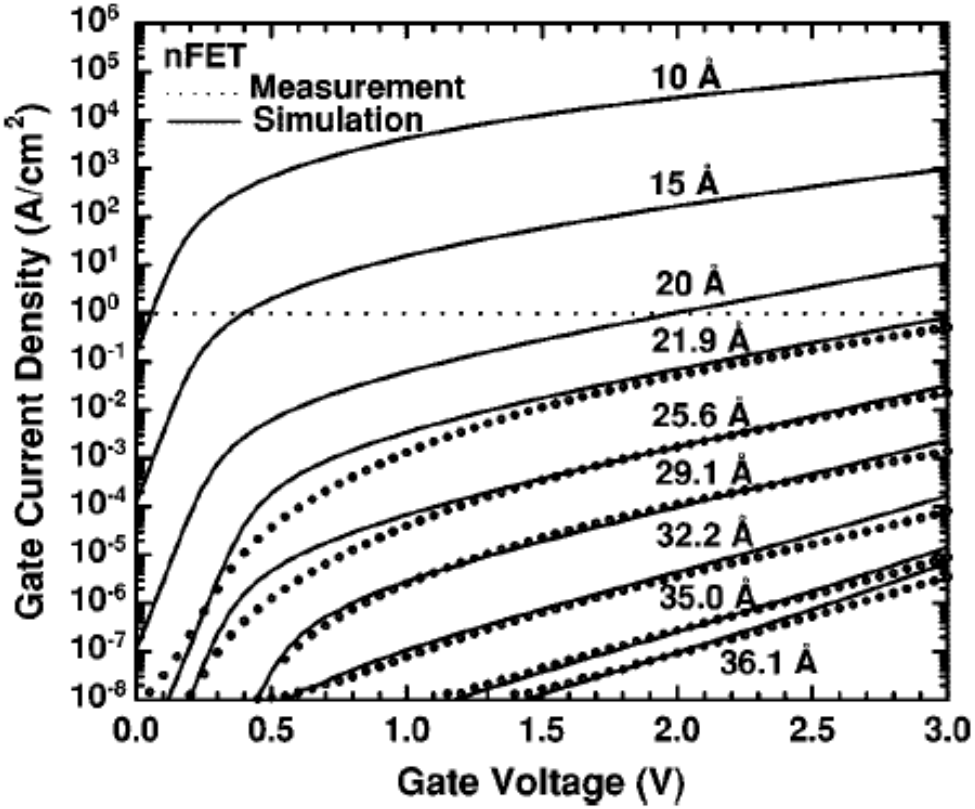
Change in the threshold voltage as a function of the total ionizing dose in narrow channel transistors from a 130 nm CMOS technology

Effects on ultra-thin gate oxides

- Reduction in the gate oxide thickness is responsible for an increase in the leakage current, which in turn results in an increase of the static power consumption, particularly harmful in digital circuits
- In the most recent CMOS technologies this problem is being addressed by replacing SiO_2 with stacks of different oxides or with so-called high-K oxides (oxides with a higher dielectric constant than SiO_2); both solutions result in a thicker oxide layer with much smaller leakage than a thinner silicon oxide layer but with the same control on the channel

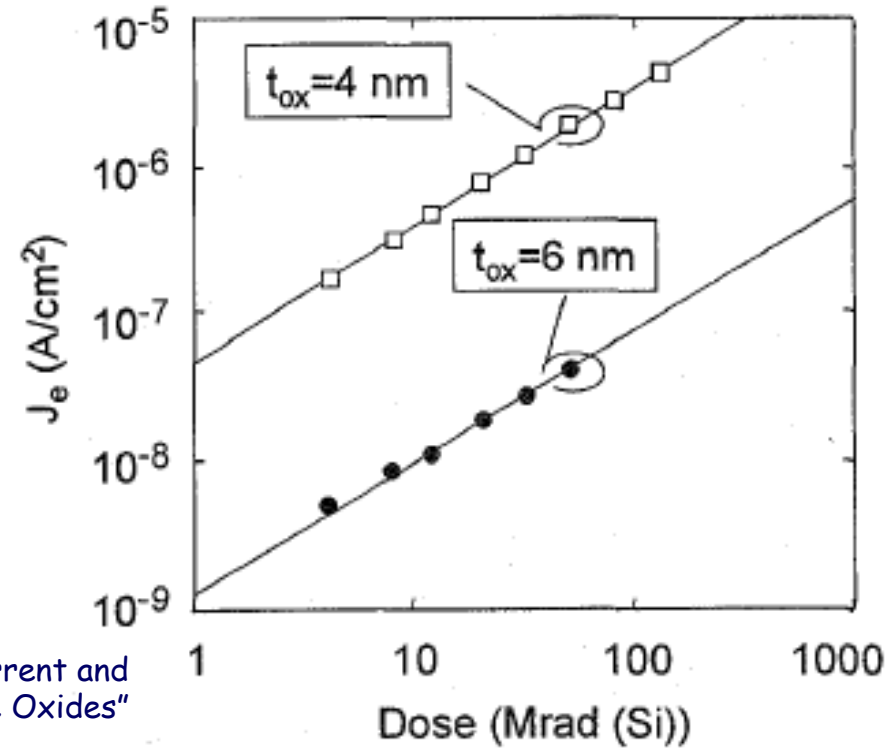
Gate current density (both simulated and measured) as a function of the gate-to-source voltage in MOSFET transistors

After D.J. Frank et al., "Device Scaling Limits of Si MOSFETs and Their Application Dependencies"



Effects on ultra-thin gate oxides

- Radiation effects on the gate leakage in ultra-thin gate oxides is at present one of the most interesting research subjects
- Exposure to ionizing radiation has the effect of increasing the gate leakage current according to a given power of the dose (experimentally found to be slightly less than unity for the samples in the figure)
- In thin oxides, quasi-breakdown phenomena can take place, due to the formation of a large area conductive path without the destruction of the insulating properties of the oxide layer, as in the case of the catastrophic breakdown



Gate current density as a function of the absorbed dose for two different oxide thicknesses exposed to 8 MeV electrons

After M. Ceschia et al., "Radiation Induced Leakage Current and Stress Induced Leakage Current in Ultra-Thin Gate Oxides"

Evolution of radiation effects in MOSFET: a conclusion

- Radiation-induced threshold voltage shift has been gradually eliminated by the natural evolution of advanced microelectronic technologies, where the gate oxide thickness has been reduced generation after generation

- Now the main radiation hardness issues in microelectronic circuits are those relevant to the isolating structures (radiation induced leakage currents, positive charge build-up in the field oxide, in particular the shallow trench isolations), affecting both static and noise properties of MOSFET devices, together with single event effects

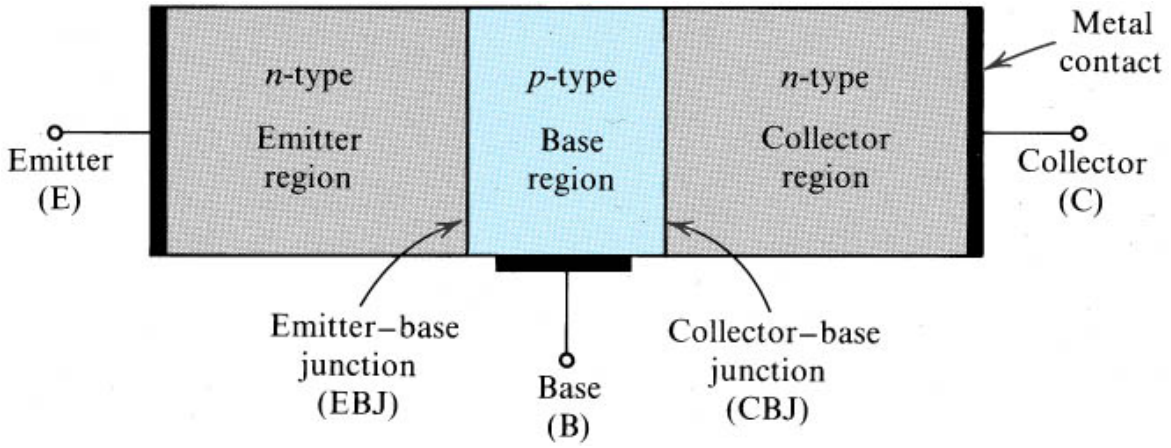
- Gate oxides with dielectric constant larger than in SiO_2 (High-K oxides) will be used to reduce the gate leakage current and alleviate some reliability issues; on the other hand, such new dielectric materials still need to be appropriately tested from the standpoint of radiation-tolerance

Radiation effects in BJTs

Bipolar junction transistors (BJTs) are widely used for analog applications where they may still offer some advantages with respect to MOSFET devices

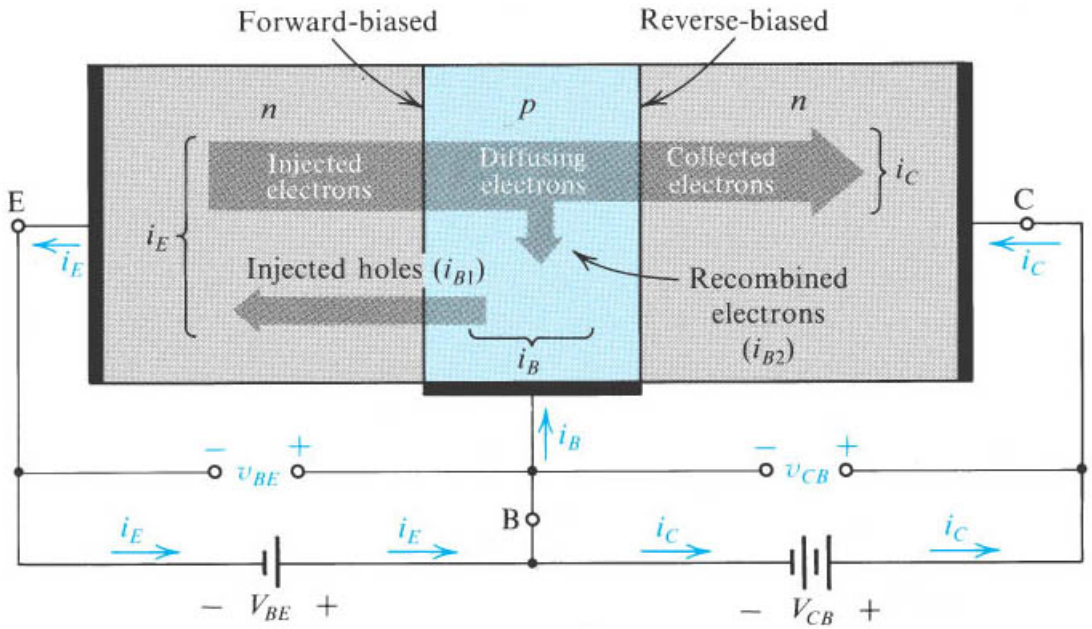
The BJT

- The bipolar transistor consists of two PN junctions connected in series (back to back in an NPN transistor); the term bipolar indicates that in the device, the current is conducted by both electrons and holes
- A BJT consists of three semiconductor regions, with alternating doping type, called the emitter, the base and the collector; therefore the BJT comes in two flavors, NPN (see the figure) and PNP; the three regions form the emitter-base and the collector-base junctions
- As an amplifier, the BJT is operated in the direct active region, i.e. with $V_{BE}>0$ (BE junction forward-biased) and $V_{BC}<0$ (BC junction reverse-biased) in an NPN device



Operation of the BJT

- Let us consider an NPN transistor operated in the direct active region
  - the forward bias on the EB junction will cause a current, the emitter current $\mathbf{I_E}$, to flow across the junction; the current will include holes injected from the base into the emitter and electrons from the emitter into the base (the latter providing the dominant contribution)
  - the electrons injected from the emitter into the base will be minority carriers in the P-type base region; they diffuse through the base region towards the collector and are swept across the CB junction depletion region
  - some of the electrons that diffuse through the base region recombine with holes, which are the majority carriers in the base and are provided by the base terminal through the $\mathbf{I_B}$ current; since the base is usually quite thin, the fraction of electrons lost through this recombination process is small; then, the collector current $\mathbf{I_C=I_E-I_B}$
  - the common-emitter current gain, $\mathbf{\beta=I_C/I_B}$, provides a measure of the electron recombination in the base



Total dose effects in bipolar transistors

- Operation of BJTs is based on the diffusion of minority carriers, e.g., electrons in the P-doped, thin base region; since BJT operation does not depend on surface potentials, as in MOS structures, bipolar transistors are less sensitive to ionizing radiation than MOSFETs
- Gain degradation and, to a lesser extent, leakage increase at the base-collector junction, are the most striking and common effects of radiation in bipolar transistors
- Two are the main causes for gain degradation
  - displacement in the bulk: bulk damage is responsible for an increase of the recombination centers, therefore reducing minority carrier lifetime
  - ionization of the passivation oxide layers (particularly of the oxide covering the emitter-base junction): by a process similar to that in MOS devices, charge trapping and generation of new interface states are responsible for the gain degradation
- Since the probability of recombination of minority carriers in the base depends on the transition time, bipolar transistors with shorter bases are more radiation-tolerant

Gain degradation due to bulk damage

- Mid-gap states in the silicon band-gap facilitate the recombination of minority carriers in the base of a bipolar transistor, therefore reducing its current gain
- Atomic displacement induced by irradiation is responsible for an increase in the concentration of the recombination centers and for a reduction of the minority carrier lifetime τ

$$\frac{1}{\tau} - \frac{1}{\tau_0} = K_\tau \Phi$$

- τ_0=pre-irradiation minority carrier lifetime
- K_τ=minority carrier lifetime damage constant (to be measured in $cm^2 s^{-1}$)
- Φ=particle fluence

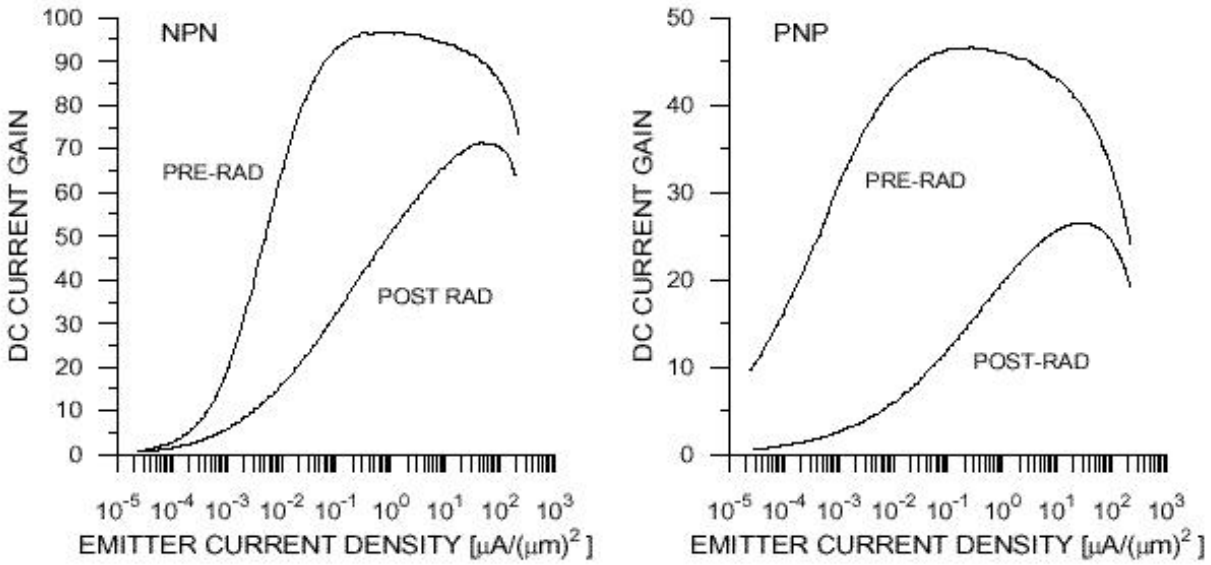
- Damage (the K_τ constant) is strongly dependent on the radiation type and energy and on the silicon doping concentration

- The reduction in the current gain induced by bulk damage is generally characterized through a gain damage figure $\Delta(1/\beta)_b$

$$\Delta(1/\beta)_b = \frac{1}{\beta} - \frac{1}{\beta_0} = K_b \Phi$$

- β_0=pre-irradiation current gain
- β=post-irradiation current gain
- K_b=gain damage constant (to be measured in $cm^2 s^{-1}$)

Gain degradation due to bulk damage

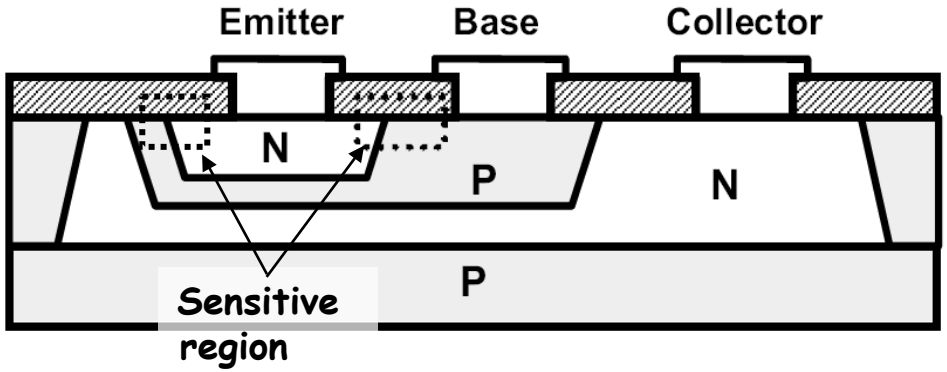


Gain degradation in an NPN and a PNP bipolar transistors; the curves show the current gain as a function of the emitter current density before irradiation and after exposure to a 1.2×10^{14} cm^{-2} fluence of 800 MeV protons

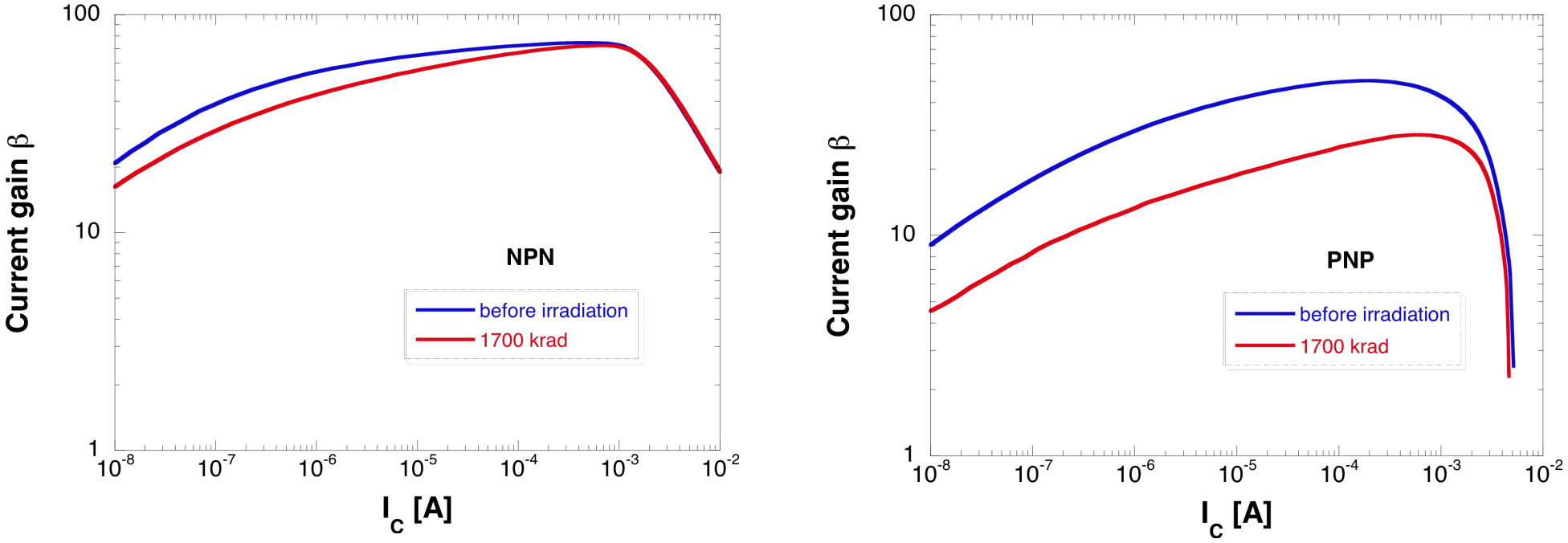
- The fractional carrier loss depends on the relative concentration of injected carriers and defects; consequently, the reduction of current gain due to radiation damage depends on current density; for a given collector current, a small device will suffer less degradation in current gain than a large one
- Transistors with shorter bases are more radiation-tolerant because of the reduced recombination probability; base width is strongly linked to device speed, so that the reduction in current gain scales inversely with the transistor unity gain frequency f_T; therefore mainstream market, driven primarily by device speed, tends to improve the radiation resistance of BJTs

Gain degradation due to ionization damage

- The electric field due to hole trapping in SiO_2 passivation over the base-emitter junction may widen the space charge region at the base surface, causing an increase in the I_B component due to recombination current in the BE depletion region
- With the same process as the one described for MOSFET, interaction of holes with oxide lattice defects containing hydrogen atoms may also be responsible for trap build up at the Si/SiO_2 boundary, thus increasing surface recombination velocity in the base region
- Hole trapping in the oxide and trap build-up at the silicon/oxide interface both contribute to gain degradation; such a contribution is represented by the relevant gain damage figure $\Delta(1/\beta)_s$
- In vertical transistors, such contributions, which come from surface effects, is more significant in devices featuring a larger emitter perimeter to emitter area ratio (the relative weight of the surface contributions to I_B increases)



Gain degradation due to ionization damage



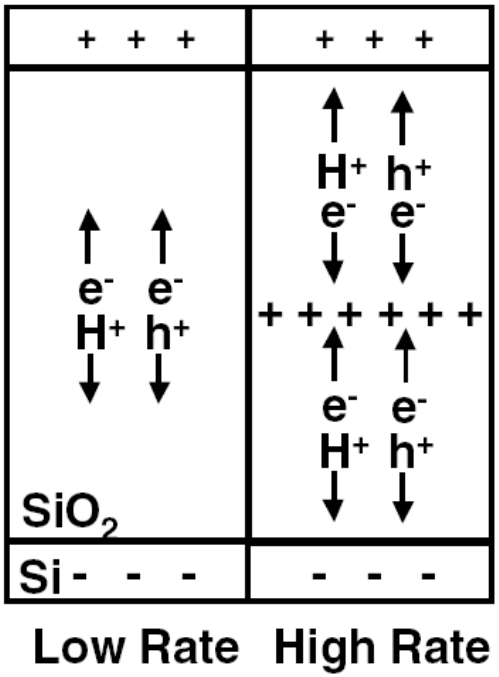
Gain degradation in an NPN and a PNP bipolar transistors before and after irradiation with a ^{60}Co total ionizing dose of 1.7 Mrad(SiO_2) (17 kGy(SiO_2))

- Degradation due to ionizing radiation is more significant at small collector currents; this is in agreement with the fact that radiation induced excess current in the device base comes from recombination phenomena in the space charge region, which predominates at small base-to-emitter voltages

Dose rate effects in BJTs

- Bipolar transistors are known to suffer from the so-called enhanced low dose rate sensitivity (ELDRS); dose rate used in ionizing radiation testing have a profound effect on the amount of surface degradation suffered by the device; this implies that accelerated radiation testing, normally done at dose rates thousands of times higher than those experienced in real applications, could have a strong impact on the test results
- While in irradiation facilities, to reduce testing time, typical dose rates lie generally between 10 $Gy(SiO_2)/s$ and a few $mGy(SiO_2)/s$, they, for instance, amount to less than 10^{-4} $Gy(SiO_2)/s$ in space applications and to about $5x10^{-4}$ $Gy(SiO_2)/s$ in high energy physics experiments
- Suppression of radiation sensitivity of thick oxides at high dose rates can be considered a space-charge limited effect; positive oxide-trapped charge provides a deterrent particularly for interface trap formation; this type of positive charge appear to be able to escape the oxide if given time or extra vibratory energy by heating; therefore, if a given dose is administered rapidly at 100°C, the result is similar to that dose being given slowly at room temperature

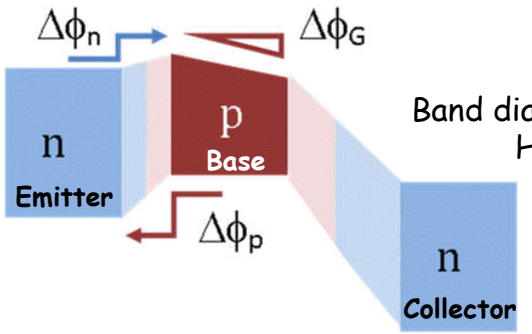
Dose rate effects in BJTs



- At high dose rates, radiation-triggered migration of H^+ ions from oxide defects to the Si/SiO_2 interface, and the consequent trap formation, is prevented by the electrostatic barrier raised by the oxide trapped charge; the opposite may happen under low dose rate conditions; low dose rates are more effective in PNP transistors, where the only ionizing damage mechanism at work is the one involving trap formation at the Si/SiO_2 interface (the very mechanism which is enhanced by low dose rates)

Heterojunction (SiGe) bipolar transistors

- Heterojunction bipolar transistors (HBTs) are becoming more and more important as high speed devices; they offer advanced electrical performance, particularly for high frequency applications, with cut-off frequencies in excess of 60 GHz
- Heterojunction transistors use different semiconductors as the elements of the device; usually the emitter is composed of a larger band-gap material than the base; the effect is to limit the injection of holes from the base into the emitter region, since the potential barrier in the valence band ($\Delta\varphi_p$) is higher than in the conduction band ($\Delta\varphi_n$); unlike BJT technology, this allows a high doping density to be used in the base, reducing the base resistance while maintaining gain.
- Use of a graded germanium (Ge) content in the base is proved to introduce a potential gradient ($\Delta\varphi_G$) resulting in a built-in accelerating field speeding the transport of electrons



Band diagram in a HBT

- High base and emitter doping levels reduce the sensitivity of the surface carrier concentration to radiation-induced charge in the oxide; HBTs were also found to be relatively immune to enhanced low dose rate sensitivity (ELDRS) effects

Radiation resistant technologies and hardening techniques

Based on the device response to radiation and on the mechanisms of radiation damage, some counteractions can be taken to improve radiation tolerant of devices and circuits

Radiation hardening techniques

- In some cases, mainstream market forces, which drive the evolution of microelectronic technologies, may indirectly improve the radiation resistance of electronic devices (e.g., device speed in bipolar transistors, device scaling in complementary MOSFETs)
- Whenever a device is not sufficiently radiation hard for the foreseen application, some measures can be taken to make it harder; this can be obtained by
  - modifying the device geometrical layout (**hardening by layout**)
  - modifying one or more steps of the fabrication process (**hardening by process**)
  - suitably designing the overall circuit or system (**hardening by design**)

Radiation hard technologies

- Commercial technologies for integrated circuits commonly evolve by improving on speed, scale of integration, complexity and power dissipation; many of the technology developments needed to achieve these results have been beneficial in terms of radiation-tolerance

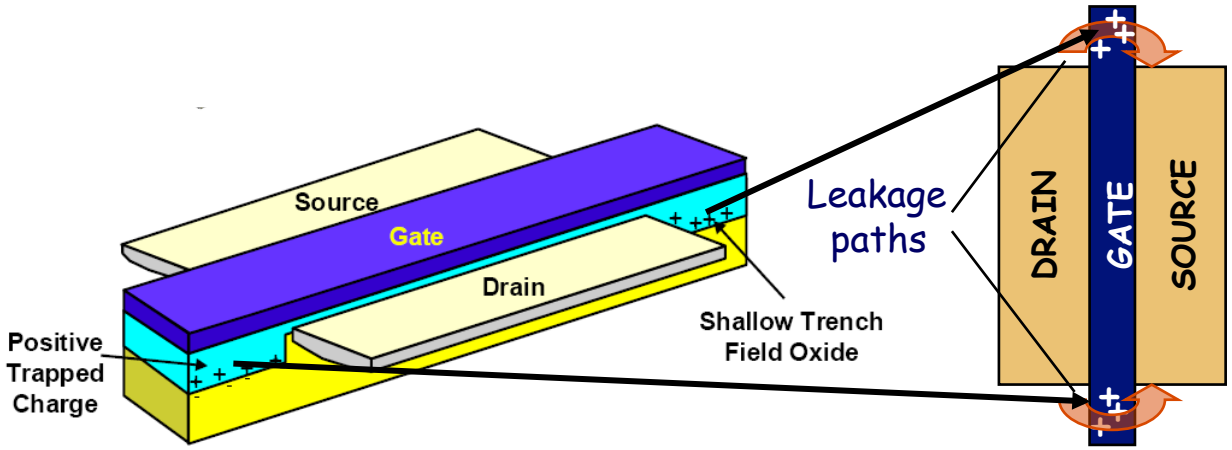
- Commercial deep submicron CMOS technologies can already provide total ionizing dose hardness levels in the range of several units up to several tens of megarad; use of ultra-thin (a few nm) oxides limits the effects of oxide trapped charge; use of thin epitaxial layers, retrograde wells and shallow trench isolation improve hardness against latch-up

- SOI technology is of significant commercial interest because of the advantages it offers in terms of speed, power and integration density; the fact that it also offers total device isolation is an advantage in terms of radiation effects; because of the insulating layer, the technology is immune to destructive latch-up

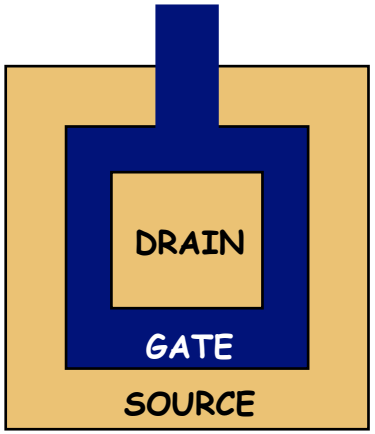
Hardening by layout

- In irradiated NMOS devices, positive charge trapped in the shallow trench isolation oxides is responsible for the formation of conductive paths along the STI sidewalls
- If an enclosed layout is used, no parasitic path can form between source and drain, because there is no thick oxide layer running along the main channel

Standard layout

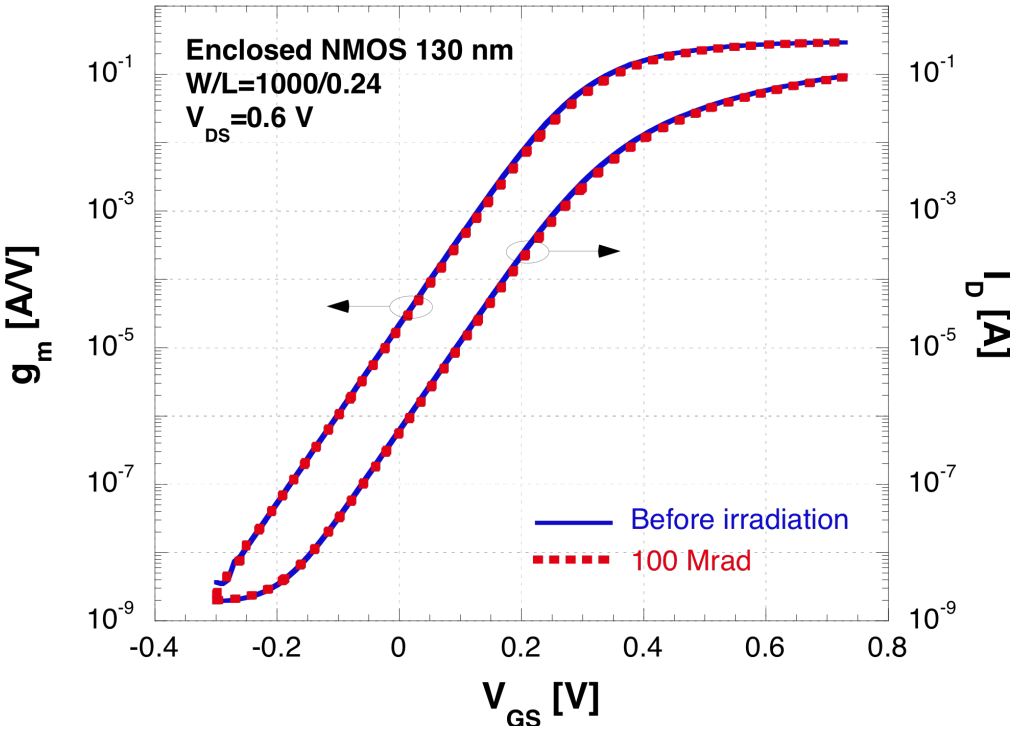


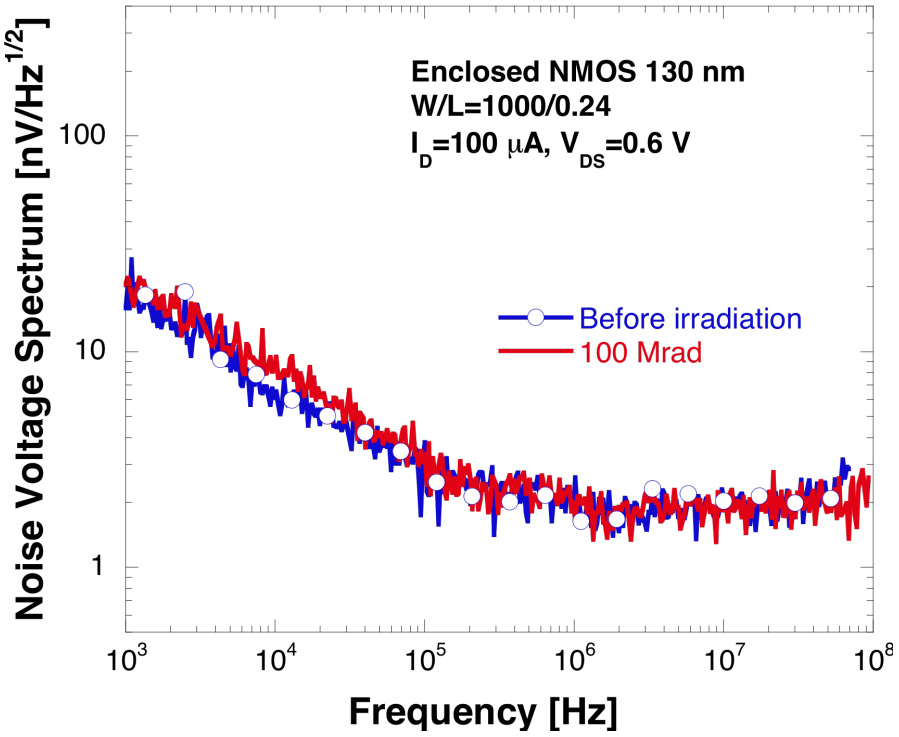
Enclosed layout



Hardening by layout

- In enclosed layout (also called edgeless) NMOS transistors, static and noise properties are affected by radiation to a very limited extent
- This radiation hardening technique has been exploited in the design of the front-end electronics for semiconductor detectors at the Large Hadron Collider experiments

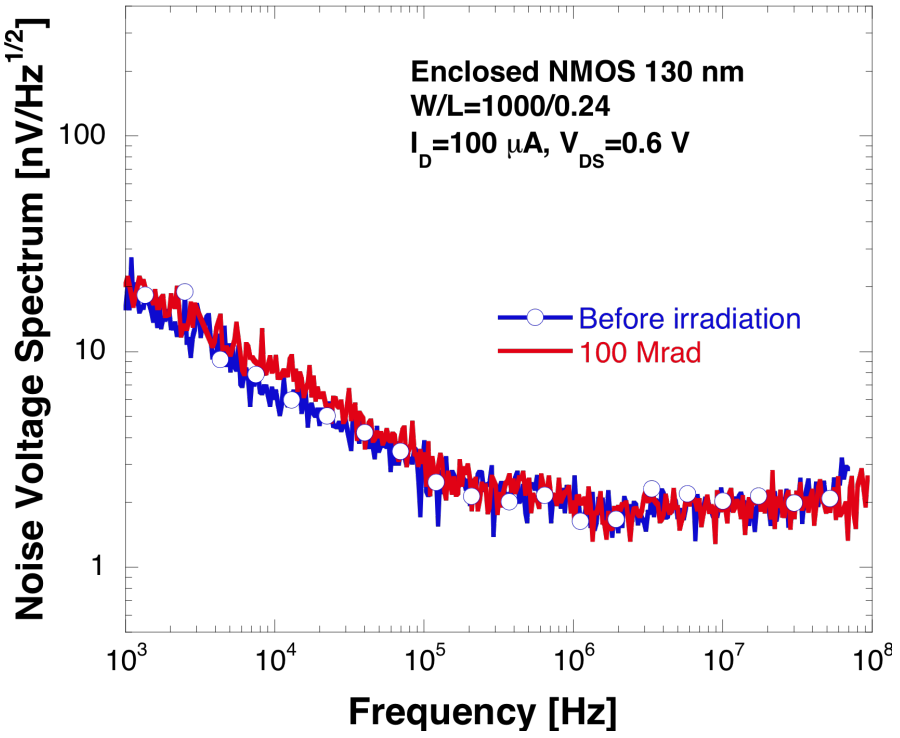




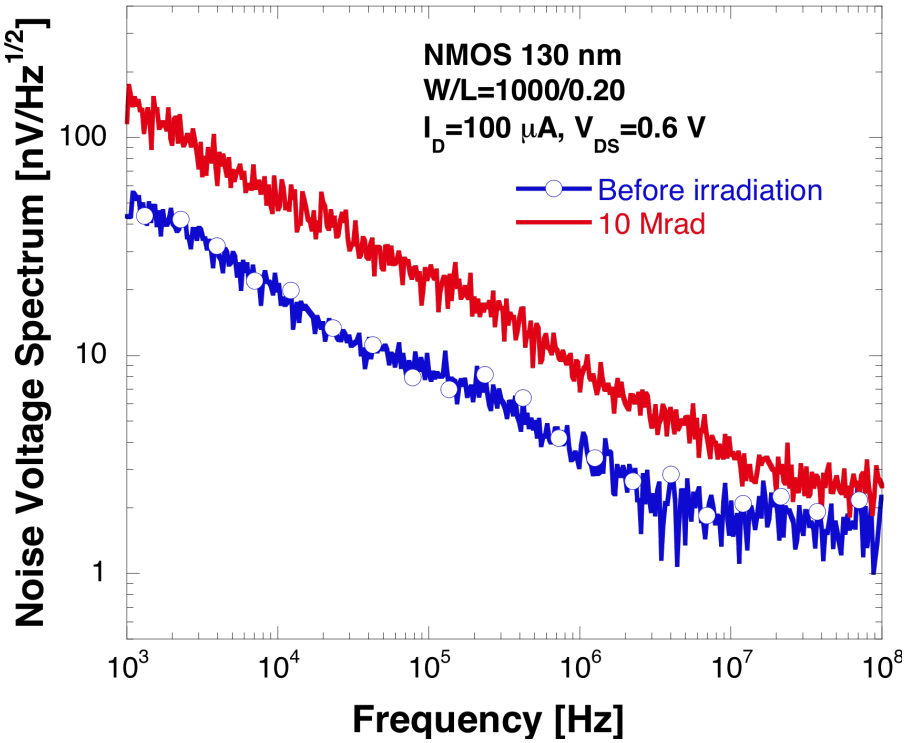
Hardening by layout

- Enclosed layout significantly improves NMOS radiation response with respect to standard interdigitated layout

NMOS 130 nm
Enclosed layout
Dose: 100 Mrad (1 MGy)



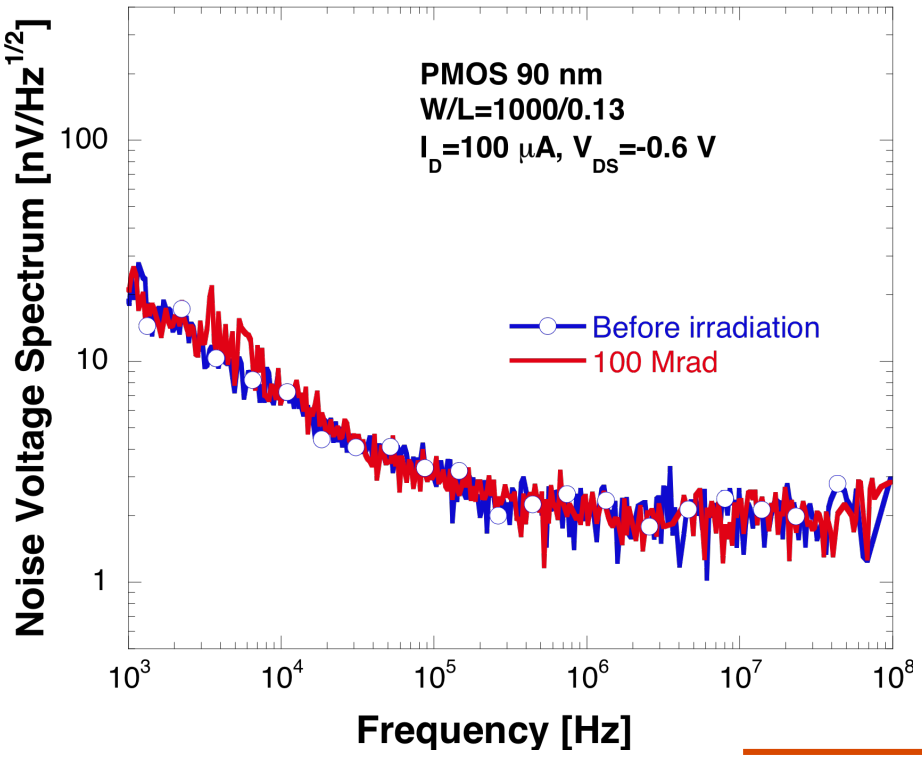
NMOS 130 nm
Standard interdigitated layout
Dose: 10 Mrad (100 kGy)



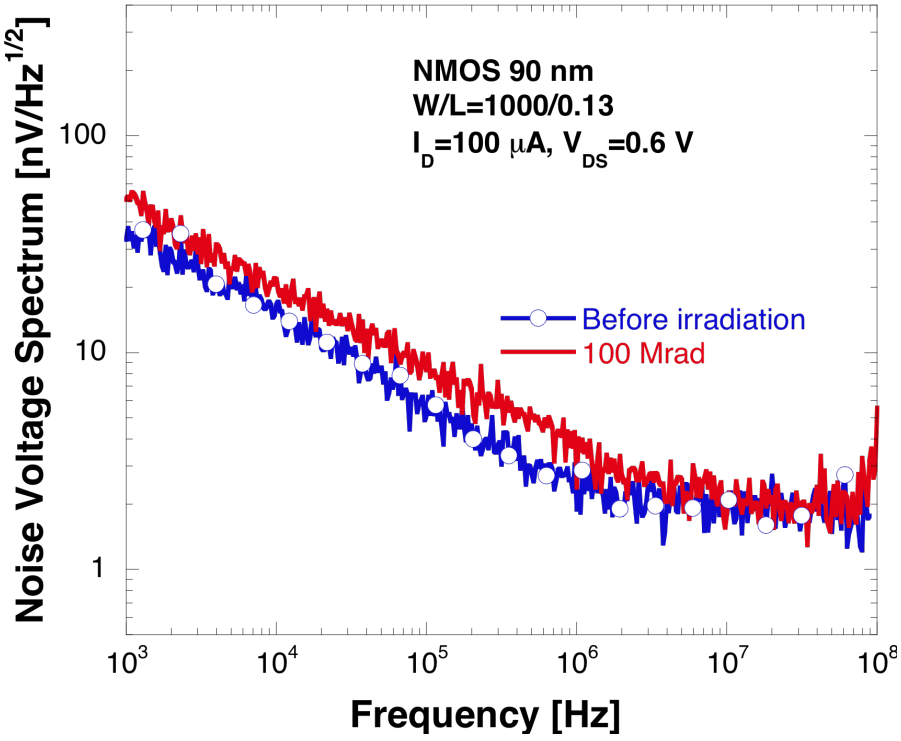
Hardening by choice of the polarity

- PMOS transistors are much harder than NMOS devices; positive charge trapped in the shallow trench isolation oxides has no effect because the substrate is N-type (as a consequence, silicon underneath the STI is accumulated instead of being inverted)

PMOS 90 nm
Standard interdigitated layout
Dose: 100 Mrad (1 MGy)



NMOS 90 nm
Standard interdigitated layout
Dose: 100 Mrad (1 MGy)



Hardening by process and by design

- A large number of steps are involved in the fabrication of a typical MOS integrated circuit and many of these steps can influence the radiation hardness of a device; the most important factors are those which affect the charge trapping characteristics of the oxides (gate oxide, field oxide, intermetal oxide) and the relevant interfaces

- Deep submicron technologies are generally more sensitive to single event upset than older technologies; however, tolerance to SEU, can be improved by means of design techniques; in the case of digital circuits, a typical solution involves using logic redundancy, which may consist, for instance, in the triplication of the digital processing chain integrated in a majority voting system (in this case, a radiation-induced error in one bit may be outvoted by the other two, not affected components)

Bibliography

- W. R. Dawes et al, "Hardening Semiconductor Components Against Radiation and Temperature", Noyes Data Corporation, Park Ridge, 1989.
- T.P. Ma and P.V. Dressendorfer, "Ionizing Radiation Effects in MOS Devices and Circuits", John Wiley & Sons, New York, 1989.
- T. R. Oldham, "Ionizing Radiation Effects in MOS Oxides", World Scientific, 1999.
- C. Claeys and E. Simoen, "Radiation Effects in Advanced Semiconductor Materials and Devices", Springer Verlag, 2002.
- A. Holmes-Siedle, L. Adams, "Handbook of radiation effects", Oxford University Press, 2002.
- Spieler, H., "Introduction to Radiation-Resistant Semiconductor Devices and Circuits", http://www-physics.lbl.gov/~spieler/radiation_effects/rad_tutor.pdf
- G. Cesura, V. Re, "Effects of g-rays and Neutrons on the Noise Behaviour Of Monolithic JFET Circuits", **IEEE Trans. Nucl. Sci.**, Vol. 41, No. 3, Jun. 1994, pp. 577-582.
- M. Manghisoni, L. Ratti, V. Re, V. Speziali, "Radiation hardness perspectives for the design of analog detector readout circuits in the 0.18 μm CMOS generation", **IEEE Trans. Nucl. Sci.**, Vol. 49, No. 6, Dec. 2002, pp. 2902-2909.
- V. Re, M. Manghisoni, L. Ratti, V. Speziali, G. Traversi, "Total ionizing dose effects on the noise performances of a 0.13 μm CMOS technology", **IEEE Trans. Nucl. Sci.**, Vol. 53, No. 3, Jun. 2006, pp. 1599-1606.
- F. Faccio and G. Cervelli, "Radiation-induced edge effects in deep submicron CMOS transistors", **IEEE Trans. Nucl. Sci.**, Vol. 52, No. 6, Dec. 2005, pp. 2413-2420.
- H. J. Barnaby, "Total-Ionizing-Dose effects in modern CMOS technologies", **IEEE Trans. Nucl. Sci.**, Vol. 53, No. 3, Dec. 2006, pp. 3103-3121.

Bibliography

- Special Issue of the IEEE Transactions on Nuclear Science, Vol. 50, No. 3, Jun. 2003.
- F. Faccio et al., "Single Event Effects in Static and Dynamic Registers in a 0.25 μm CMOS Technology", **IEEE Trans. Nucl. Sci.**, Vol. 46, No. 6, Dec. 1999, pp. 1434-1439.
- N.S. Saks et al., "Radiation effects in MOS capacitors with very thin oxides at 80°K", **IEEE Trans. Nucl. Sci.**, Vol. 31, No. 6, Dec. 1984, pp. 1249-1255.
- N.S. Saks et al., "Generation of interface states by ionizing radiation in very thin MOS oxides", **IEEE Trans. Nucl. Sci.**, Vol. 33, No. 6, Dec. 1986.
- M. Manghisoni, L. Ratti, V. Re, V. Speziali, G. Traversi, A. Candelori, "Comparison of ionizing radiation effects in 0.18 and 0.25 μm CMOS technologies for analog applications", **IEEE Trans. Nucl. Sci.**, Vol. 50, No. 6, Dec. 2003, pp. 1827-1833.
- M. Ceschia et al., "Radiation Induced Leakage Current and Stress Induced Leakage Current in Ultra-Thin Gate Oxides", **IEEE Trans. Nucl. Sci.**, Vol. 45, No. 6, Dec. 1998, pp. 2375-2382.
- D.J. Frank et al., "Device Scaling Limits of Si MOSFETs and Their Application Dependencies", **Proceedings of the IEEE**, Vol. 89, No. 3, Mar. 2001, pp. 259-288.
- G.F. Dalla Betta, M. Manghisoni, ,L. Ratti, V. Re, V. Speziali, G. Traversi, A. Candelori, "Proton induced damage in JFET transistors and charge preamplifiers on high-resistivity silicon", **IEEE Trans. Nucl. Sci.**, Vol. 51, No. 5, pp. 2880-2886, Oct. 2004.
- L. Ratti, L. Gaioni, M. Manghisoni, G. Traversi, D. Pantano, "Investigating Degradation Mechanisms in 130 nm and 90 nm Commercial CMOS Technologies Under Extreme Radiation Conditions", **IEEE Trans. Nucl. Sci.**, Vol. 55, No. 4, pp. 1992-2000, Aug. 2008.
- M. Manghisoni, L. Ratti, V. Re, V. Speziali, "Selection criteria for P- and N-channell JFETs as input elements in low-noise radiation-hard charge preamplifiers", **IEEE Trans. Nucl. Sci.**, Vol. 48, No. 4, pp. 1598-1604, Aug. 2001.

Backup

Dosimetry

Dosimetry

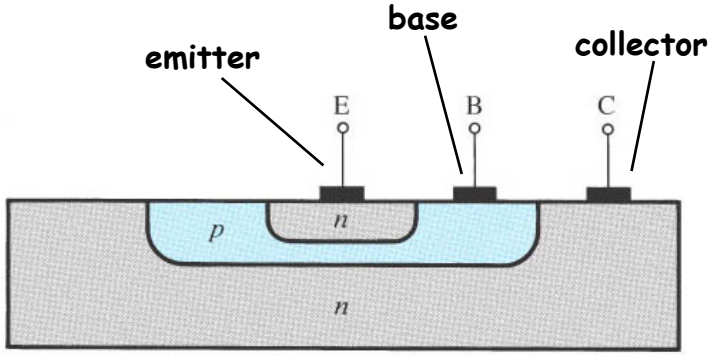
- Measurement of the amount of energy absorbed by (or of the particle or photon flux striking) a sample exposed to a radiation source
- Dosimetry methods have been developed to deal with the two different effects radiation may have on crystals
  - deposition of **ionization energy** in silicon dioxide, silicon and a few other materials involved in the fabrication of electronic circuits
  - **non-ionizing energy loss** (**NIEL**), mainly in the form of atomic displacement in crystalline lattices
- Deposited energy is measured in rad (corresponding to the specific energy of 100 erg/g) or Gray (Gy, an SI unit, corresponding to the specific energy of 1 J/kg); based on the definitions, 1 Gy=100 rad (remember that 1 erg=10^{-7} J)
- Particle flux is generally measured in (number of particles) $cm^{-2}s^{-1}$; particle fluence is measured in (number of particles) cm^{-2} and is, by definition, the time integral of the particle flux

Basic mechanisms of radiation damage

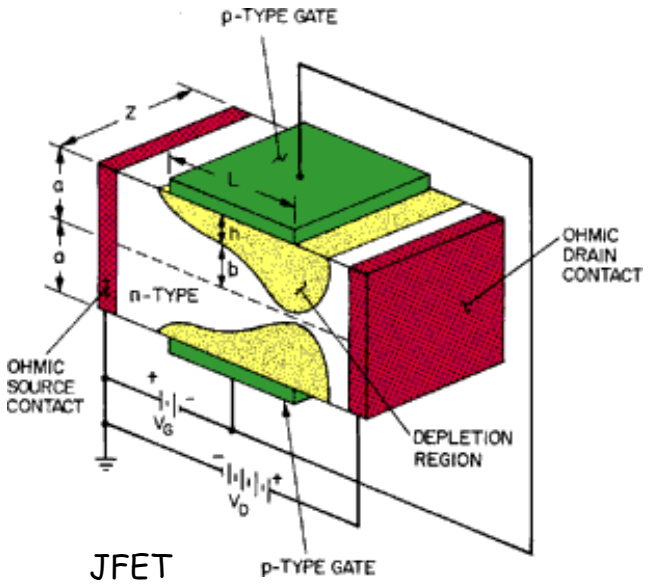
Radiation can interact with matter (and, in particular, with semiconductor material) through different mechanisms, producing different effects on different kinds of devices and circuits

Effects in bulk-effect devices

- In bulk-effect devices, the main device current flows in the bulk of the device, generally far enough from any surface between different materials (e.g., Si and SiO_2)
- Bulk-effect devices are particularly sensitive to dislocation damage, which is responsible for degradation of average carrier lifetime (due to recombination phenomena), mobility decrease and carrier density reduction
- Bipolar junction transistor (BJT) operation is based on minority carrier diffusion and can be strongly affected by average carrier lifetime degradation, leading to degradation in the current gain
- Junction field-effect transistor (JFET) operation is based on majoritity carrier dirft and can be strongly affected by carrier trapping phenomena leading to gate leakage current increase and appearance of Lorentzian noise components in the drain current



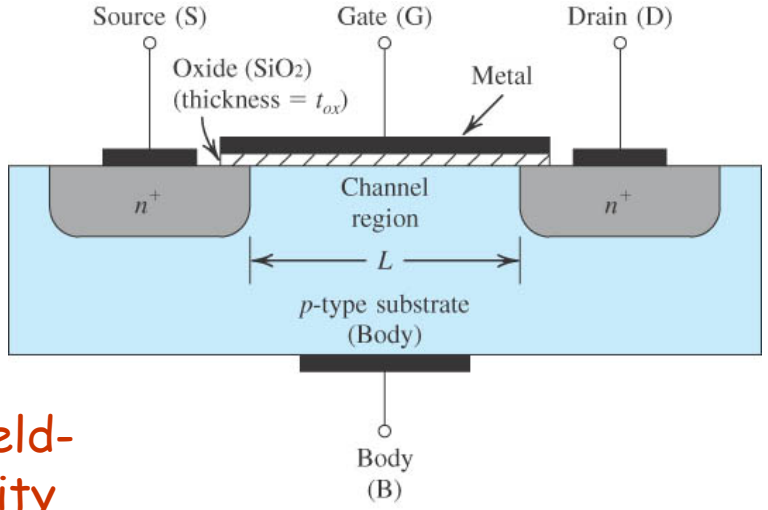
Bipolar junction transistor



JFET

Effects in surface controlled devices

- In surface-controlled devices, the main device current flows at the interface between two layers of different materials, e.g. silicon and silicon dioxide in MOSFETs



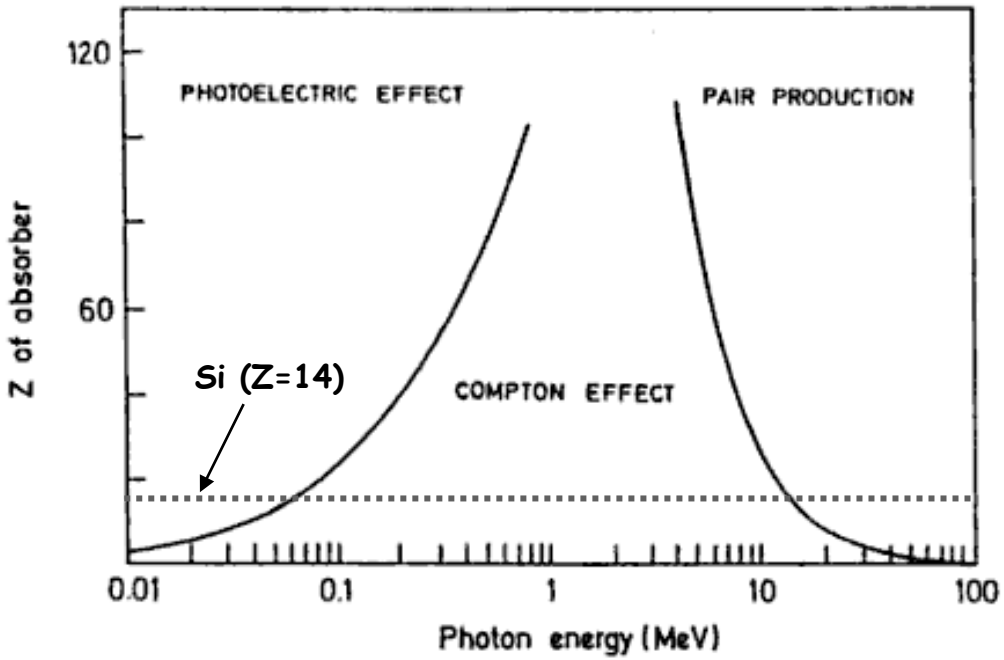
- Surface-controlled devices are particularly sensitive to ionizing dose effects, which are responsible for charge trapping in SiO_2 layers and for an increase in Si/SiO_2 interface state density
- Operation of the metal oxide semiconductor field-effect transistor (MOSFET) is based on majority carrier drift at the interface between SiO_2 and Si (on the silicon side); it can be strongly affected by charge trapping in the gate oxide and by surface effects due to capture and release of carriers from the device channel, which can lead to threshold voltage shift, parasitic leakage currents and mobility degradation
- MOSFETs are also sensitive to single event effects, which can produce destructive (e.g., circuit burnout) or non-destructive (e.g. bit flip) damage

Interaction of radiation with matter

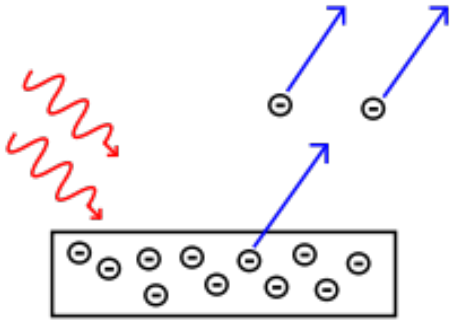
- As already observed, there are many different sorts of radiation environments where an electronic system may happen to be operated
- In each environment, electronic circuits may be exposed to (a mix of) different kinds of radiation and particles which, from the standpoint of radiation-matter interaction properties, can be grouped in three major categories
  1. photons (highly energetic photons, X and γ-rays are of particular interest)
  2. charged particles (electrons, protons, α-nuclei and heavy ions)
  3. neutrons
- The interaction of such particles with matter depends on several factors, namely on the mass, charge state and kinetic energy of the incident particle and on the atomic mass A, atomic number Z and density of the target material
- A particle (whether a photon, a charged particle or a neutron) impinging on a semiconductor electronic device may damage it through one of two basic mechanisms
  1. ionization
  2. displacement

Photon interaction with matter

- Photons interact with matter through one of three different mechanisms, according to the atomic number of the target atom and the energy of the incident particle:
  1. photoelectric effect
  2. Compton scattering
  3. pair production

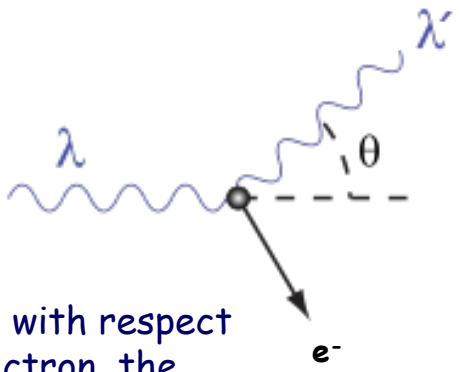


- **Photoelectric effect**: in the photoelectric absorption process, the incident photon, after interacting with an atom of the target material, completely disappears; in its place, an energetic photoelectron is ejected by the atom from one of its bound shells; the photoelectrons appears with an energy $E_{e^-}=h\nu-E_b$, where $h\nu$ is the energy of the incident photon and E_b is the binding energy of the electron in its original shell



Photon interaction with matter

- **Compton scattering**: it is the predominant interaction mechanism for γ-ray energies typical of radioisotope sources (like ^{60}Co); for silicon (Z=14) the Compton effect dominates for energies of the incident photon between 50 keV and 10 MeV

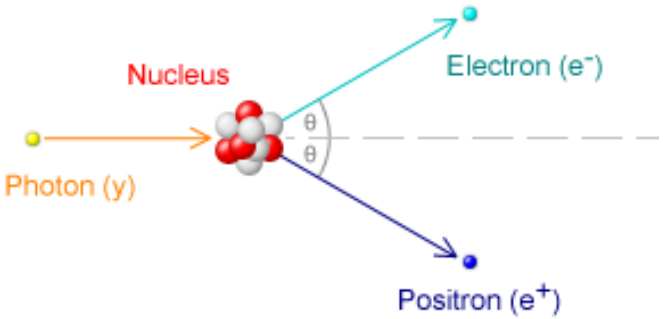


  - In Compton scattering, the incoming photon is deflected through an angle θ with respect to the original direction; part of the energy is transferred to the recoil electron, the amount of energy depending on the scattering angle; the energy of the photon before and after the interaction and the scattering angle are related as follows

$$h\nu' = \frac{h\nu}{1 + \frac{h\nu}{m_0 c^2} \cdot (1 - \cos\vartheta)}$$

- h=Plank's constant
- m_0=electron rest mass
- c=light speed

- **Pair production**: the process becomes energetically possible when the energy of the incident photon exceeds twice the rest mass of the electron, i.e. 1.02 MeV (the probability is actually very low below 2 MeV); in the interaction the photon disappears and is replaced by an electron-positron pair; all the energy exceeding 1.02 MeV goes into kinetic energy of the newly generated particles



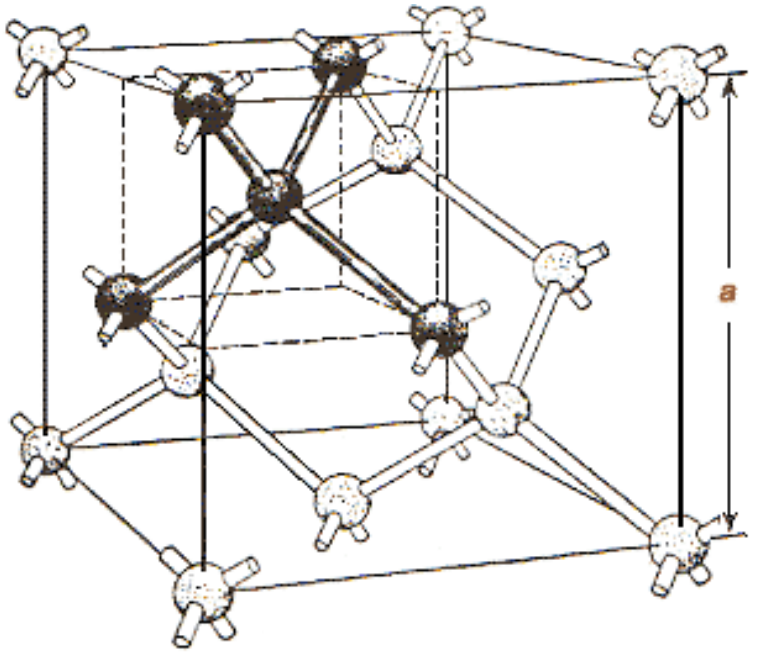
Charged particle and neutron interactions with matter

- **Charged particles** interact with matter mainly through Coulomb scattering; the charged particle, upon entering the target material, immediately interacts with many electrons simultaneously; depending on how close the particle gets to atoms, Coulomb forces may be sufficient to either rise an electron to a higher lying shell within the atom (**excitation**) or to completely remove the electron from the atom (**ionization**); **nuclear interaction**, including elastic scattering and possible atom displacement or transmutation of the target atom can take place when heavy charged particles are involved

- **Neutrons** interact with matter by collision with atomic nuclei
  - In an **elastic scattering process**, the neutron gives up a portion of its energy to an atom of the target material, eventually dislodging the atom, which is referred to as primary recoil, from its lattice position; the primary recoil can in turn displace other lattice atoms
  - **Inelastic scattering** involves the capture of the incident neutron by the nucleus of the target atom and subsequent emission from the nucleus at a lower energy; the nucleus, left in an excited state returns to its original condition by emission of a gamma-ray
  - **Transmutation reaction** involves the capture of the incident neutron by the target nucleus and subsequent emission of another particle (a proton or an α particle); the remaining atom is thereby converted into another element

Semiconductor devices and circuits

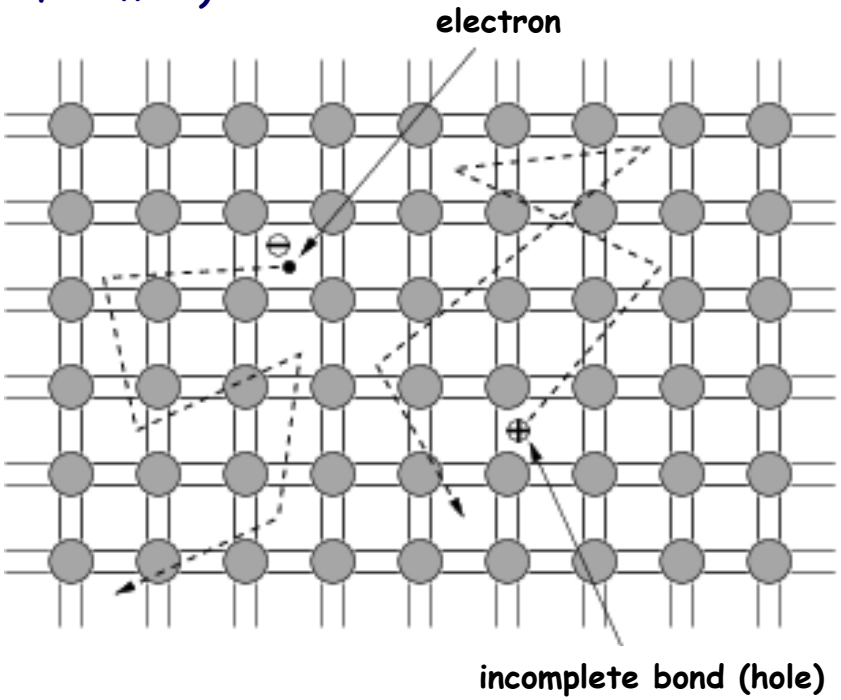
- Modern microelectronic industry relies upon the properties of semiconductor materials and, in particular, of silicon (Si); planar processing technology derives its success from the properties of thermally grown silicon dioxide (SiO_2), which features a reticular constant very close to that of silicon
- A silicon crystal has the same periodical structure as diamond; each silicon atom has four valence electrons forming four covalent bonds with four neighbor atoms
- The electrical characteristics of silicon can be modified by suitably adding impurities (P, As, B) with controlled concentration and growing thin oxide layers in well defined places; an integrated circuit also includes metal (Al, Cu) strips for device interconnection and silicon nitride for intermetal isolation



Three dimensional representation of atoms position in a silicon crystal

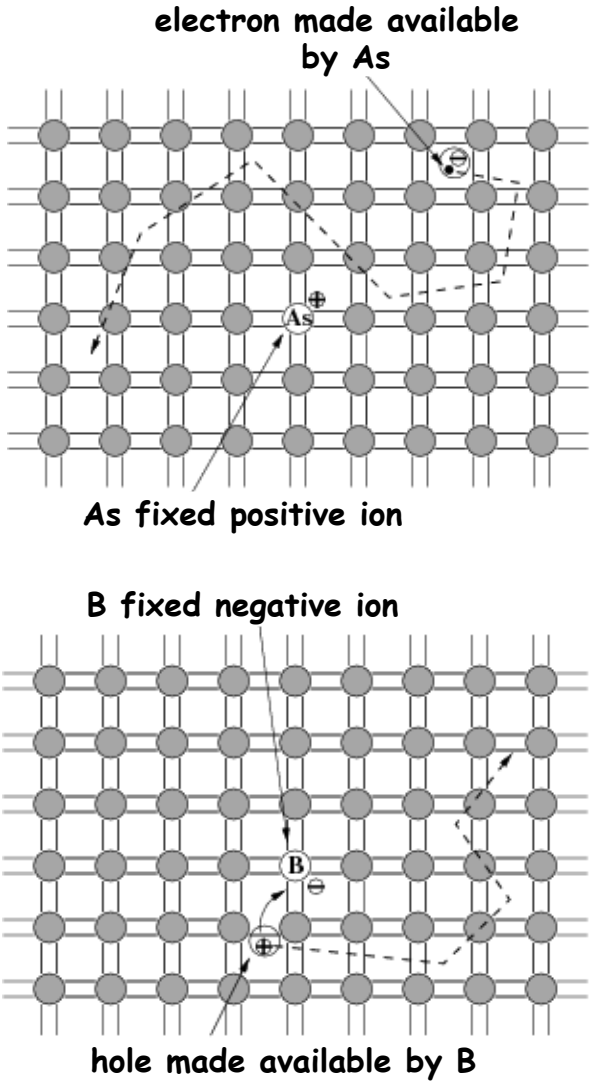
Semiconductor devices and circuits

- In intrinsic (i.e. pure) silicon, at room temperature, an electron can acquire energy due to thermal agitation and break free from a covalent bond, leaving behind an unbalanced positive charge unit in the atom it belonged to and an incomplete bond or hole (electron-hole generation)
- An electron from a neighbor atom can be attracted by the positive charge and fill the first hole (electron-hole recombination) while in turn leaving behind another hole (i.e. breaking the covalent bond it formed)
- This break (a covalent bond) and fill (a hole) mechanism can recur in such a way that a hole (and the associated unbalanced positive charge unit) can be carried around in the lattice, therefore behaving like a positive charge carrier; this mechanism is actually exploited to drive currents in electronic devices



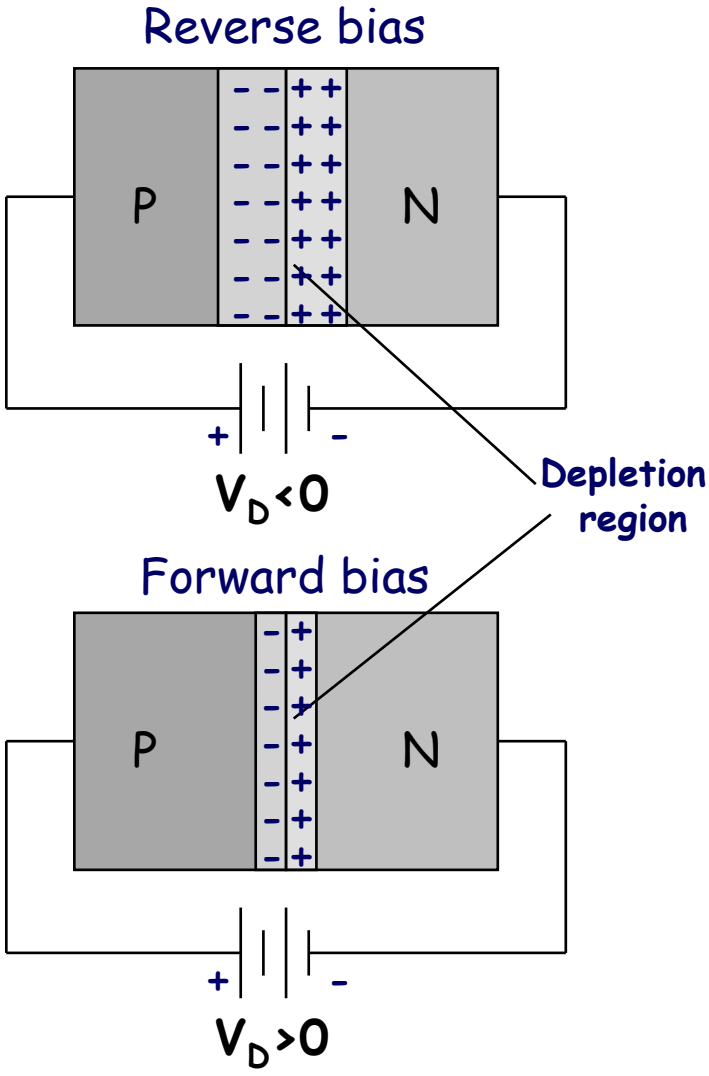
Semiconductor devices and circuits

- The electrical properties of silicon, in particular to enhance the concentration of free carriers, can be changed by the so called doping process, which involves adding impurities with a given concentration to the silicon lattice
- **N-doping**: increases the concentration of electrons by adding donor atoms (atoms of a pentavalent element like As or P), each **donating** an electron to the silicon lattice; an N-doped piece of silicon is called N-type silicon
- **P-doping**: increases the concentration of holes by adding acceptor atoms (atoms of a trivalent element like B), each **accepting** an electron from the silicon lattice; a P-doped piece of silicon is called P-type silicon



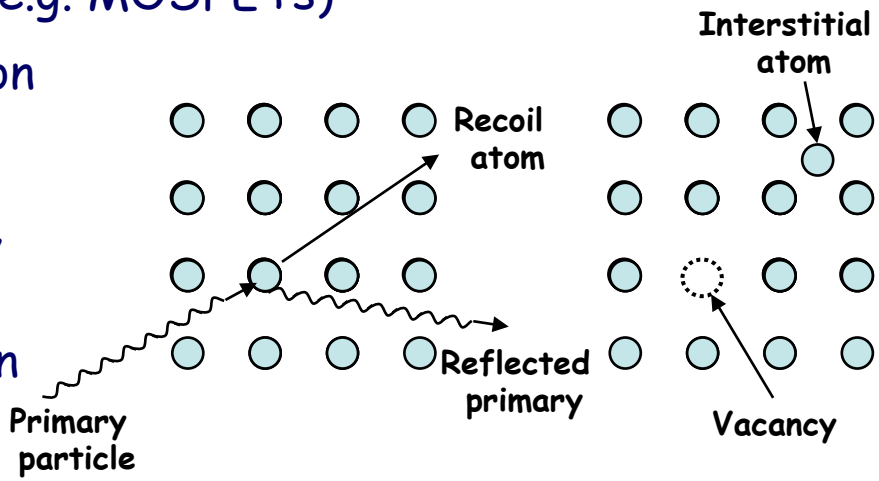
PN junctions

- PN junctions are ubiquitous in semiconductor devices; they consist of two regions, one P-doped, the other one N-doped facing each other on a single silicon crystal
- If the N side is biased at a higher potential than the P side, then the junction is operated in a reverse bias condition; a very small drift current flows from the N region to the P one; the depletion region (also called space charge region) gets wider
- If the P side is biased at a higher potential than the N side, then the junction is operated in a forward bias condition; large hole and electron diffusion currents flood the N and P side respectively; the depletion region (also called space charge region) gets smaller



Basic damage mechanisms in semiconductor devices

- Despite the complexity of the interaction processes and their dependence on the properties of the incident particle and of the target material, two are the basic radiation damage mechanisms affecting semiconductor devices
- **Ionization damage**: takes place when energy deposited in a semiconductor or in insulating layers, chiefly SiO_2, frees charge carriers (electron-hole pairs), which diffuse or drift to other locations where they may get trapped, leading to unintended concentrations of charge and parasitic fields; this kind of damage is the primary effect of exposure to X- and γ-rays and charged particles; it affects mainly devices based on surface conduction (e.g. MOSFETs)
- **Displacement damage (DD)**: incident radiation dislodges atoms from their lattice site, the resulting defects altering the electronic properties of the crystal; this is the primary mechanism of device degradation for high energy neutron irradiation, although a certain amount of atomic displacement may be determined by charged particles (including Compton secondary electrons); DD mainly affects devices based on bulk conduction (e.g. BJTs, diodes, JFETs)



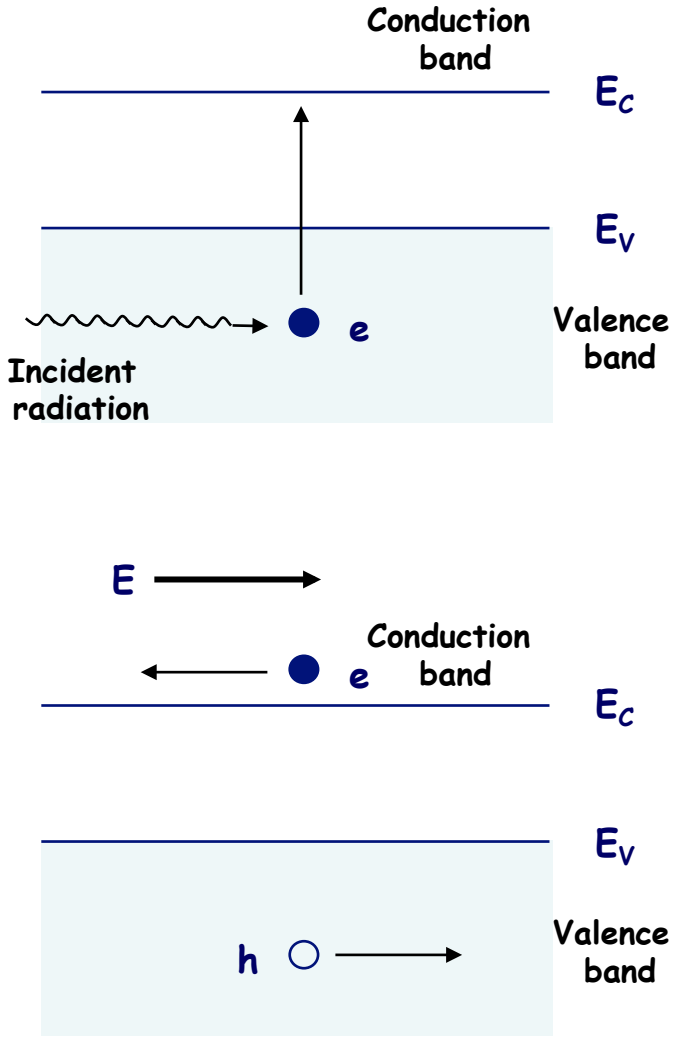
Displacement effect in a bidimensional crystal

Basic effects of radiation damage

- Effects of radiation in semiconductor devices can be included in one of two broad classes
- **Total dose (TD) effects**: are due to the progressive build-up of trapped charge in insulating layers or at the Si/SiO_2 interface (as a consequence of ionization phenomena) or of defects in the bulk of the devices (originating from accumulation of displacement events)
- **Single event effects (SEE)**: are due to charge deposition induced by a single particle that crosses a sensitive device region; the effects may lead to destructive or non-destructive damage of the device
  - SEEs occur stochastically, while TD is cumulative and may become visible after the device has been exposed to radiation for some time
  - TD is usually related to long term response of devices, whereas SEE is concerned with short time response
  - Only a tiny part of the device is affected by SEE, corresponding to the position of the particle strike, while TD uniformly affects the whole device, because it results from the effect of several particles randomly hitting the device
  - As far as SEE is concerned, the most important figure is the rate of occurrence; TD is characterized by the maximum drift of the main device parameters

Ionization damage effects

- As a consequence of the interaction with a charged particle or with a photon, electrons may get into an excited state, i.e. may go from the valence band to the conduction band through the band-gap leaving behind a hole
- In general, a single charged particle or photon (for example from a ^{60}Co γ source) has enough energy to ionize many atoms along its track, therefore releasing electron-hole pairs with a certain linear density (3.6 eV/e-h are needed in Si, 17 eV/e-h in SiO_2)
- The free electrons and holes may diffuse or drift (under the effect of an electric field) away from the generation point
- After generation, carriers can
  1. recombine
  2. get trapped in defects
  3. be collected at a device electrode



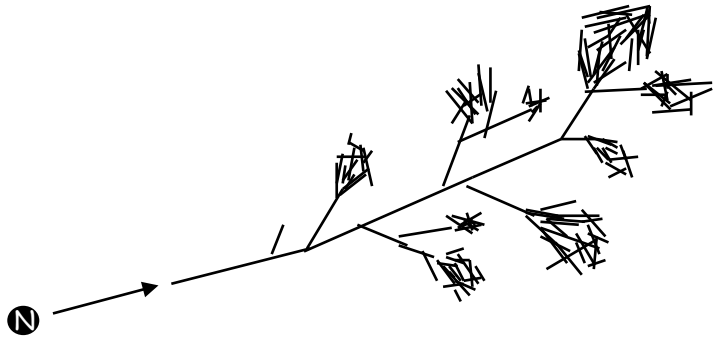
Ionization damage effects

- Ionizing events may produce transient or permanent effects
- **Transient (or single event) effects**: if an electric field is present in the region where the interaction takes place and carriers are released, electrons and holes are separated and recombination is negligible; for instance, in a PN junction region, radiation interaction with silicon is responsible for current (or photocurrent) generation
- **Permanent (or total dose) effects**: in isolating layers the number of generated carriers and their mobility are smaller than in (intrinsic or doped) silicon; therefore no photocurrent can be observed; on the other hand, insulators (such as SiO_2) and the interface between two layers of different materials (e.g. Si and SiO_2) may feature a relatively high density of traps, where carriers (holes in particular) can get stuck; as a consequence of several subsequent ionizing events, trapped charge density increases together with the generated, parasitic field, which in turn may be responsible for a shift in the characteristic of the irradiated electronic devices

Dislocation damage effects

- An impinging particle (e.g., a neutron) may interact with an atom and transfer to it enough energy to dislodge it from its position in the lattice (the minimum energy needed to dislodge a silicon atom is about 20 eV)

- The dislodged atom may travel a certain distance, possibly dislodging other atoms (a 1 MeV neutron may transfer 60/70 keV to a lattice atom, which in turn may produce cluster defects by dislodging hundreds of atoms in regions a few hundred of nm in size)

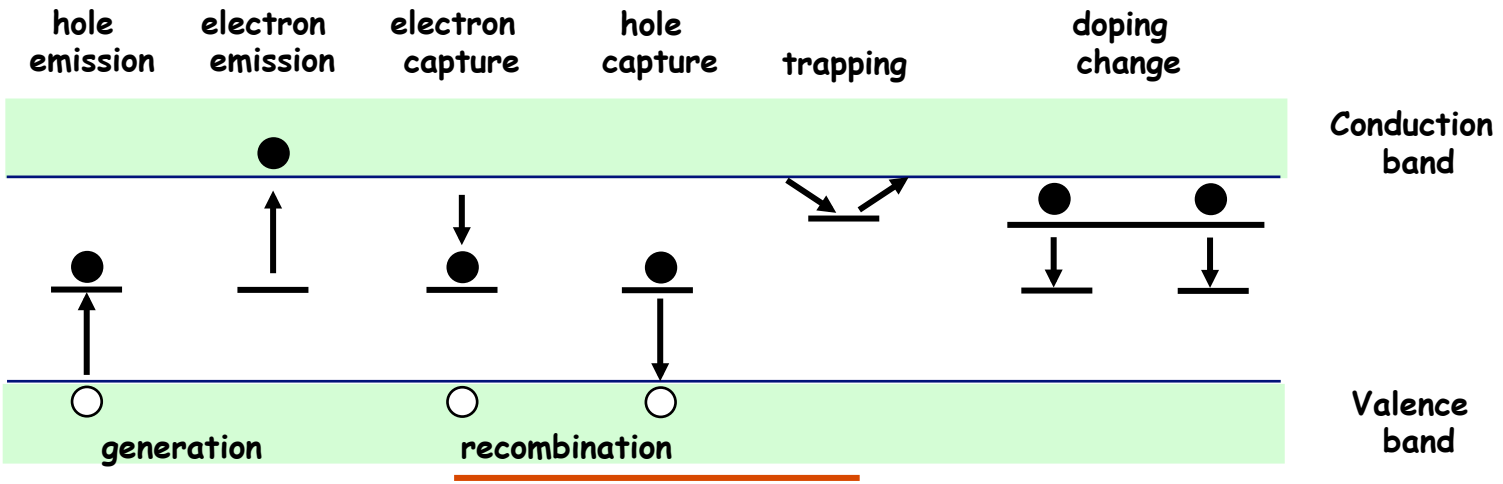


Cluster defects in silicon lattice due to an impinging neutron

- The created defects alter the crystal periodicity and are responsible for the formation of energy levels inside the band-gap; these energy levels alter the electrical properties of the material and of the electronic devices (e.g., minority carrier lifetime, carrier concentration, mobility)

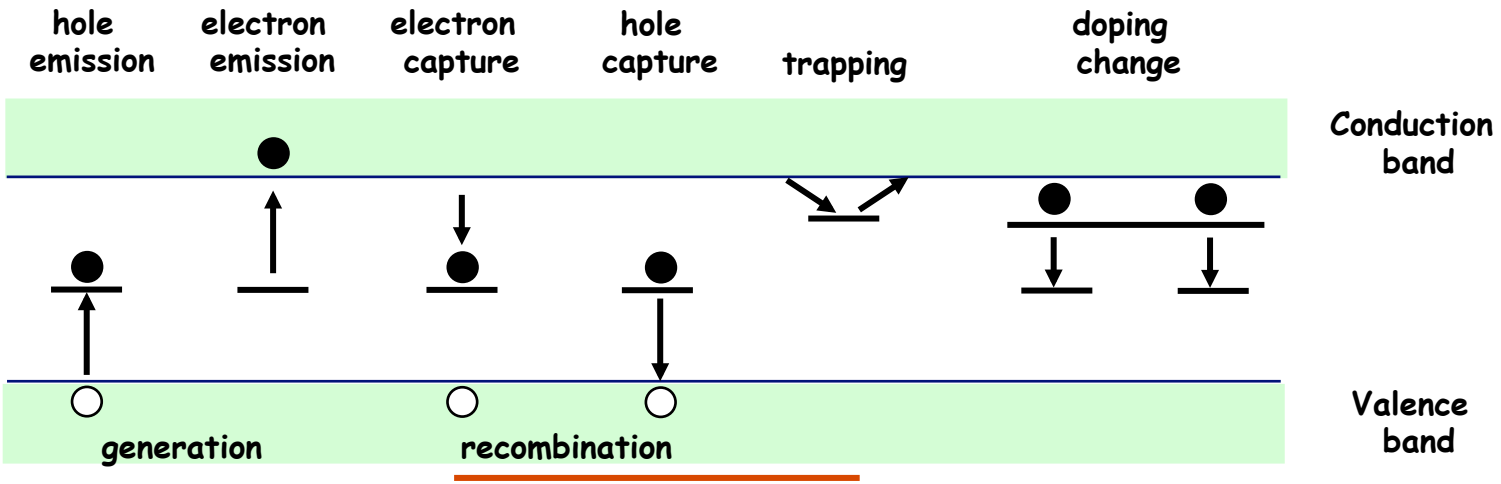
Dislocation damage effects

- Displacement damage manifests itself in several ways
- **Formation of mid-gap states** facilitates the transition of electrons and holes between bands; since transition probabilities are exponential functions of the energy difference, processes involving transitions between both bands require mid-gap states to proceed at an appreciable rate; whether recombination (electron and hole capture) or generation (electron and hole emission) dominates depends on the relative concentration of carriers and empty defect states; generation prevails in depletion regions, where the conduction band is underpopulated, increasing the reverse current in PN junctions; recombination prevails in forward biased junctions, where carriers flood the conduction band, resulting in charge loss and current decrease



Dislocation damage effects

- Displacement damage manifests itself in several ways
- **States close to the band edges** facilitate trapping, where charge is captured and released after a certain time
- **Mid-gap states** may capture electrons and holes from doping atoms (majority carriers), therefore changing the doping characteristics of the crystal
- **Defect states in the band-gap** may act as scattering centers for charge carriers and reduce their mobility; they can also facilitate defect-assisted tunneling of carriers through potential barriers, which is responsible, for instance, for the increase of the reverse current in PN junctions and of the leakage current in thin oxides



Single event effects

Single event (transient) effects

- Single event effects are due to a single particle crossing the sensitive area of a device or circuit; some of these events are classified as soft, since they do not induce any physical damage, but only loss of information, such as a bit flip in a memory array; other events, such as the gate oxide rupture following the strike of a heavy ion, are termed hard, because they do induce permanent damage
- The main classes of soft effects are:
  - single event upset (SEU), the corruption of a single bit in a memory array
  - multiple bit upset (MBU), the corruption of multiple bits due to a single particle
  - single event transient (SET), a transient signal induced by an ionizing particle in a combinatorial or analog part of a circuit
- The main classes of hard effects are:
  - single event gate rupture (SEGR), rupture of gate oxide occurring especially in power MOSFETs
  - single event burnout (SEB), burnout of a power device
  - single event latch-up (SEL), the activation of parasitic bipolar structures, leading to a sudden increase of the supply current

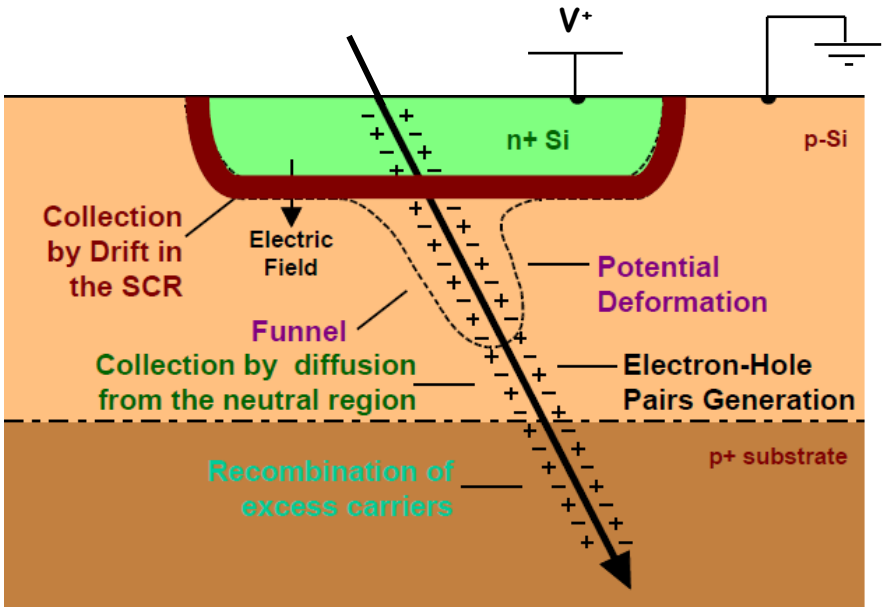
Single event (transient) effects

- SEEs are generally characterized in terms of their cross section, expressed as

$$\sigma_{SEE} = \frac{\text{number of events}}{\text{particle fluence}}$$

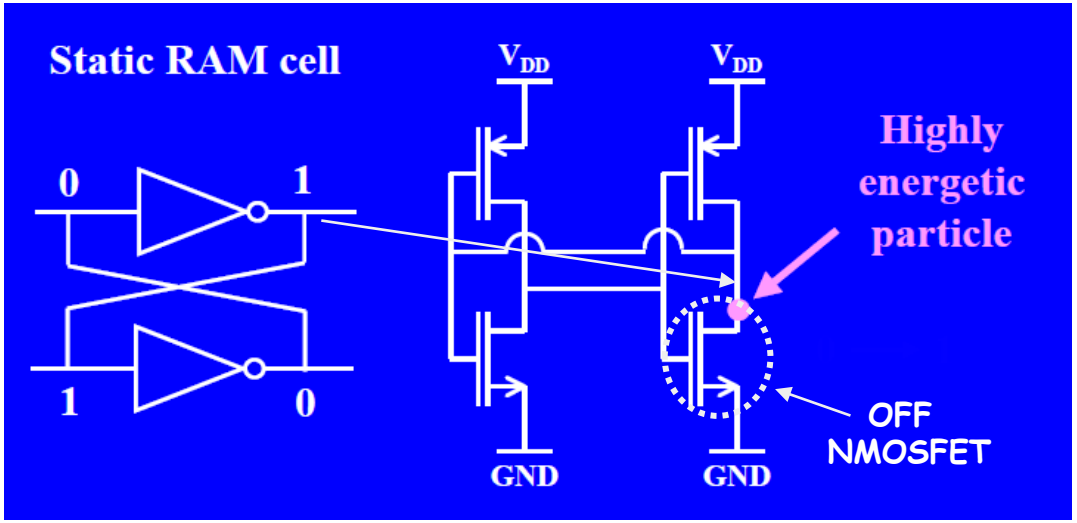
- Cross section varies as a function of the impinging particle LET (linear energy transfer, giving a measure of the energy deposited by the particle); a particle produces an observable effect if its LET is larger than the threshold LET

- The charge released by the impinging particle in an SEE event is collected through the so-called funneling mechanism; most of the charge is sucked in at the struck junction through a deformation of the junction potential, while the remaining charge diffuses in the substrate and may be collected or not at the same junction



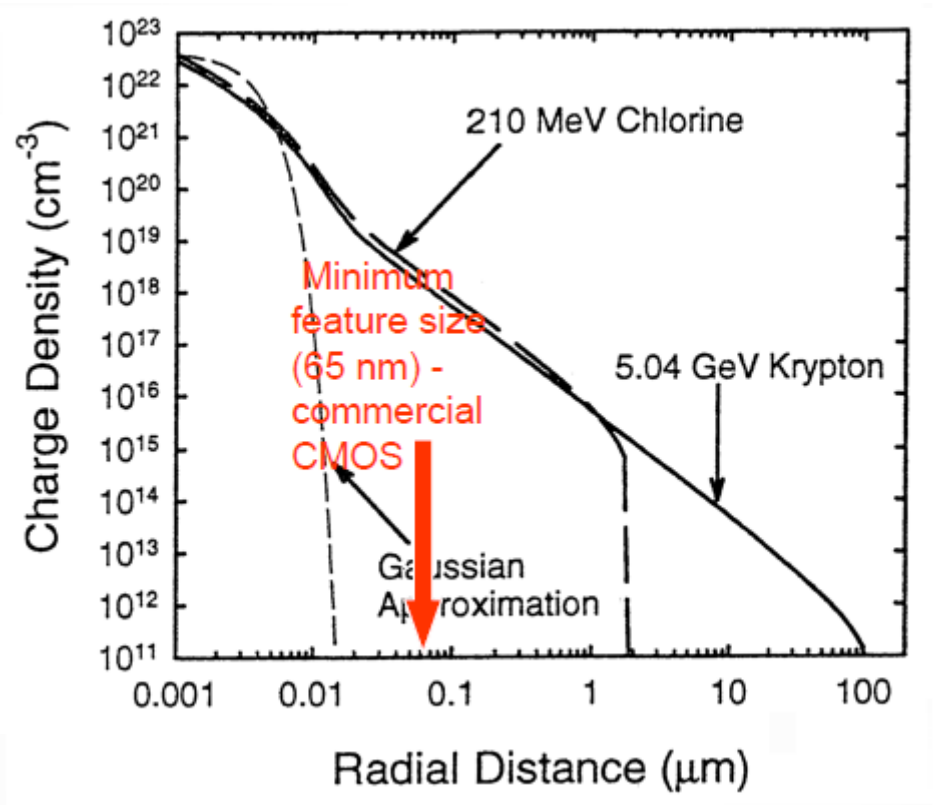
Single event upset (SEU)

- To cause disturbance in a circuit, the charge generated by a particle (a heavy ion) strike must be collected by a sensitive node; reverse biased pn junctions (semiconductor junctions with the p side at a lower potential than the n side) are the most likely candidate to collect charge, since they feature a large depletion region and a strong electric field
- In the case of a static RAM cell, the particle may strike the drain electrode of the off NMOSFET; the released charge is collected at the reverse-biased drain pn junction; the voltage at the struck node tends to decrease, turning the radiation-induced current into a voltage transient; the current decreases the potential at the drain node, possibly below the cell switching voltage, therefore changing the initial state
- Single event upset depends on the LET of the impinging particle, on the incidence angle **θ** (effective LET=LET/cosθ) and on the charge collection capability of the hit junction



Multiple bit upset (MBU)

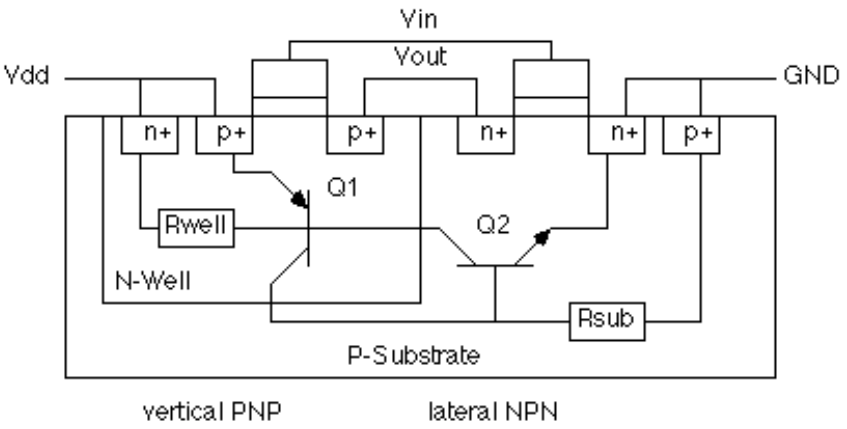
- Single event effects have become more complex to study as the feature size of CMOS processes (the minimum length that can be obtained by the lithography), has been scaled down to the submicron realm
- Indeed the size of the ion track has become comparable to the feature size of modern chips (see figure); therefore, phenomena that were confined to a single circuit node can now involve multiple nodes and charge sharing can occur
- The rate of occurrence of MBU phenomena is bound to rise as fabrication processes evolve



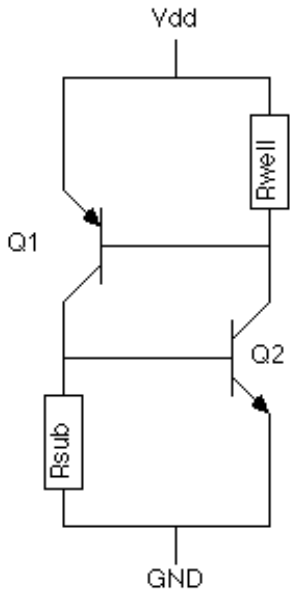
Charge density as a function of the distance from the center of the track for different ions

Radiation-induced latch-up

- Built in a CMOS structure there are two parasitic bipolar transistors, an NPN and a PNP; they are cross-connected in such a way that the base-collector junctions are common, therefore forming an SCR (semiconductor-controlled rectifier)

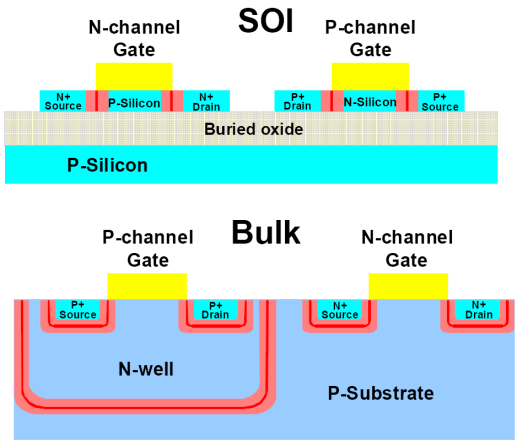


- During normal operation, the SCR is off; a radiation-induced voltage transient at one of the device terminal may initiate latch-up by triggering the SCR and its regenerative feedback; as a consequence, if a protection mechanism has not been implemented, the involved devices (and the circuit using them) may end up malfunctioning or even being destroyed due to overcurrent

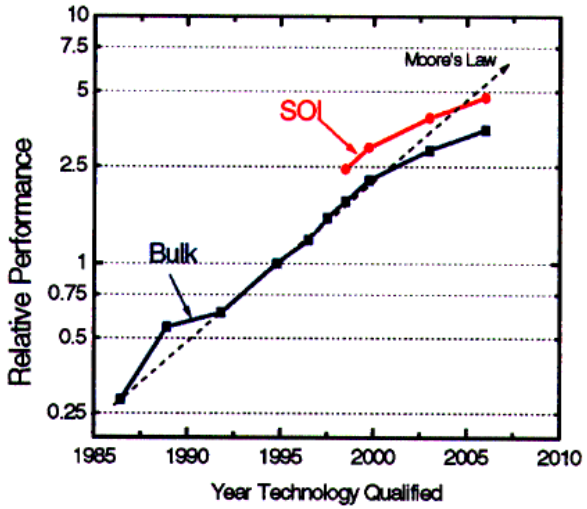


Fully depleted SOI MOSFETs

- One of the limitations to processing speed in bulk CMOS transistors is given by the parasitic capacitance at the source/channel and drain/channel junctions
- This problem is overcome in the so-called SOI (silicon on insulator) CMOS technologies
  - In an SOI MOSFET, the device is fabricated in an ultra-thin (of the order of a few tens of nanometers) silicon layer on top of a thicker (several hundreds of nanometers) oxide layer (so-called buried oxide, or BOX)
  - In fully depleted (FD) SOI MOSFETs, the source and drain regions reach down to the buried oxide layer, reducing the parasitic capacitance, while the device region between source and drain, in normal operation, is fully depleted



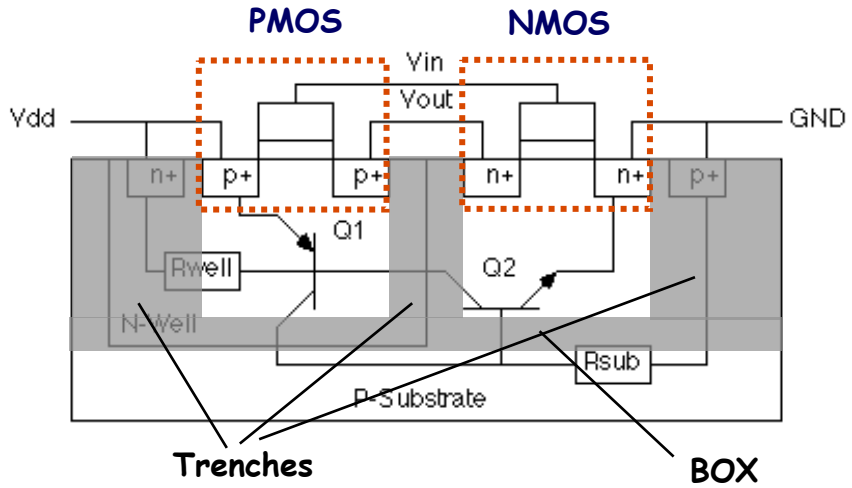
- SOI technologies may provide high integration density, high speed and low power dissipation, and are widely used, for instance, in the design of microprocessor; their performance easily exceeds that of bulk CMOS



Relative performance of Bulk and SOI CMOS as a function of time (performance=1 for bulk CMOS process qualified in 1995)

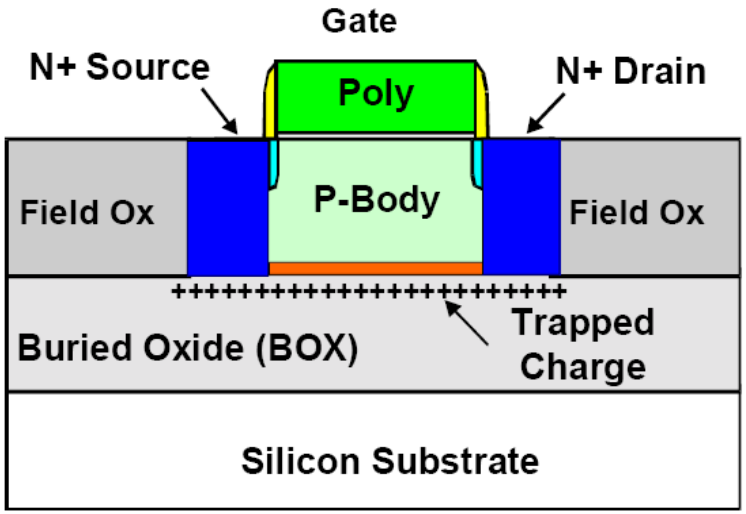
Radiation tolerance of FD SOI MOSFETs

- SOI technologies are inherently immune from latch-up effects (whether radiation-induced or not); P and N MOS parts in a SOI CMOS process are electrically isolated from each other by means of oxide trenches; therefore, no SCR, with its regenerative configuration, can be triggered by possible radiation-induced photocurrents
- SOI processes have in general the capability of reducing transient radiation-induced photocurrents and charge collection from the passage of a single ionizing particle



Radiation tolerance of FD SOI MOSFETs

- On the other hand, fully depleted SOI MOSFETs are more sensitive to total ionizing dose effects with respect to bulk CMOS transistors due to the presence of the buried oxide layer, where positive charge build-up can take place; accumulation of holes in the buried oxide may lead to
  - formation of a back-channel leakage path (a conductive path just in the silicon layer at the interface with the buried oxide); it depends on the quality of the back silicon/BOX interface and on the initial threshold voltage of the parasitic transistor between source and drain
  - threshold voltage shift due to electrical coupling between the front (actual) gate terminal and the back (parasitic) gate terminal (recall that the device silicon layer is extremely thin)

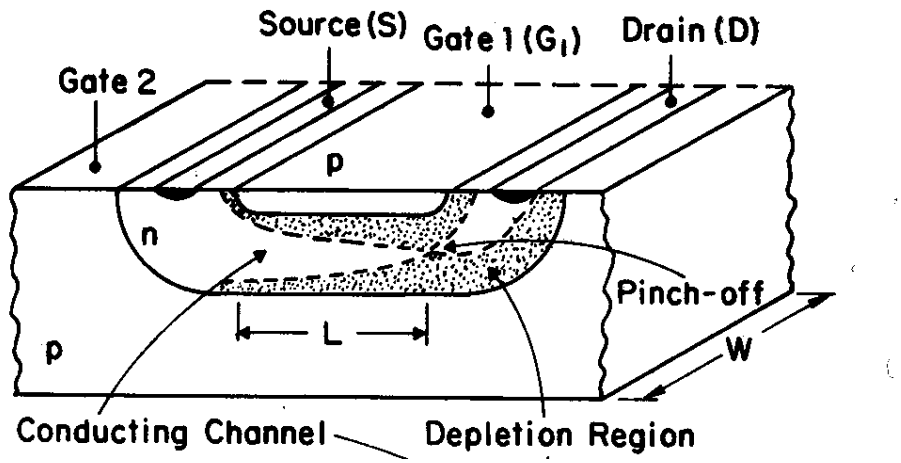


Radiation effects in JFETs

The junction field-effect transistor has been for a long time the device of choice for rad-hard applications, in particular in high energy physics applications

Operation of the JFET transistor

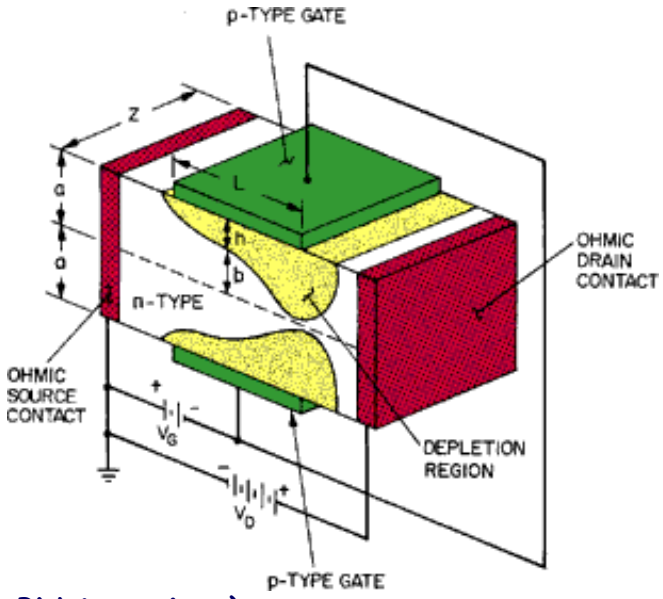
- Operation of the junction field-effect transistor (JFET) is based on the transport of majority carriers (electrons in N-JFET and holes in the P-JFET) in the silicon bulk of the device; in the case of an N-type JFET
  - heavily doped N-type source and drain regions are fabricated at the two ends of the device channel, an N-type pocket featuring a much lower doping concentration
  - a (usually) shallow implanted P-well is used as the top gate terminal while the device substrate can act as the bottom gate terminal
  - when a reverse bias is applied at the (top and/or bottom) gate/channel junction, a depleted region is created; if a potential difference is applied between source and drain, by modulating the width of the depletion region, it is possible to control the channel section and, as a consequence the current flowing between the drain and the source



- As in the case of the MOSFET, the minimum value of the channel length L which can be achieved in a given technology is used to provide a measure of the lithographic limits of the fabrication process

Radiation effects in JFET transistors

- Since in JFET operation is based on the transport of carriers in the device bulk, junction FETs are much less insensitive to ionizing radiation than MOSFETs (no gate oxide nor channel at a Si/SiO_2)
- Moreover, since the current flowing between the source and the drain is made of majority carriers, JFETs are also quite insensitive to degradation of the average lifetime of minority carriers; therefore JFETs can tolerate quite high neutron fluences, since the channel doping concentration is generally quite high (in the order of 10^{16} cm^{-3})

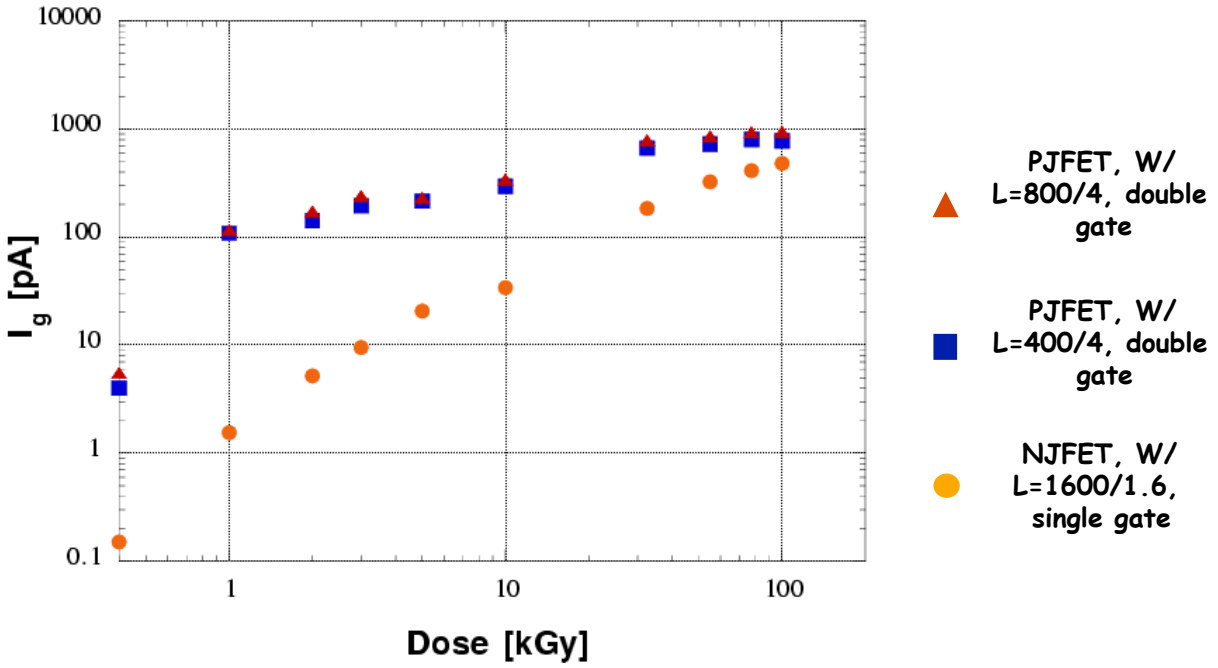


- On the other hand, dislocation damage can produce
  - a sizeable increase in the gate leakage current (reverse current of a PN junction) due to increase in the carrier generation rate in the gate/channel depletion region
  - a considerable increase in the power spectral density of the noise due to the generation of lattice defect in the device bulk; they become active as generation/recombination centers when they are located in the depletion region and close to the channel; therefore their activity depends on the bias condition of the device (in particular on V_{GS})
- Depending on the device layout, also field oxide ionization may be responsible for some gate current increase

Effects of ^{60}Co γ-rays on the gate current

- Exposure of junction FETs to γ-rays was proven to produce a significant increase in the device gate current
- As a general consideration, the detected increase in the gate current can result form one (or both) of the following effects
  - atomic dislocation in the junction depletion region, where the resulting energy levels act as generation centers (recall that γ-rays from cobalt 60 may dislodge atoms from their location in the lattice through secondary Compton electrons)
  - doping type inversion beneath the field oxide between source and drain due to positive charge trapping

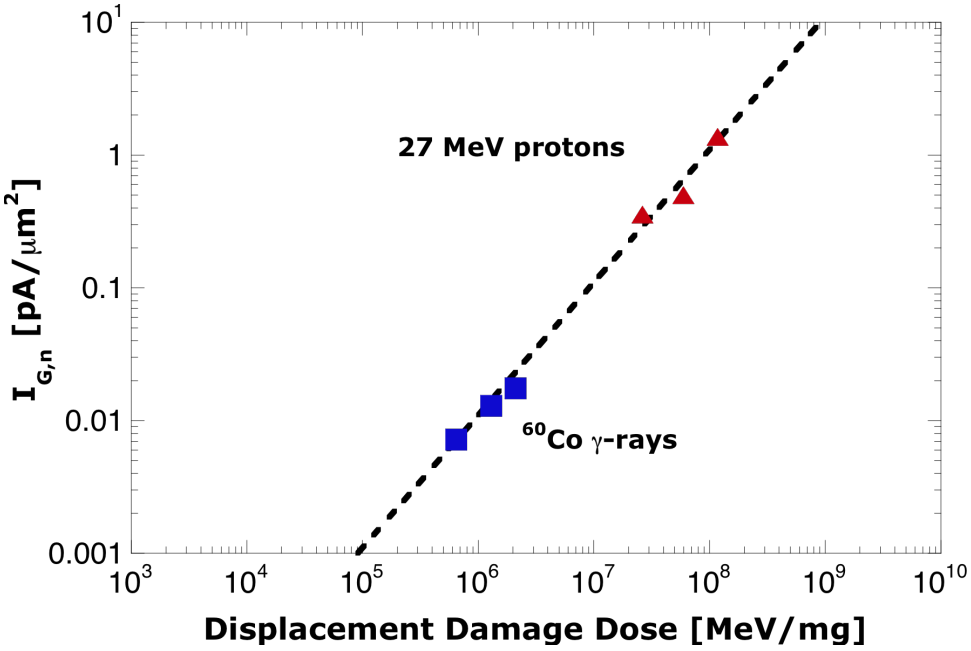
Gate current as a function of the absorbed γ-ray dose in three junction FET with different channel length and width and different gate configuration



γ-rays and proton effects on the gate current

- In most cases, ^{60}Co γ-rays just produces pure dislocation damage effect; this can be shown by taking a device parameter (the gate current) as the figure of merit of the technology with respect to the investigated radiation damage (displacement) and comparing the effects on that parameter of γ-rays and of another type of radiation (e.g., protons)
  - in order to compare the displacement damage effect (expressed in terms of variation of the normalized gate current) due to protons and γ-rays, the NIEL (non ionizing energy loss) of each particle has to be known
  - displacement damage dose can be calculated based on the particle fluence
  - change in the gate current is found to be proportional to the displacement dose and independent of the particle type, thereby demonstrating that displacement damage predominates over ionization in γ-irradiated JFETs

Normalized gate current (gate current divided by the junction area) as a function of the displacement damage dose for proton and γ-irradiated NJFETs



Lorentzian noise in the drain current

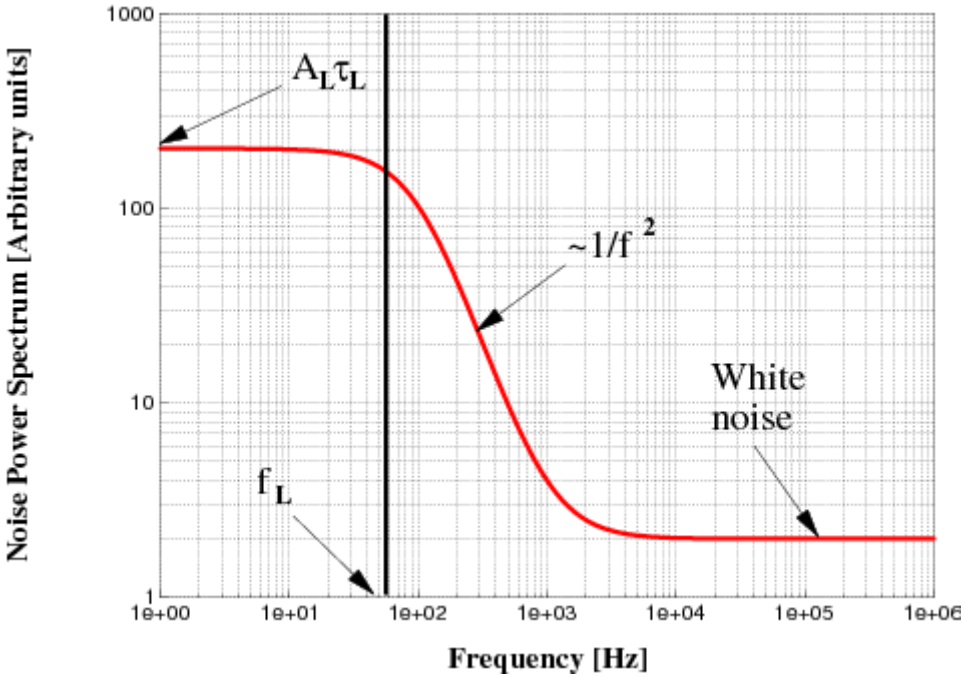
- Lorentzian noise is generally detected in JFETs, where it is caused by trapping and detrapping of carriers by localized traps in the gate/channel depletion region
- Generally, above 1 Hz at room temperature, the noise in the drain current features one or two Lorentzian components $S_{L,i}(\omega)$ with the following frequency dependence

$$S_{L,i}(\omega) = \frac{A_{L,i}\tau_{L,i}g_m^2}{\left(1+\tau^2\omega_{L,i}^2\right)}$$

- $A_{L,i}$ =power coefficient of the Lorentzian term
- $\tau_{L,i}$ =characteristic time of the Lorentzian term ($\tau_{L,i}=1/(2\pi f_{L,i})$, with $f_{L,I}$ characteristic Lorentzian frequency)

- The amplitude of the Lorentzian components in the noise spectrum tends to increase in devices exposed to high radiation doses or high neutron fluences, which are responsible for atomic dislocation in the lattice and for the creation of defects acting as trapping centers

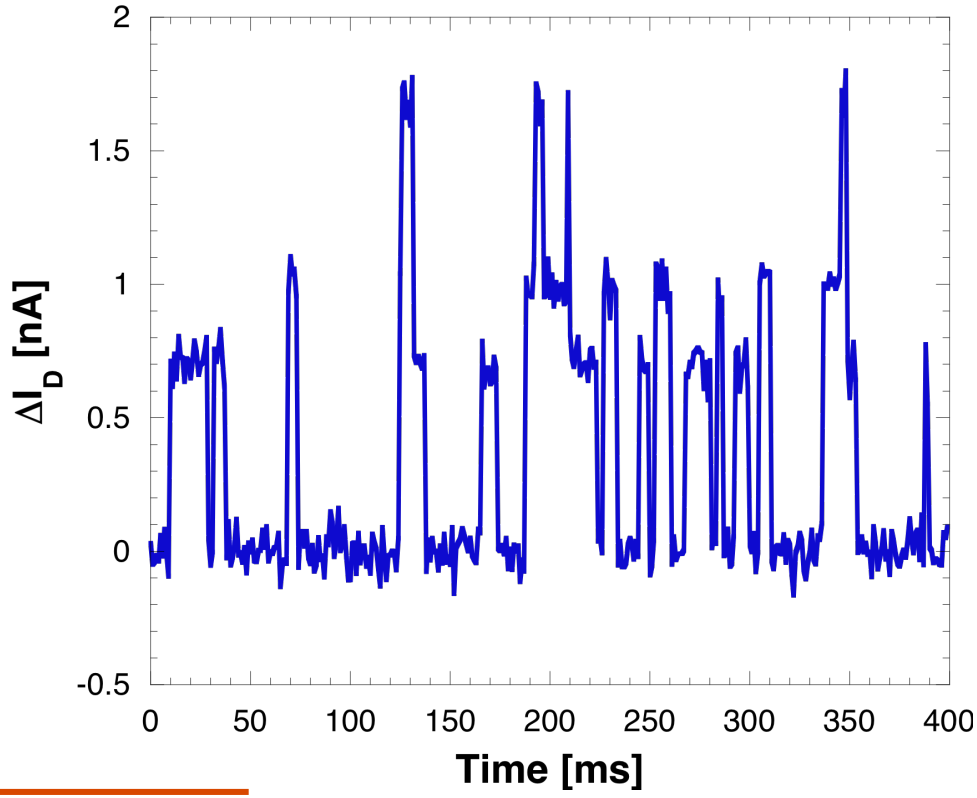
Power spectral density of a Lorentzian component



Random telegraph signal waveforms in JFETs

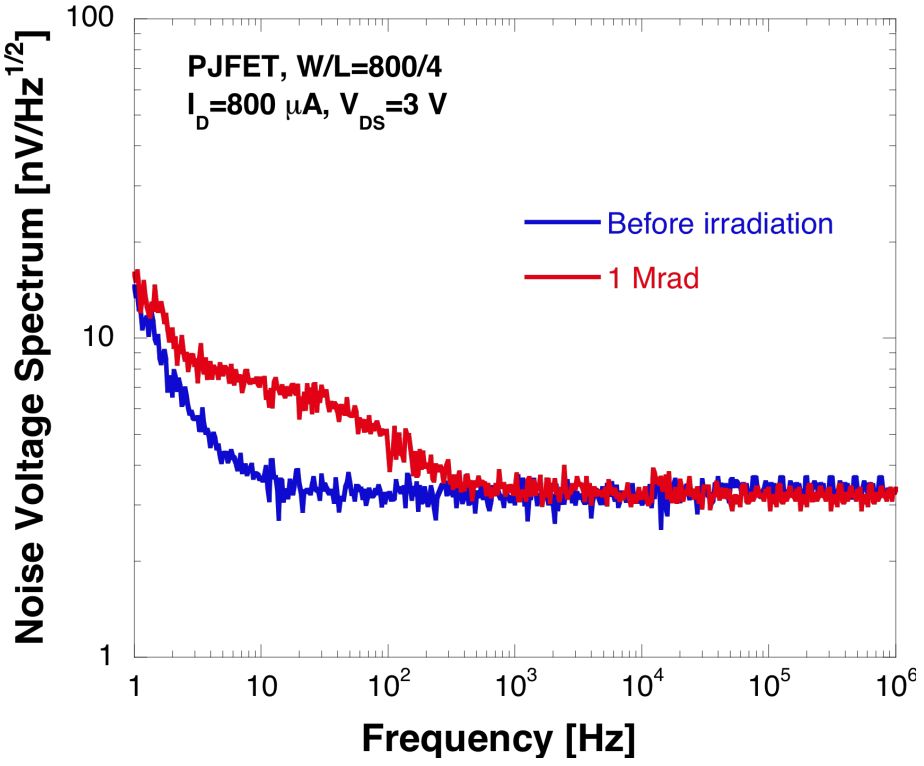
- Random telegraph signal (RTS) noise, also called burst noise, trapping noise or generation-recombination noise has been proved to result from the random capture and release of carriers at one or more localized electrical traps
- In an RTS signal, the current switches between two or more average levels in correspondence to every change of the occupation state of the traps
- RTS noise has been found in forward and reverse biased diodes, BJTs, in the drain current of JFETs and MOSFETs; a Lorentzian noise power spectral density is associated to RTS noise

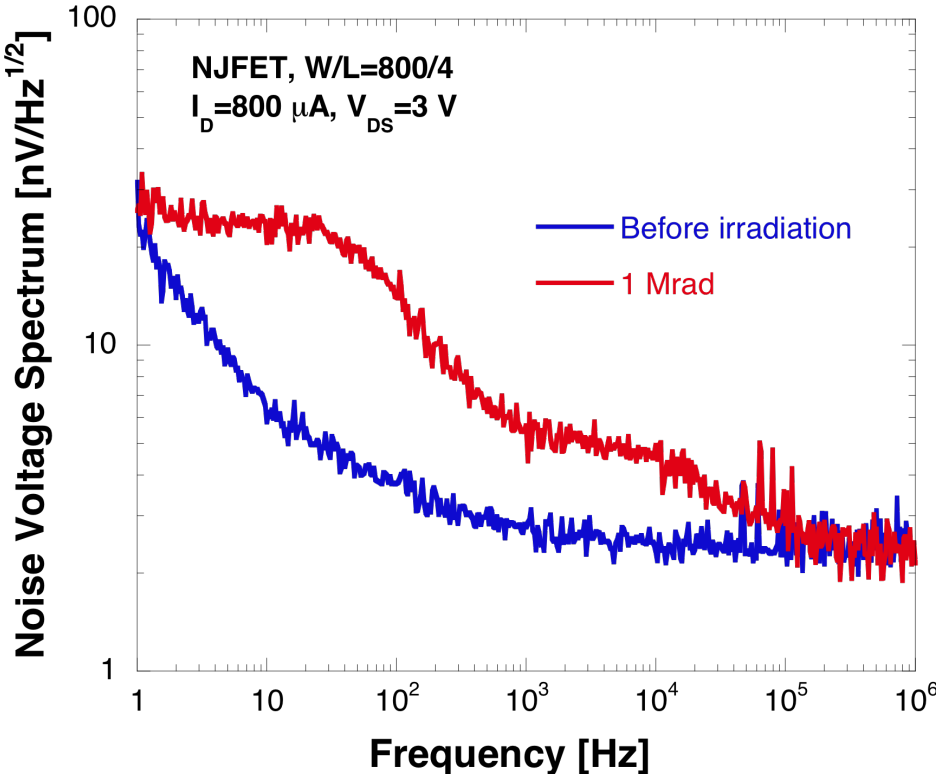
Two level random telegraph signal waveform; also white noise (faster and smaller variations in the signal) is superimposed to the signal



Lorentzian noise in the drain current

- 60Co γ-rays produce different effects in the noise spectrum of P and N-channel JFETs
  - In PJEFTs, a single Lorentzian component appears, with characteristic frequency around 100 Hz
  - In NJEFTs, two Lorentzian contributions appear, with characteristic frequencies at about 100 Hz and 10 kHz

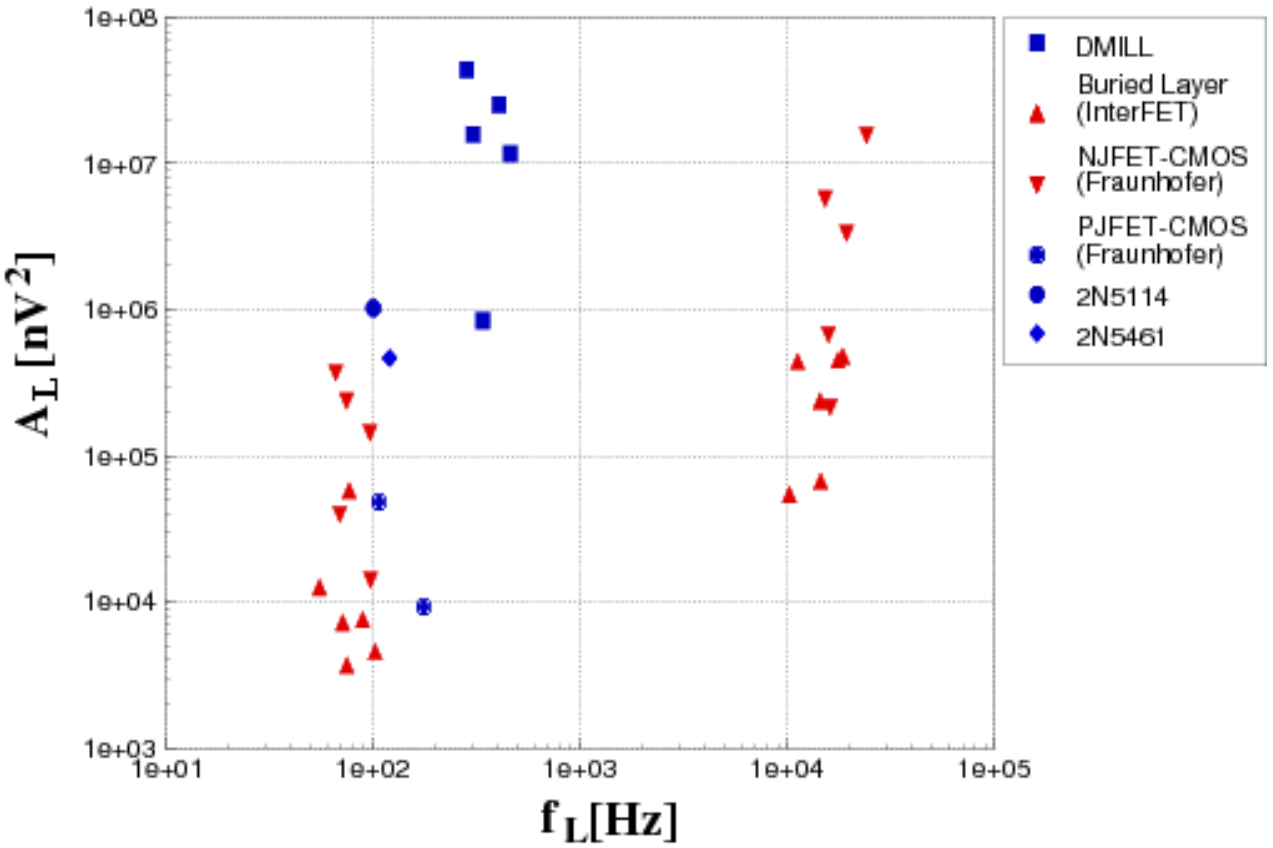




Lorentzian noise in the drain current

- The difference in the radiation response of P and N-channel JFETs was found to be to a good extent technology independent; similar behavior was detected in several device from different fabrication processes and foundries

- The behavior of the characteristic frequencies of the Lorentzian components as a function of the temperature can be used to extract information about the energy levels of the involved traps

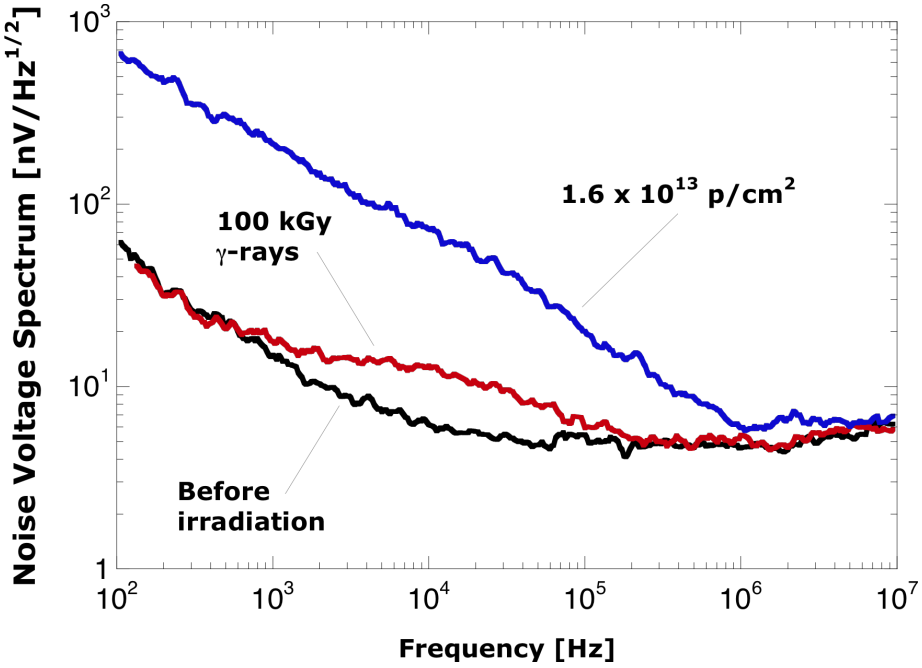


Characteristic frequencies of the Lorentzian components appearing in irradiated P and N-channel JFET devices

γ-rays and proton effects on noise

- Irradiation with γ-rays leads to the appearance of a Lorentzian noise component, whose characteristic frequency is found to be independent of the fabrication technology but to some extent related to the device polarity; in devices exposed to protons, noise increase at low frequency has definitely a 1/f shape

- While secondary Compton electrons on the average may dislodge a single atom at a time, creating point defects, more massive particles, like protons, may produce, directly or through secondary dislodged atoms, cluster defects; the latter results in a continuous distribution of energy levels inside the band-gap, whereas γ-ray induced defects concentrate around definite levels in the silicon forbidden gap



Gate referred noise voltage spectrum in NJFETs with W/L=1000/4, before irradiation and after exposure to ^{60}Co γ-rays and 27 MeV protons

Experimental tools for radiation environment simulation

Several facilities have been built around the world for simulating different radiation environments and testing radiation hardness of devices and circuits in view of specific applications

Radiation testing

- Sensitivity of devices and circuits to radiation is often very variable and virtually unpredictable simply on theoretical grounds; actual irradiation tests must therefore be performed on the electronic parts of a system; for this purpose, irradiation facilities have been built around the world, making a variety of radiation sources available, and test procedures have been devised to provide reference standards for radiation hardness assurance of electronic components
- The selection of the irradiation tool depends on the kind of damage expected for the device under test in the actual application; tools for damage testing can be subdivided in three categories
  - Tools for **total ionizing dose (TID) testing**: for this kind of characterization, device parameters need to be tested at different dose levels; cobalt 60 is widely used to simulate ionizing environments; also proton accelerators can be employed, although protons generate also displacement damage
  - Tools for **displacement damage (DD) testing**: in this case device parameters need to be measured at different particle fluences corresponding to different displacement doses; neutron sources are the best ones for producing displacement damage; also particle (electron, proton, heavy ion) accelerators are used, although charged particle also produce ionizing damage
  - Tools for **single event effect (SEE) testing**: require on line testing of the different device or circuit parameters and functionalities; proton or heavy ion accelerators can be used

Tools for total ionizing dose testing

- TID testing is routinely performed using radioactive sources, such as cobalt 60 (^{60}Co) and cesium 137 (^{137}Cs)
  - Cobalt 60 is the most used among radioactive sources; it is an artificial isotope produced commercially by means of accelerators or as a byproduct of nuclear reaction operation, when ^{59}Co is exposed to neutron fluxes; it emits two gamma photons at 1.173 MeV and 1.333 MeV; with a half-life period of 5.27 years, facilities need to perform regular dosimetry to take decay into account (a dosimeter should be placed on each test board to know accurately the final delivered dose)
  - Cesium 137 is a byproduct of nuclear fission processes in nuclear reactors, with a half life of 30 years; it emits two beta-rays at 0.51 and 1.17 MeV and a gamma at 0.662 MeV
- Due to their wide distribution and relatively low cost, also X-ray generating machines are used for ionizing dose testing; in particular, use of low energy (10 keV) X-ray testers has become widely accepted where total dose values in the tens of Mrad (hundreds of kGy) range are required (military and high energy physics applications)
  - X-rays are generated when an electron beam bombards a target, usually of a high-Z metal such as tungsten or copper; the electron beam, colliding with the target, excites a white spectrum of bremsstrahlung X-rays (actually peaked broadly at about half the beam energy) upon which the K and L peak emissions of the target metal are superimposed (for W, K-peak at 59.3 keV and L-peak at 8.396 keV, for Cu K-peak at 8.04 keV)

Tools for displacement damage and SEE testing

- Neutron sources provide the best tool for displacement damage simulation; different kind of facilities are available
  - White spectra beam: these facilities are used to simulate real terrestrial neutron environment; since the required energy spectrum is quite large, high energy accelerators are needed, available only in a few facilities around the world (Los Alamos National Laboratories in the USA, TRIUMF in Canada and ISIS in UK)
  - Quasi monoenergetic lines: in such facilities, a collimated neutron beam can be produced using a proton beam to irradiate a lithium target; the CYCLONE facility in Belgium can produce quasi monoenergetic neutron beams in a wide energy range (a few tens to several tens of MeV); at Svedberg Laboratory (Uppsala, Sweden), a large range of quasi monoenergetic neutron beams is available between 20 and 180 MeV
  - High flux lines: such facilities were developed to match typical fluences of high energy physics experiments (the LHC at CERN) and of the fusion domain, in the order of 10^{14}-10^{15} n/cm^2; for example, at the CYCLONE facility, a 50 MeV deuteron beam is used to bombard a ^{9}Be target, resulting in a maximum neutron flux of 6.6×10^{12} n s^{-1}sr^{-1})
  - Nuclear reactors: can be used for exposure of samples to fast neutrons and may provide very high peak pulse fluxes, in the order of 10^{17}-10^{18} n cm^{-2}s^{-1}
- Quasi monoenergetic lines and high flux lines can also be used for SEE testing

Tools for displacement damage and SEE testing

- Cyclotrons are most often used for proton and heavy ion testing; in cyclotrons, particles are immersed in a uniform magnetic field and subjected to a radiofrequency accelerating field; a number of modifications (leading, for instance, to the so called synchrocyclotron) have been made to the original cyclotron design to overcome the relativistic limitations to the maximum achievable energy for the accelerated particle
  - Proton and heavy ion accelerators are made available by several facilities around the world (UCL in Louvain, Belgium, JYFL in Jyväskylä, Finland, the Paul Scherrer Institute in Switzerland, the Lawrence Berkeley Laboratory in the US); maximum proton energy ranges from a few tens of MeV to 1 GeV
- Other accelerator types are DC machines; they consist of an isolated pipe connected at one end to the particle source and to the target at the other end; voltage is applied from end to end to produce the accelerating field; two DC accelerator types are available
  - In the Cockroft-Walton accelerator, the voltage is generated by a sequence of voltage-multiplying rectifier circuits
  - In the Van de Graaff accelerator, the voltage is created by transport and accumulation of electrical charges on the electrode containing the particle source

Tools for displacement damage and SEE testing

- Heavy ion facilities can be classified based on the energy range they cover; some examples of such facilities are Ganil in France, HIF in Belgium, RADEF in Finland, SIRAD in Italy (Legnaro); energies may vary from a few tens of MeV to several hundreds of MeV
- In general, heavy ion facilities can provide different ion species
  - High energy machines are actually quite complex; the tuning time is so large that changing from one species to another may take several hours and so only one ion type is available per day
  - Instead, one of the advantages of medium energy cyclotrons is the possibility to provide ion cocktails; in this case, by finely tuning either the magnetic filed or the RF frequency of the machine each ion species can be extracted separately and very fast ion changing can be obtained
- It is very important to remember that protons and neutrons can activate the samples and all the surrounding equipment; a cooling period is needed before users are allowed to bring their devices and circuits back to their laboratories for electrical testing

Standards and test methods

- The design of a valid radiation simulation test is not easy; it is important that guidelines for testing are agreed and made public, so that the tests can be validated by comparison
- Procedures for qualification and test of devices under irradiation have been developed in particular with reference to space and military applications; their objectives are:
  - to ensure that the long-lived degradation produced by radiation lies within an acceptable range
  - to produce data which will be of further aid to the electronic designer in estimating the degraded "end-of-life" characteristics of the part
  - to produce data showing whether a device is sensitive to single-event phenomena and produce a quantitative estimate for latch-up or soft error rates
- Such data enable the designers to introduce radiation-tolerance into their designs in two different ways
  - by accepting only the more tolerant devices
  - by accepting also sensitive devices and making the overall design robust enough to accommodate for strongly degraded device performance at "end-of-life"
- Specifications for radiation test procedures have been developed by the European Space Agency (ESA/SCC Basic Specification No. 22900, Issue 4, 1995) and by the US Department of Defence (MIL STD)