# CMOS pixel development for the ATLAS experiment at the HL-LHC

## XVI Incontri di Fisica della Alte Energie
## Trieste, 20 April 2017

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**Università di Milano and INFN**

***on behalf of the CMOS pixel working group within the ATLAS/ITk collaboration***

# Outline

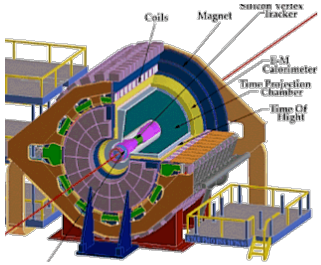
- Depleted-CMOS sensors
  - Motivations for HL-LHC
  - Detector features
- Experimental results on CMOS sensors
  - Covering large- and small- fill factor
  - Charge collection
  - Efficiency
  - Timing
  - Radiation hardness
- From sensors to detectors: the next R&D frontier
  - hybrid detectors
  - monolithic solutions

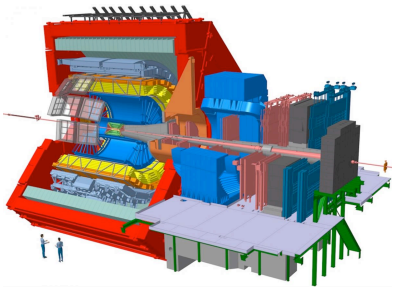
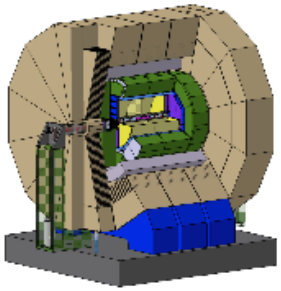
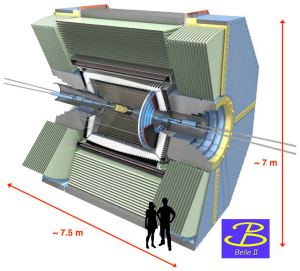
**A non exhaustive list of references to recent conference talks is provided at the end of the presentation**

# Pixel Detectors in HEP

Detector requirements depend strongly on the experimental environment:

- particularly demanding for general purpose LHC experiments



| | STAR | ALICE | ILC | BELLE II | ATLAS | ATLAS@HL-LHC |
|---|---|---|---|---|---|---|
| Beam type | pp/AA | pp/AA | $e^+e^-$ | $e^+e^-$ | pp | pp |
| Energy [TeV] | 0.2 A | 8 A | 0.25-0.5 | 0.01 | 14 | 14 |
| Time resolution [ns] | 200 000 | 20 000 | 350 | 20 000 | 25 | 25 |
| Particle rate [MHz/mm$^2$] | 0.1 | 0.01 | 0.25 | 0.1 | 1 | 10 |
| NIEL [1 MeV n/cm$^2$] | $10^{12}$ | $10^{13}$ | $10^{12}$ | $10^{13}$ | $10^{15}$ | $2\times10^{16}$ |
| Dose [MRad] | 0.3 | 0.7 | 0.4 | 10 | 80 | 1000 |

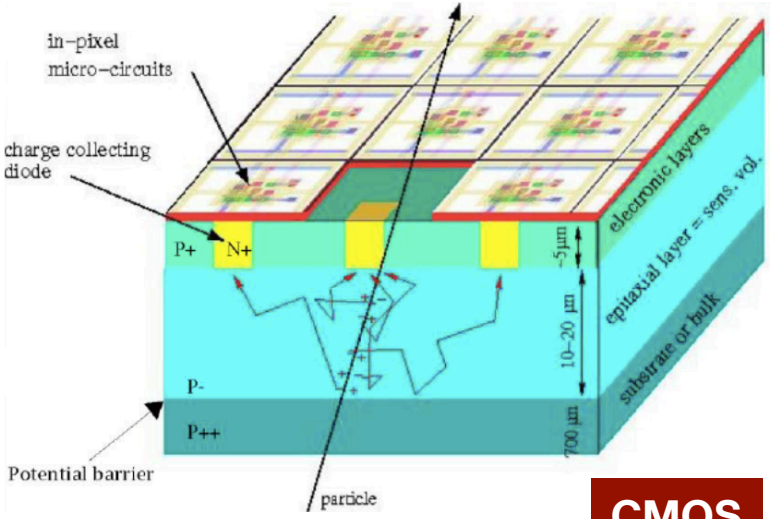
Fast

High data rate

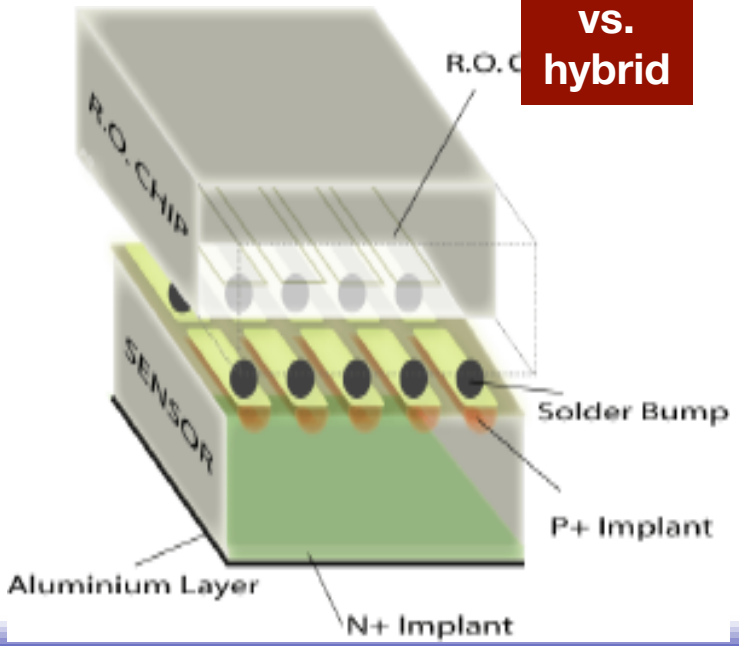
Rad-hard

# CMOS pixel detectors

- **CMOS detector:**
  - detector + front-end electronics + readout in a single device
  - commercial technology: large volume/low cost productions
  - low resistivity substrate (1-10 Ω · cm):
    - very small depletion region
  - **charge collection by diffusion**
    - charge carriers diffuse in the substrate
    - until either recombine or are collected by an electrode
    - long collection time / partial charge collection
  - **not suitable for high rate application**
  - **not radiation hard:** sensitive to reduction of trapping time




**CMOS vs. hybrid**

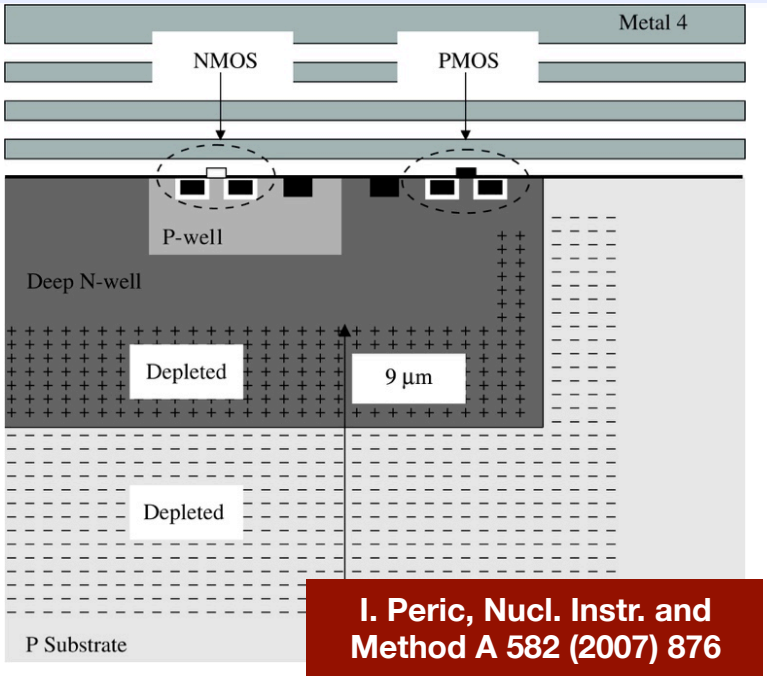


# Depleted CMOS detectors

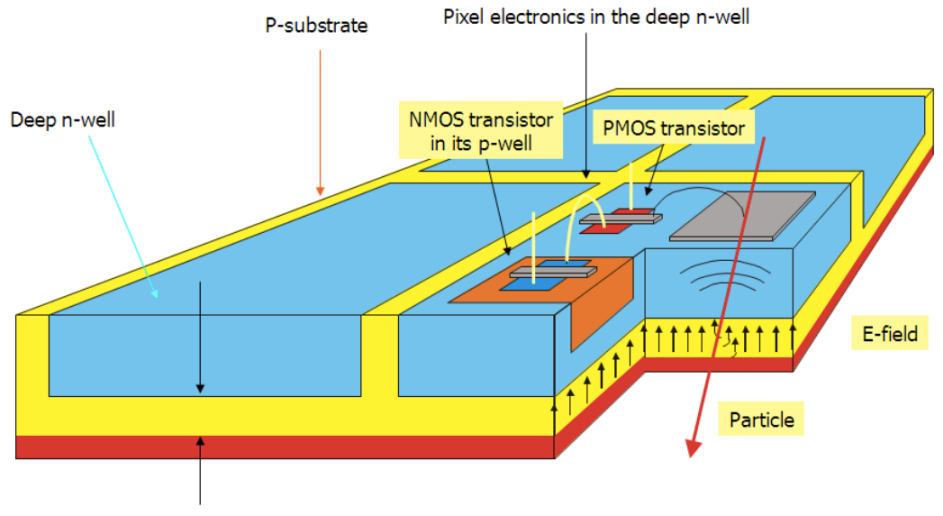
- Can one merge the two detection approaches?
  - CMOS detector with a **depleted layer**
  - *e-h* produced in the depleted layer are collected by drift:
    - full ionization signal (in the depleted region)
    - fast: no trapping
    - additional slow signal from holes and diffusion
- Enabling technologies:

$$d = \sqrt{\varepsilon_{Si}\varepsilon_0\mu_{carrier}\rho(V + V_{BI})}$$

  - **High Voltage** processes
    - Availability of processes with high voltage capability, driven by automotive and power management applications
  - **High Resistivity** substrates
    - Foundries accepting/qualifying wafers or epitaxial substrates with mid-high resistivity
  - **130-180 nm feature size**
    - deep submicron technologies needed for the design of radiation hard electronics
    - multiple-well process to decouple front-end electronics from the sensitive region

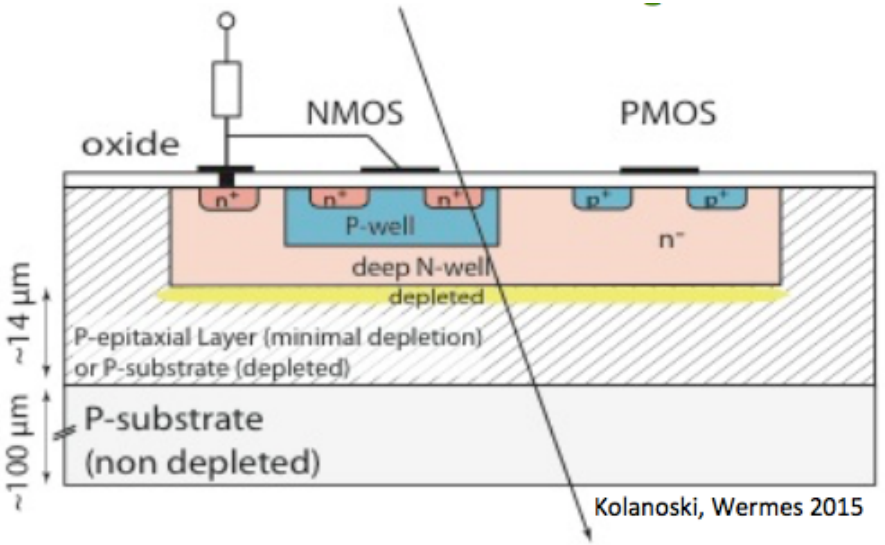



I. Peric, Nucl. Instr. and Method A 582 (2007) 876

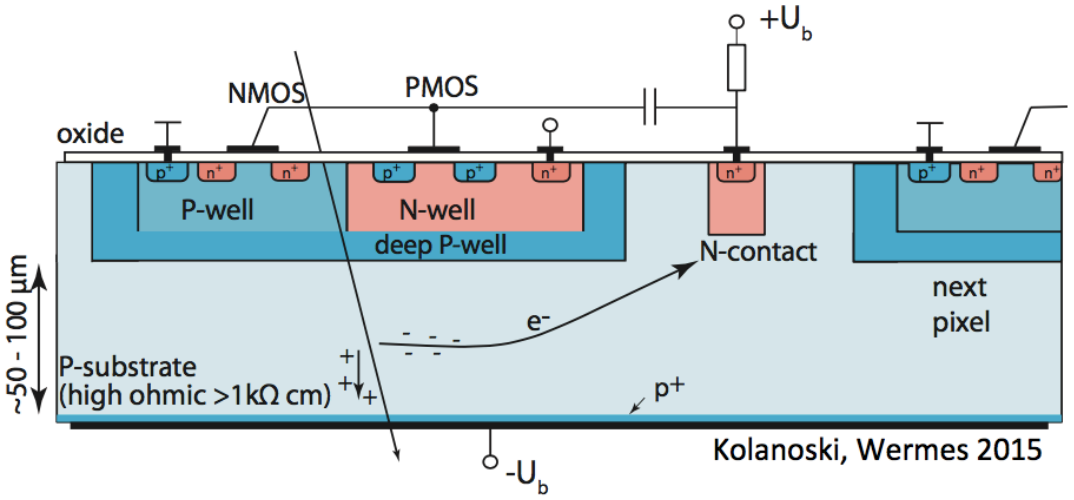


# Depletion technologies

- Depletion zone built in a 10-30 µm mid-resistivity p-type epitaxial layer,
- Growth on top of an undepleted p-type substrate.
  - Can be fully depleted with ~ few V
  - Signal 1-2 ke
- Example: AMS, TowerJazz



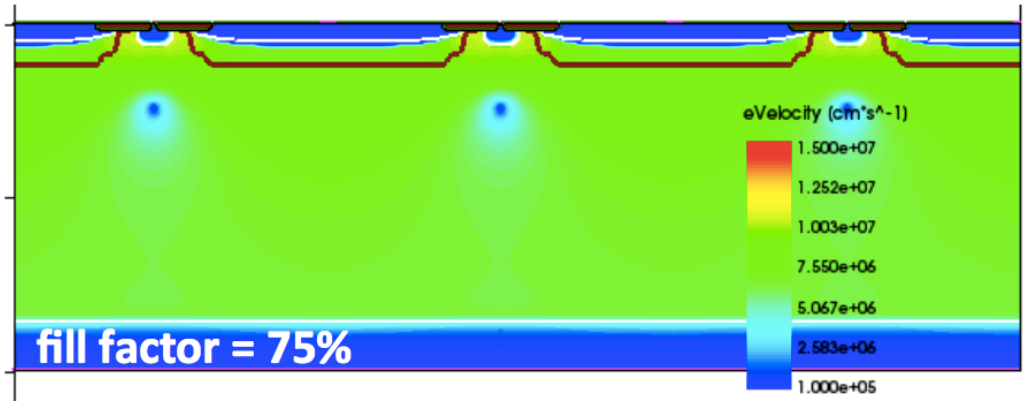

- Collection electrode is a deep n-well or a buried n-layer,
- Direct implant onto a p-type substrate.
  - Size of depleted region limited by the breakdown voltage (technology dependent)
  - Signal up to 10-20 ke (varying with irradiation)
- Example: LFoundry, STMicroelectronics

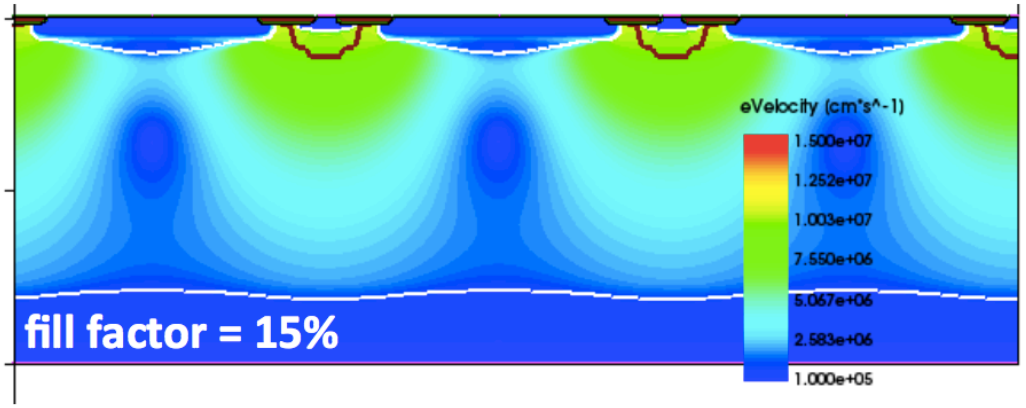



  - n-MOS devices always available, availability of p-MOS devices depends on the **number of deep wells** and on the **electrode layout**

# Large vs. small elecrodes

**Electron drift velocity**
**(T. Hemperek from ref. 5)**



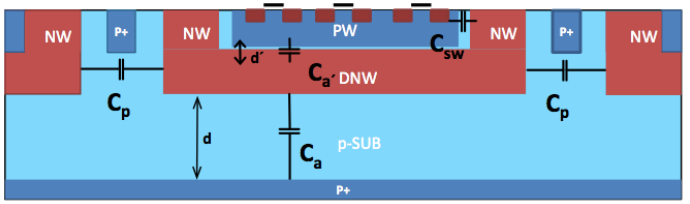




Collecting electrode is always an n-well

- **fast electron signal**

**Two major configurations:**

- front-end electronics **inside** the collecting well (large electrode/large fill factor)
  - **uniform charge collection**
  - **short drift path → less trapping**
  - **large electrode capacitance** ~100 fF, dominated by parasitic capacitance between the deep wells




- front-end electronics **outside** the collecting well (small electrode/small fill factor)
  - **non uniform drift field**
  - **long drift path, includes low-field regions between electrodes → more sensitive to trapping**
  - **small electrode capacitance** <10 fF

# Capacitance, noise, risetime

References 1,2

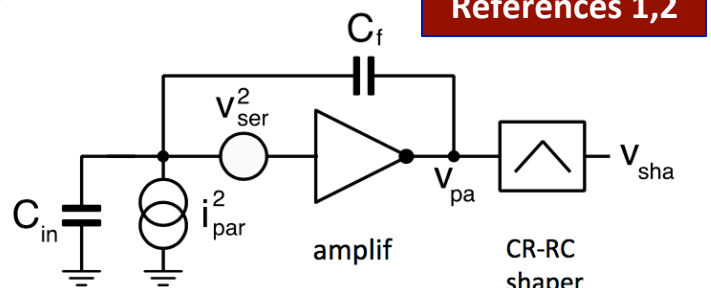
- Integrated front-end electronics: charge amplifier+shaper
- Equivalent Noise Charge (ENC)
  noise measured as equivalent signal at input

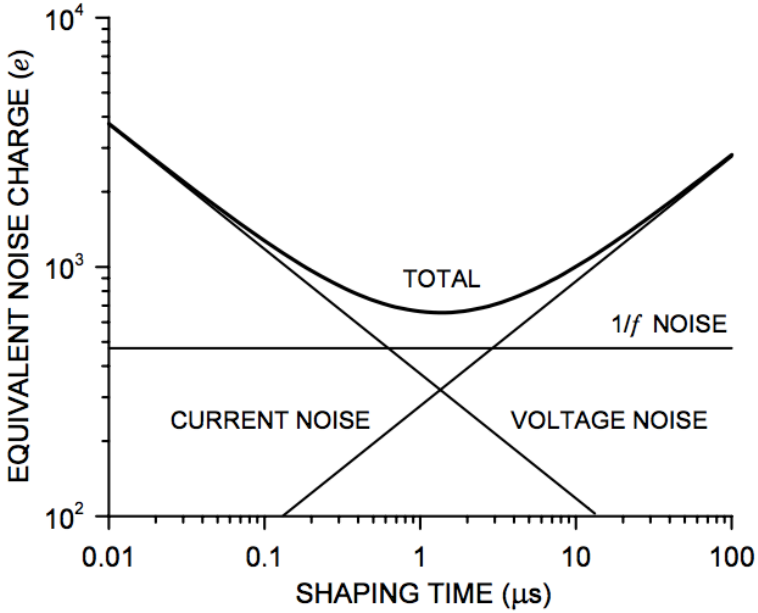
$$ENC^2 = \frac{e^2}{4q^2}\left(\frac{\tau}{2}I_0 + \frac{1}{2\tau}V_0 C_{in}^2 + 2V_{-1}C_{in}^2\right)$$

  - $e = 2.718$, $q$ = electron charge $1.6\times10^{-19}$ C
  - $\tau$ = shaping time
  - $I_0 = 2qI_{leak}$ from detector leackage current
  - $V_0 = \frac{8}{3}\frac{kT}{g_m}$ from transistor channel noise
  - $V_{-1} = \frac{K_f}{C_{ox}WL}$ from excess flicker (1/f) noise

$K_f$ = 1/*f* noise energy
$C_{ox}$ = oxide capacitance per unit area
*W*,*L* = transistor width and length

- Risetime $t_{rise} \propto \frac{1}{g_m}\frac{C_{in}}{C_f}$




- High **input capacitance $C_{in}$** can be compensated with **transconductance $g_m$**, at price of power (ALPIDE 24 mW/cm², ATLAS target 500 mW/cm²)

# ATLAS Depleted CMOS R&D























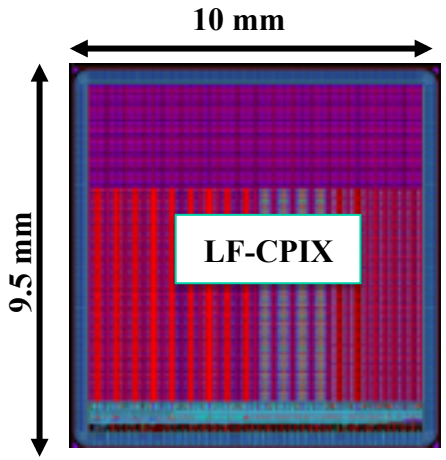


- Collaborative effort of ~25 ATLAS ITK institutes
- Capable of attracting also **non-ATLAS institutes** and resources

# Example of smart sensors

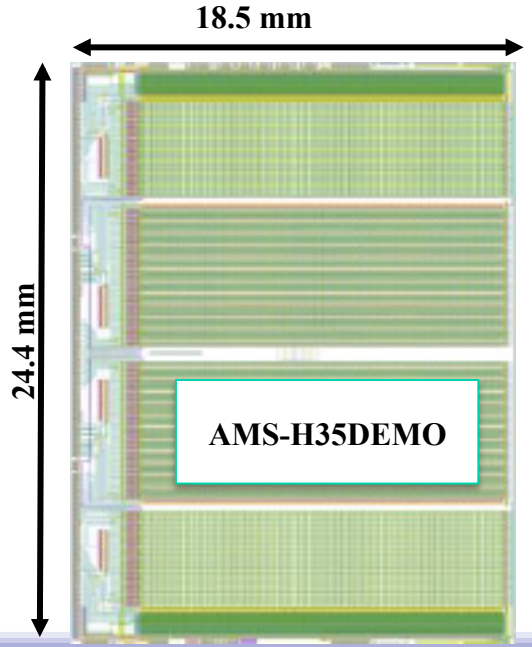
## LFoundry

- 150 nm process
- Both deep n-well and p-well
- Up to 7 metal layers
- Substrate >2 kΩ·cm
- **CCPD_LF** small (5×5 mm$^2$) prototype
- **LF-CPIX** "demonstrator" 50x250 μm$^2$ pixel



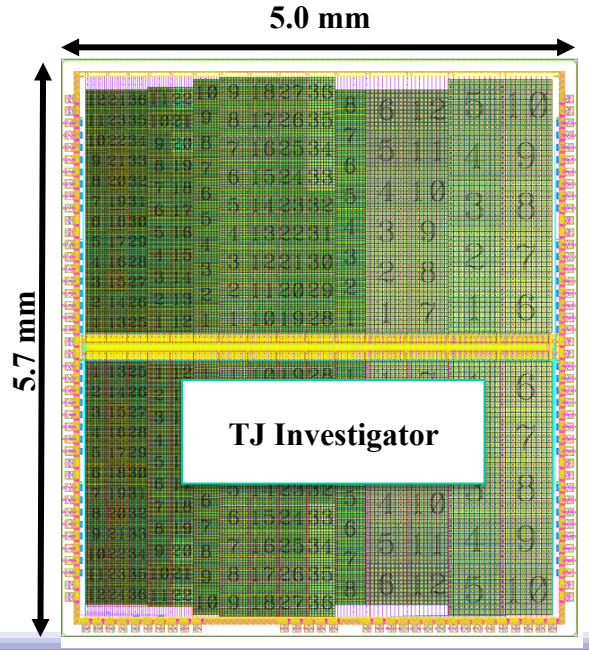

## AMS

- 350 nm and 180 nm HV-CMOS process
- 20—1000 Ωcm substrates
- **CCPD** prototype in H18, 33x125 μm$^2$ pixel
- **H35DEMO**, H35 process 50x250 μm$^2$ pixel



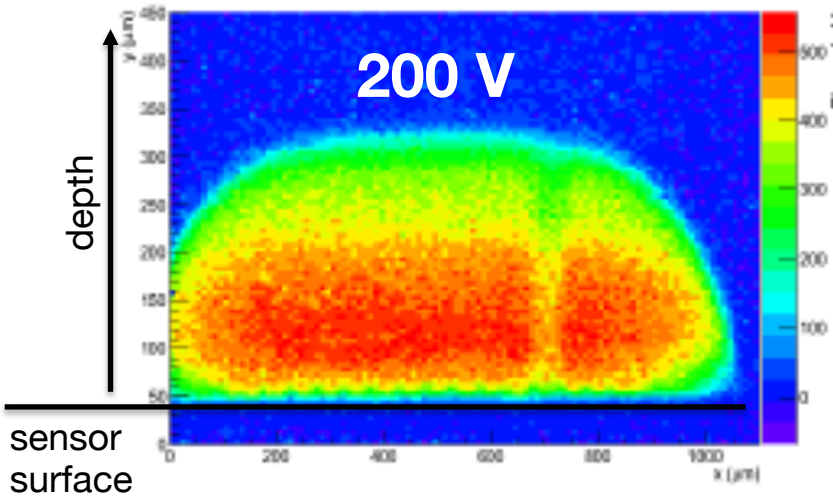

## TowerJazz

- 180 nm epitaxial process
- **Investigator** chip (ALICE)
- Small fill-factor
- Pixel dimensions from 20x20 to 50x50 μm$^2$
- 25 μm epi layer

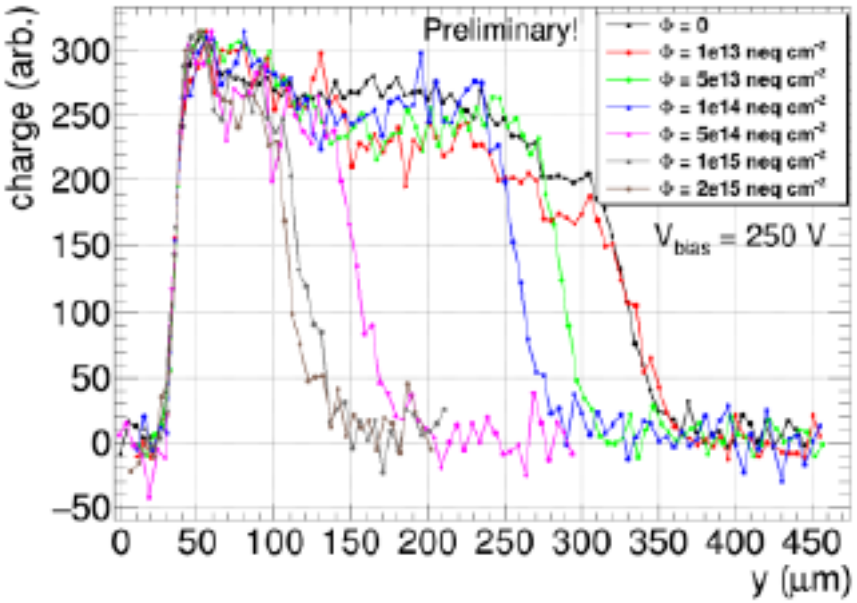


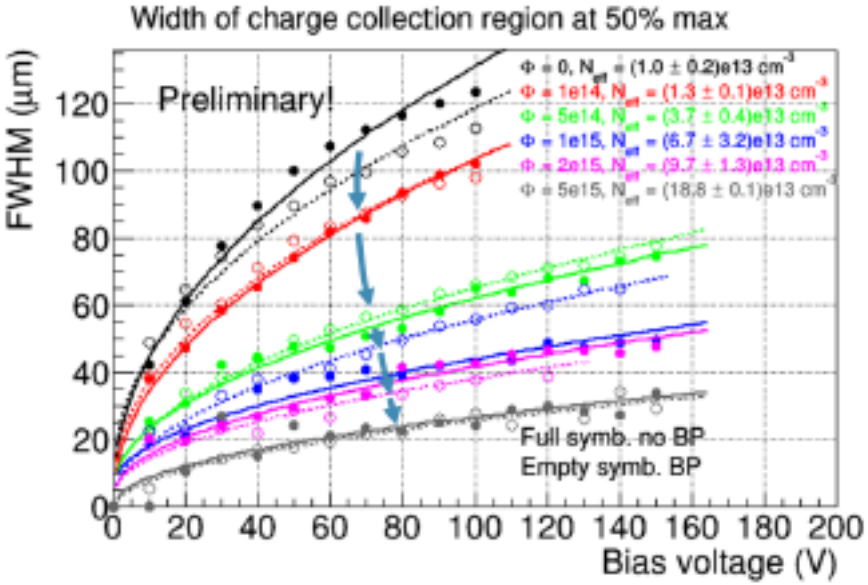
# LFoundry CPIX: Edge-TCT

- >2 kΩ·cm substrate
- Laser scan of the depleted region:
  **T**ransient **C**urrent **T**echnique
- Measuring charge collection as function of laser beam position
- **Irradiation up to $5\times10^{15}$ $n_{eq}/cm^2$**
- **Still significant size of the depleted region**




B. Hiti, I. Mandic (Ljubljana)



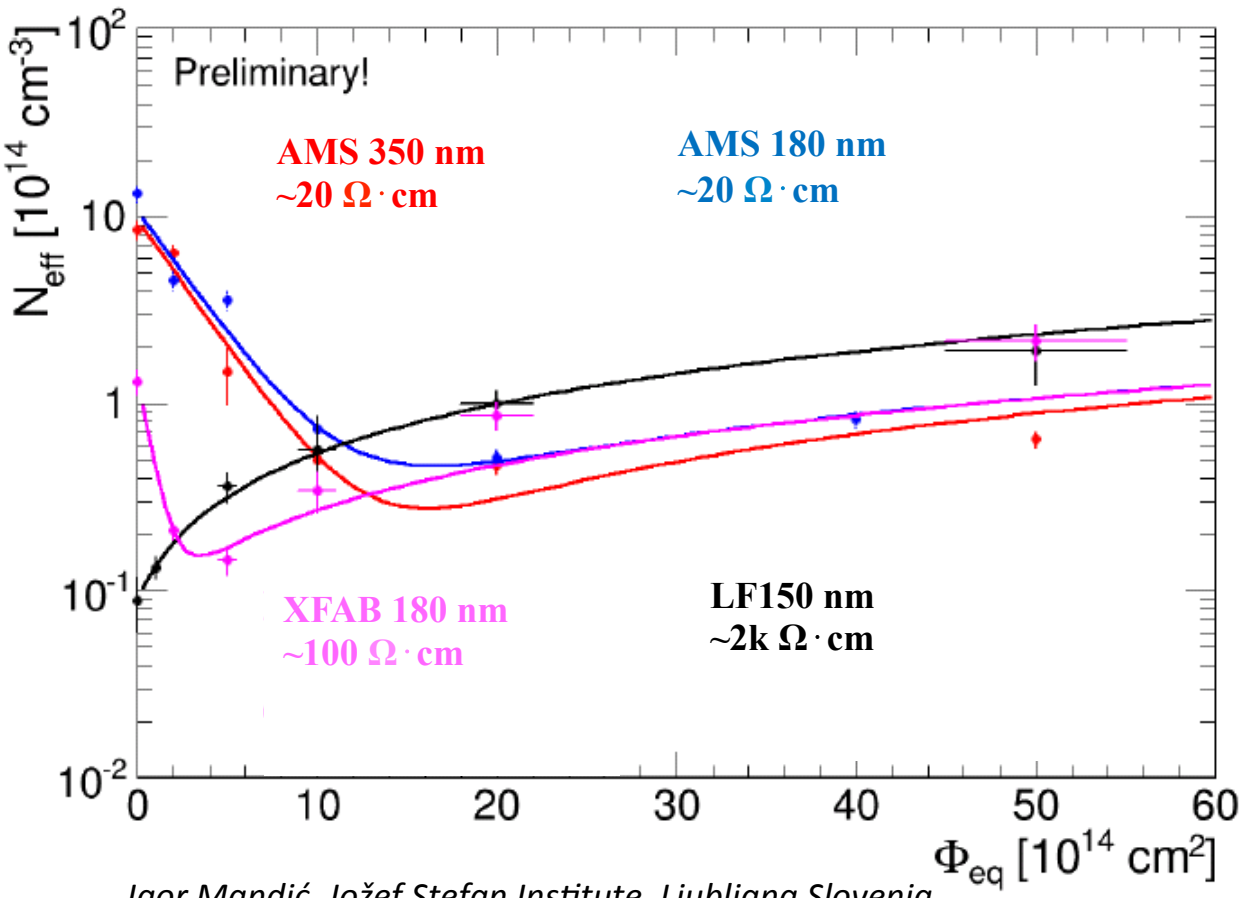
# Acceptor removal

- Depletion depth can be interpreted as an effective doping concentration:

$$d = \sqrt{\varepsilon_{\mathrm{Si}}\varepsilon_0 \frac{V + V_{\mathrm{BI}}}{qN_{A,\mathrm{eff}}}}$$

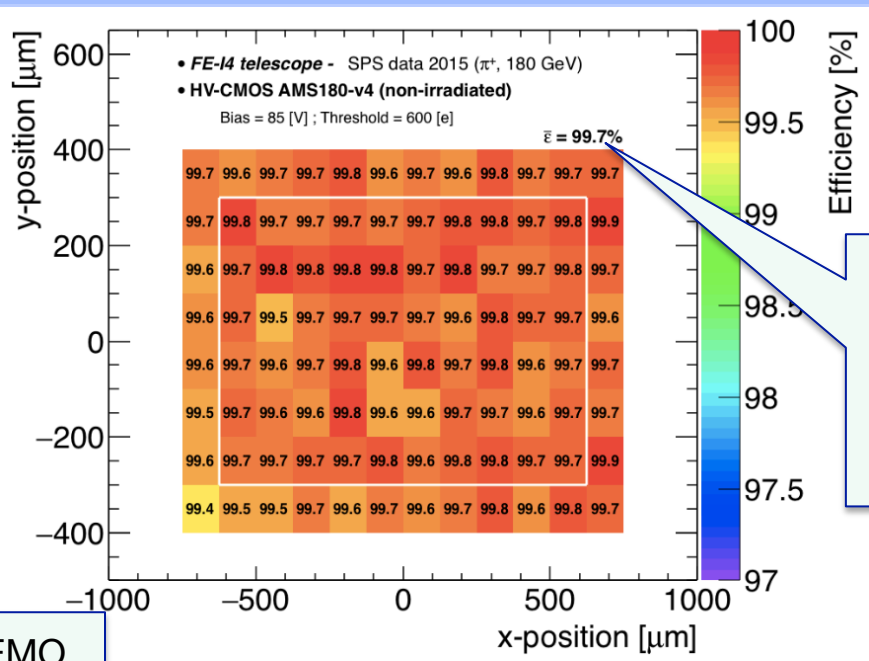
- At low dose acceptors are effectively neutralized

- Above $10^{15}$ $n_{eq}/cm^2$ the behaviour is approximately independent from the starting point.

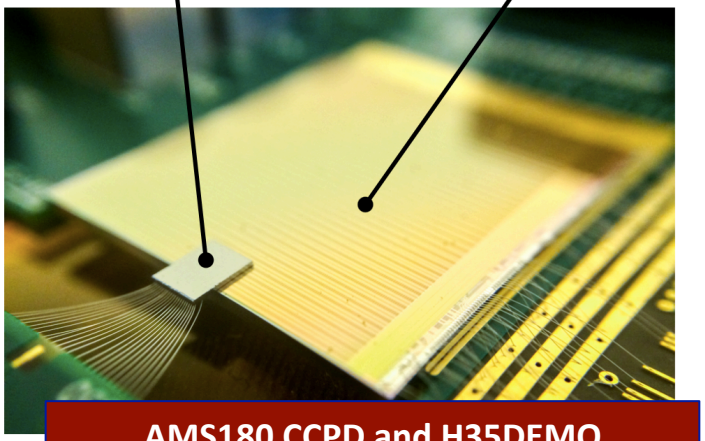



*Igor Mandić, Jožef Stefan Institute, Ljubljana Slovenia*
*11th "Trento" Workshop, February, Paris, 2016*

# AMS: test beam data

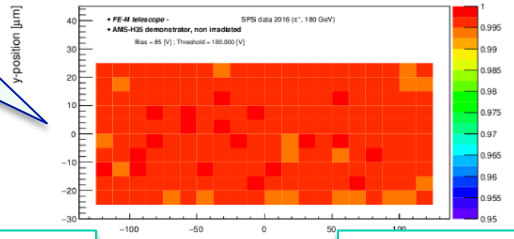


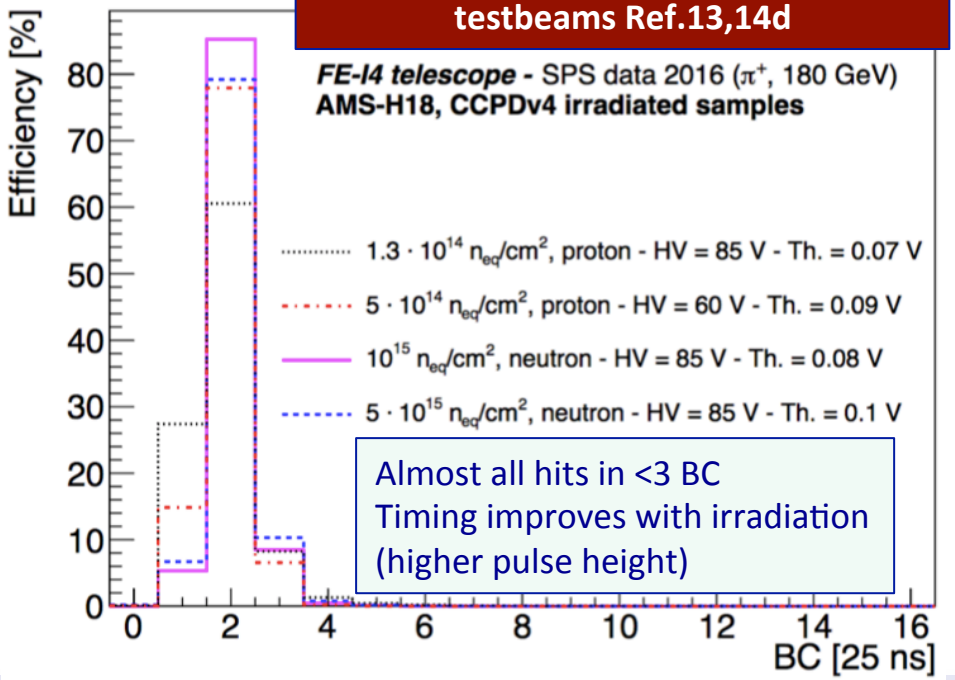

Efficiency 99.7% ~constant up to $10^{15}$ $n_{eq}/cm^2$




**AMS180 CCPD and H35DEMO testbeams Ref.13,14d**

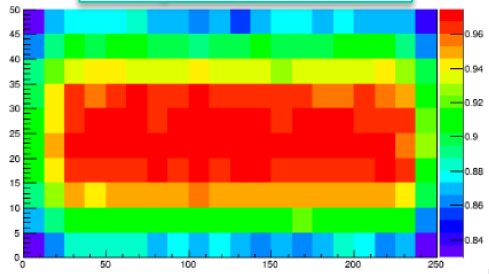
H35DEMO in-pixel position



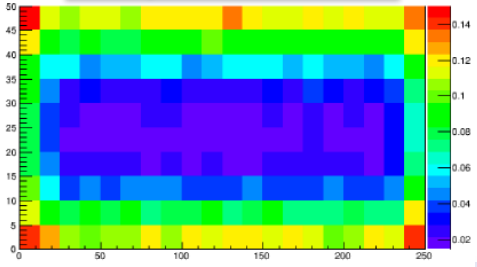



Almost all hits in <3 BC
Timing improves with irradiation (higher pulse height)

**1-pixel clusters**

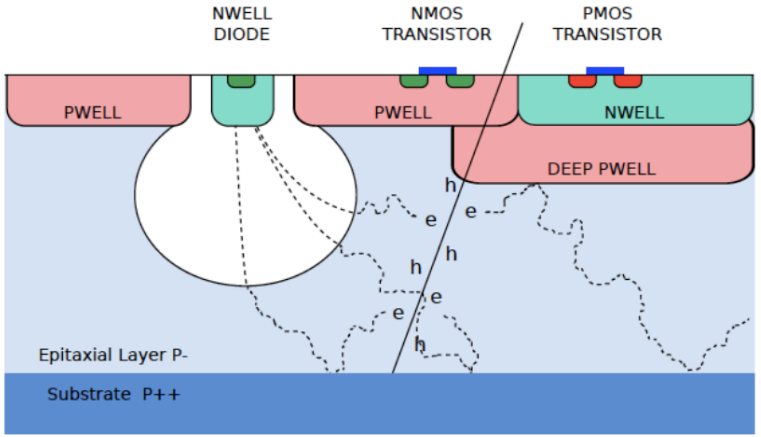


**2-pixel clusters**

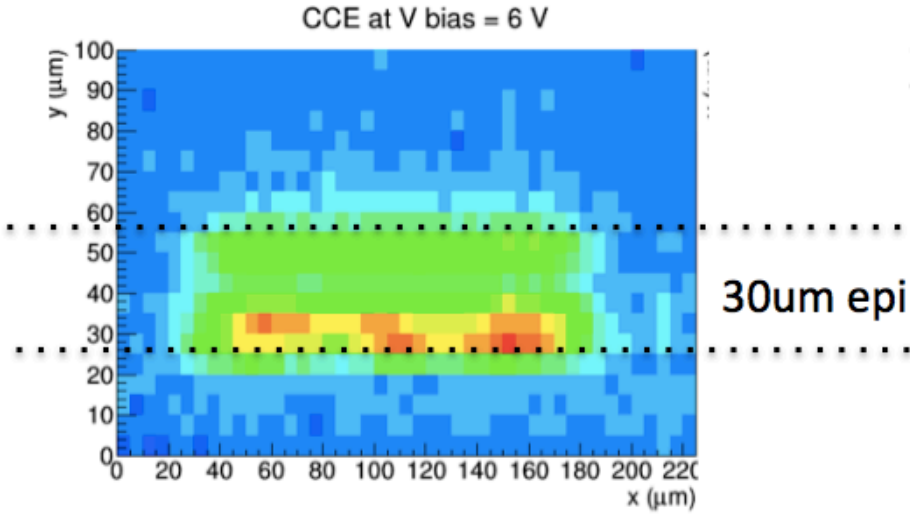


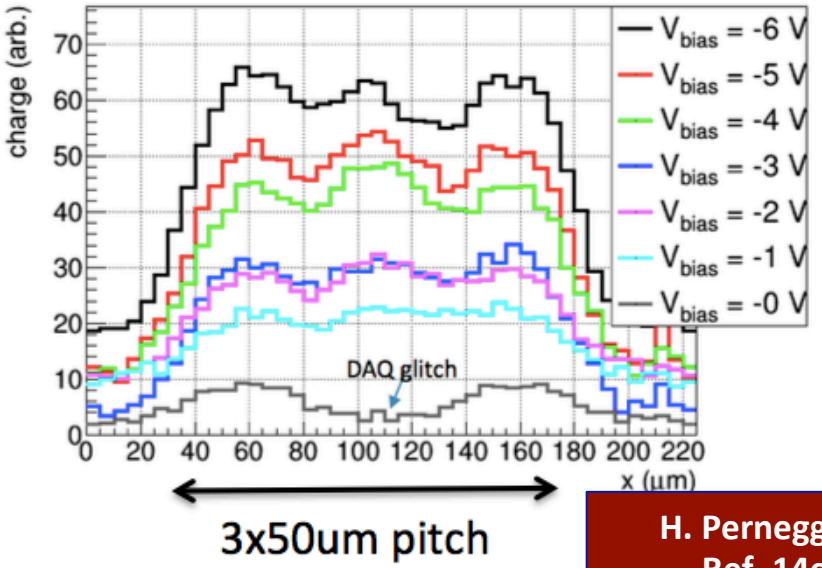
# TowerJazz: small fill factor

- Small collection electrodes:
  - Higher gain and faster response due to smaller capacitance (~5fF) and higher Q/C
  - Potentially lower power consumption
  - Signal collection under DPW after irradiation more difficult on edges
- Modified process to improve charge collection under the deep p-wells
  - uniform charge collection in the inter-pixel region
  - verified at $10^{15}$ $n_{eq}/cm^2$




Schematic cross-section of CMOS pixel sensor
(*ALICE ITS Upgrade TDR*)



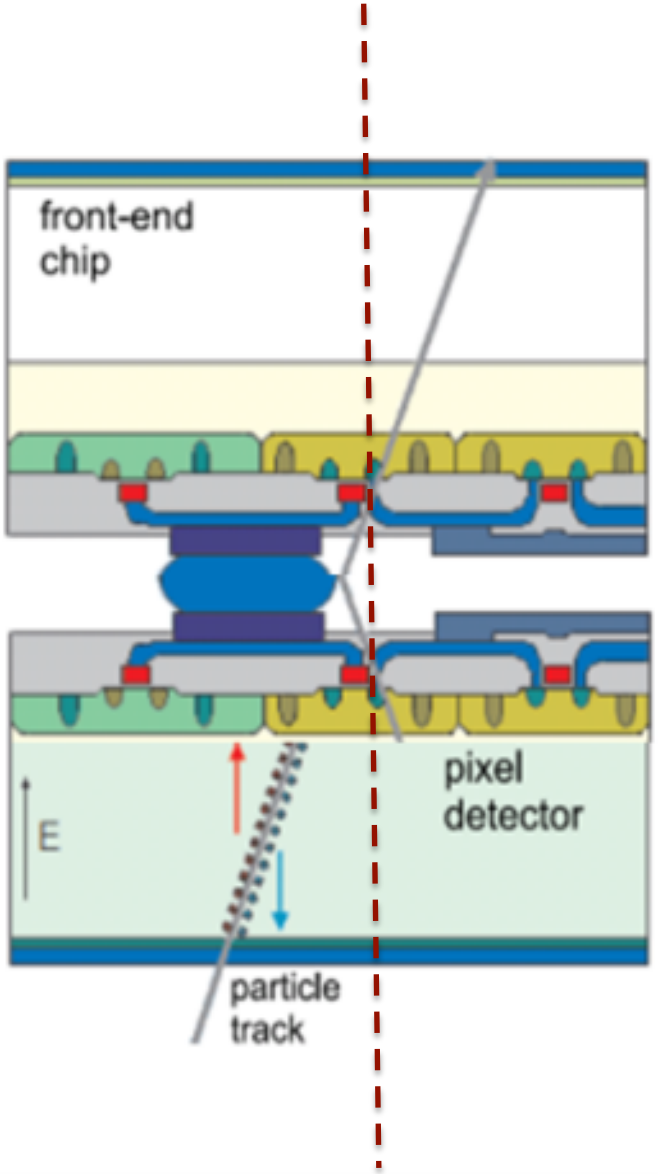




H. Pernegger
Ref. 14c

# FROM SMART SENSORS TO DETECTORS

# Capacitive Coupling

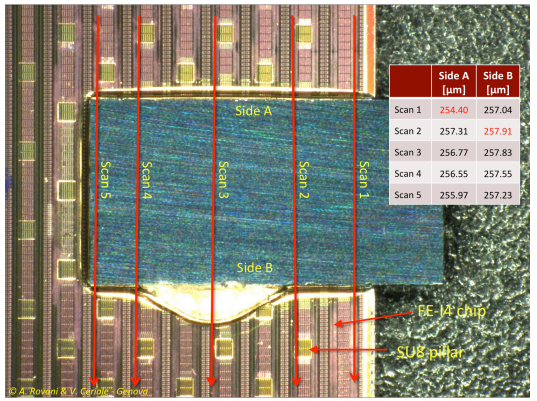
- Connection of passive sensors to a front-end chip by bump-bonding is a mature technology.
- The interconnection cost is significan fraction of the total detector cost
  - similar to sensitive part
- Challenges for HL-LHC detectors:
  - ×5 bump density
  - thin detector and chips (planarity)




- Exploit local amplification integrated front-end
  - or broadcast digital signal
- via capacitive coupling
  - dielectric glue layer
  - provides both mechanical and electrical coupling.
  - **simpler and faster process**
- **Separate functionality** of smart sensor and readout chip:
  - may exploit best available technologies on each side

# Uniformity and repeatability

- Uniformity by inserting spacers on chip
- Deposition of photoresist pillars tested on single dies in the past years.




| | Side A [µm] | Side B [µm] |
|---|---|---|
| Scan 1 | 254.40 | 257.04 |
| Scan 2 | 257.31 | 257.91 |
| Scan 3 | 256.77 | 257.83 |
| Scan 4 | 256.55 | 257.55 |
| Scan 5 | 255.97 | 257.23 |

- Full wafer tests running just now:

**Basic process**

Spin SU-8 photoresist
Pattern pillars by mask


Glue deposition

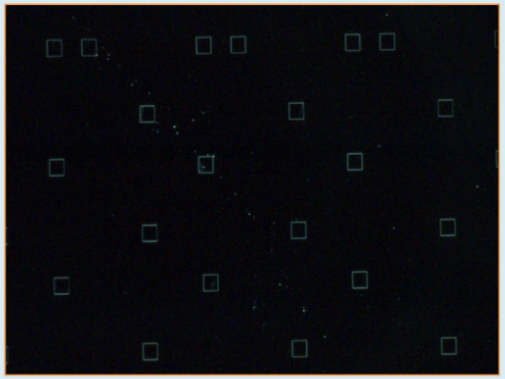

Align & pressure

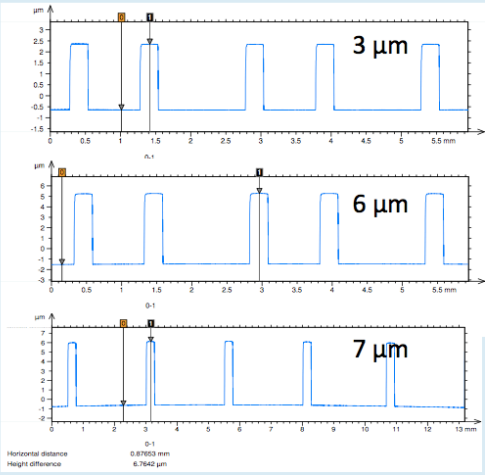

Deposition of SU8 photoresist by spinning

Credits: Giovanni Darbo

**Pillars deposition only @ Selex: Very promising results!**

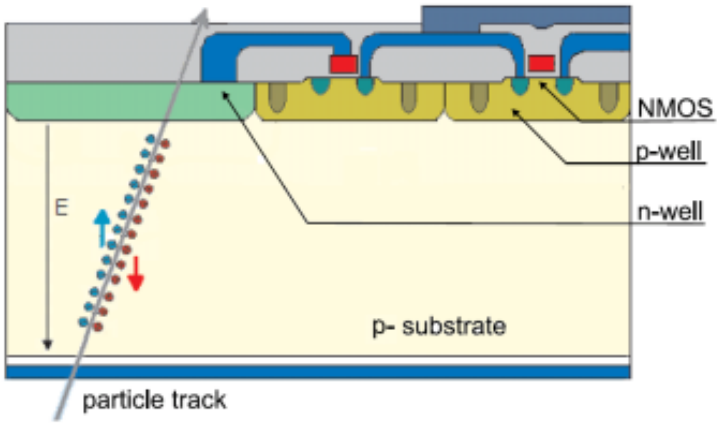
- 3 wafers with pillars at 3,6 and 7 µm
- Good planarity






A. Gaudiello
Ref.15d

# Monolithic architectures




- Integrate smart sensor and readout chip in a single device:
  - Depleted Monolithic Active Pixels (DMAPS)
  - **less material**
  - **no interconnection required: simpler and faster production time**
  - **integration level of HV/HR CMOS processes lower than the 65 nm process used for the HL-LHC front-end:** limitation on it rate and local memory size
  - **potential cross talk between analog cell and digital readout part**

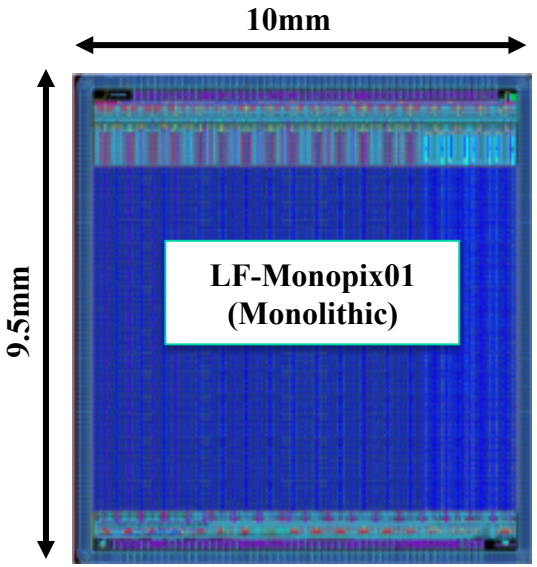
Two approaches currently under evaluation:

- **Column drain**
  - Similar to various implementations in FEI3, FEI4, RD53 chips
  - Local buffering of hits in the matrix
  - Readout synchronous with clock
  - Require distributions of clock and (in some implementations) trigger signal along the whole pixel matrix
- **Asynchronous readout**
  - Analog or digital output sent directly to chip periphery
  - Time stamping and hit storage at periphery
  - A first implementation in the MUPIX chip for the MU3E experiment

# Monolithic prototypes

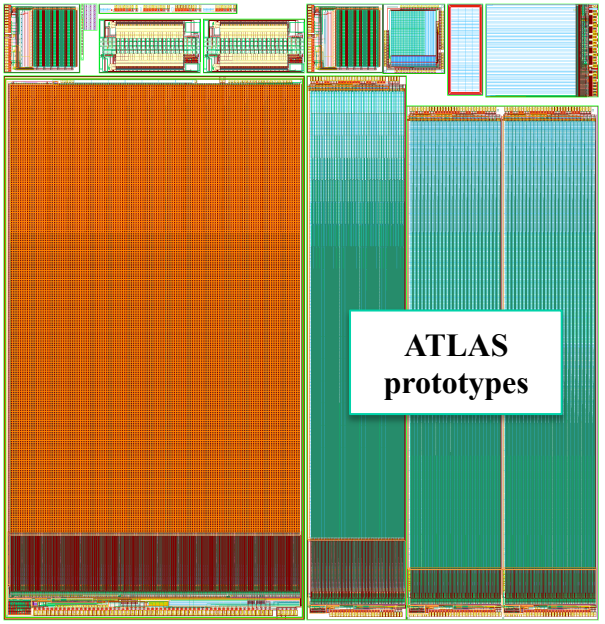
## LFoundry

- Subm. in **Aug. 2016**
- **Monopix01** and **Coolpix1**
- "Demonstrator size"
- 50 x 250 μm$^2$ pixels
- Fast standalone R/O
- Column drain approach



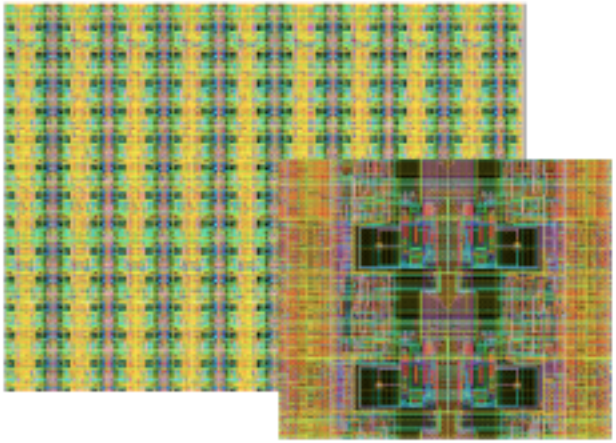

## AMS H180

- Subm. in **Jan. 2017**
- **Mu3E** + **ATLAS** (monolithic)
- Additional production step – isolated PMOS
- 80 and 200 Ωcm wafers
- Reticle size about 21mm x 23mm



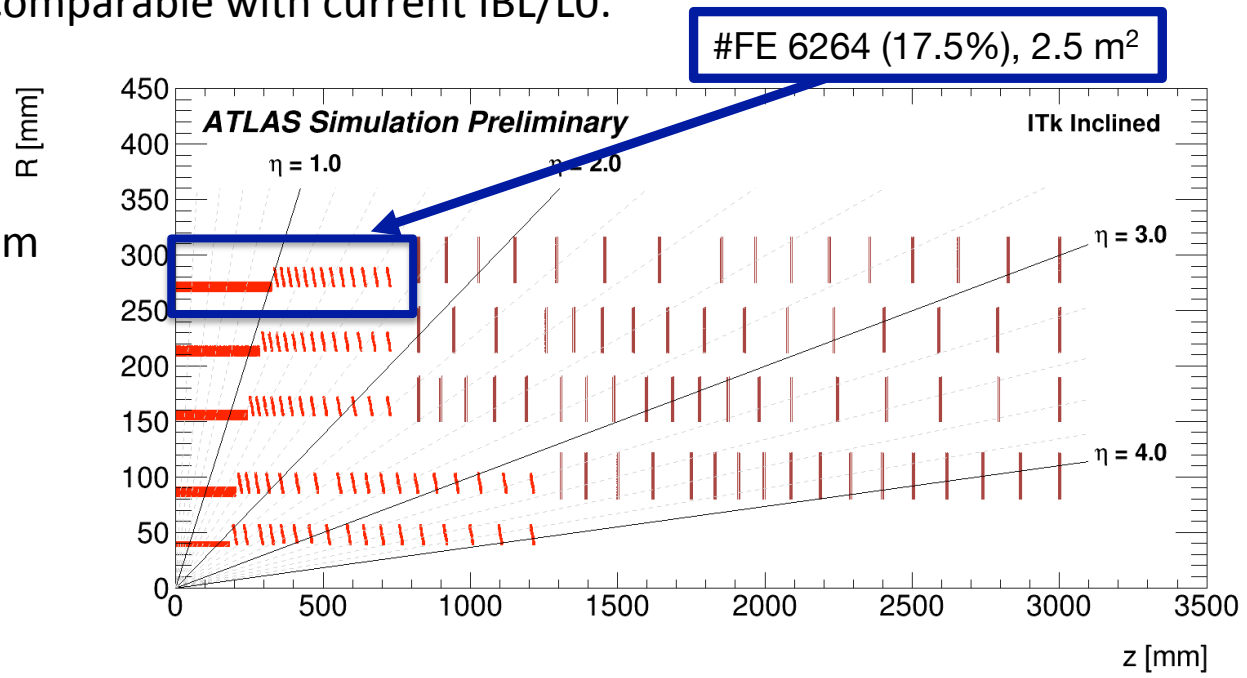

## TowerJazz

- Subm. in **May 2017**
- Two large scale demonstrators **MALTA** and Monopix:
  - Focus on small fill-factor pixels
  - Asynchronous matrix readout (no clock distribution over the matrix)
  - Column Drain Read-Out (based on Monopix)



# HV-CMOS for ATLAS

- **Monolithic CMOS detector are an interesting option for ATLAS ITk**
  - reduction of material, simplification of assembly, potential reduction of power consumption
- Candidate application is for the **outermost pixel layer**
  - largest area layer, where practical benefits are outstanding
  - reducing pressure on bump bonding and simplifying the assembly, it provides contingency to the whole pixel project
  - radiation level and data rates comparable with current IBL/L0:
    NIEL $1.2\times10^{15}$ $n_{eq}/cm^2$,
    TID 60 Mrad,
    hit rate 0.9 MHz/$mm^2$
  - compatible with the 130-180 nm integration level provided by HV/HR technologies



# Conclusions

- Depleted-CMOS sensors are undergoing an active R&D phase
  - This presentation focuses on developments from the ATLAS pixel community
  - Efforts also within ATLAS strip groups, MU3E collaboration, and other INFN projects (SEED, HVR_CCPD) and European grants (IMPACT, some WP in AIDA2020)
- Many progresses have been achieved on the CMOS sensors
  - Good understanding of the depletion zone and charge collection
  - Efficiency is >99% even after irradiation at fluences >$10^{15}$ $n_{eq}/cm^2$
  - Recently very encouraging results have been shown also on a small fill factor design, which is very attractive for applications, due to the low input capacitance and low power
- The major next R&D step is the integration of the sensors with a high rate readout architecture
  - For extremely high rate, a hybrid solution, with capacitive coupling to a highly integrated front-end, is under development
  - The 130-180 nm feature size of the currently available technologies should allow monolithic solutions able to sustain the hit rate of the external pixel layers at the HL-LHC
  - Different prototypes will become available and will undergo extensive characterizaion in the next months
  - Development of **fast-thin-radiation hard CMOS sensors** will provide an interesting opportunity for future tracking detectors

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12) M. Benoit et al., *Results of the 2015 testbeam of a 180 nm AMS High-Voltage CMOS sensor prototype*, JINST 11 (2016) P07019, doi: 10.1088/1748-0221/11/07/P07019

13) G. Kramemberg et al., *Charge collection studies in irradiated HV-CMOS particle detectors*, JINST 11 (2016) P04007, doi: 10.1088/1748-0221/11/04/P04007

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   a) I. Peric, HVCMOS Sensors for high rate particle tracking
   b) B. Hiti, Measurements of passive structures on irradiated HV-CMOS detectors
   c) H. Pernegger, First tests of a novel radiation hard CMOS sensor process for Depleted Monolithic Active Pixel Sensors
   d) T. Weston, An overview of recent HV-CMOS results
15) 8th International Workshop on Semiconductor Pixel Detectors for Particles and Imaging, Sestri Levante, September 2016, https://agenda.infn.it/conferenceDisplay.py?confId=10190
   a) I. Peric, Status of HVCMOS development for ATLAS, JINST 12 (2016) C02030
   b) F. Meier Aeschbacher, MuPix7 — A fast monolithic HV-CMOS pixel chip for Mu3e, JINST 11 (2016) C11029
   c) T. Hemperek, Overview and perspectives of HR&HV CMOS
   d) A. Gaudiello, Pixel hybridization technologies for HL-LHC, JINST 11(2016) C12077
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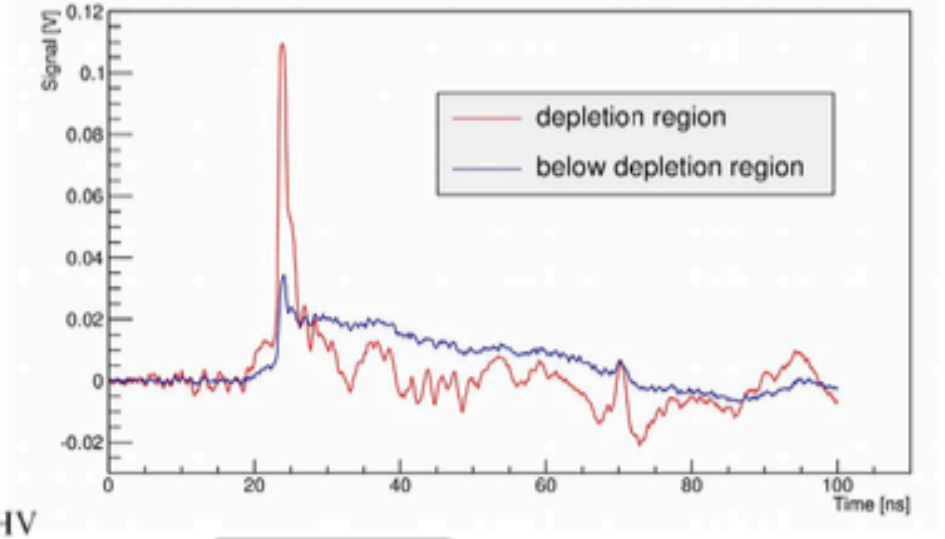
# BACKUP

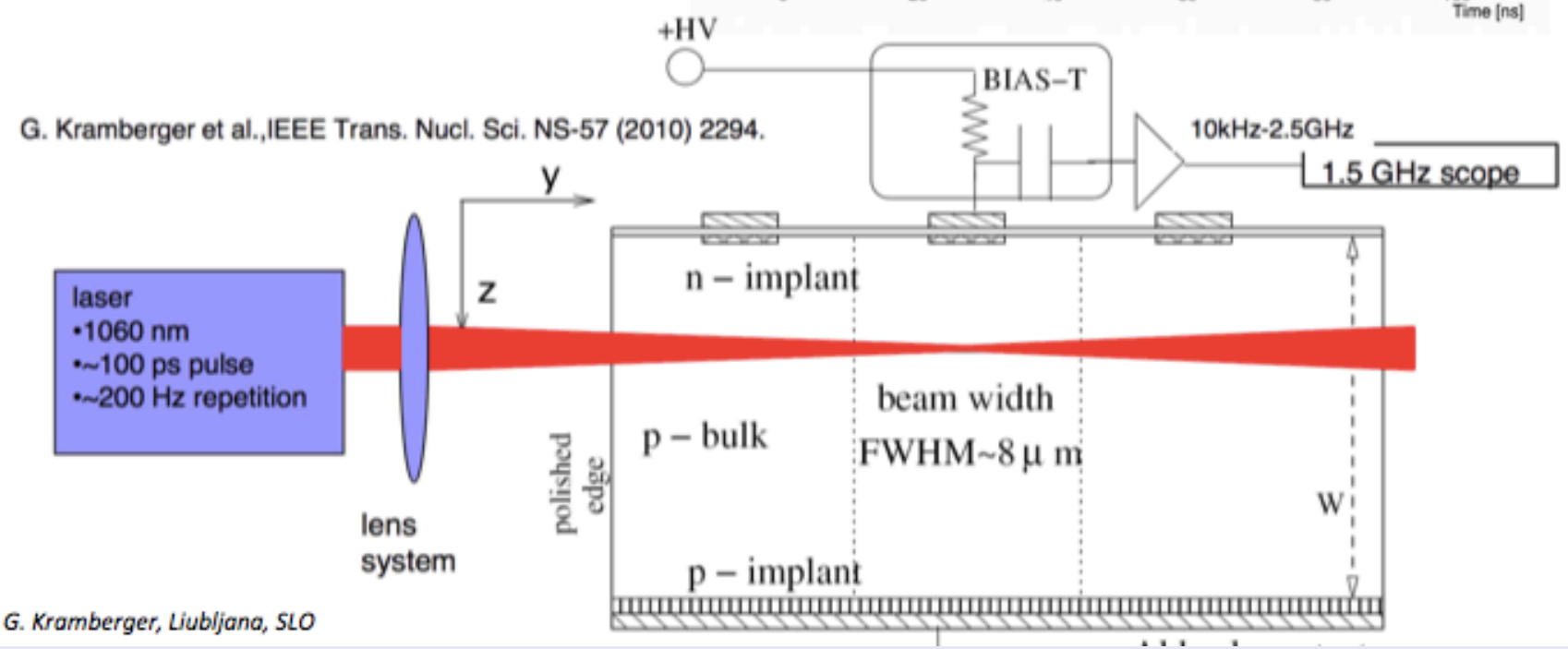
# Transient Current Technique

**TCT**: Transient Current Technique, i.e. observe the time-resolved charge collection generated by MIP, alpha or **laser pulse**

- Fast current contribution: collection by drift
- Slow current contribution: collection by diffusion




G. Kramberger et al.,IEEE Trans. Nucl. Sci. NS-57 (2010) 2294.

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# Acceptor removal

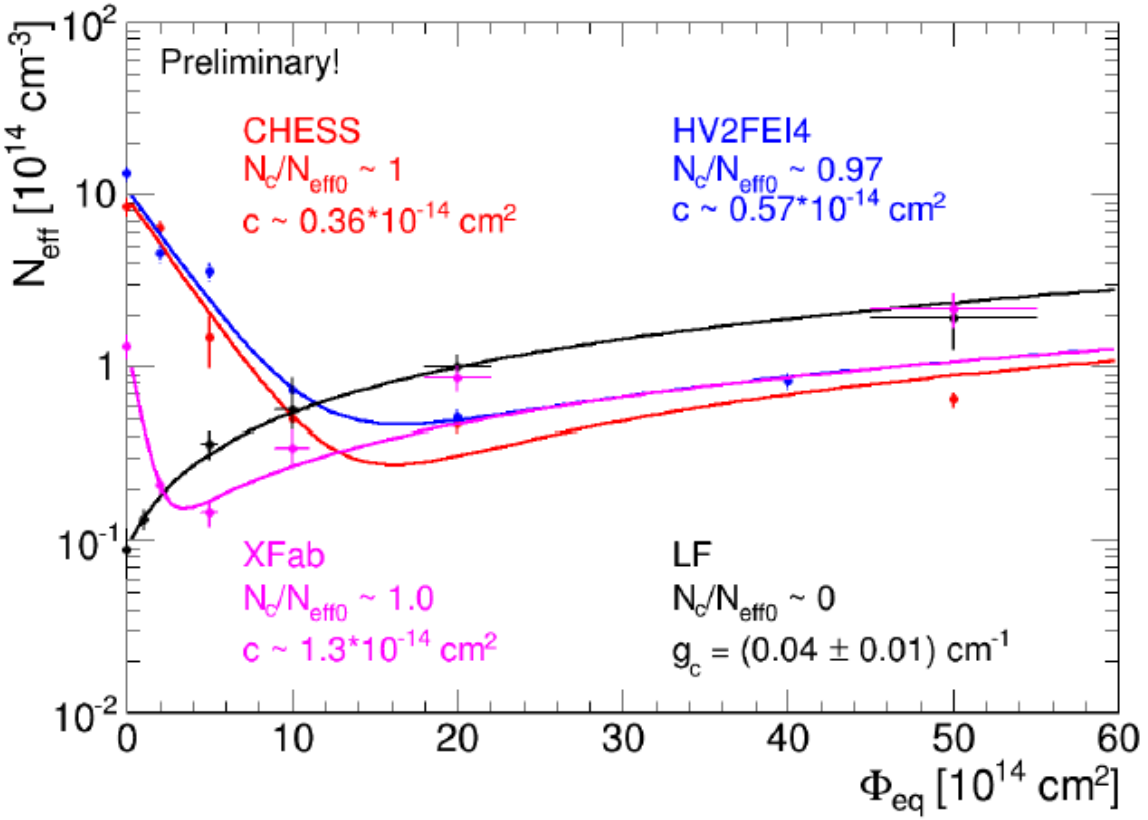
**$N_{eff}$ vs fluence**

acceptor removal

Radiation introduced deep acceptors: $g \sim 0.02\ cm^{-1}$

AMS and XFab: $N_{eff} = N_{eff0} - N_c \cdot (1 - \exp(-c \cdot \Phi_{eq})) + g \cdot \Phi_{eq}$ $N_c$, $N_{eff0}$ and $c$ free parameters, $g$ fixed

LFoundry: no removal ($N_c \sim 0$), fit: $N_{eff} = N_{eff0} + g \cdot \Phi_{eq}$ $N_{eff0}$ and $g$ free

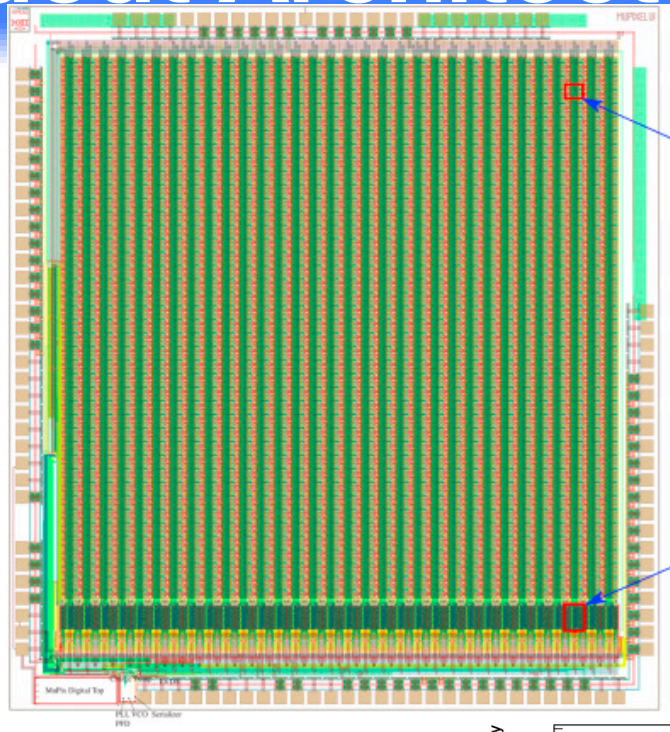



AMS (CHESS and HV2FEI4)
G. Kramberger et al., 2016 *JINST11 P04007*

I. Mandic (IJS Ljubljana)

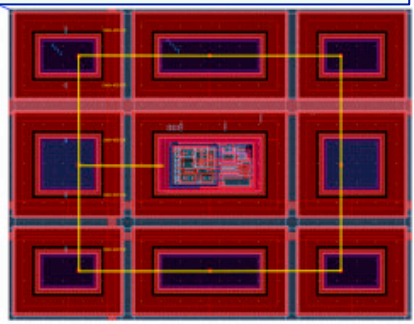
# MUPIX Readout Architecture

- For high rate applications **sparse readout** is required:
  - hit information is transferred from the **pixel cell** to the **chip periphery**...
  - ...where it is usually serialized and transmitted to off-detector readout electronics.
- Split the pixel cell in a pure analog sensor and mirror pixel in the periphery with all digital functionality.
- Asynchronous readout:
  - analog signal cell transmitted to the periphery.
  - where it is time-stamped and readout.
- **Pros**: no digital-to-analog cross talk, low power.
- **Cons**: large number of interconnections: line-to-line pickup noise, may not scale to large matrices.



**MuPix chip – Ref.12, 15b**

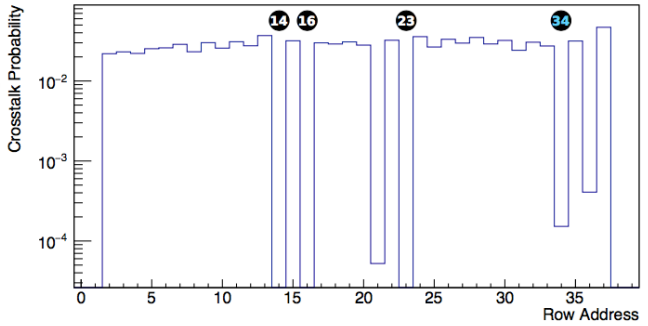
sensitive pixel in active region

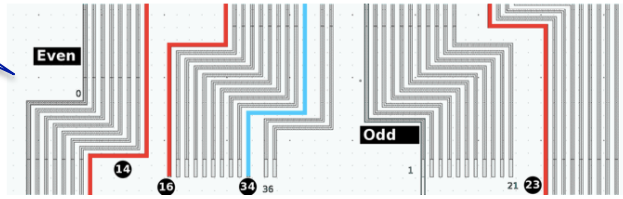


mirror pixel in periphery

~2% cross talk

Except for widely spaced lines

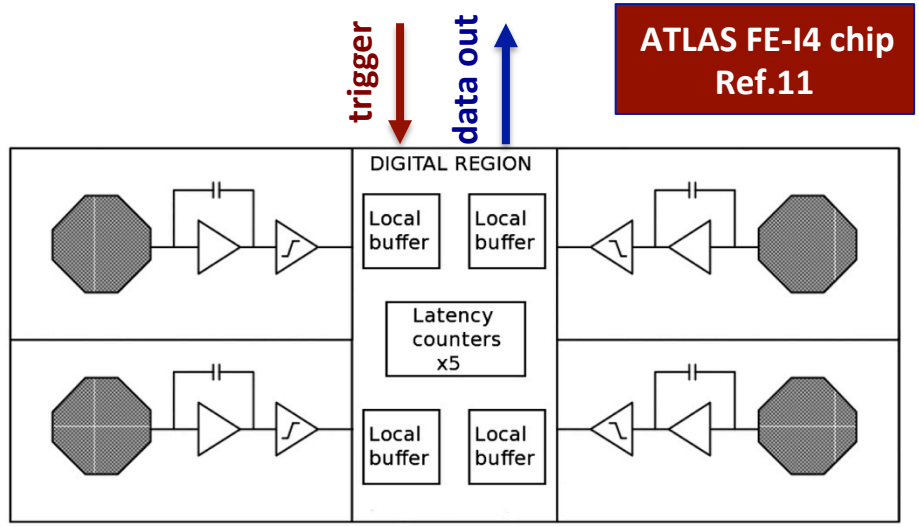


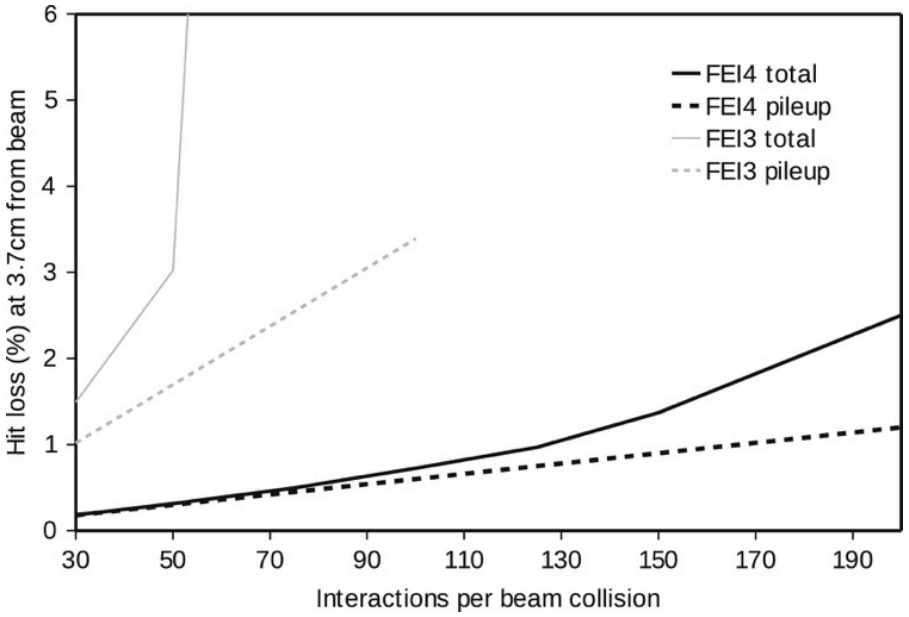



# FEI4 Readout Architecture

- *store-filter-readout* architecture:
  - *store*: when analog signal exceeds a defined threshold, a hit is created.
  - *filter*: all hits are registered in local buffers, shared by block of pixels. They are stored for the time needed for trigger decision, and deleted if the even is not triggered.
  - *readout*: only hits corresponding to the triggered events are sent to the chip periphery and trasmitted to the off-detector electronic.
- **Pros**: distributed memory, less data transfer.
- **Cons**: it requires clock **and trigger** distribution on the whole chip (skew <2ns).
- It provides significant improvements at high hit rate:
  - used in the ATLAS FE-I4 chip
  - base of the RD53 design

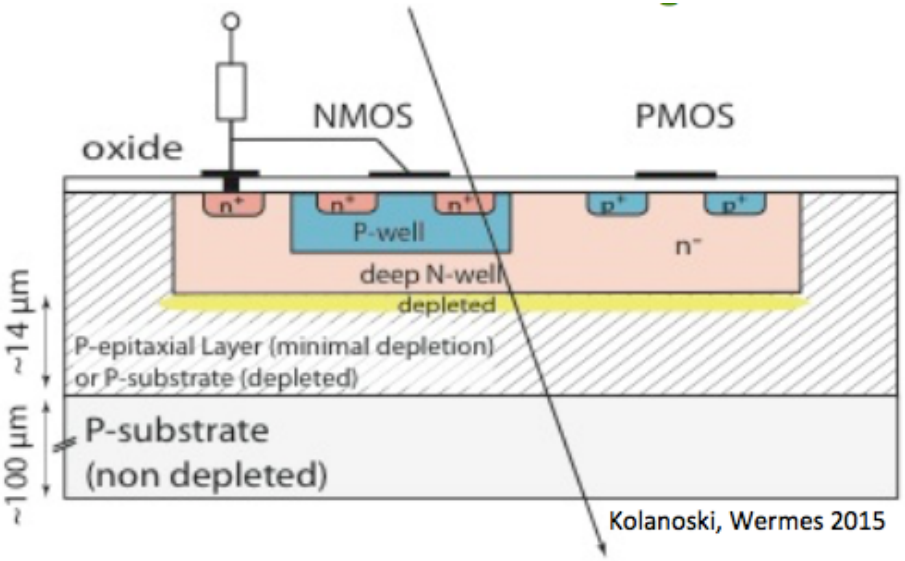
**ATLAS FE-I4 chip Ref.11**

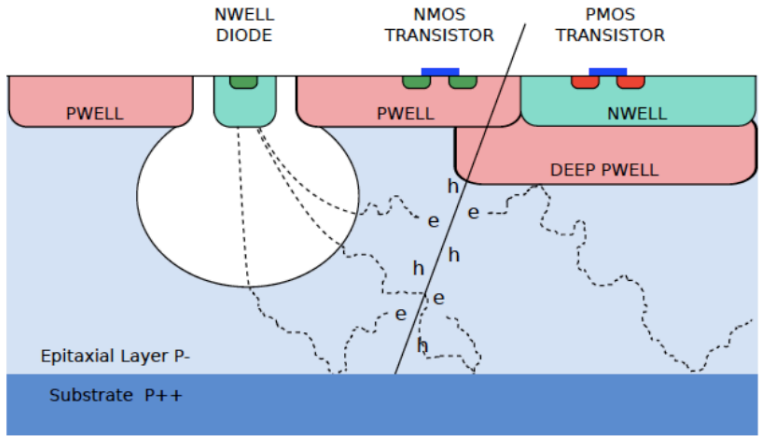


# Depletion: epitaxial layers

- Depletion zone built in a 10-30 μm mid-resistivity p-type epitaxial layer,
- Growth on top of an undepleted p-type substrate.
  - Can be fully depleted with ~ few V
  - Signal 1-2 ke
  - n-MOS devices always available
  - availability of p-MOS devices depends on the **number of deep wells** and on the **electrode layout**
- Example: AMS, TowerJazz




Schematic cross-section of CMOS pixel sensor
(*ALICE ITS Upgrade TDR*)

# Depletion: high resistivity

- Collection electrode is a deep n-well or a buried n-layer,
- Direct implant onto a p-type substrate.
  - Size of depleted region limited by the breakdown voltage (technology dependent)
  - Signal up to 10-20 ke (varying with irradiation)
  - **Multiple-wells** process gives access to the full set of CMOS devices
  - Depending on the process large- or small-electrode configurations may be available
- Example: LFoundry, STMicroelectronics