The SuperB Accelerator Control System: Plans and R&D Status

—

i.e. an attempt to innovate the standar model of control systems

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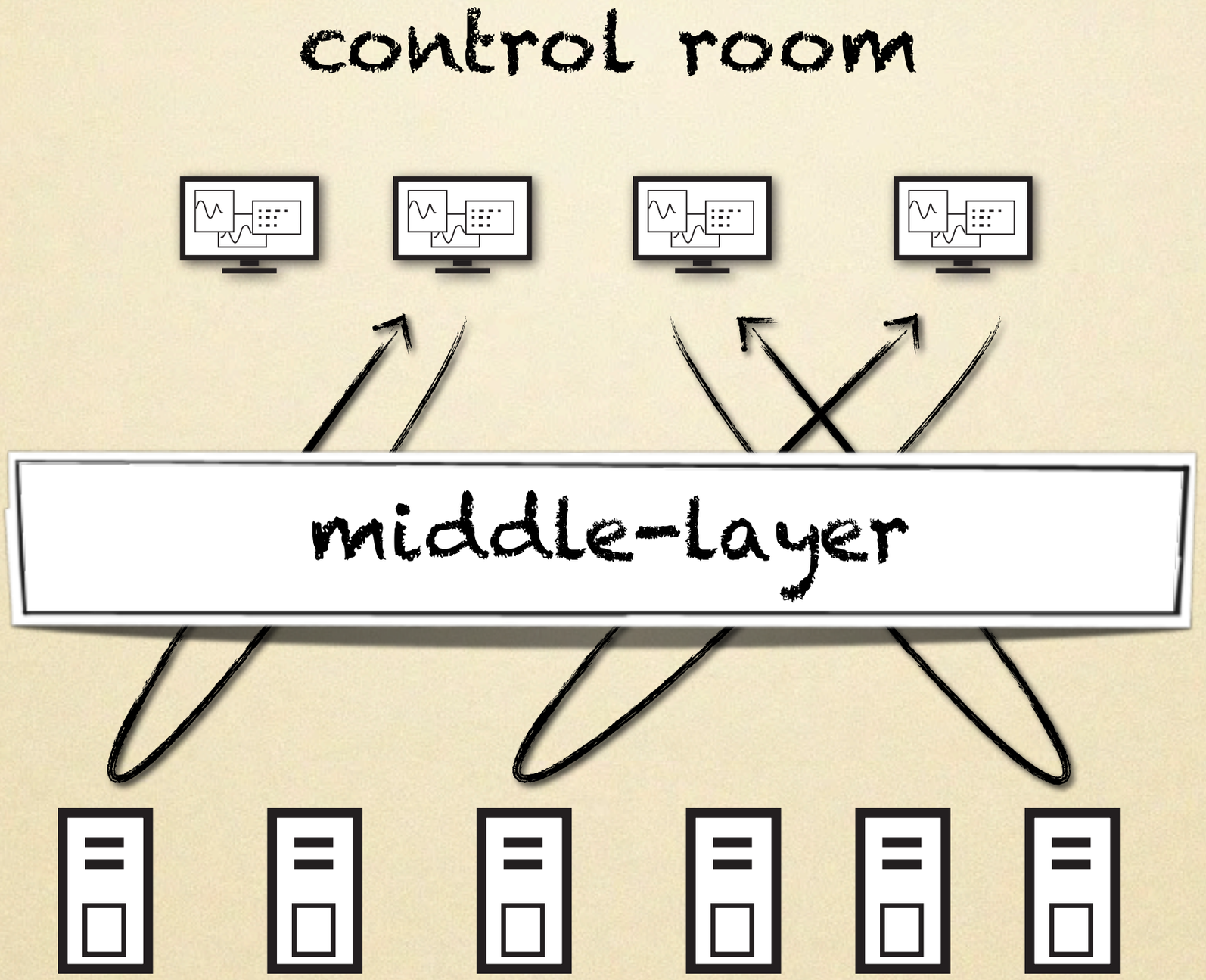
SuperB Computing R&D Workshop 2011 Ferrara, 4-7 July 2011

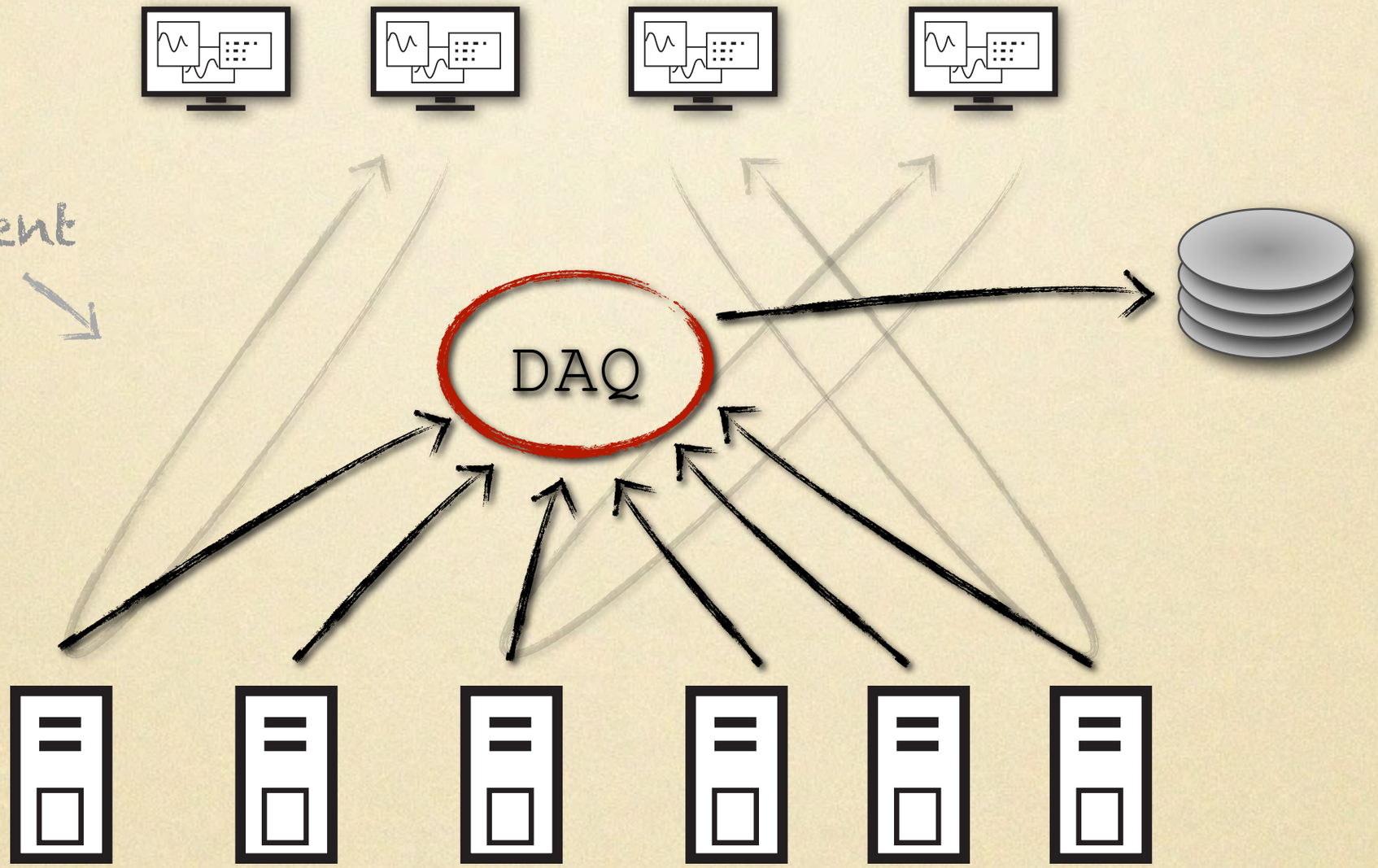
"The *standard model* consists of a local area network providing communication between front end microcomputers, connected to the accelerator, and workstations, providing the operator interface and computational support."

“standard model”



standard model + DAQ

control room



two different topologies ↘

accelerator

the starting point

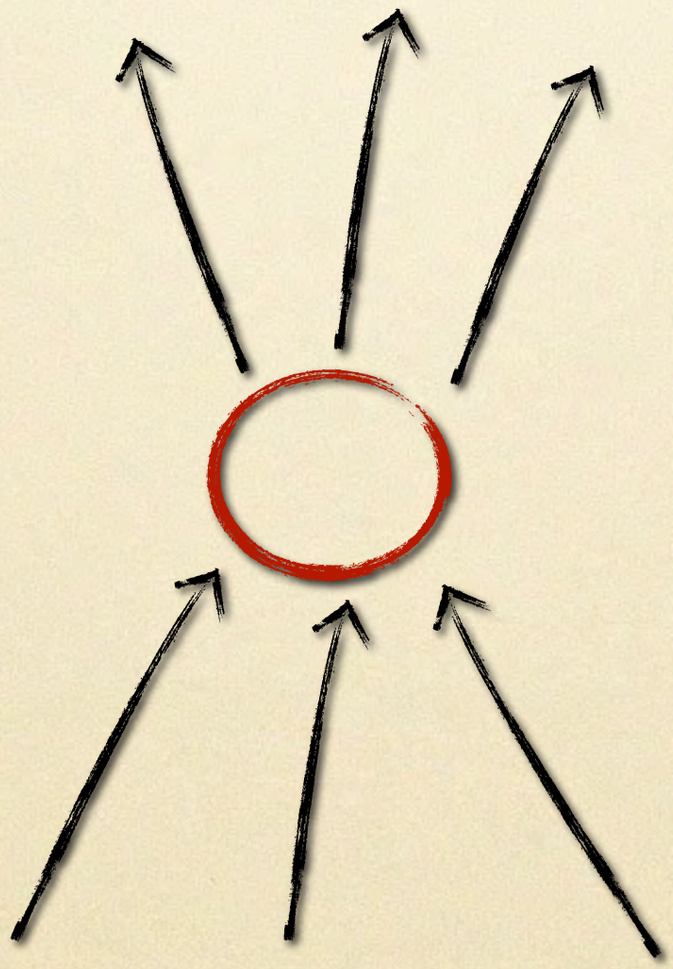
- **goal**: develop a new solution for a control system's DAQ
- use key/value db as alternative to RDBMS
  - fast, scalable, distributed storage, low-cost servers

the next step

- **extended goal**: *key/value* db looks great, can we use it for **live data** ?
  - data retrieving still slow
- use distributed caching instead
  - same topology, same data structure, same scalability

the new paradigm

control room

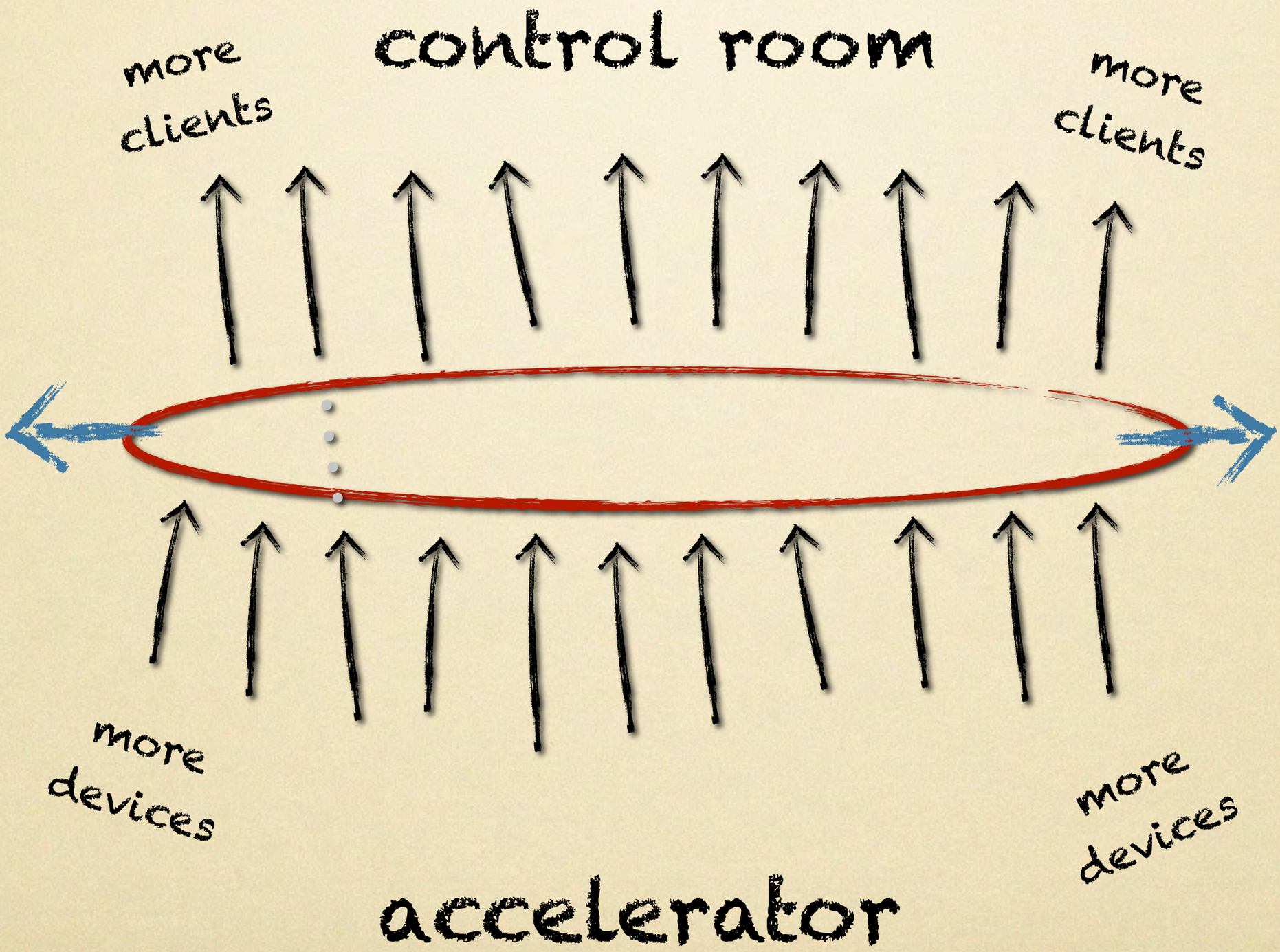


bottleneck ?

accelerator

the new paradigm:

(scalability eliminates bottleneck)



query db data

pull live data

commands

memcache

mongodb

write db data

push live data

meta-data server

orchestrator

Control Lib.

Control Unit

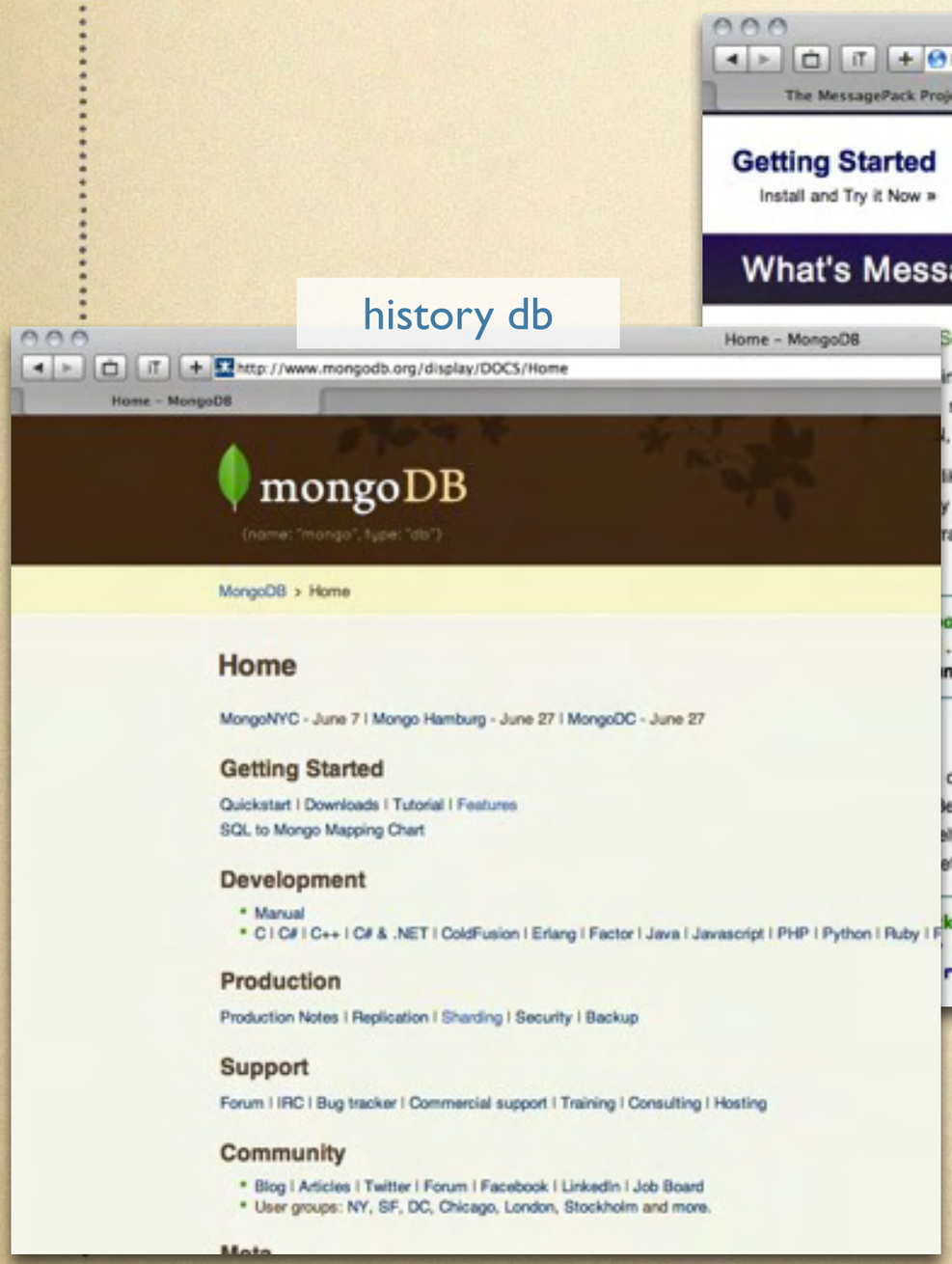
I/O channels

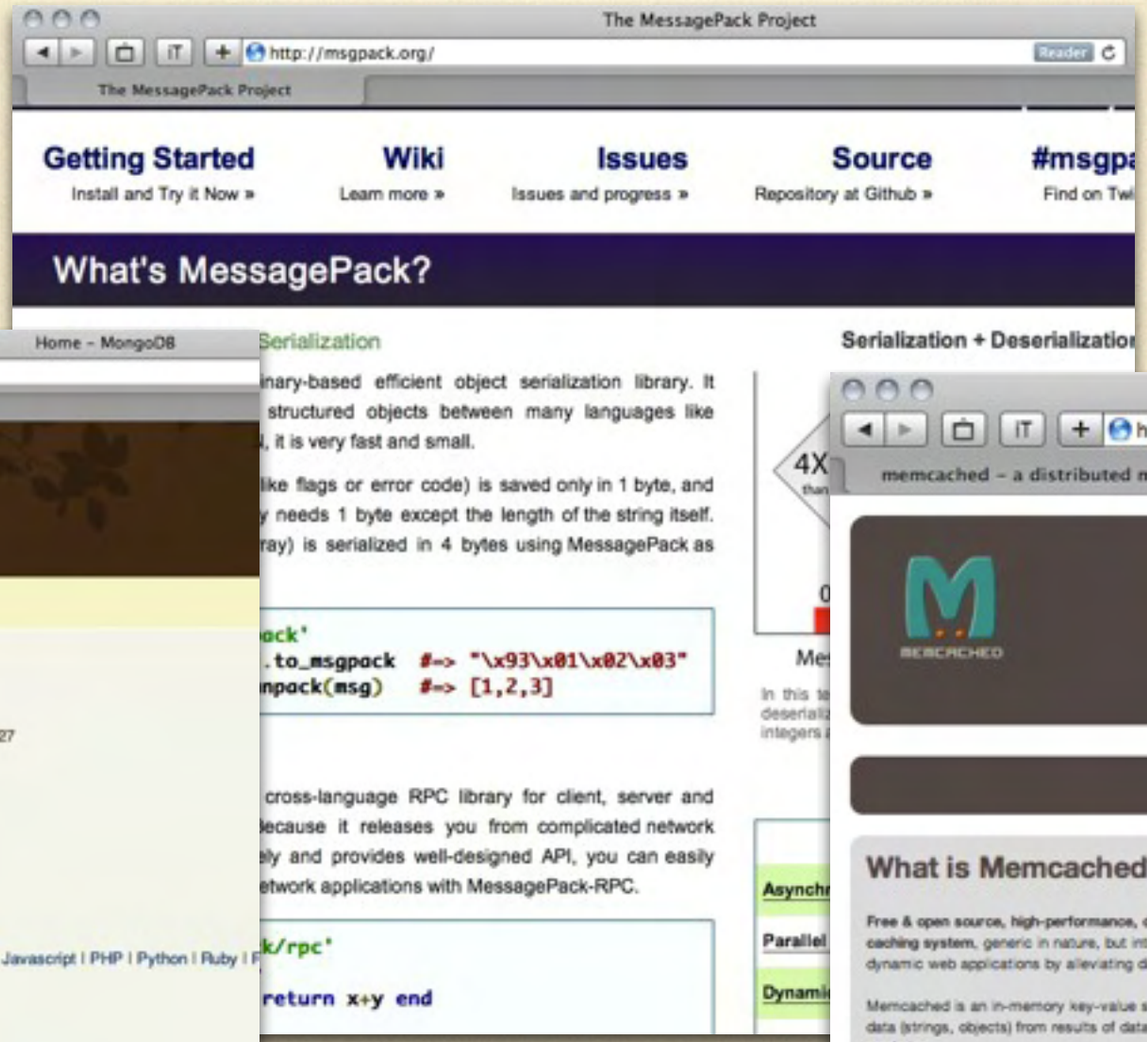
accelerator

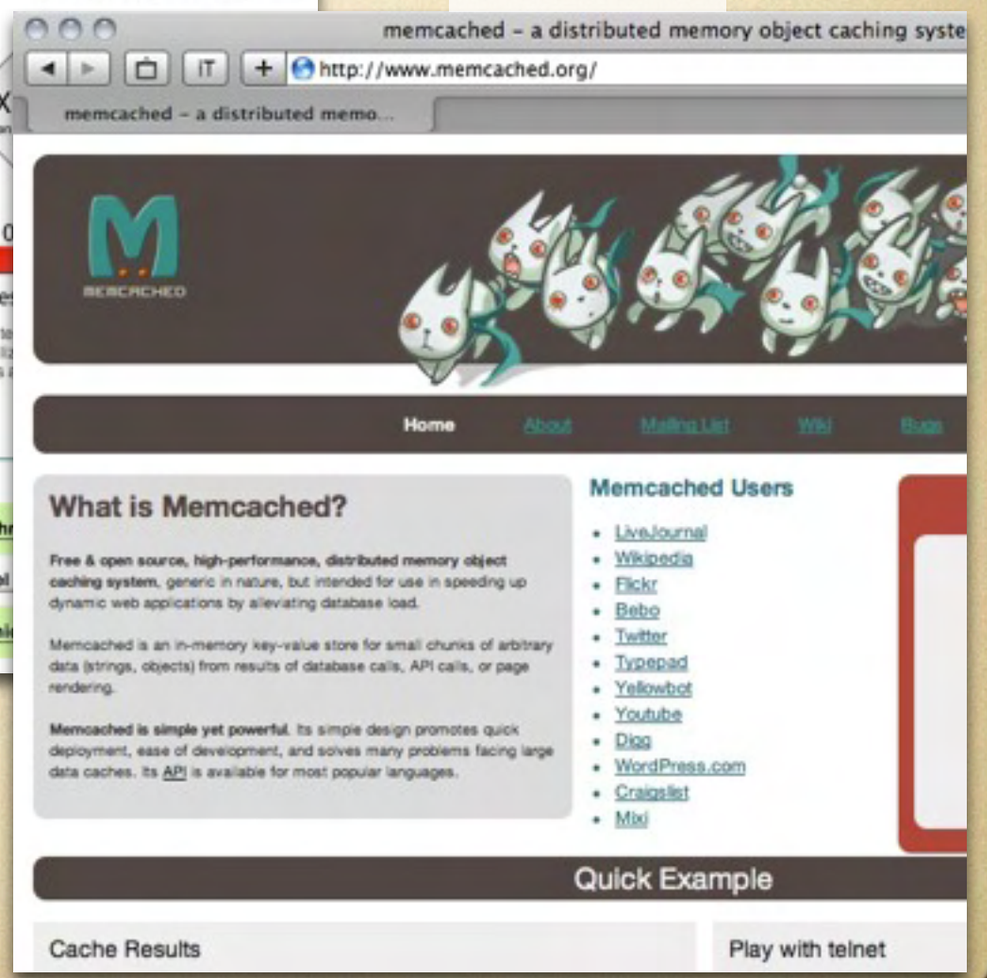
core services candidates

history db

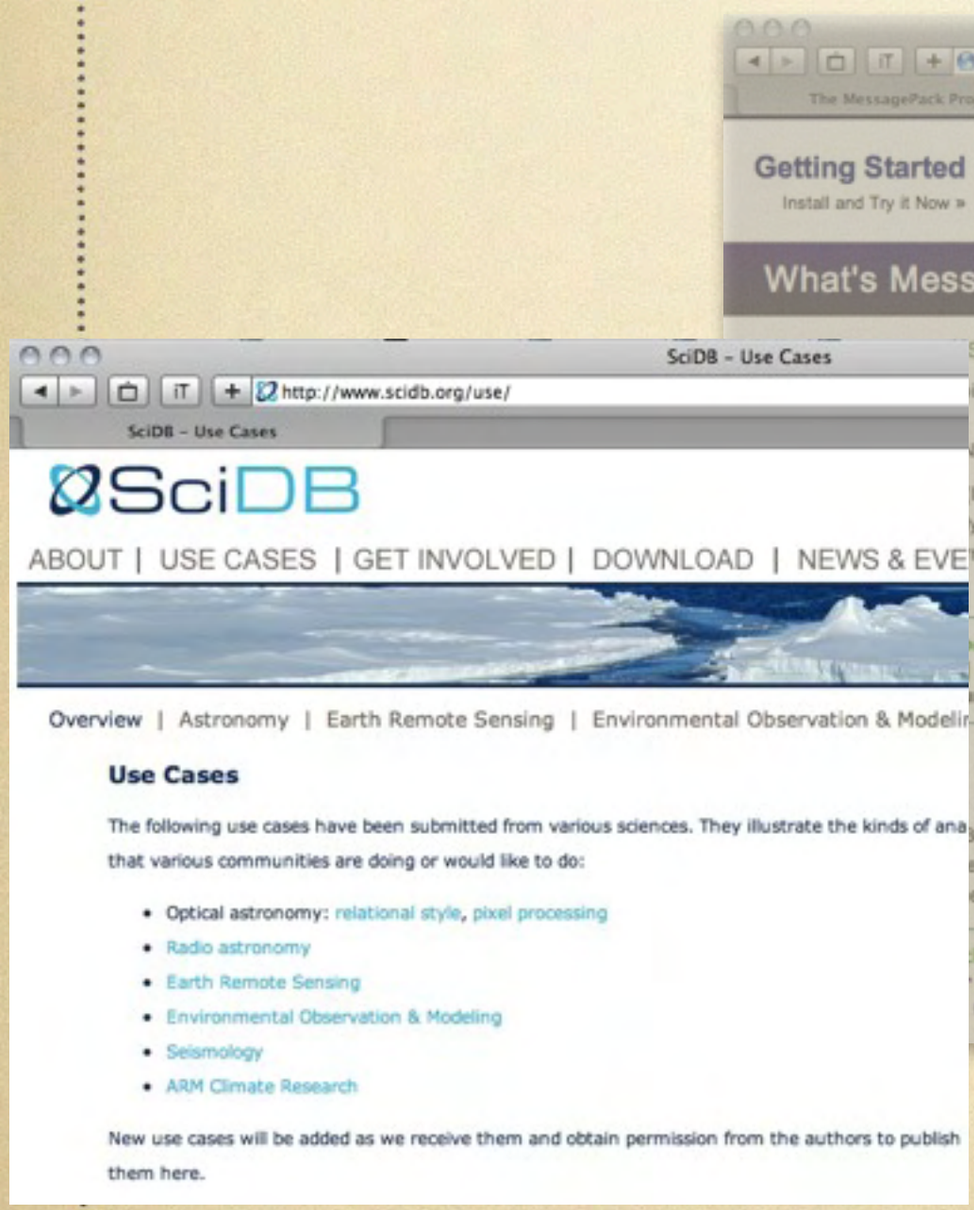
live data

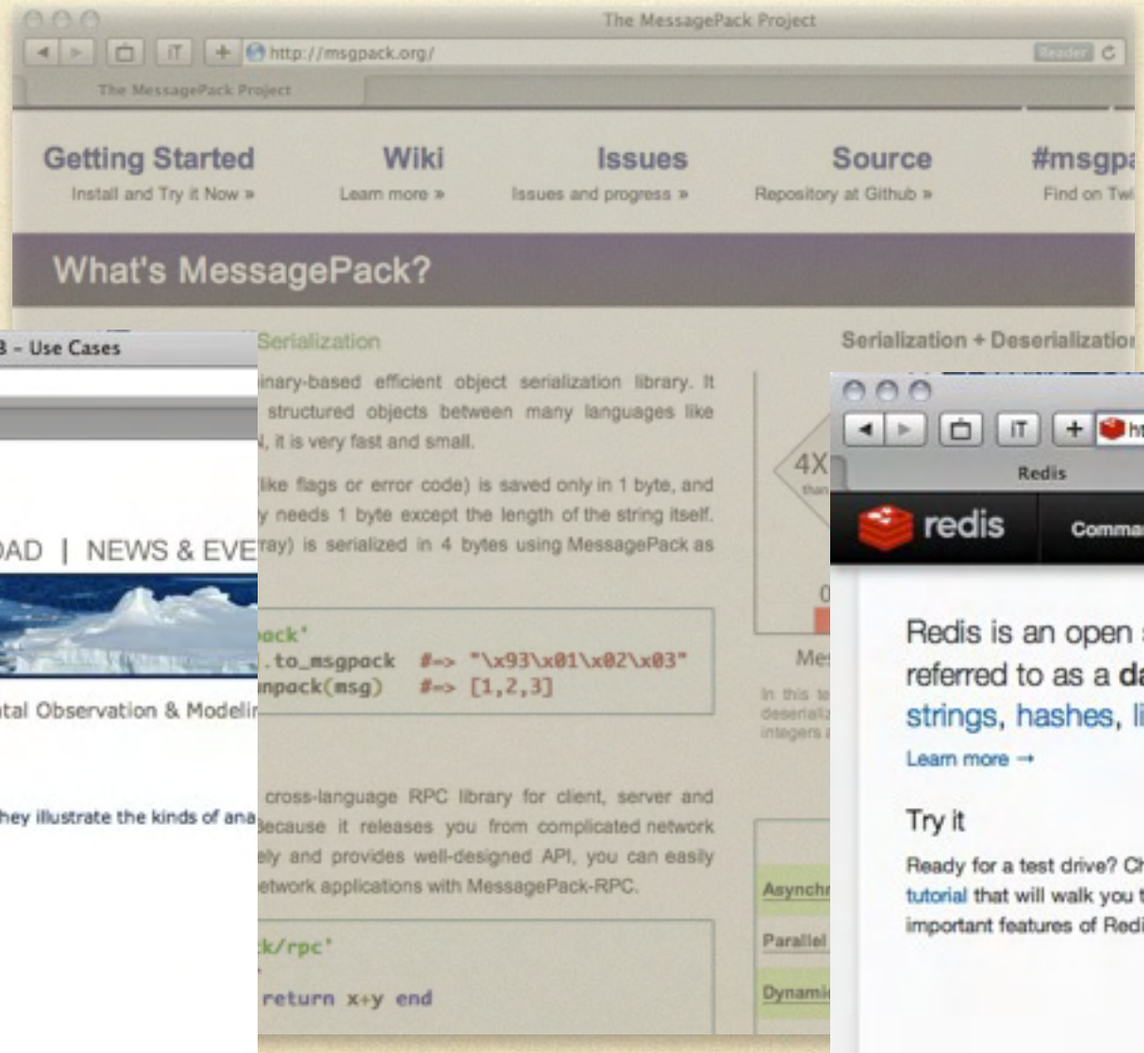


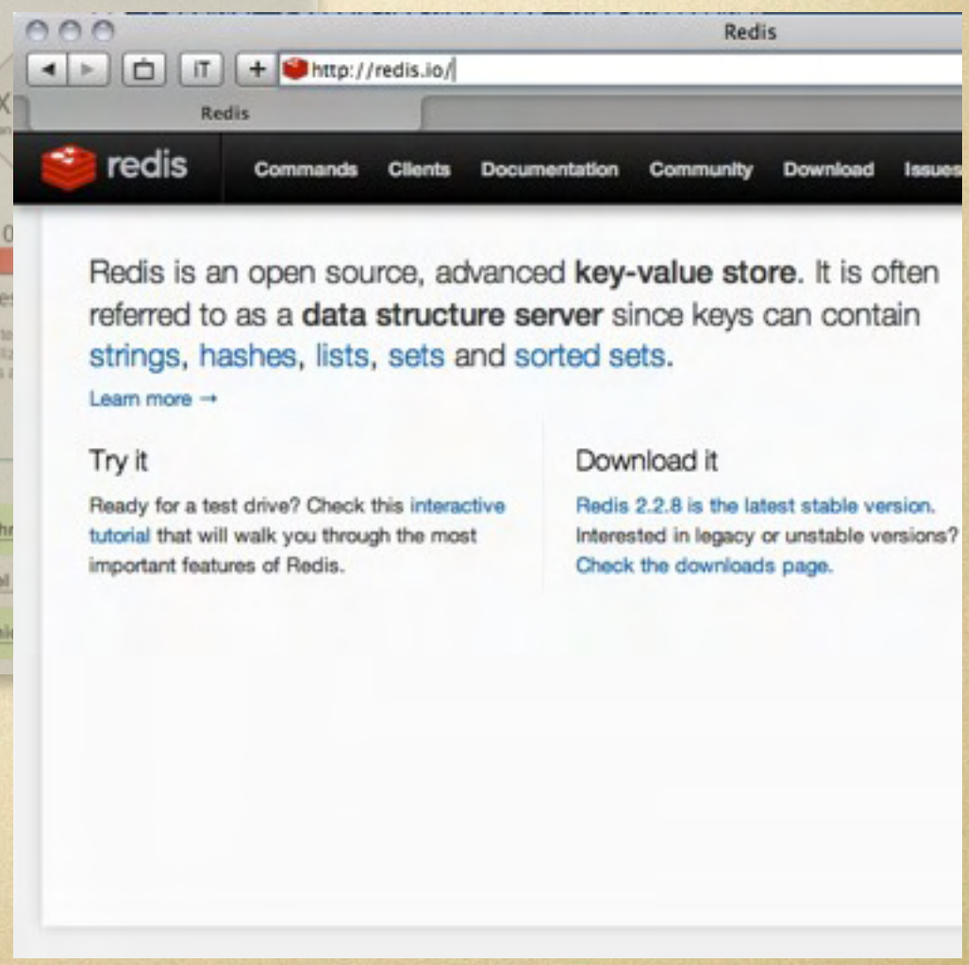




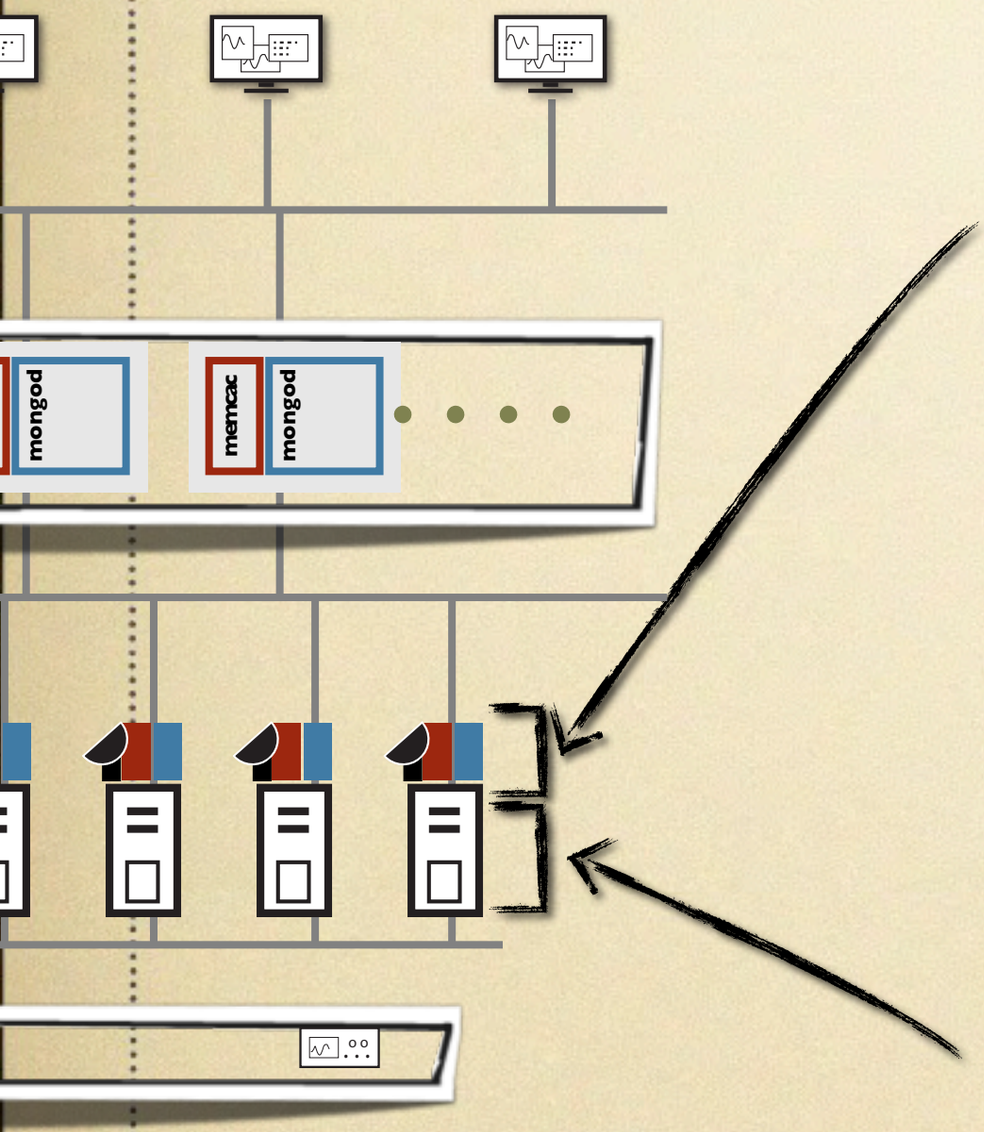
core services alternatives







Control Library e Control Unit

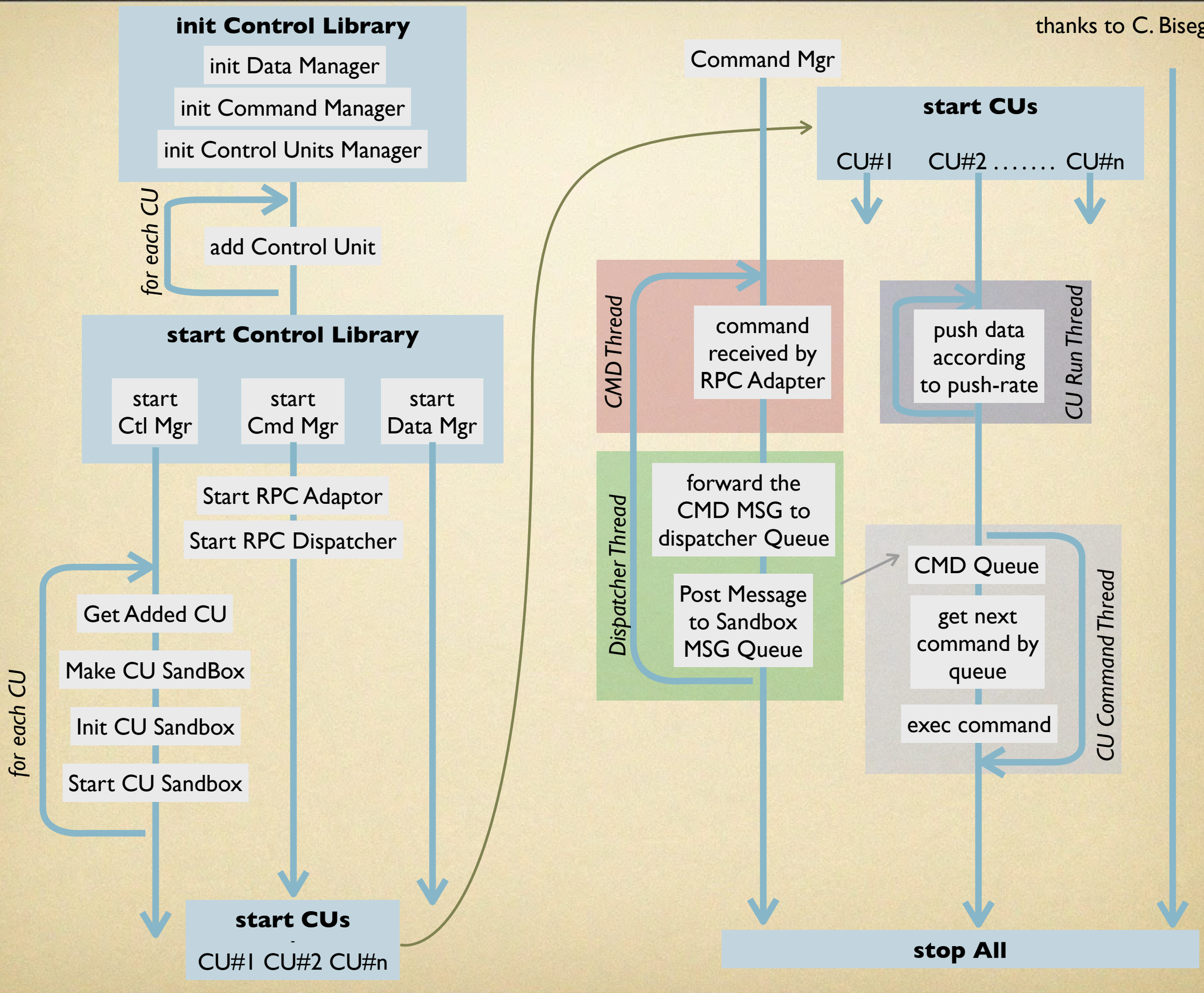


multi-threads

- The Control Library (CL) is the set of functions needed to hw-drivers developers for communicating with the CS. It allows:
  - managing configurations
  - writing data to Live and History
  - Commands dispatching & handling

- Each Control Unit employ the CL to export to the CS an accelerator component or a family thereof.

thanks to C. Bisegni



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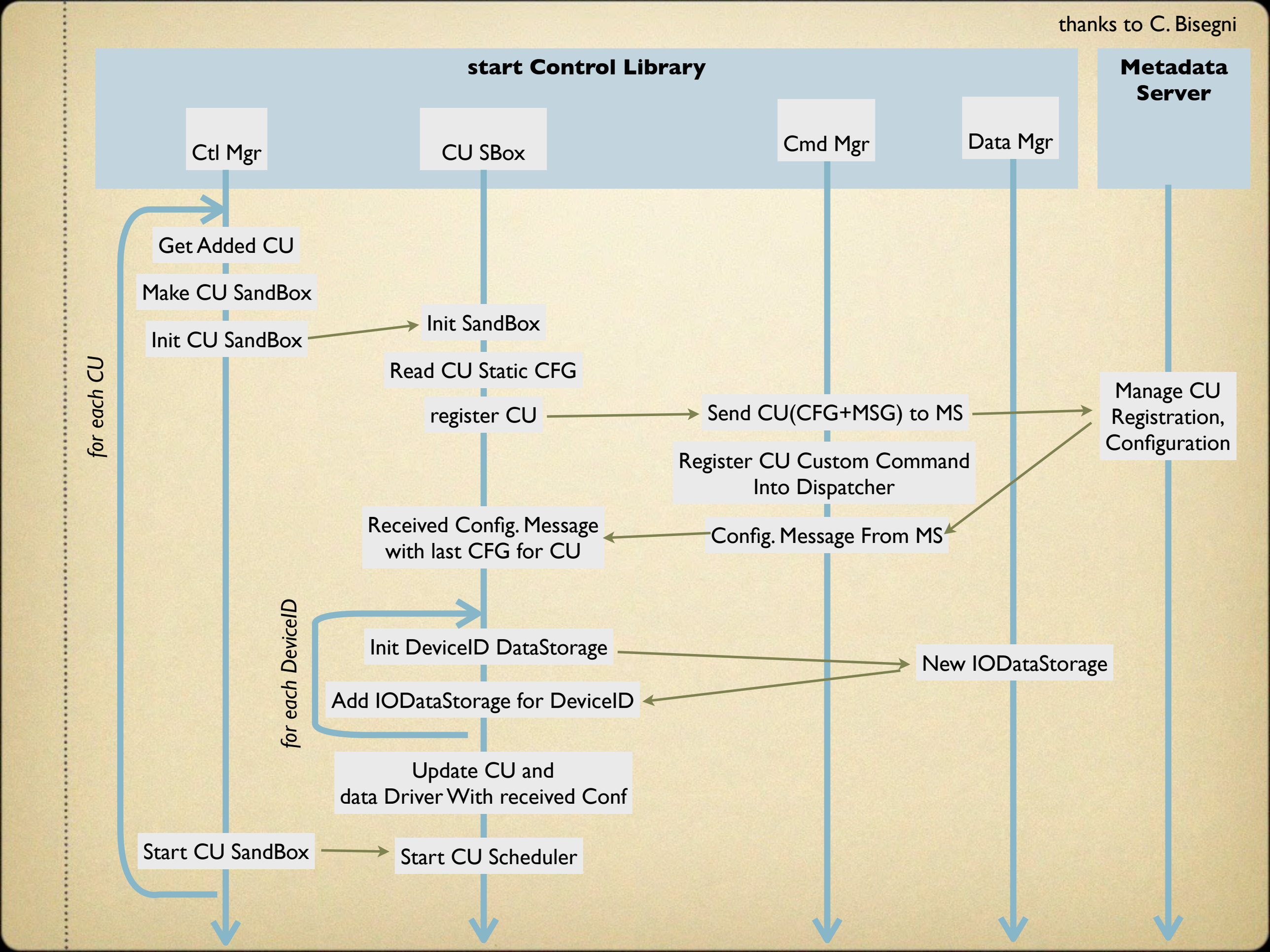
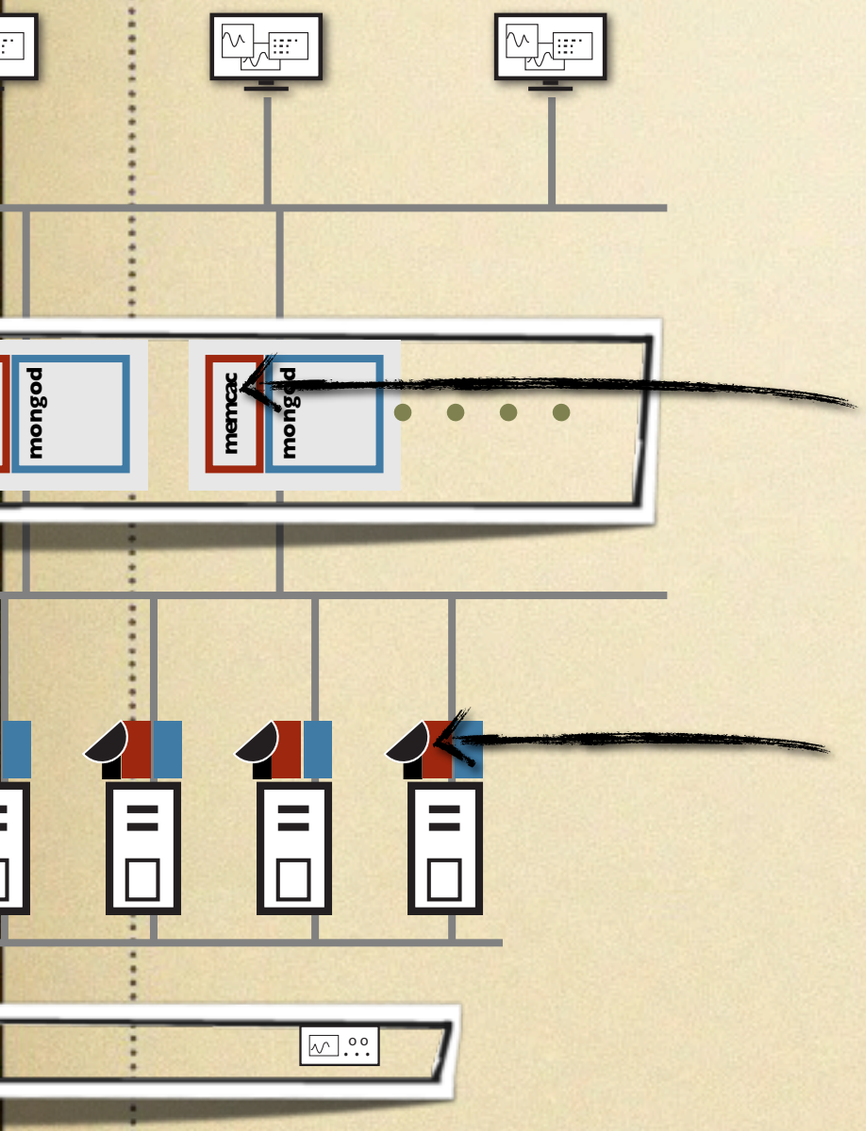


Live data



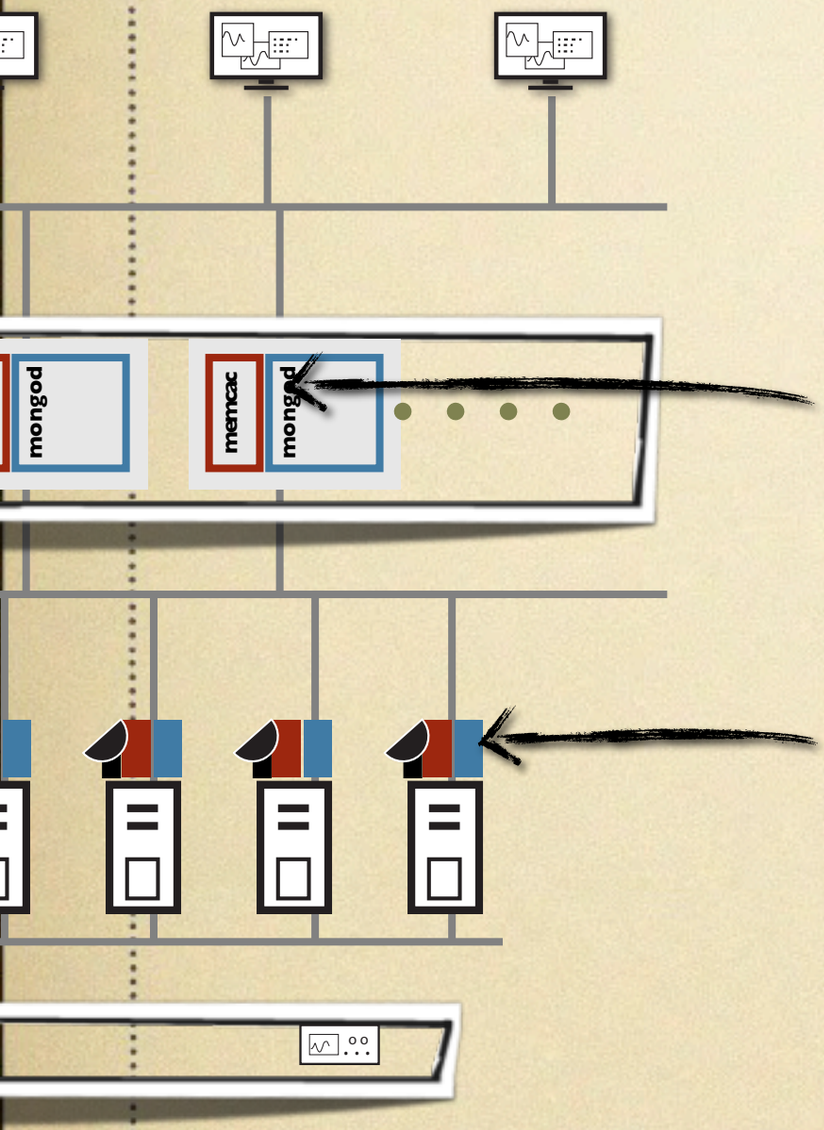
- Allows high-performance caching of data produced by any component managed by CS.

- one *key* per data (a single "container" continuously updated

r/w of a value
subset now available !

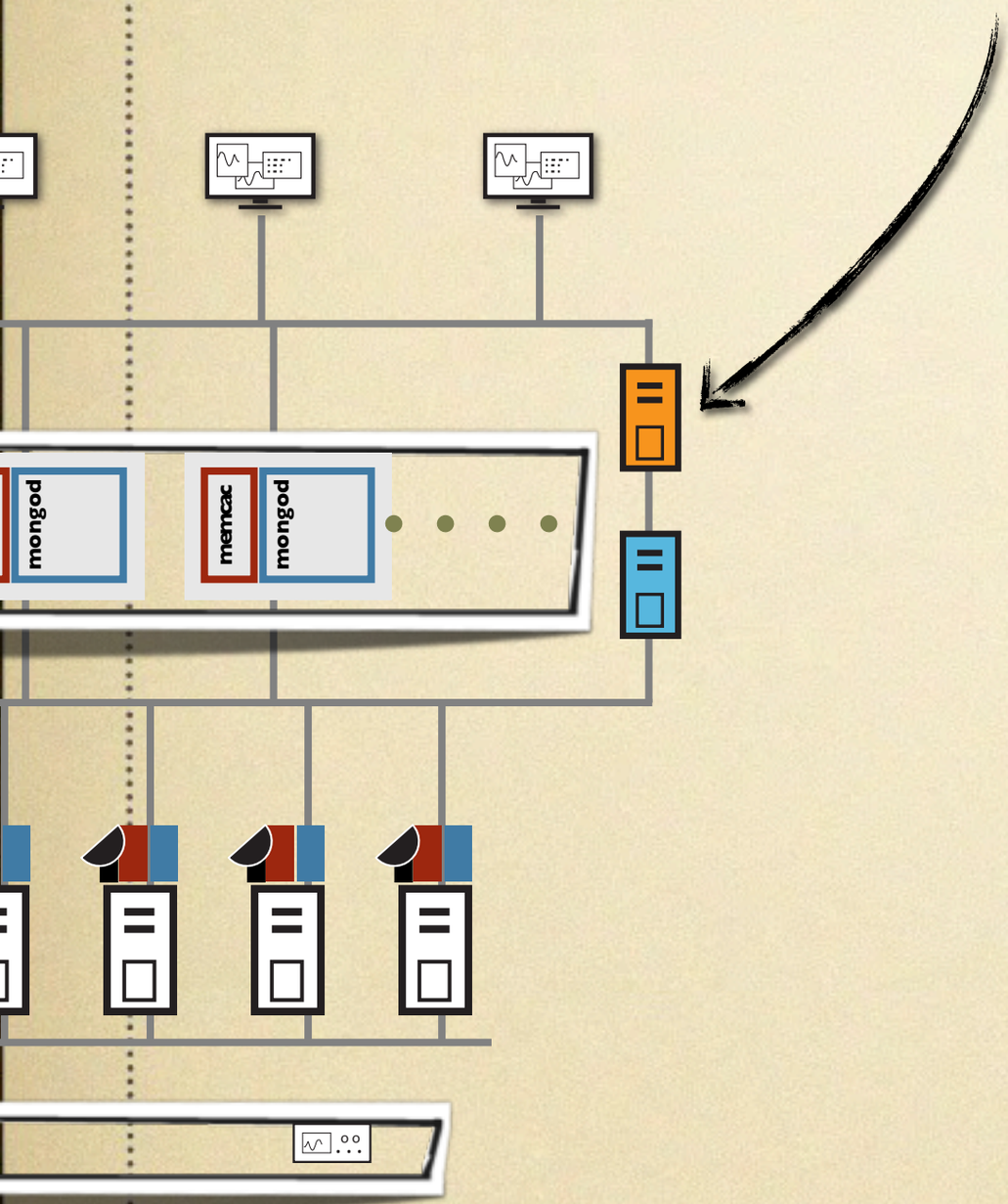
- dynamical *keys* re-distribution allows automatic failover by redirecting to other servers the load of failed one.
- Scalability is also guaranteed by the same feature

History data



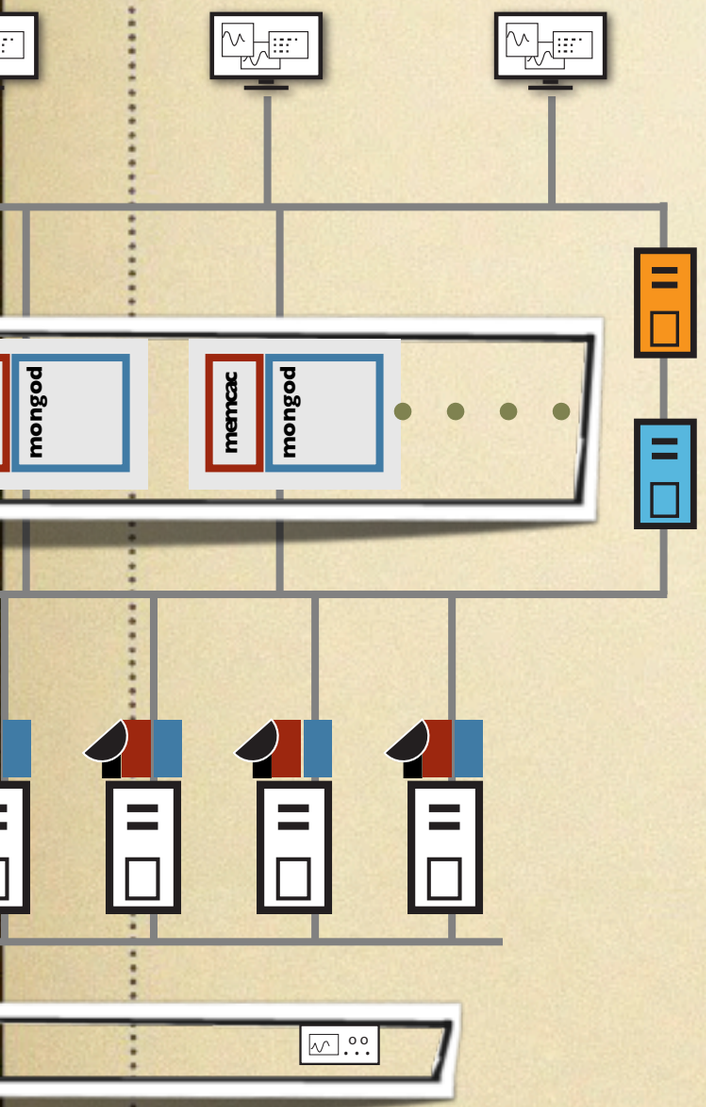
- *key/value* non-relational database
- scalability and load balancing by *sharding*
- fast record writing (simpler structure because it doesn't use tables)
- fast queries on primary keys
- (fast) parallel search on cluster nodes

Metadata Server



- CU configuration manager
  (e.g. managing of pushing data rate)
- Semantic of data (e.g. db records structure)
- Command's list and semantic
- Naming service

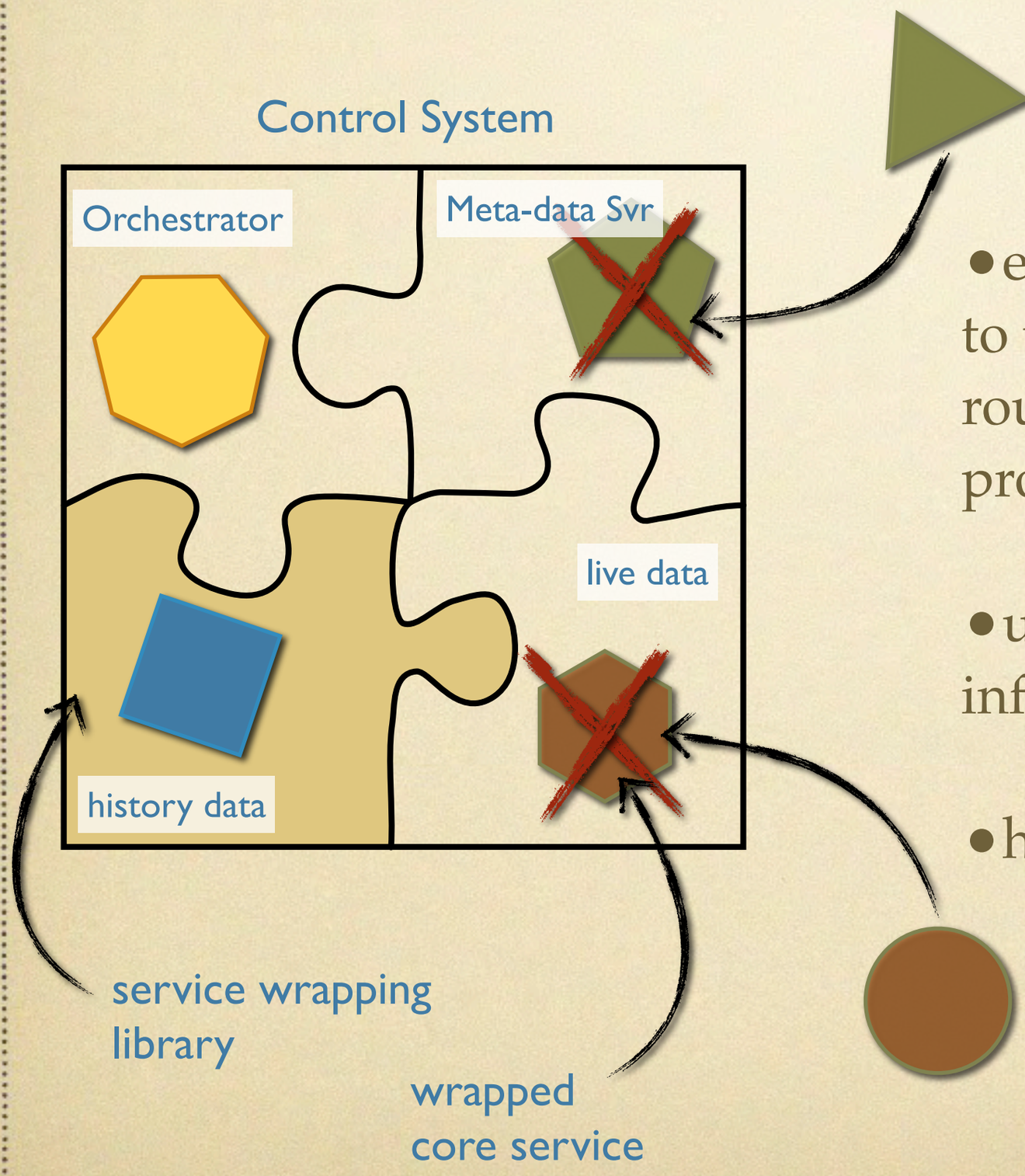
Orchestrator



- Provides middle-layer services, e.g. locking of CUs to prevent command conflicts

- multi-CUs commands, e.g.
  - global set-points save/restore
  - software feedback
  - on-line measurements
  - ...

Abstraction of components

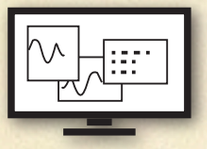


- each service isn't directly offered to users; glueing and wrapping routines will be developed to provide an high level of abstraction

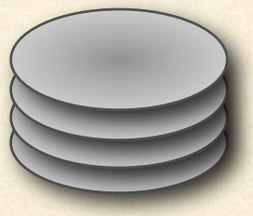
- updates of core services doesn't influence the user applications

- higher flexibility in defining API

pull live data

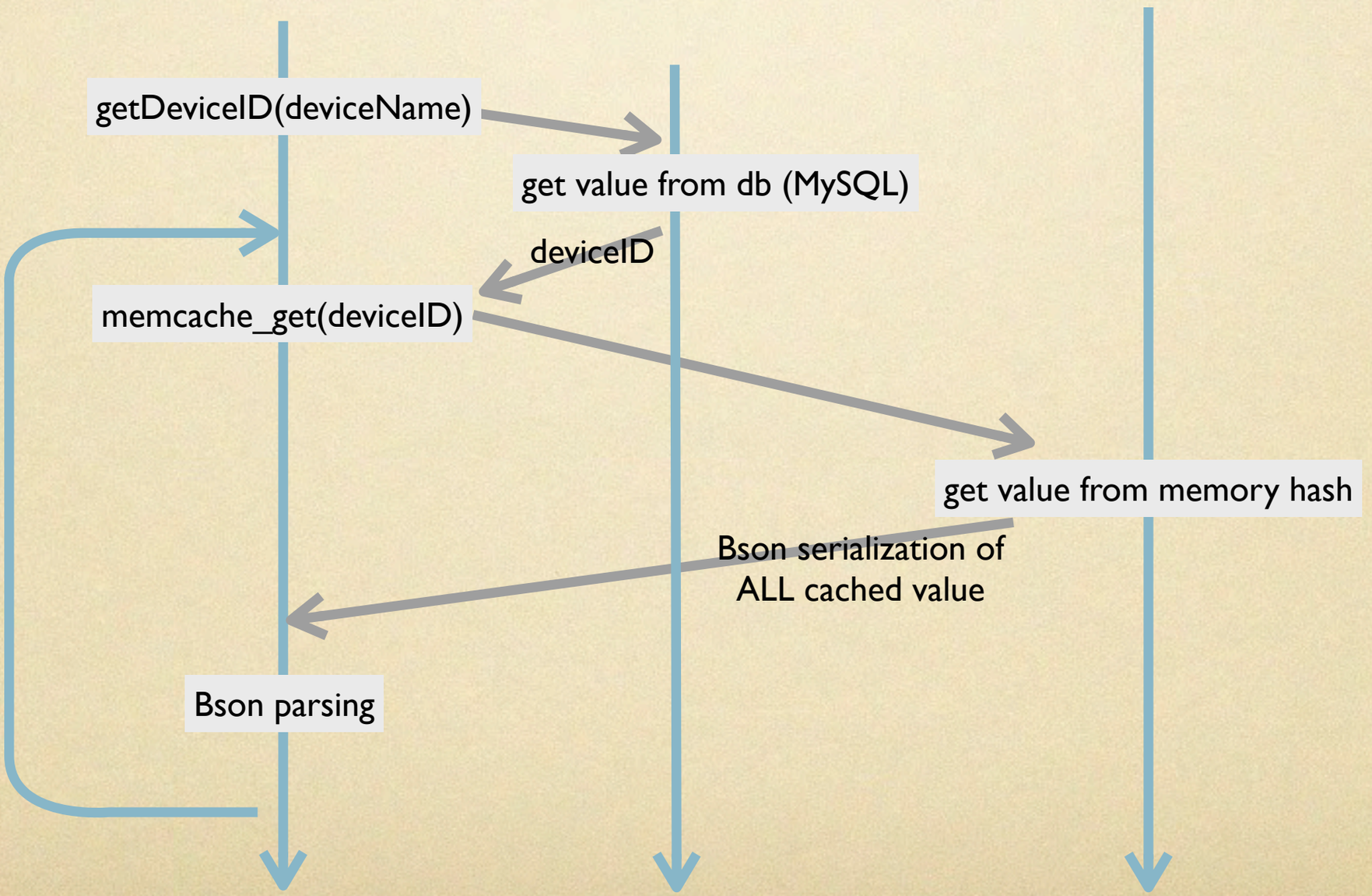


client

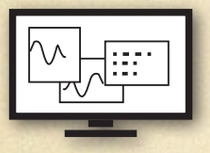


meta-data server

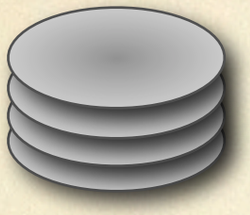
live data server



send command



client

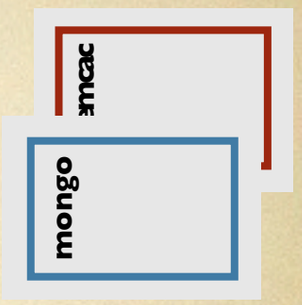


meta-data server

Control Unit Host

Control Library

Control Unit



getDeviceSocket(deviceName)

build Command

get value from db (e.g. MySQL)

device socket

send Command

detect CU

command

msg received

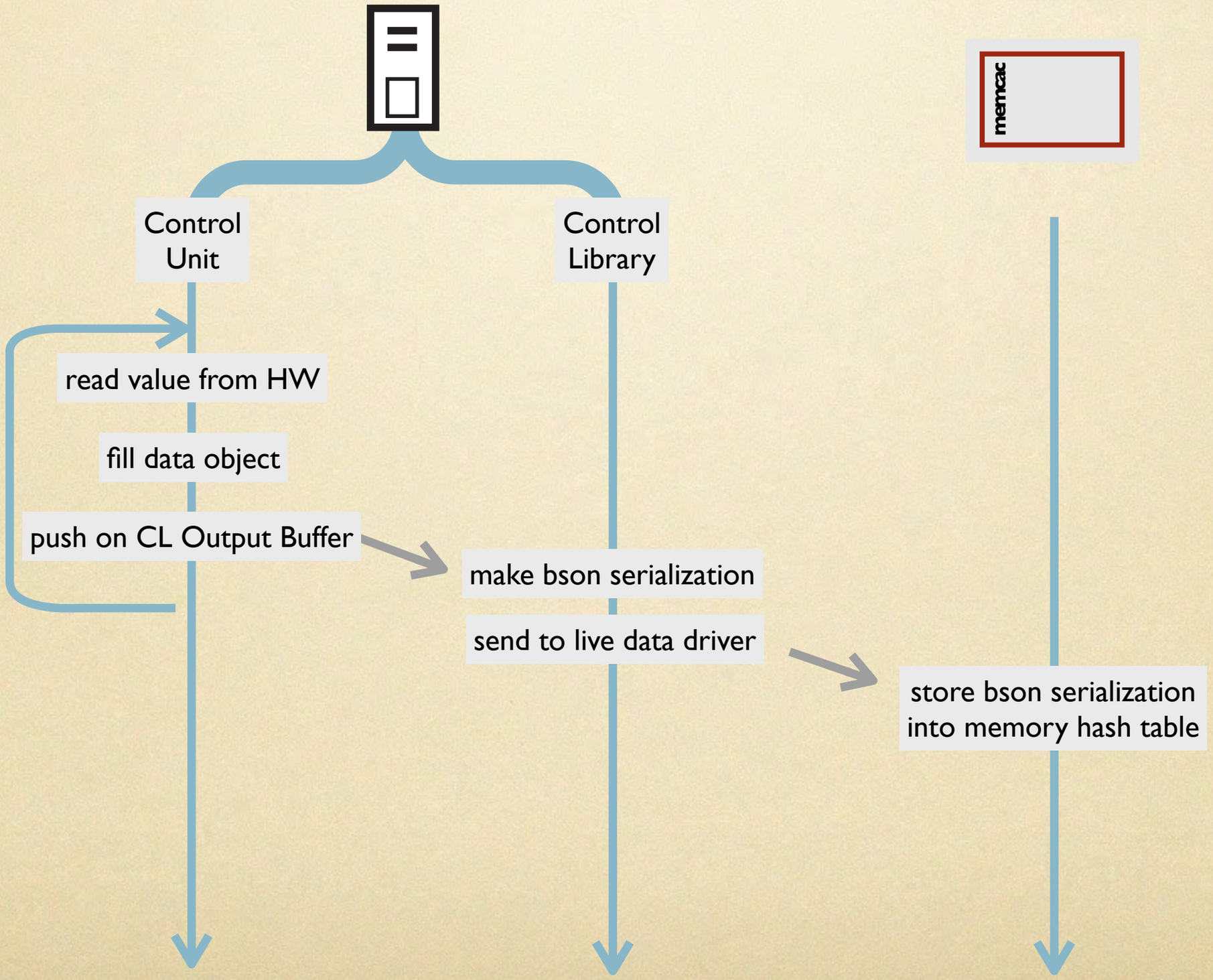
(....)

exec

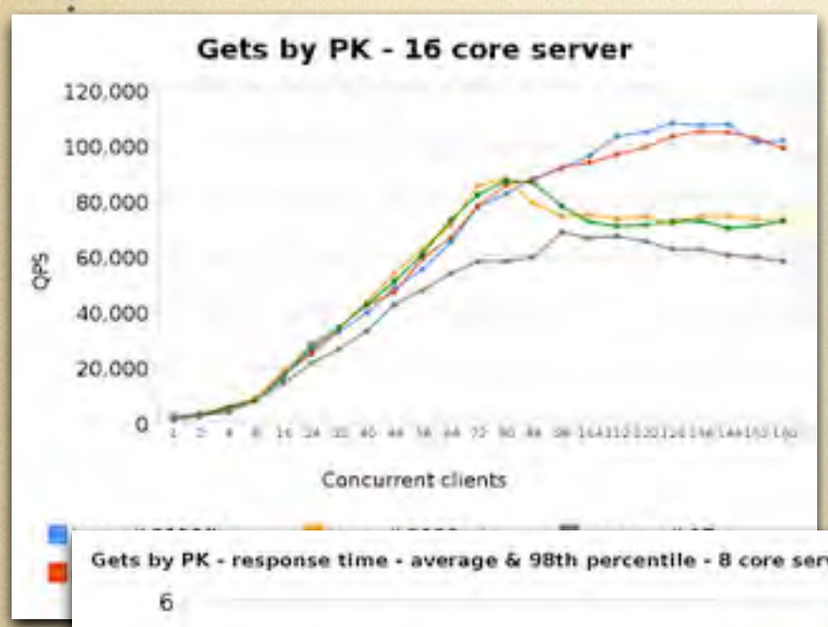
message dispatched

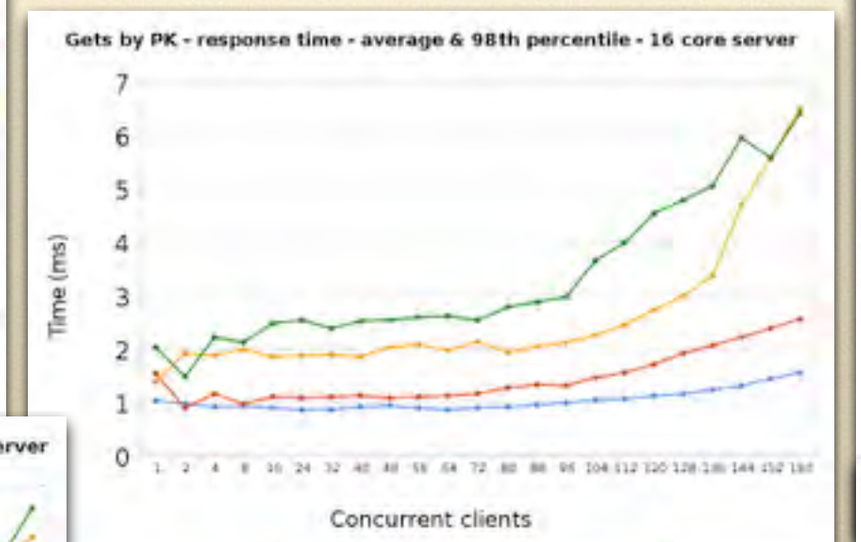
increase live&hst
refresh rate during
message execution

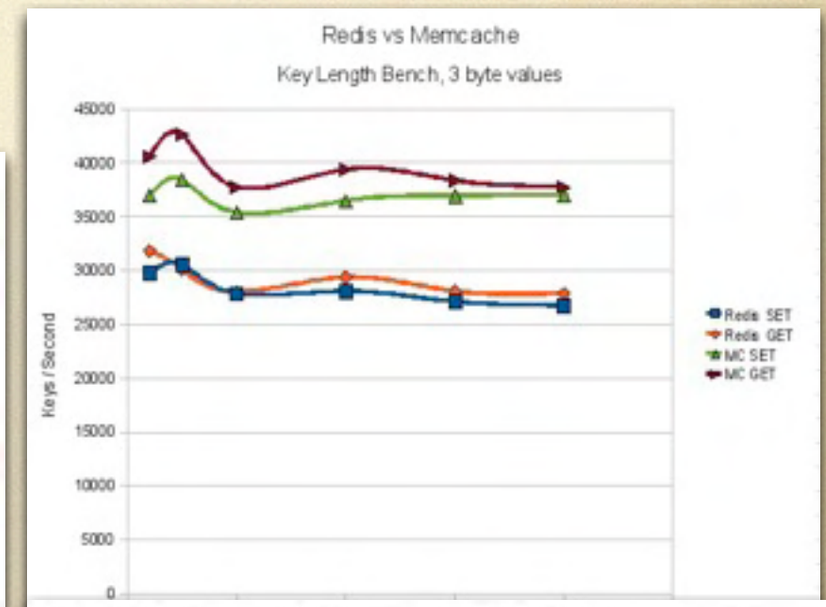
push live data

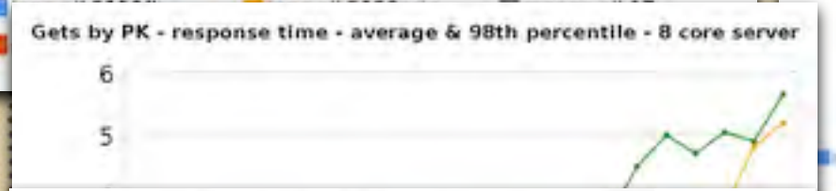


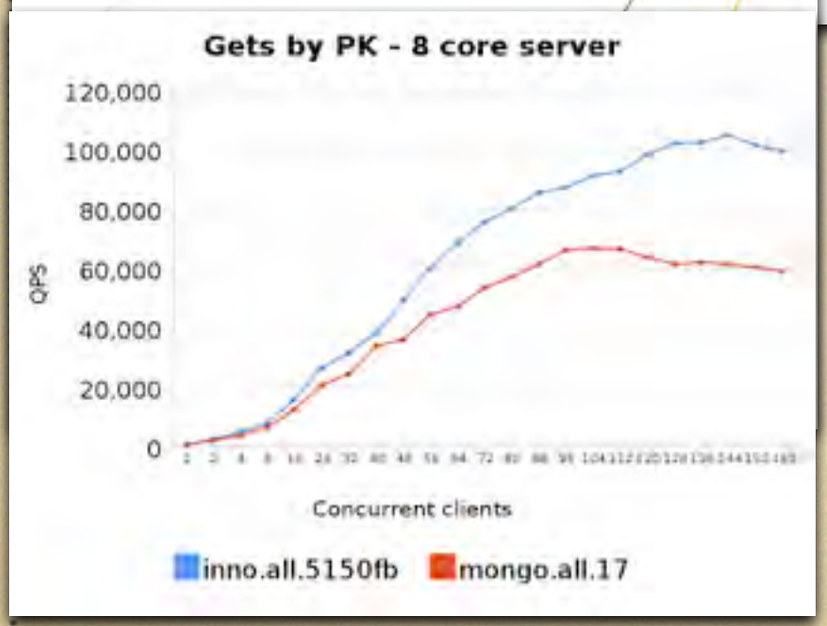
memcached performance

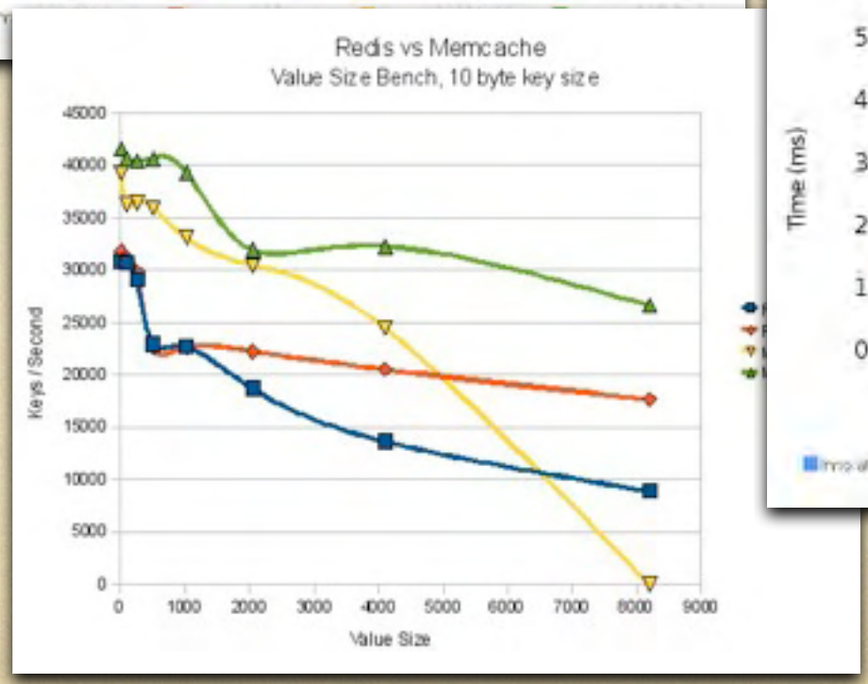


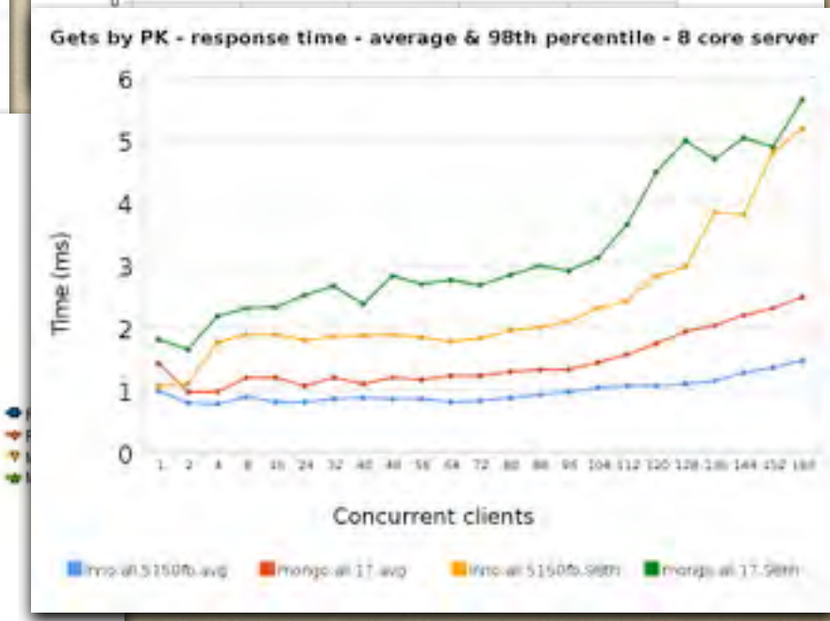






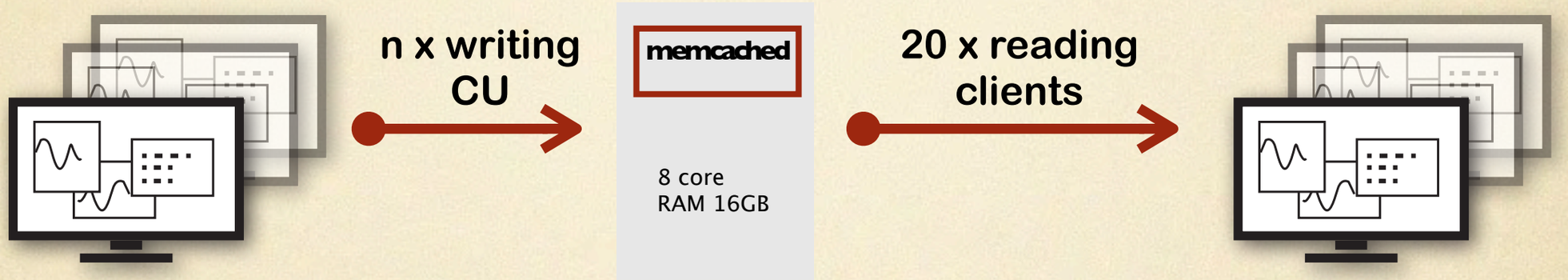






thanks to C.Bisegni/F.Zani

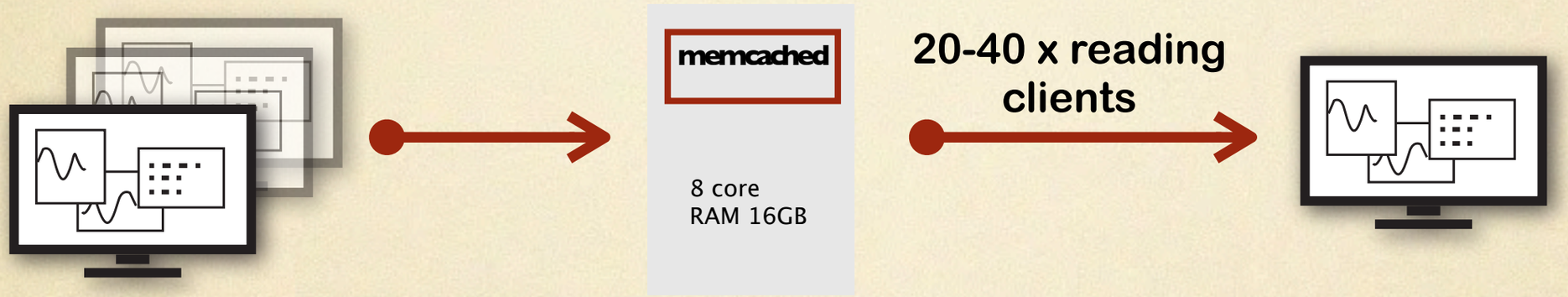
test#3.1



writing every... (msec)	#CU (Write)	#clients (Read)	#servers	#processes/ server	CPU load (%)
20	60	20	1	1	3-5
20	80	20	1	1	4-6
20	80	20	2	1	2-3
50	60	20	1	1	1-3
50	80	20	2	1	0-2
100	60	20	1	1	?
100	80	20	2	1	?

thanks to C.Bisegni/F.Zani

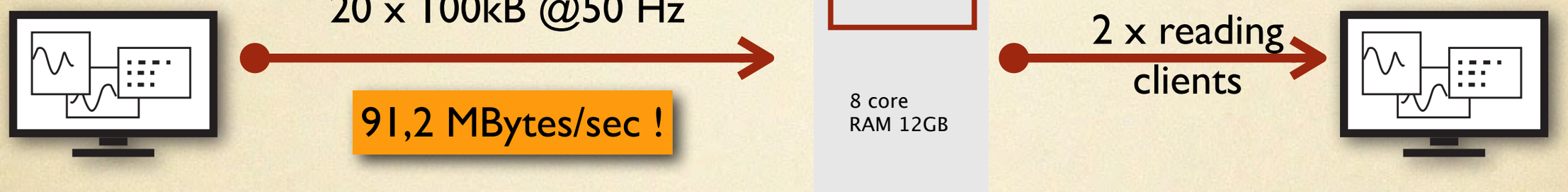
test#3.2

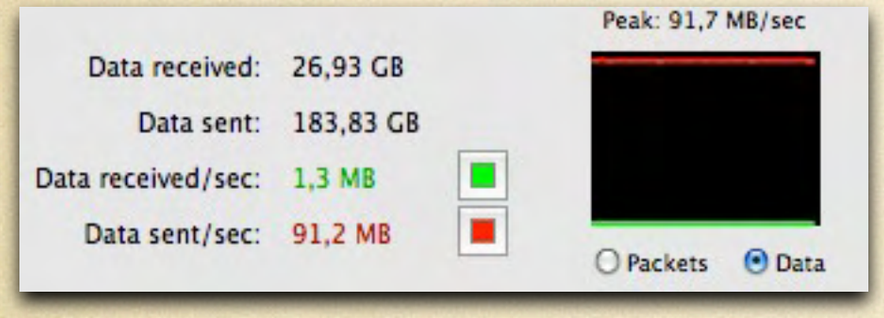


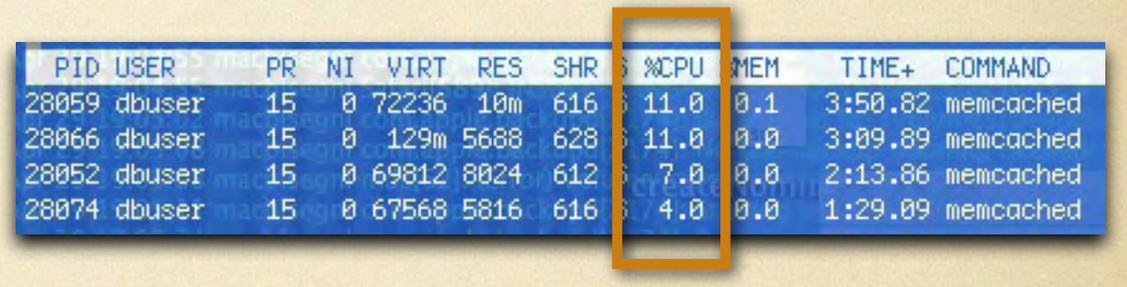
writing every... (msec)	#CU (Write)	#clients (Read)	#servers	#processes/ server	CPU load (%)
20	80	20	1	4 (1 per core)	2-3
20	80	40	1	4 (1 per core)	2-3
		40	1	4 (1 per core)	0

thanks to C.Bisegni/F.Zani

test#4

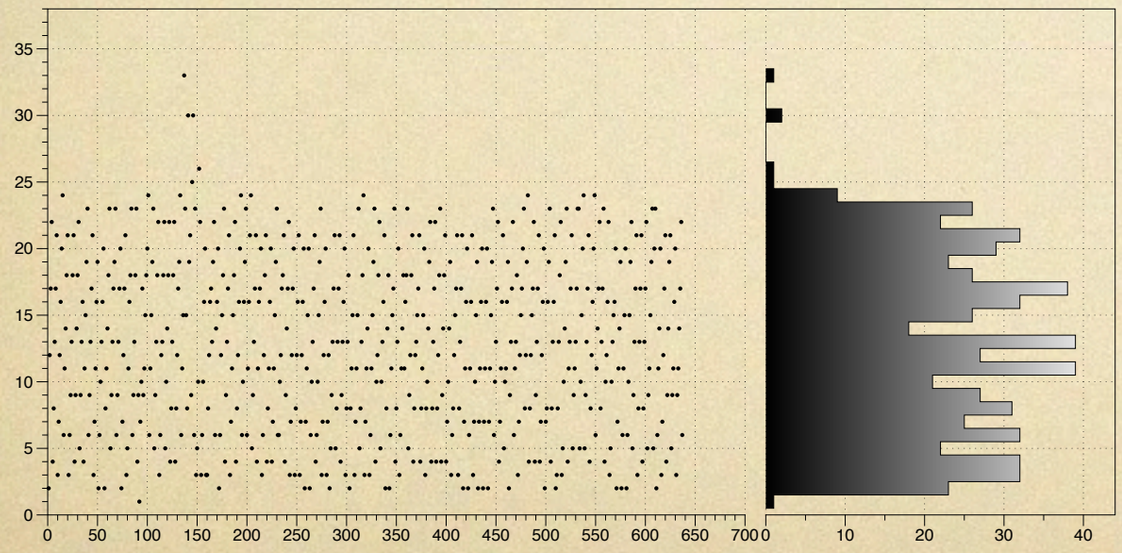




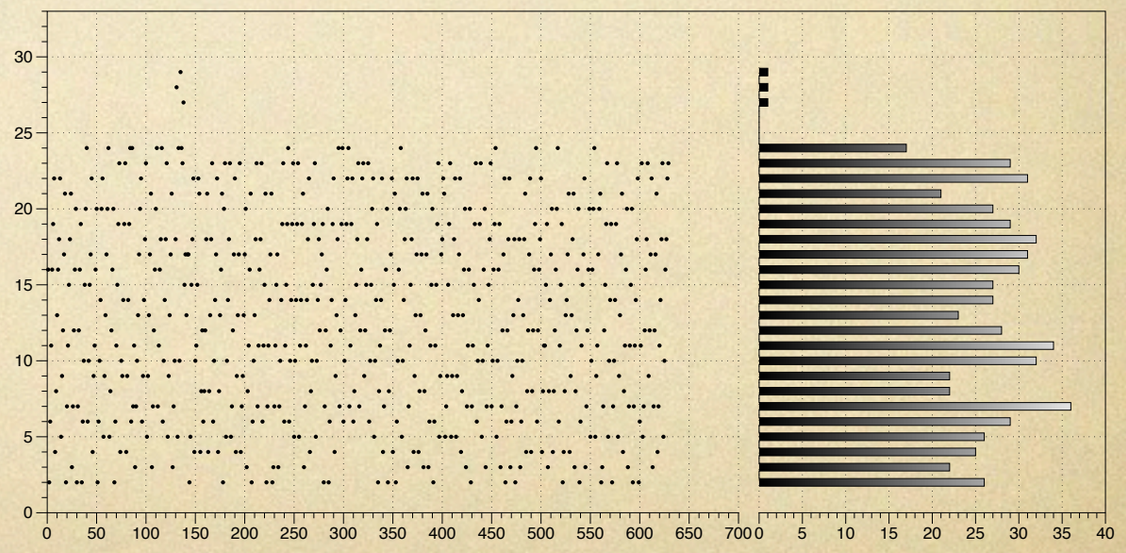


PID	USER	PR	NI	VIRT	RES	SHR	%CPU	%MEM	TIME+	COMMAND
28059	dbuser	15	0	72236	10m	616	11.0	0.1	3:50.82	memcached
28066	dbuser	15	0	129m	5688	628	11.0	0.0	3:09.89	memcached
28052	dbuser	15	0	69812	8024	612	7.0	0.0	2:13.86	memcached
28074	dbuser	15	0	67568	5816	616	4.0	0.0	1:29.09	memcached

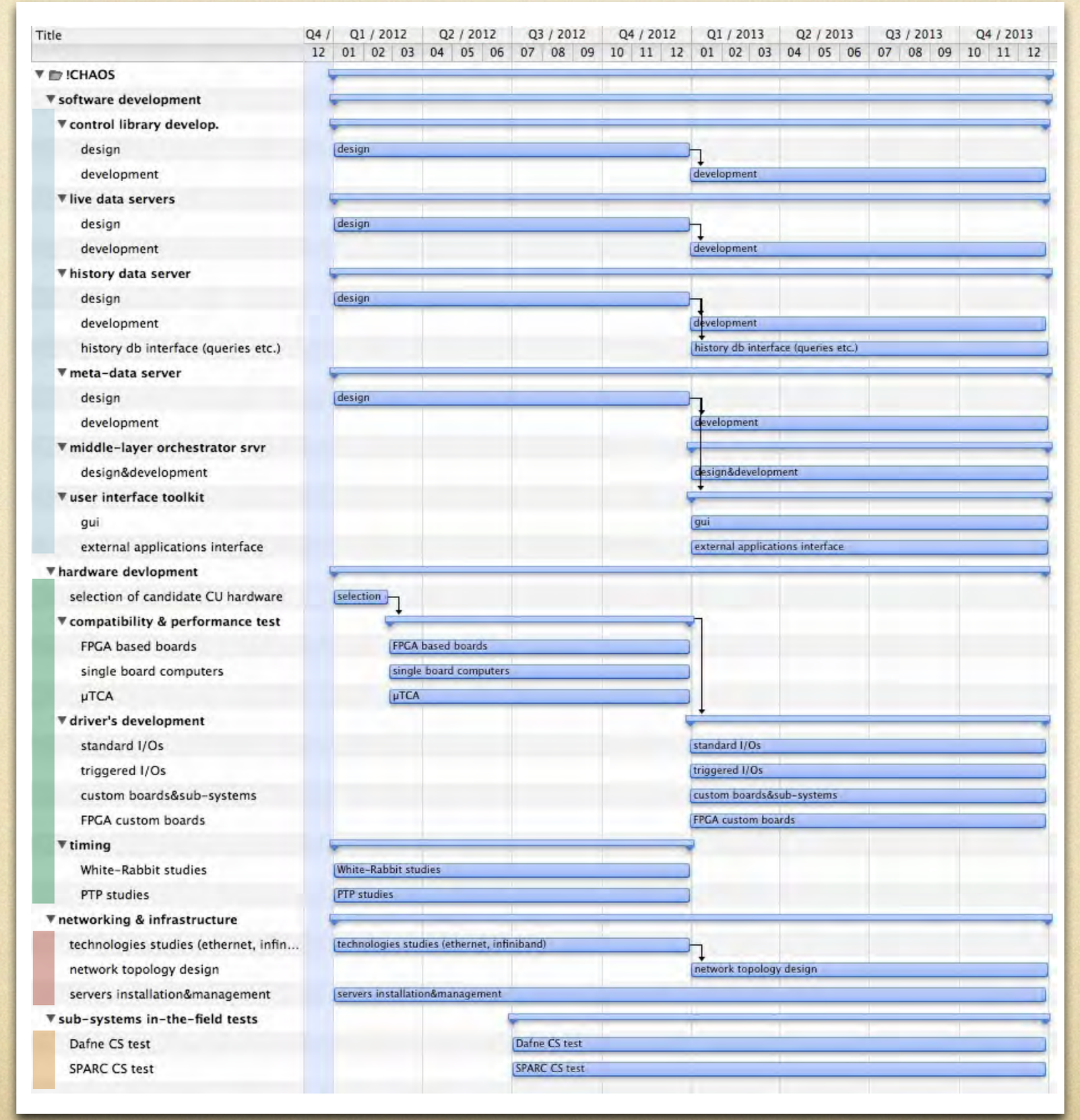
s4_hardware1_w20_m20_buff100000_rd10.log



s4_hardware1_w20_m20_buff100000_rd12.log



The !CHAOS R&D activity



conclusions and future plans

motivated by the preliminary results and consistency of the overall design:

- start an R&D activity (funded by INFN CSN5) for completing system design and continue performance and stress tests of components
- continue tests on the field by adding CS components to Dafne&SPARC prototypes
- finalize the project as a candidate for the SuperB Control and DAQ System
- evaluate costs, man power and define time schedule

!CHAOS

Memcached functional tests in two real contexts: the DAFNE Control System and the SPARC Control System

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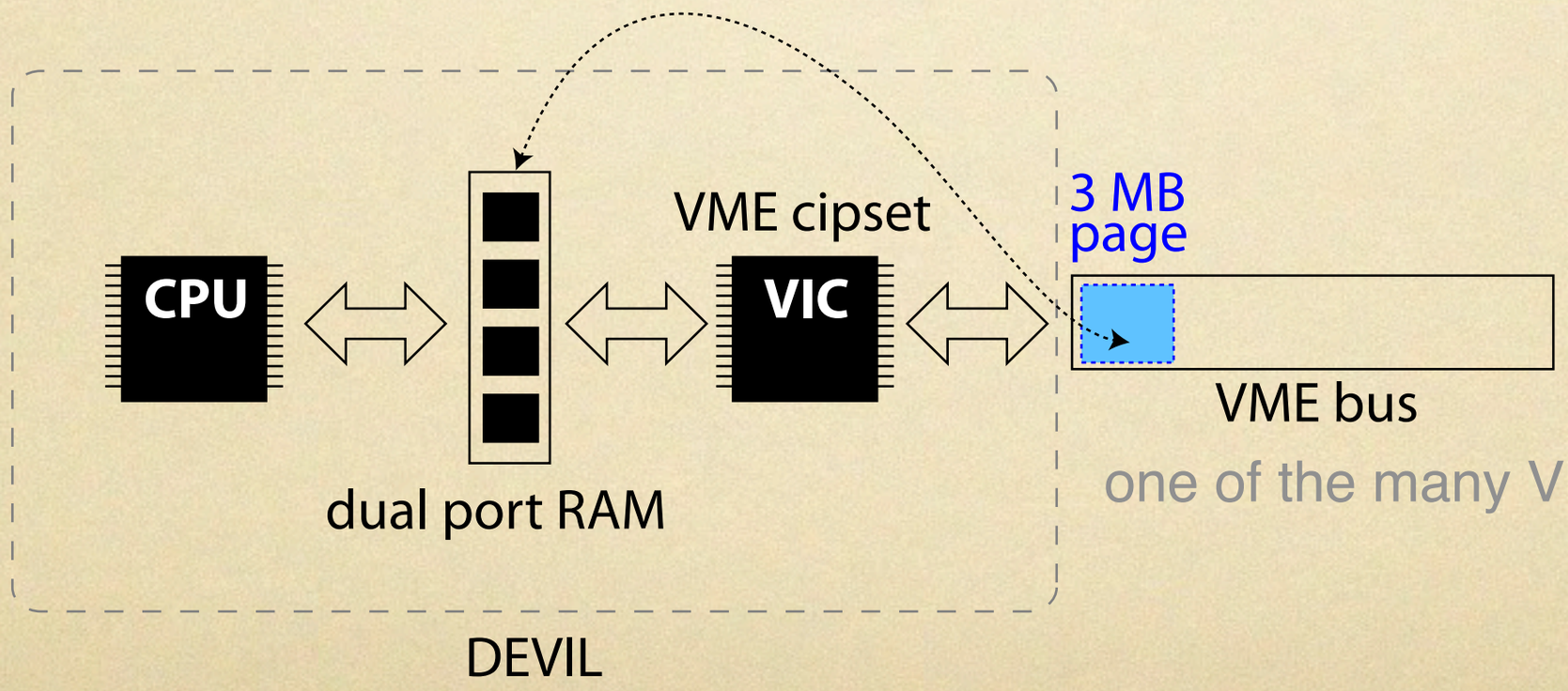
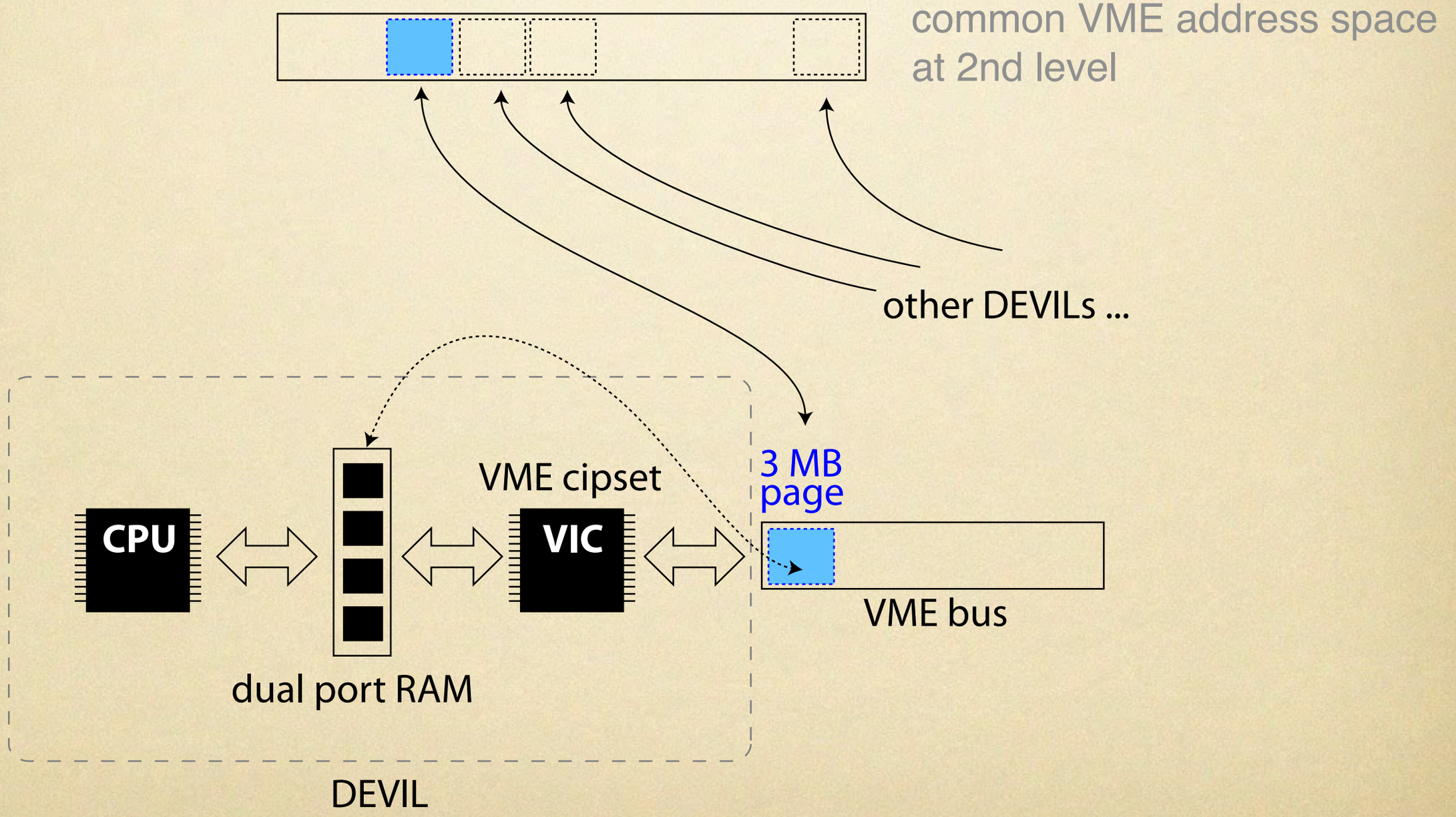
L. Foggetta	*LAL / INFN - LNF*
G. Mazzitelli	*INFN - LNF*
F. Zani	*INFN Roma-TV*

The DAFNE Control System relies on many distributed VME embedded processors (the 3rd level)

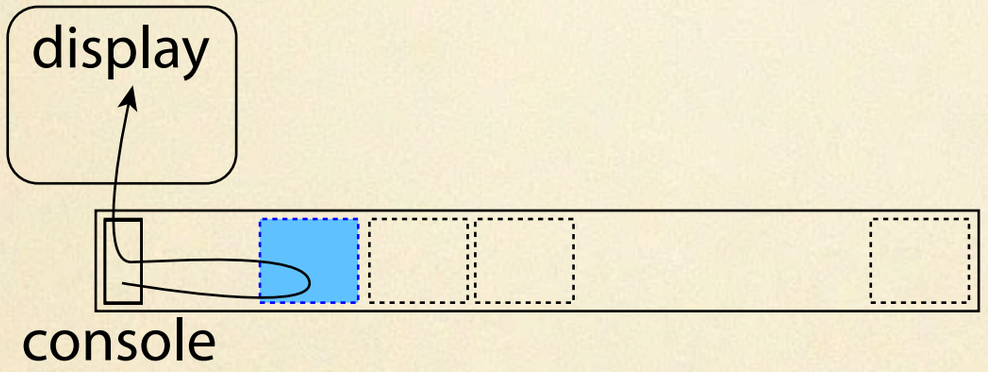


one of the many VME bus at 3rd level

Employing many point-to-point VME optical links, all the distributed processors contribute, with theirs RAMs, to the constitution of a common VME address space (the 2nd level)...

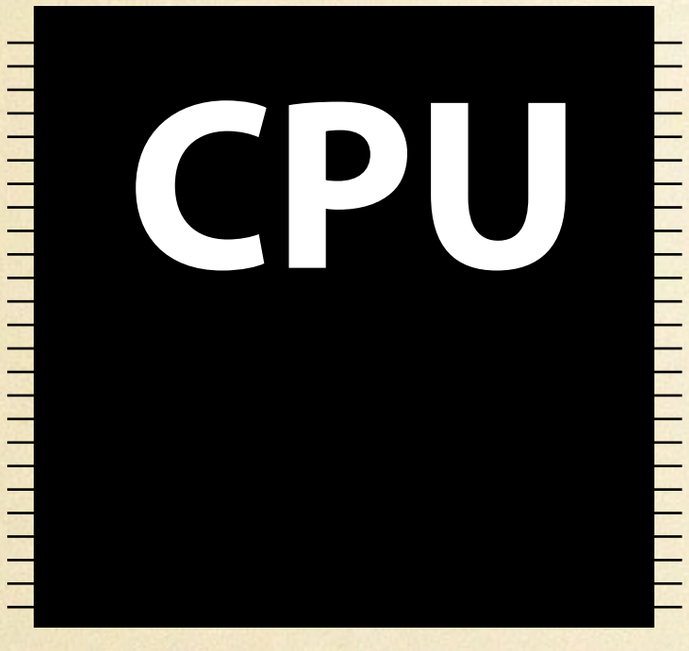


... that is available to the console applications (the 1st level)

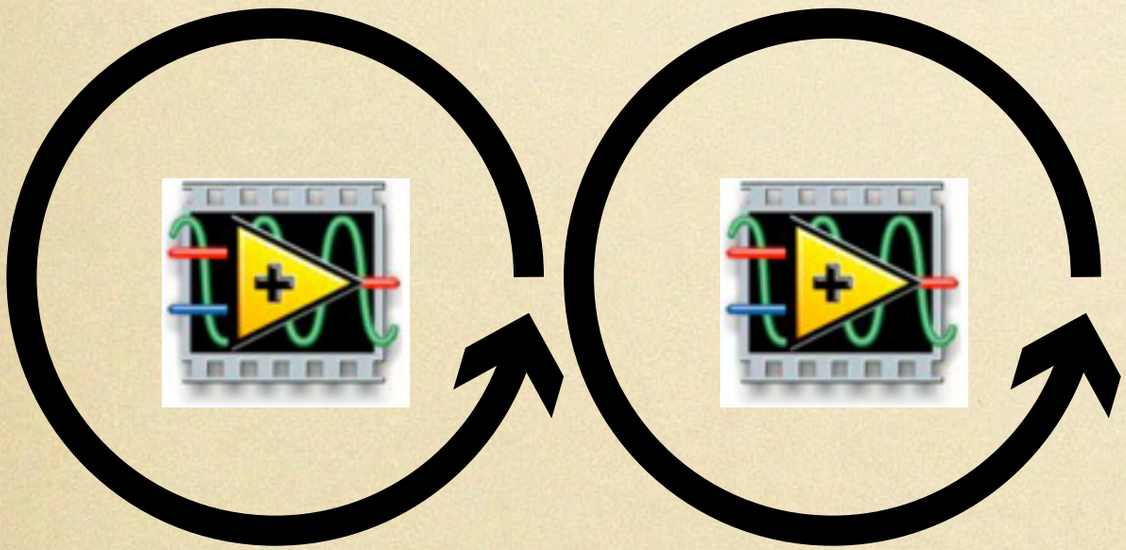


common VME address space at 2nd level

The 3rd level at a glance



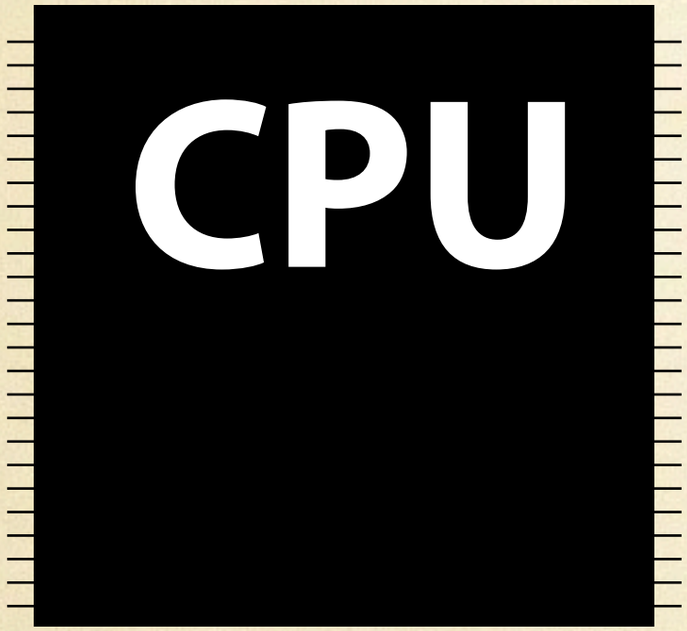
Each distributed CPU runs a LabVIEW® application that takes care of monitoring and controlling the devices under its responsability

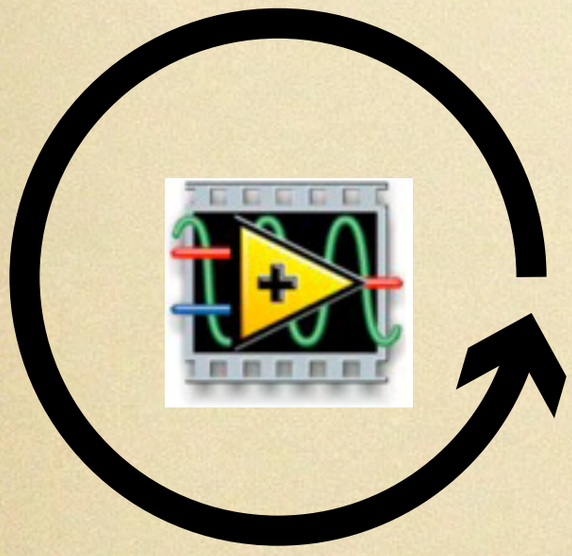


control loop

command loop

The 3rd level at a glance

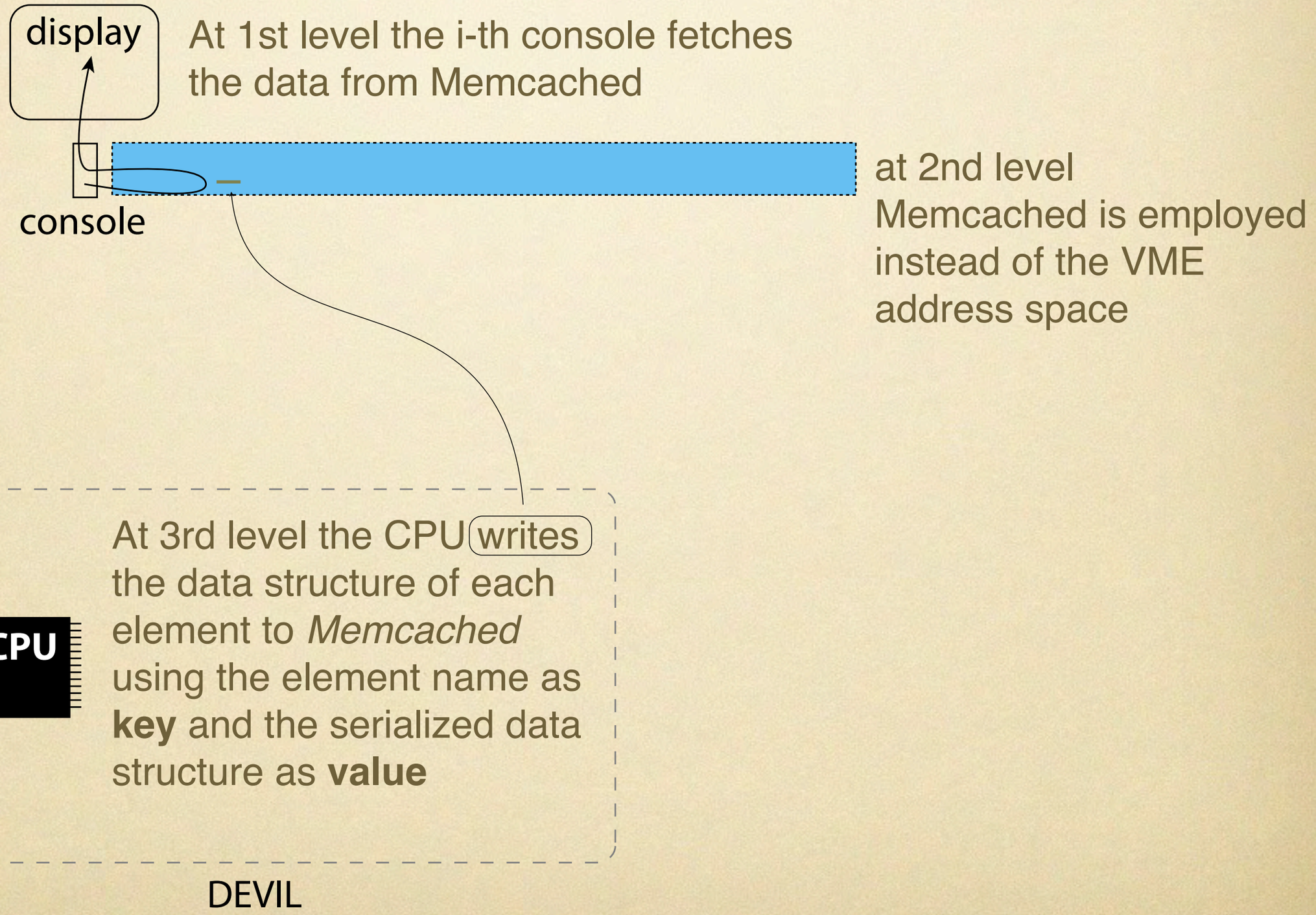




The control loop

- reads the devices *by means of proper drivers*
- for each device:
  - builds a data structure *with the current values*
  - updates the data structure in the local RAM

The idea: replace the 2nd level VME address space with the *Memcached* associative memory



For the preliminary test on the DAFNE Control System, *Memcached* has been installed on a very basic machine:

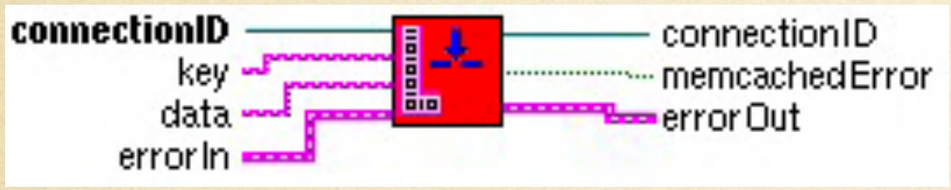
Sun V20z
- AMD Opteron 244 @ 1.8 GHz
- 2 GB RAM
- Ethernet @ 100Mbps

The OS is Linux
- CentOS 5.5 (64 bit)

Memcached version 1.4.5 (latest stable)
- with 512 MB of RAM allocated

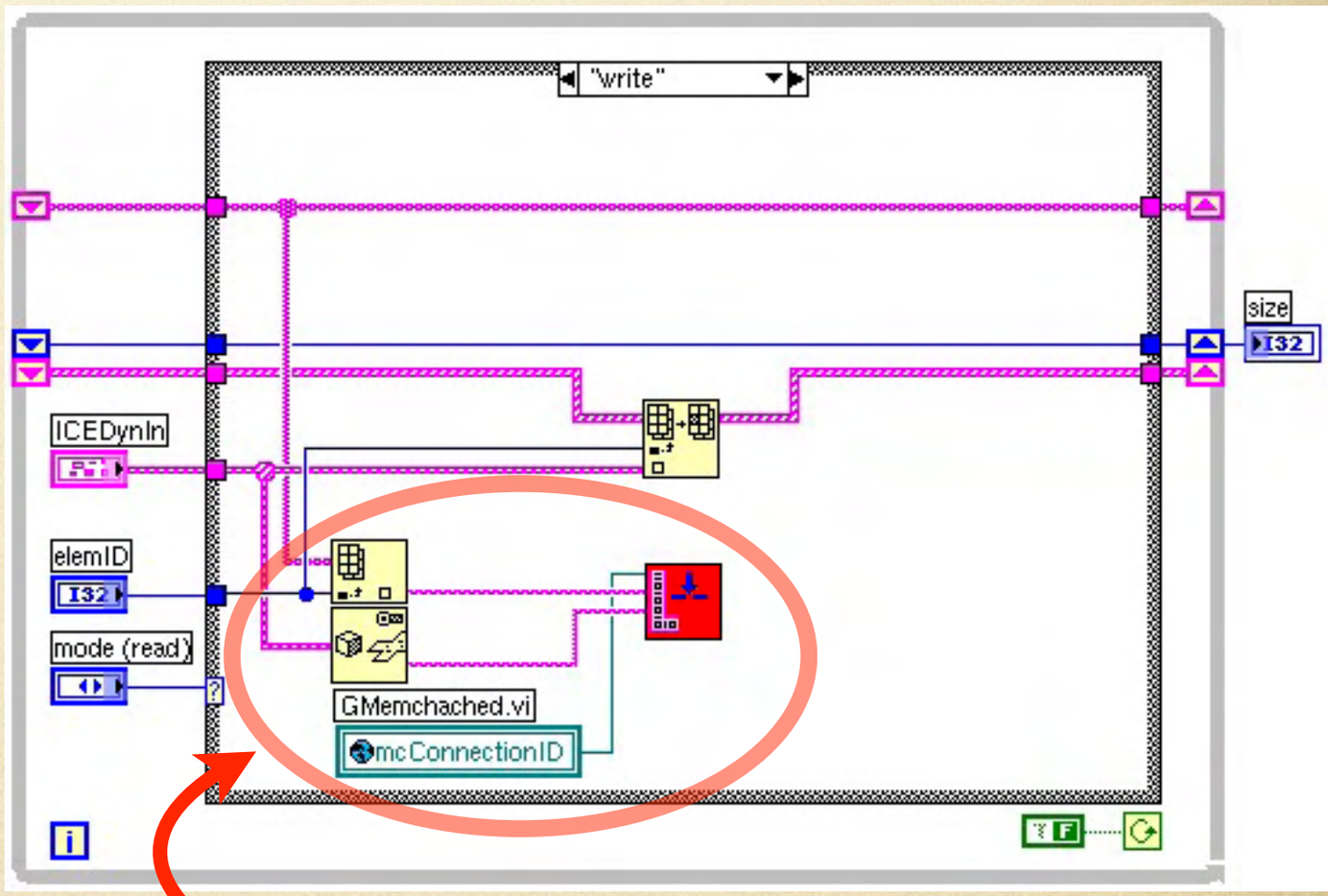
The modification has been applied to the element class ICE (Ion cleaning Electrodes)

In the 3rd level CPU a new LabVIEW routine for writing to memcached has been inserted

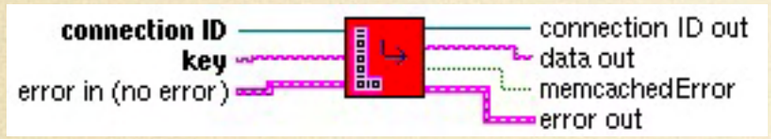


Besides a few initialization tasks, all the rest of the code stays unmodified.

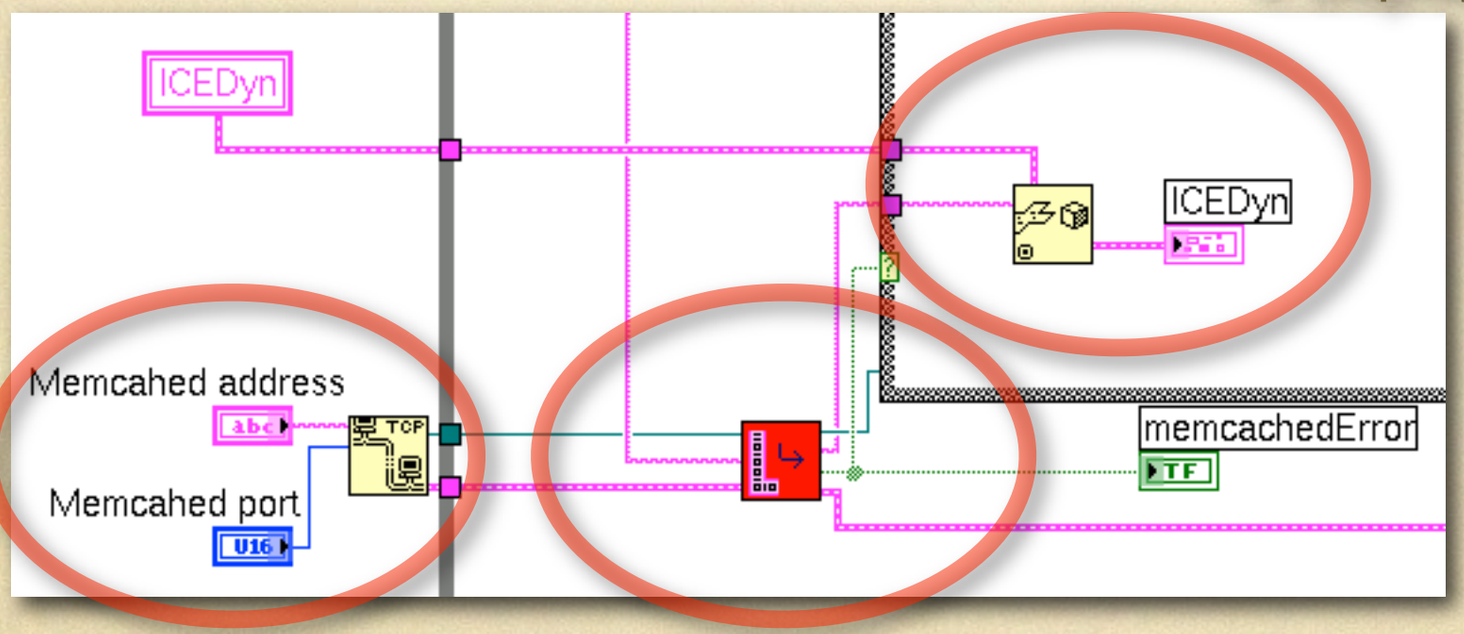
This simple and localized change is sufficient for making the data available to Memcached.



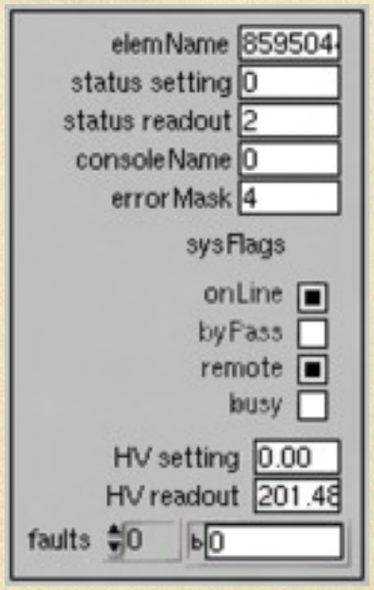
The first level reads the element data from Memcached and de-serializes it to restore the original element data structure.



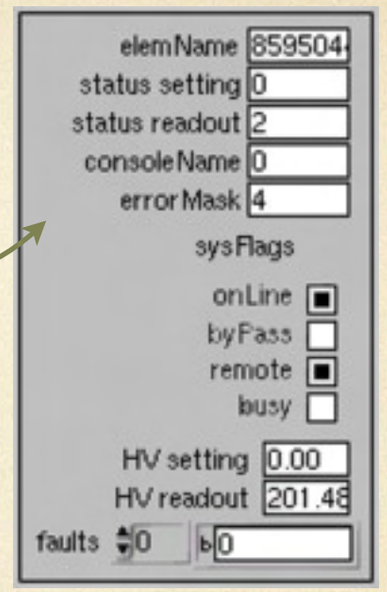
LabVIEW routine for reading from Memcached



1. Memcached connection
2. Memcached read
3. de-serialization
4. display



Preliminary measurements



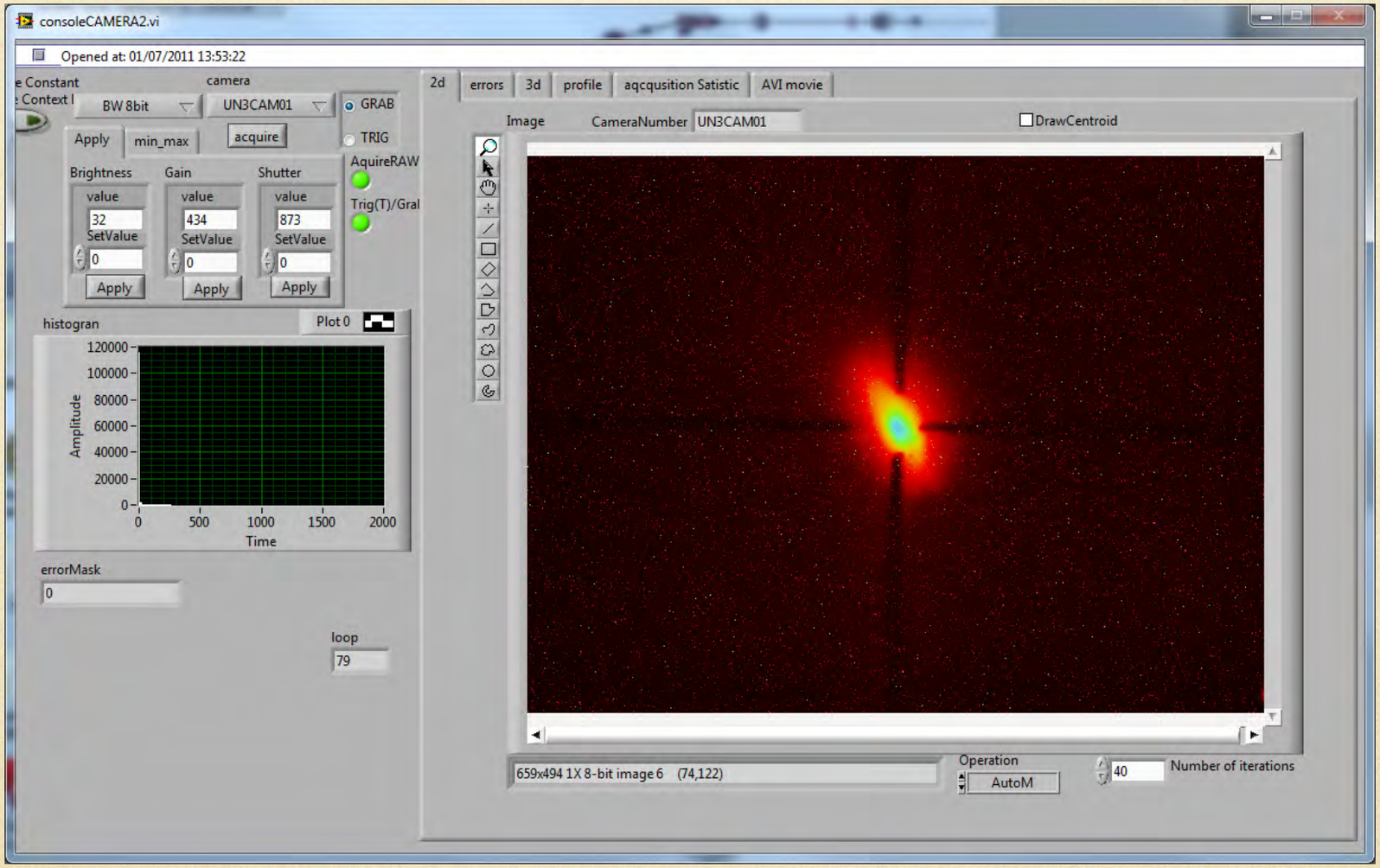
data size: 64 bytes for packet read

fetch frequency ~ 100 Hz
with no dependency on the number of fetching consoles (up to 7 in our test)

Memcached server load (measured with the *top* command)
CPU: 0.3% - 0.7% memory: ~ 0.1%

An similar test has been carried out on the SPARC Control System

Memcached has been used for storing the beam spot image from a digital camera



- network: Ethernet @1 Gbps
- image size: 640x480@8 bit = 300 kByte
- measured fetch frequency: ~ 25 Hz with no dependency on the number of fetching consoles (up to 4 in our test)

Conclusions:

Memcached demonstrated to be very stable, and to have a low impact on the CPU load

Very good overall performance *(Ethernet 100Mbps has been employed instead of 1 Gbps or even 40 Gbps Infiniband in the future...)*

We are seriously considering the possibility to adopt *Memcached* for a real upgrade of the DAFNE & SPARC Control Systems

We are encouraged to go on with a deeper integration of !CHAOS components in the DAFNE Control System