CMOS pixel sensors developments in Strasbourg

Outline

- sensor performances assessment
- state of the art: MIMOSA-26 and its applications
- Strasbourg work plan: 0.18 µm and 3D
- sensor integration: PLUME
- tracking and alignment: AIDA
- detector geometry optimisation studies
- conclusion

Isabelle Ripp-Baudot

for the PICSEL group @ Strasbourg

http://www.iphc.cnrs.fr/-PICSEL-.html

IPHC - CNRS/IN2P3 and Université de Strasbourg

CMOS pixel sensors for vertex detectors

- Prominent advantages:
  - **granularity**: pixels of ~ 10x10 μm^2
    - ➤ excellent spatial resolution
  - **monolithic**: signal processing within the sensor
    - ➤ easier to integrate
  - **material budget**: total thickness < 50 μm
  - and also: room T° operation, manufacturing, cost, power consumption, ...
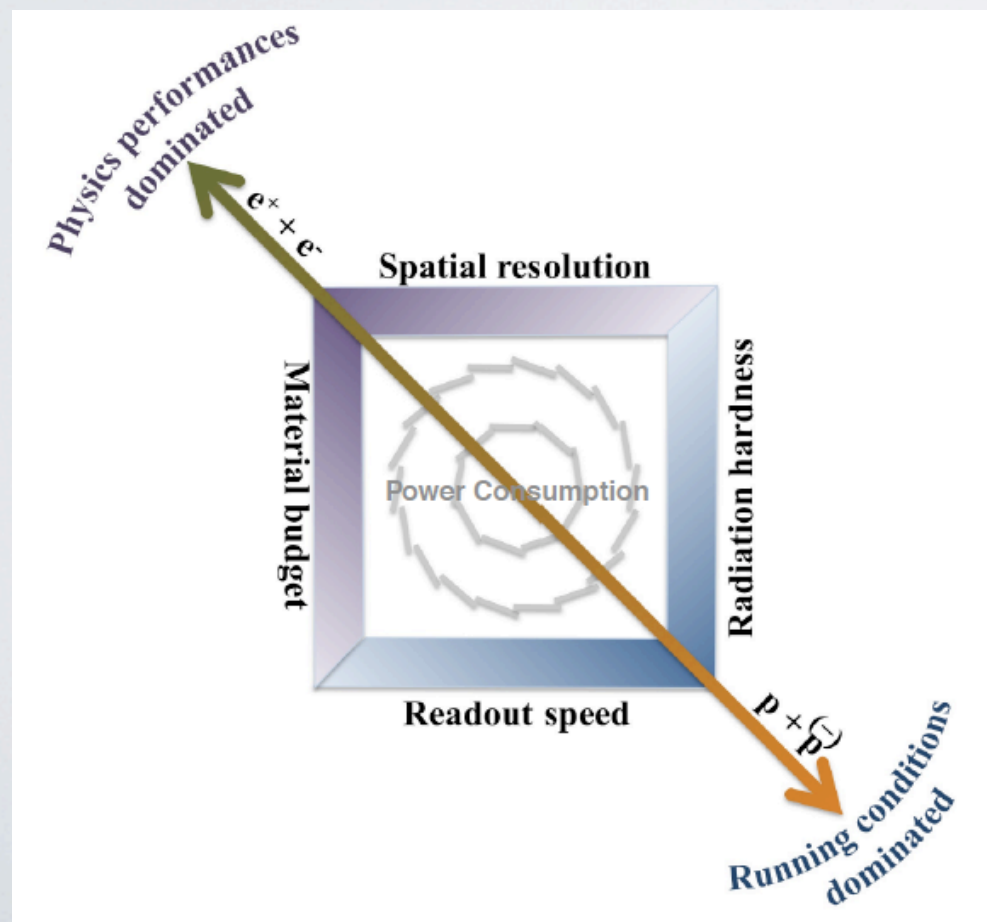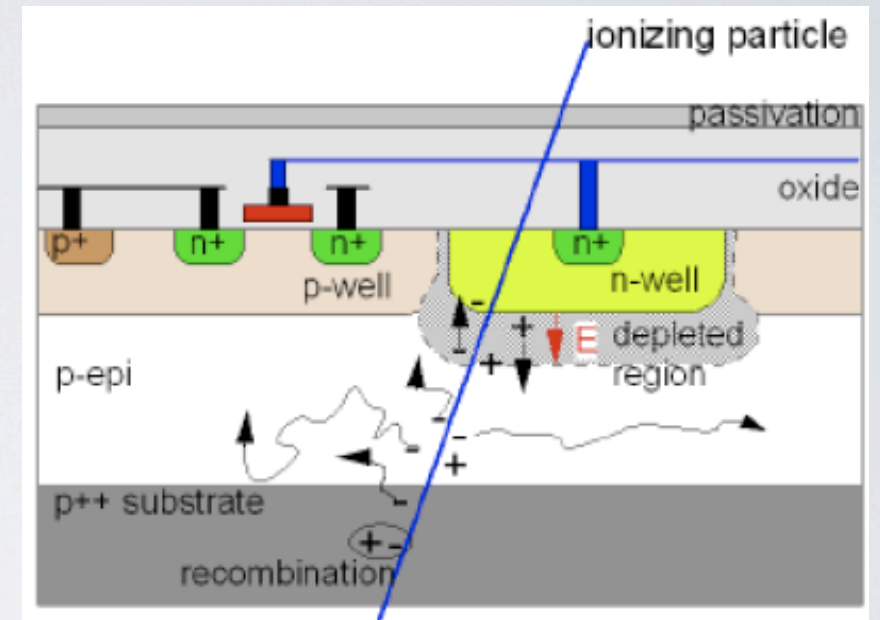
➤ CMOS pixel sensors appear as an optimal solution for the next generation of vertex detectors, but developments are needed to optimise them according to different requirements.

sensor performances assessment

MIMOSA sensor prototypes:
see: http://www.iphc.cnrs.fr/List-of-MIMOSA-chips.html

- various technologies:
  - 2 different 0.35 µm processes
  - 2 different 0.18 µm processes
- various pitches:
  - 10×10 µm^2 ⟶ 40×40 µm^2,
  - elongated pixels 16×64 µm^2, $18.4\times(36.8$ to $73.6)$ µm^2.
- various sensitive volumes:
  - w/ and w/o epitaxial layer ➤ various thicknesses and dopings,
  - standard and high resistivities.

➤ more than 10 years of **exhaustive studies** (S/N, ε, $\sigma_{s.p.}$, clustering, charge sharing) under different operating conditions (T°, irradiation, read-out frequency) and **systematic beam test validations**.

➤ useful data base of the charge collected per pixel for each technology & architecture.
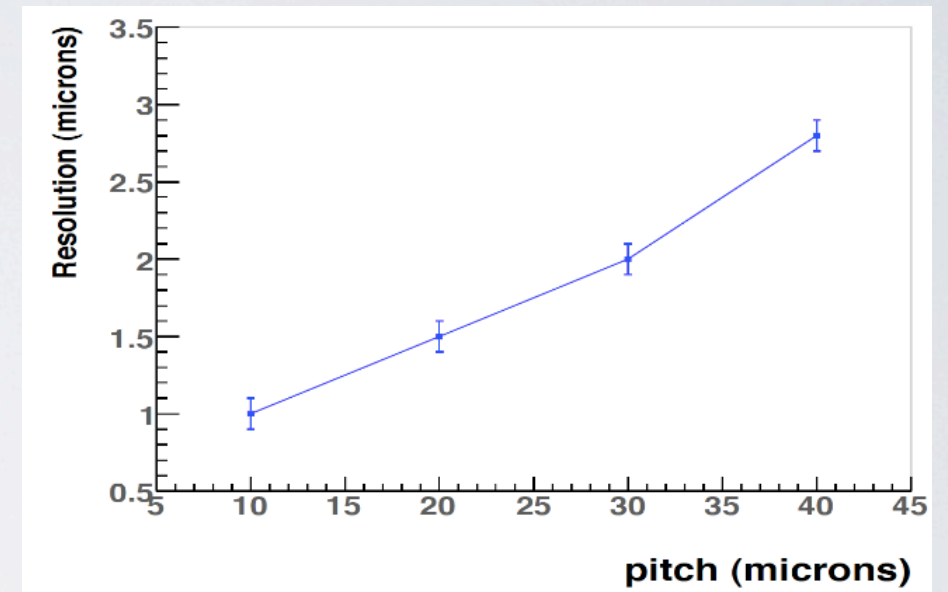
MIMOSA sensors: state of the art

- **MIMOSA-26 prototype:**
  - **0.35 μm process with high resistivity epitaxy**
  - fabricated 2008-2010: > 90 sensors tested with different features
  - active area 1152 columns of 576 pixels (21.2 x 10.6 mm^2)
  - pitch 18.4x18.4 μm^2 ➤ 660k pixels with $\sigma_{s.p.}$= **3.5 μm**
  - detection efficiency ~ 100 % for very low fake rate (~10^{-4})
  - in-pixel amplification and CDS
  - end-of-column discrimination and 0 suppression (digital output)
  - **rolling shutter read-out**: pixels grouped in columns, readout in //
    - ➤ **no dead-time**
  - read-out time: 10^4 frames/s ➤ **~ 100 μs** ➤ **suited for > 10^6 particles/cm^2/s**
  - **power dissipation**: 250 mW/cm^2
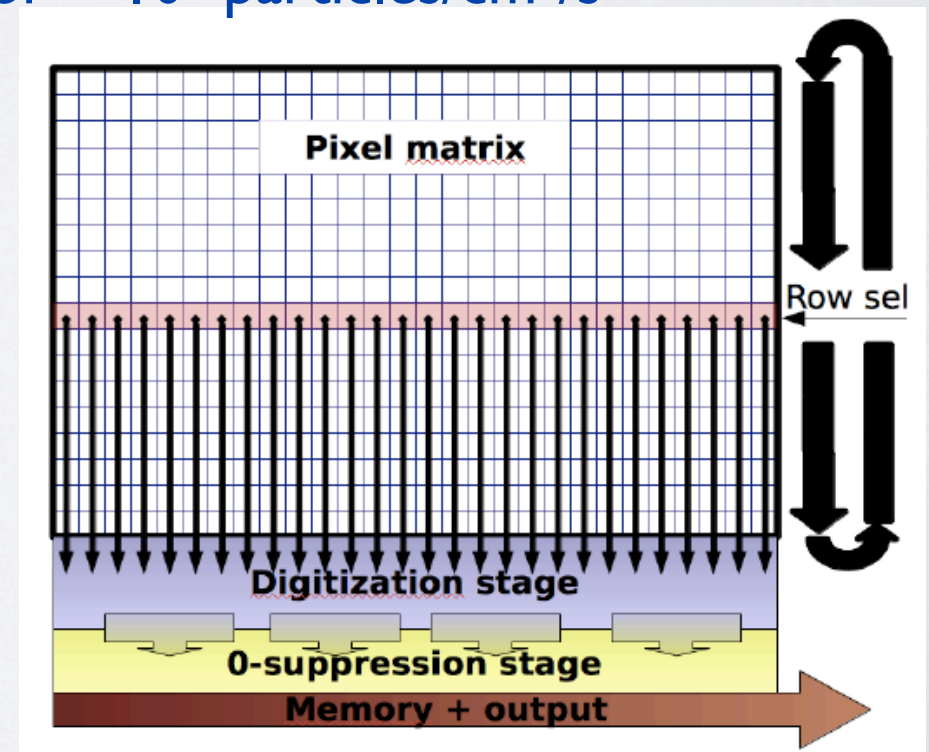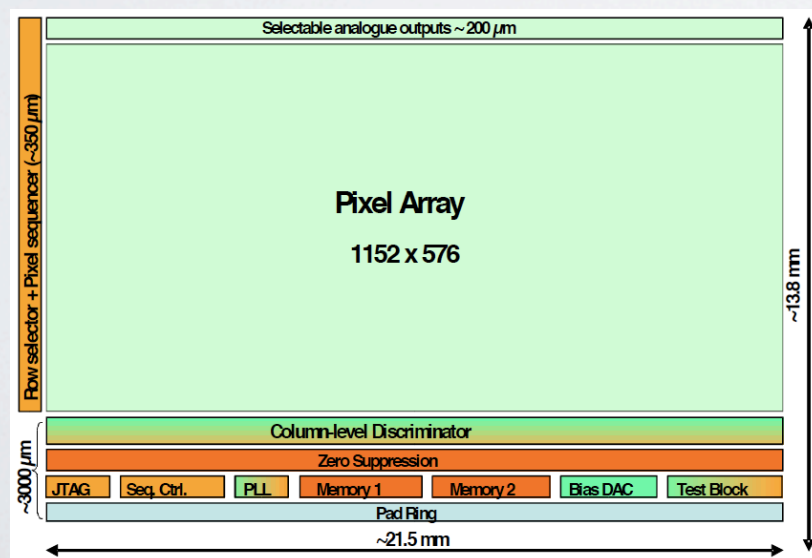
MIMOSA-26 applications

- **applications of MIMOSA-26 technology** in different projects and vertex detector upgrades, requiring:
    - **material budget 0.15 % - 0.5 %**
    - **tolerance up to several MRad and fluences $> 10^{13}$ n_{eq}/cm^2**
                    depending on T°, pitch, read-out time.
    - **~ few µs read-out time**
            - Beam Telescope of the FP6 project EUDET
            - STAR @ RHIC ➤ data taking in 2013-2014,
                                first vertex detector equipped with CMOS sensors
            - CBM @ FAIR ➤ data taking > 2016 (SIS-100)
            - Hadrontherapy: FIRST (GSI)
            - other applications: ALICE @ LHC, ILD vertex @ ILC, ...

- see details in previous review on Strasbourg activities by M. Winter,
October 2010 SuperB meeting @ LNF
http://agenda.infn.it/conferenceDisplay.py?confId=2303

next steps

- **exploration of 0.18 µm technologies:**
  - · MIMOSA-32: 1st 0.18 µm prototype will be studied in 2012
    (Multi Project Wafer Run #62 24/10/11)
  - ① · MIMOSA-22THR: study of pixel architecture ➤ 2013
  - · MISTRAL-like: first big prototype for ALICE and CBM,
    with read-out time ~ 20 to 40 µs
  - ② · investigate all features: 3T, 4T, all metallisation layers used, ...
  - ③ · study of parallel rolling-shutter read-out ➤ read-out time < 10 µs ≥ 2016

- **exploration of 3D Integration Technologies:**
  - · participation to the 3D Integration Consortium (coordinated by FNAL):
    CAIRN chips (CMOS Active pixel sensors with vertically Integrated Read-out and Networking functionalities) submitted to foundry in Spring 2009.
  - · high expectations
  - · longer term program

Conventional MAPS 4 Pixel Layout   3D 4 Pixel Layout

➤ Strasbourg: improve performance of the charge collection (S/N, noise reduction) and the pre-amplification.
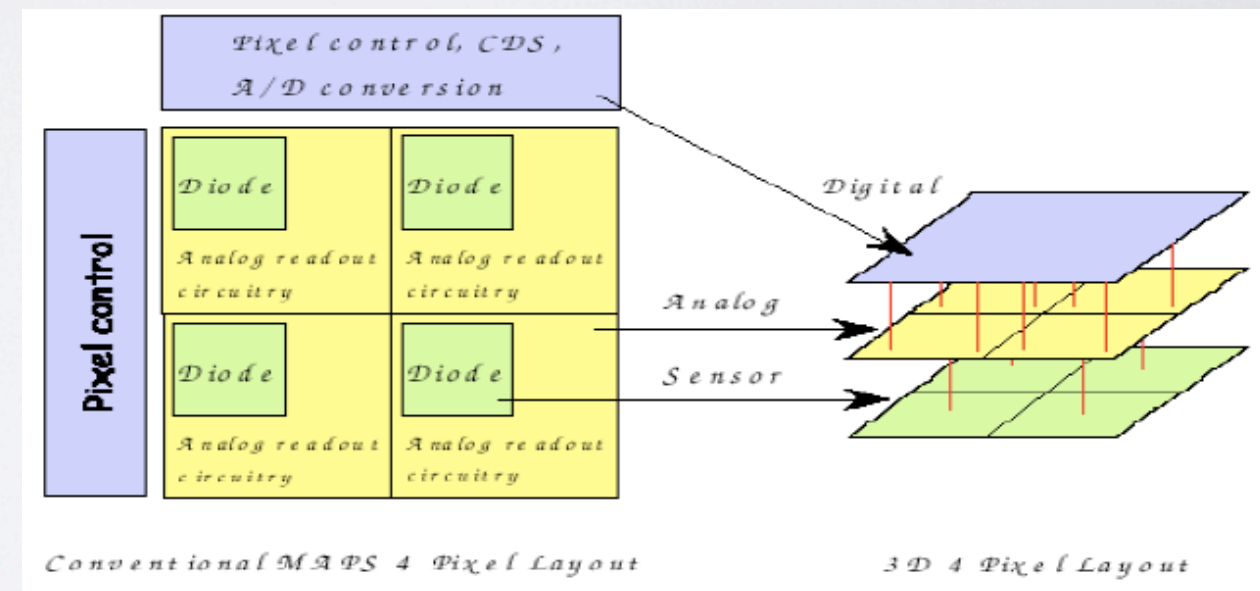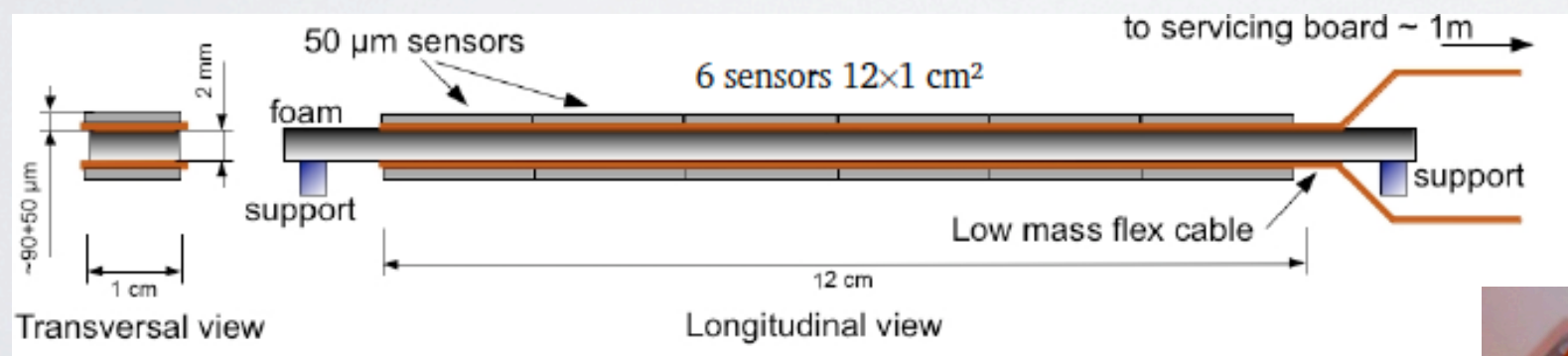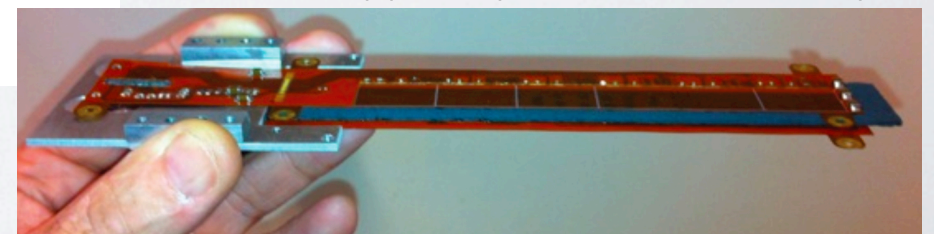
sensor integration

the PLUME project: Pixelated Ladder with Ultra-low Material Embedding
collaboration between IPHC Strasbourg, DESY, Oxford and Bristol
see: http://www.iphc.cnrs.fr/CMOSILCPLUME.html

- motivation: ILD vertex detector at the ILC

- goal: **to achieve by ≥ 2012 a prototype double-layer ladder equipped with CMOS pixel sensors with material budget ≤ 0.3 % X_0**

→ added value of a double-sided layer w.r.t. a single-sided layer?

- design: sensitive area $2 \times 12 \times 1$ cm^2
  2×6 MIMOSA-26 thinned down to 50 μm
 binary read-out
  air cooling

bare support (foam stiffener+flex)

sensor integration (2)

- Prototype 0 (2009-2010):
  - 2x2 MIMOSA-20 2x4x1 cm^2 sensitive area, 204k pixels
  - analog readout
  - material budget ~ 0.6 % X_0 (copper cable)
  - beam test @ SPS (CERN) with 120 GeV in November 2009:
    - ➤ feasibility study and beam test procedure implementation

- Prototype 1 (2010-2011): focus on functionalities
  - 2x6 MIMOSA-26 2x12x1 cm^2 sensitive area, 660k pixels
  - digital read-out
  - material budget ~ 0.6 % X_0
  - already tested @ IPHC
  - work plan:

  - Summer 2011: thermo-mechanical measurements,
  - November 2011: beam test @ SPS.

- Prototype 3 (2011-2012): optimised for material budget
  - ~ the same as proto-1 with material budget ~ 0.3-0.4 % X_0
  - new tool to glue the sensors on the flex with high precision (Fall 2011).
 - first ladder ~ Fall 2011, beam test ~ Summer 2012.
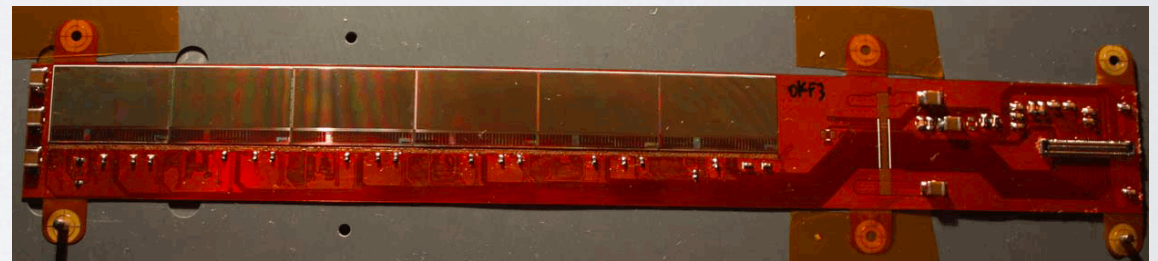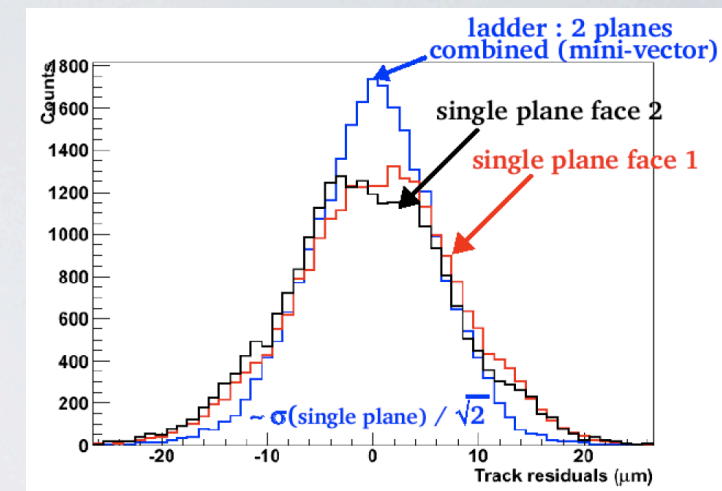
alignement and tracking

the AIDA project: Advanced European Infrastructures for Detectors and Accelerators
collaboration between IPHC Strasbourg, IRFU Saclay + PLUME
see: http://www.iphc.cnrs.fr/AIDA-Project.html

- On-beam test infrastructure:
    - Large Area Beam Telescope (LAT, now Single Arm LAT):
      EUDET-like Beam Telescope
      aim at providing impact positions on DUT with 2 μm resolution
    - Alignment Investigation Device (AID): PLUME ➤ 2012-2013
    - very thin removable target
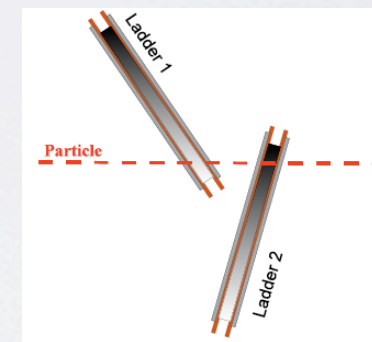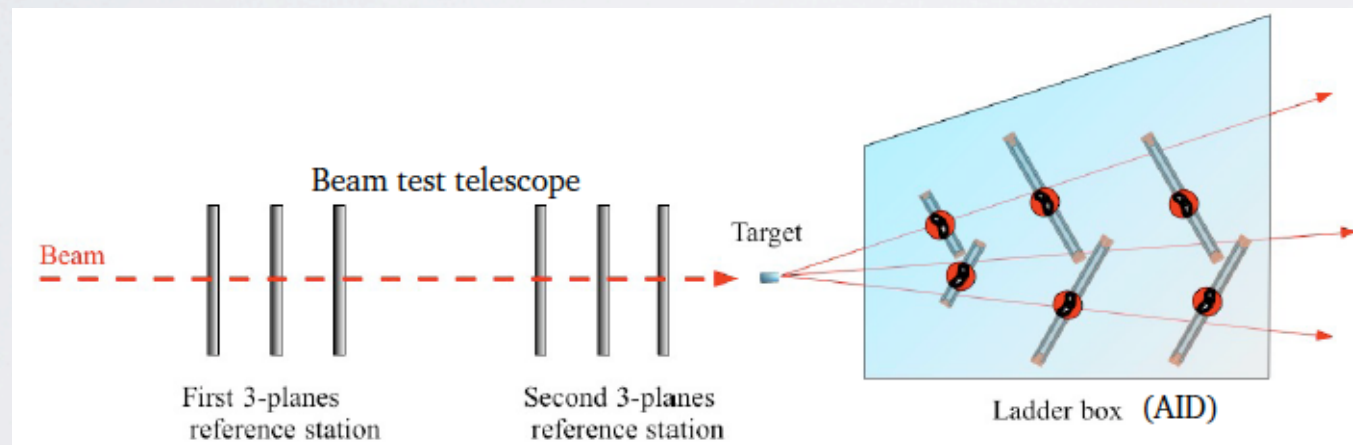
- SALAT demonstrator with current sensors (MIMOSA-28 from STAR-PXL)
➤ commissioning 2012
Final chips: large active area 5x5 cm^2, 2500 x2500 pixels with 20x20 μm^2 pitch,
based on multi-reticule sensors: **stitching process to be investigated** (advantage of 0.18 μm)
➤ expected Summer 2014

detector geometry optimisation

- **Estimation of the added value from double-sided layers:**
   - better pointing accuracy,
    - mini-vector could help working under unfavourable conditions (high occupancy rate w.r.t. read-out time),
    - combination of time resolution on one side and time resolution on the other side,
    - improved neighbouring hit separation,
    - may also help for the alignment.

    ➤ **especially interesting in high density conditions.**

- **Importance of the quality from the extrapolated track** on the Layer-0, reconstructed with the other layers from the tracker.

- Twofold investigation:
    - beam tests with PLUME and AIDA,
    - simulations: "super-fastsim", and in the future, physics benchmarks studied within the *a la* SuperB fastsim.

Spatial resolution

Time resolution
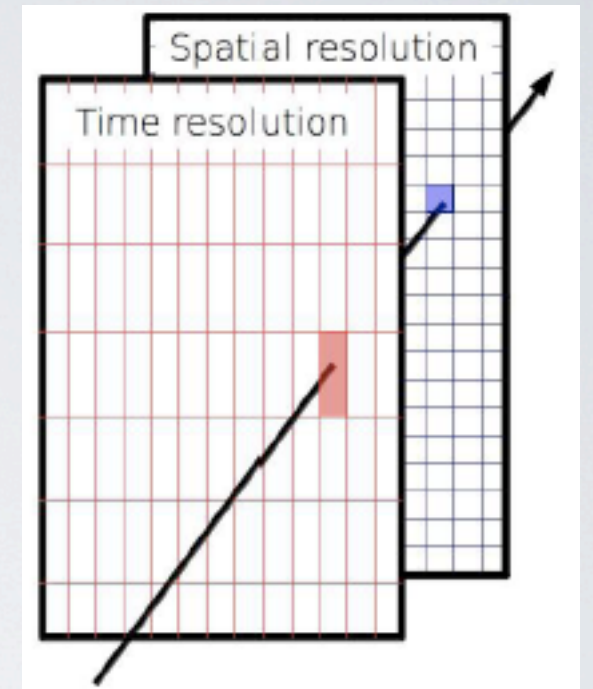
detector geometry optimisation (2)

fast-estimation tool of a tracker system performances:
tool inherited from STAR (J. Thomas) via our ALICE colleagues.

- Principle:
  - easy to calculate σ_{IP} for a track reconstructed with 2 layers:

$$\sigma_{IP}^2 = \frac{\sigma_1^2\, r_2^2 + \sigma_2^2\, r_1^2}{(r_2 - r_1)^2} + \frac{\theta_{MCS}^2\, r_1^2}{\sin^2\theta}$$

  - more complicated with more than 2 measurements
    - ➤ P. Billoir method (NIM 225 (1984) 352) based on an outside-in Kalman filter:

    matrix method [Mult. Cb Scatt.] [Drift] [Measur.] [MCS] [D]

- Given the detector parameters (r, x/X_0, $\sigma_{s.p.}$, $t_{r.o.}$) and the collider quantities (background and physics cross-sections, luminosity), we are able to study:
  - pointing resolution at collision point,
  - transverse momentum resolution,
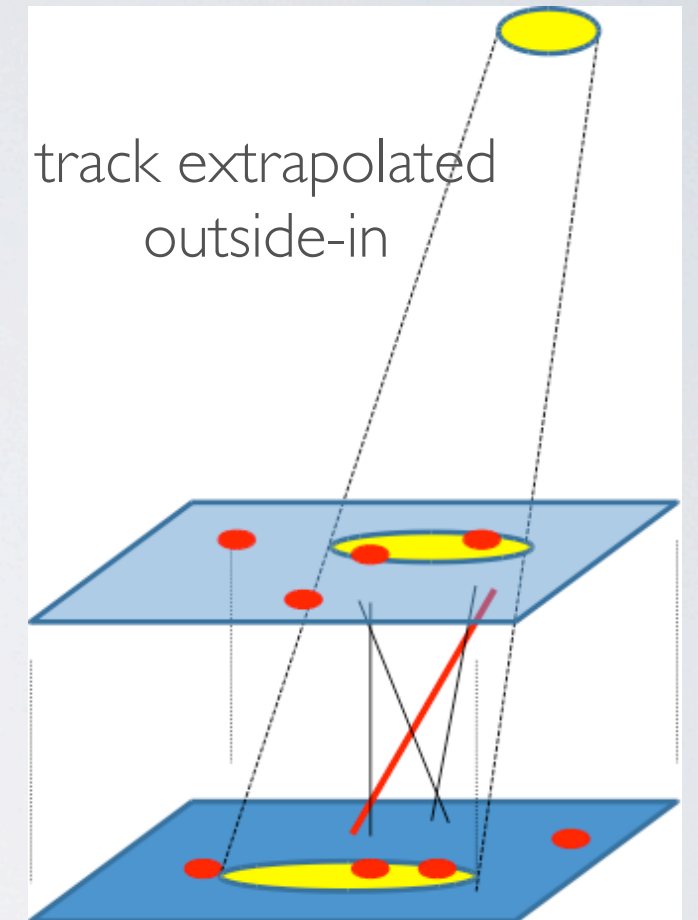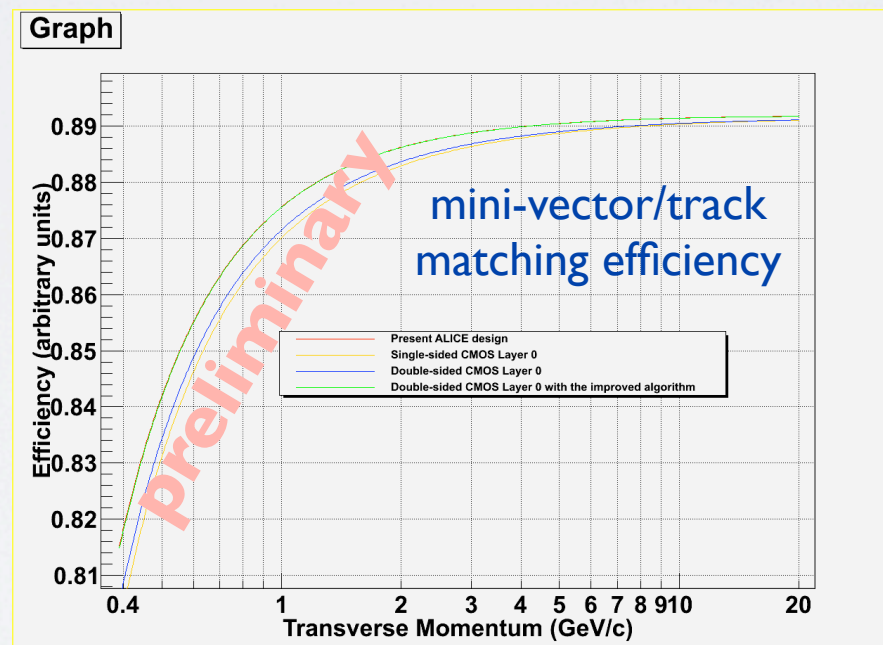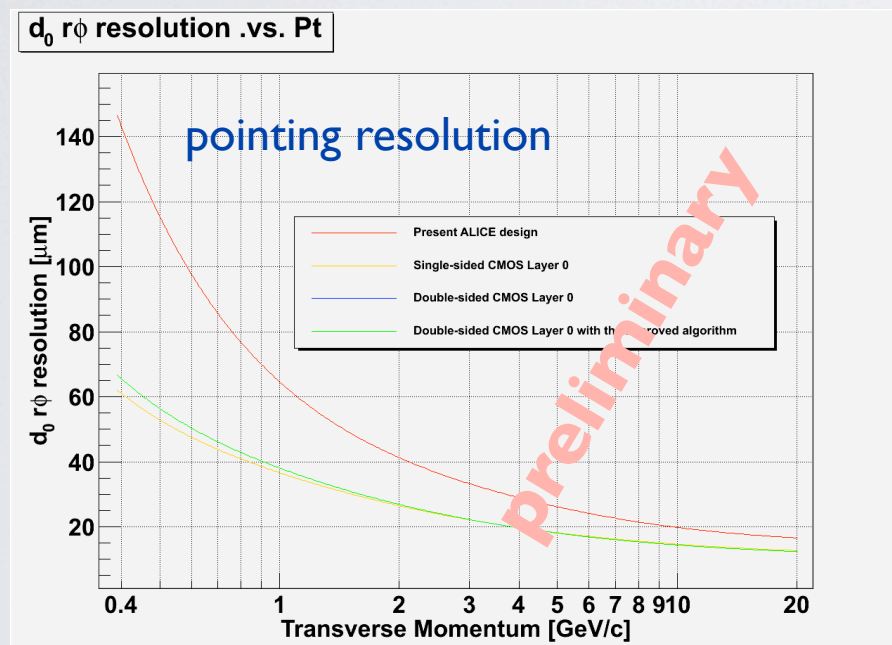 - efficiency to match a measured point on a given layer to a reconstructed track: to ensure that the hit finding can be done efficiently at each layer in a high hit density environment,
  - **global vertex detector geometry optimisation**: interplay between all layers.

detector geometry optimisation (3)

- Example of study (S. Senyukov and J. Baudot, PICSEL group, IPHC Strasbourg):
  - study for the ALICE vertex detector upgrade,
  - **mini-vector with the hits from the double-sided CMOS layers are matched to the reconstructed track** rather than only using the 2 measured points separately.
  - further investigation varying detector parameters: position of layers, material budget, ...

track extrapolated outside-in

d_0 rφ resolution .vs. Pt

pointing resolution

preliminary

- Present ALICE design
- Single-sided CMOS Layer 0
- Double-sided CMOS Layer 0
- Double-sided CMOS Layer 0 with the improved algorithm

d_0 rφ resolution [μm] — Transverse Momentum [GeV/c]

Graph

mini-vector/track matching efficiency

preliminary

- Present ALICE design
- Single-sided CMOS Layer 0
- Double-sided CMOS Layer 0
- Double-sided CMOS Layer 0 with the improved algorithm

Efficiency (arbitrary units) — Transverse Momentum (GeV/c)

➤ **double-sided layer + mini-vector approach interesting for the tracking efficiency.**
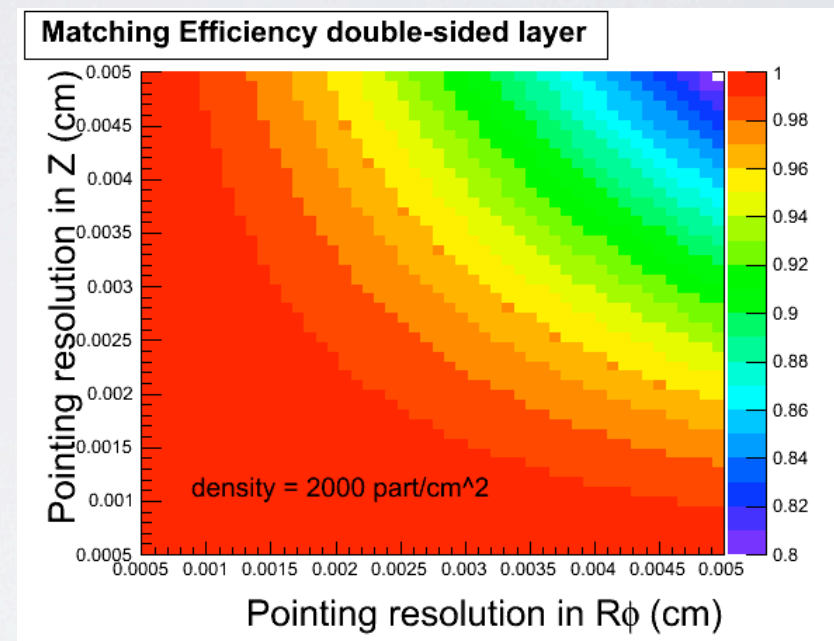
detector geometry optimisation (4)

• Added value of mini-vectors from a double-sided layer of CMOS pixel sensors in SuperB: measured-point/extrapolated-track matching efficiency as a function of the total resolution on the extrapolated track, in both directions, for different particle densities.
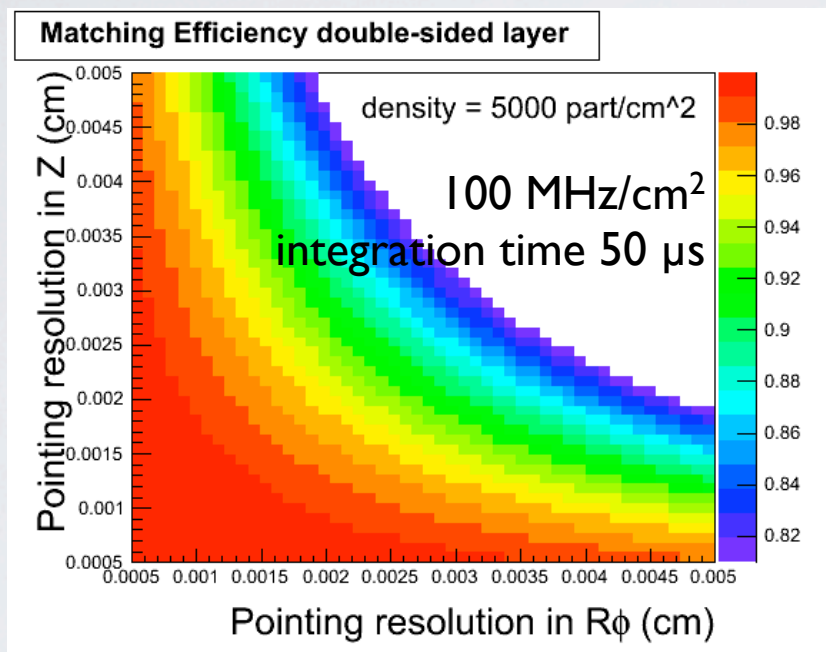
for instance: $\sigma_{eff} \sim 15\mu m$
needed in both directions

for instance: $\sigma_{eff} \sim 25\mu m$
needed in both directions

with $\sigma_{eff} = \sqrt{(\sigma_{extrapolation}^2 + \sigma_{detector}^2)}$, for instance $15 = \sqrt{(11^2+10^2)} = \sqrt{(14^2+5^2)}$
$$25 = \sqrt{(23^2+10^2)} = \sqrt{(24^2+5^2)}$$

� need more investigation but a moderate read-out time may do the work, especially during the first years.

(ALICE note in preparation by J. Baudot and S. Senyukov: "Comparison of hit-track matching efficiency with single-sided and double-sided layers")

conclusion

- Strasbourg expresses interest in joining the SuperB collaboration with a twofold contribution:

  - hardware developments focused on a vertex detector equipped with CMOS pixel sensors:
    - ➦ explore 0.18 µm and 3D technologies, focusing on charge collection and pre-amplification, in synergy with INFN,
    - ➦ design of the low mass flex cable,
    - ➦ architecture of the ladder.

  - physics analyses, beginning with studies in relation with the tracking system performances:
    - ➦ investigate the asset of a double-sided layer of CMOS pixel sensors,
    - ➦ global optimisation of the whole vertex detector (which layer 1?),
    - ➦ study the mandatory read-out time in parallel rolling shutter read-out mode.

- Synergy between all developments performed in Strasbourg in the PICSEL group (which is involved in several projects) and SuperB vertex detector developments.

more information

- **Sensor organisation:**
  - ✳ Signal sensing and analog processing in pixel array
  - ✳ Mixed and Digital circuitry integrated in chip periphery
  - ✳ Read-out in rolling shutter mode

    (pixels grouped in columns read-out in //)

Pixel Array

Column-level ADC

Controller+Memory+DAC+Trans.

- **Main consequences:**

  - ✳ **Read-out speed :**

    ≡ integration time

    ≡ nb of pixels $\times$ pixel read-out time (O(100 ns))
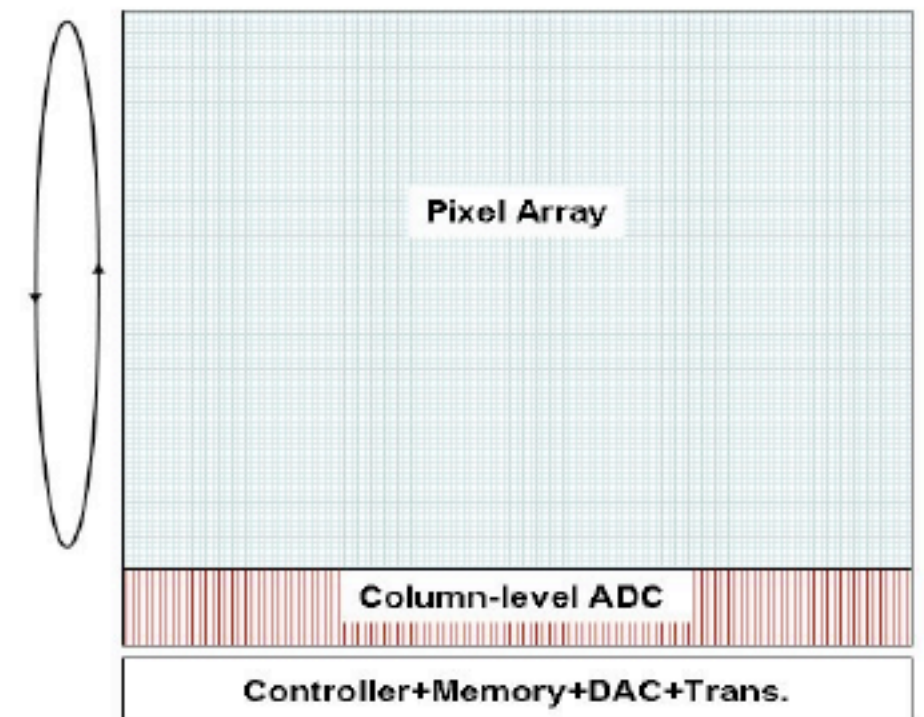
  - ✳ **Power consumption :**

    limited inside the pixel array to the row being read out

  - ✳ **Material budget :**

    peripheral band(s) for mixed+digital circuitry, insensitive to impinging particles ($\sim$ 10 % of chip surface)
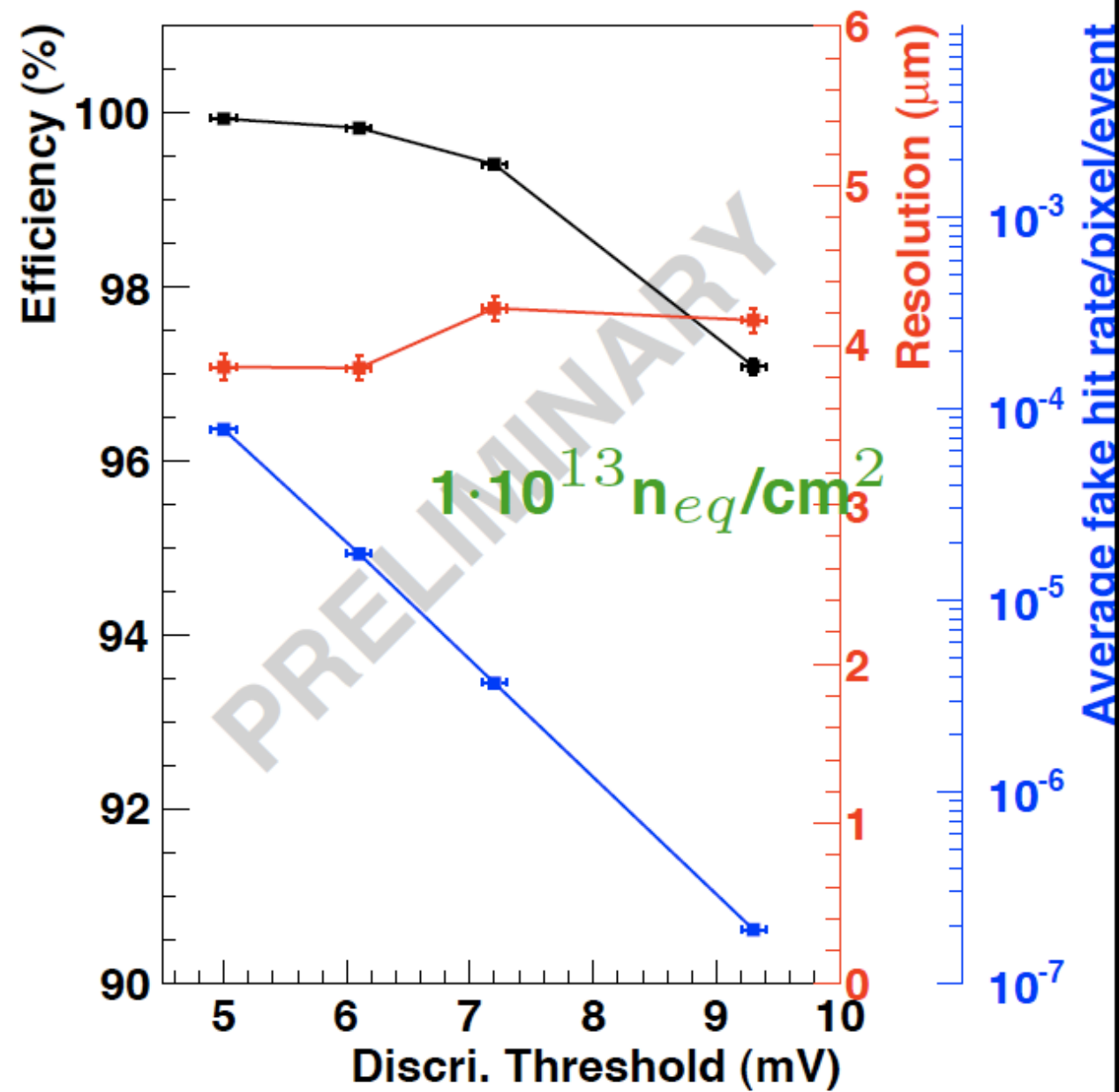
  - ✳ **Time stamp :**

    each row corresponds to a specific time intervalle $\Rightarrow$ adapt track reconstruction code

(courtesy of M. Winter)

Mi26 HR-15 Efficiency, Fake rate and Resolution for a chip irradiated with a $1.10^{13} N_{eq}$ dose at $T_{op} \sim 0^\circ$ C

(courtesy of M. Winter)

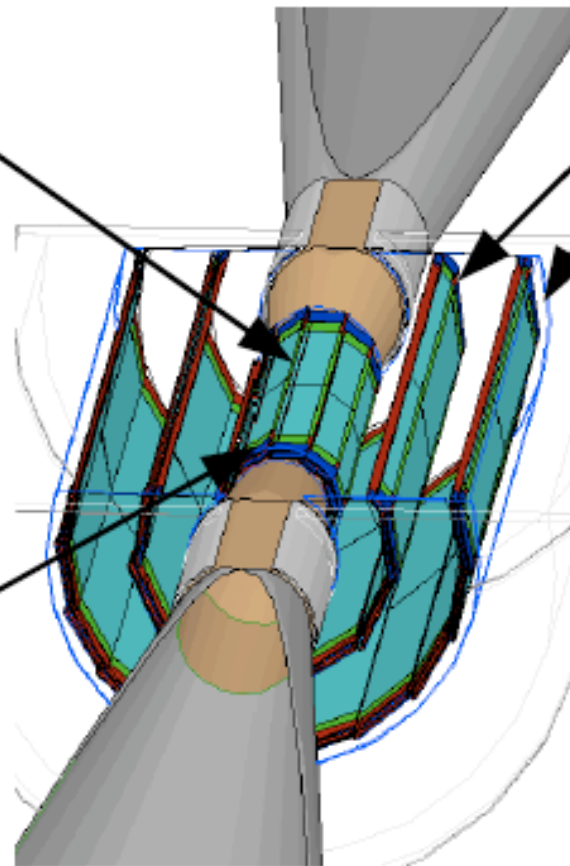# The CMOS sensor-based VXD

Inner layer – internal side

- ✗ Optimized for resolution
- ✗ $16 \times 16~\mu m^2$
- ✗ Q encoding: binary
- ✗ $t_{Integration}~\sim 40~\mu s$
- ✗ Sensitive area $\sim 2~cm^2$

Inner layer – external side

- ✗ Optimized for r.o. speed
- ✗ $16 \times 64~\mu m^2$
- ✗ Q encoding: binary
- ✗ $t_{Integration}~\sim 10~\mu s$
- ✗ Sensitive area $\sim 2~cm^2$

Outer layer

- ✗ Optimized for low power
- ✗ $35 \times 35~\mu m^2$
- ✗ Q encoding: 4-bits
- ✗ $t_{Integration}~\sim 100~\mu s$
- ✗ Sensitive area $\sim 4~cm^2$

layer	radius (mm)	length (mm)	# ladders	# sensors*	$\#.10^6$ pixels	t_{int} (μs)	$\sigma_{s.p.}$ (μm)
1	16/18	125	14	168	66 + 16	40 / 10	< 3
2	37/39	250	26	312	2x112	100	< 4
3	58/60	250	40	480	2x173	100	< 4
total			80	960	652		

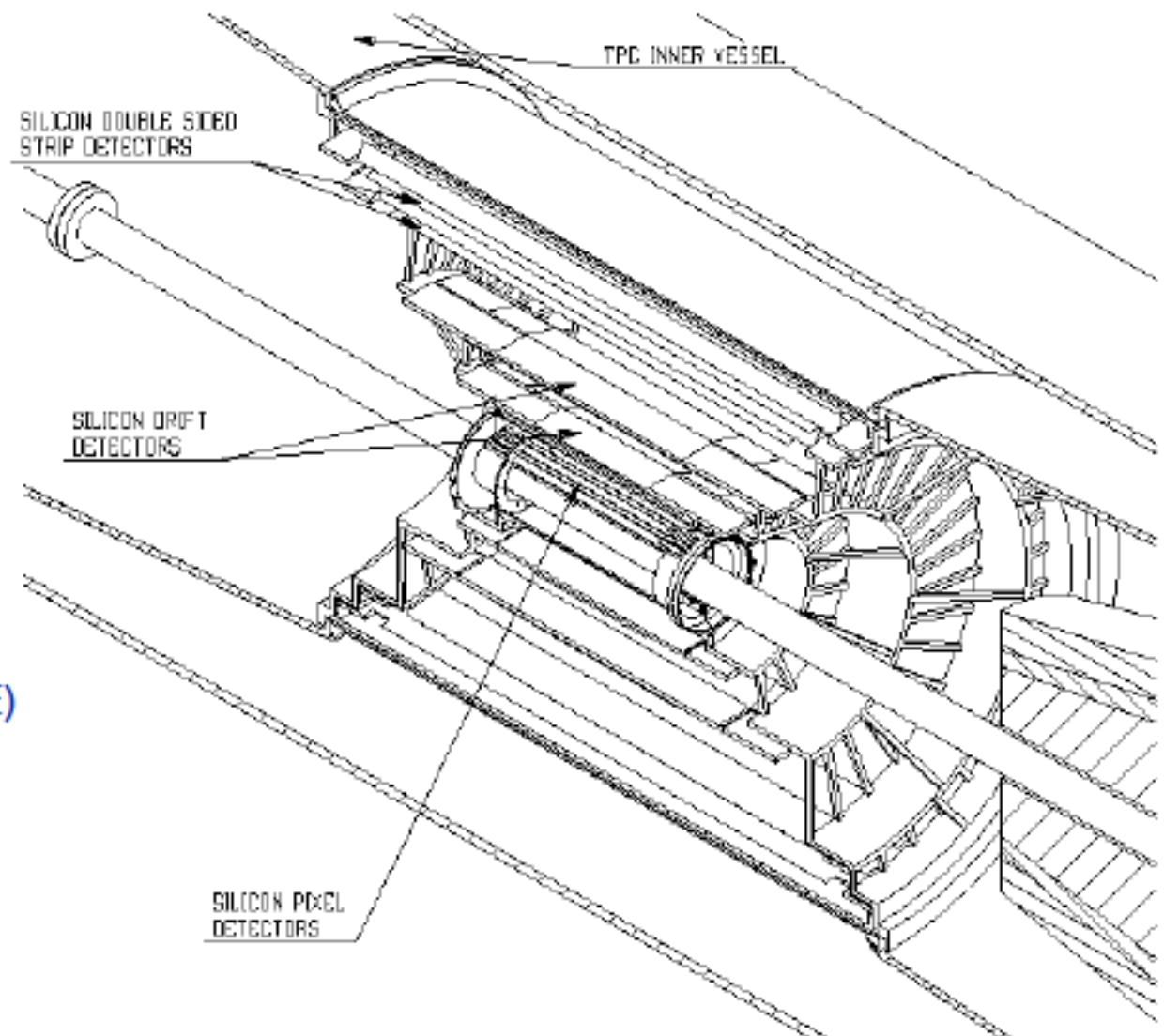* Numbers corresponding to current CMOS technology (0.35 μm) prototypes

(courtesy of J. Baudot)

- ● ITS upgrade :

  - ✳ envisionned for "2016" LHC long shutdown

  - ✳ exploits space left by replacement of beam pipe
    with small radius (19 mm) section

  - ✳ consists (at least) in introducing L0
    ≡ additionnal layer at $\lesssim$ 25 mm radius
    (potentially : replace part of the ITS)

  - ✳ 2 pixel otions considered :
    - ◇ Hybrid pixels with reduced material budget & pitch
    - ◇ CMOS pixel sensors derived from STAR-PXL (ULTIMATE)

  - ✳ main characteristics of CMOS option :
    - ◇ double-sided ladder derived from PLUME ($< 0.5 \% X_0$)
    - ◇ $\lesssim 50 \, \mu s$ read-out time
    - ◇ $\sim 4 \, \mu m$ spatial resolution
    - ◇ > 1 MRad & $10^{13} n_{eq}/cm^2$ at T $= 30^{\circ}$C (target values)
      ↪ move to $0.18 \, \mu m$ technology

  ▷▷▷ **Technical Proposal due for 2011**

TPC INNER VESSEL

SILICON DOUBLE SIDED STRIP DETECTORS

SILICON DRIFT DETECTORS

SILICON PIXEL DETECTORS

"standard" PCB process for chip embedding in plastic foils (R. de Oliveira, CERN)

- Gluing between two kapton foils

- Opening vias using lithography

- Metallization: Al (5-10 μm)
- Lithography to pattern metal

- Single module: intermediate tests

- Complete ladder assembling, laser cut along sensor edges

- Gluing of another kapton foil for deposition of second metal layer

(courtesy of W. Dulinski, FEE 2011 Bergamo)