CALICE: status of a data acquisition system for the ILC calorimeters

Valeria Bartsch, on behalf of CALICE-UK Collaboration
• use particle flow algorithms to improve energy resolution
  => 1cm×1cm segmentation results in 100M channels with little room for electronics or cooling
• Bunch structure interesting:
  – ~200ms gaps between bunch-trains
  – Trains 1ms long, 300ns bunch spacing
• Triggerless
=> ~250 GB of raw data per bunch train need to be handled
Objectives

• Utilise off the shelf technology
  – Minimise cost, leverage industrial knowledge
  – Use standard networking chipsets and protocols, FPGAs etc.
• Design for Scalability
• Make it as generic as possible
  – exception: detector interface to several subdetectors
• Act as a catalyst to use commodity hardware

⇒ build a working technical prototype (verify mechanics and cooling) and a DAQ system to be used by the prototype by 2009
DAQ architecture

DAQ software

Off Detector Receiver (ODR)

Link Data Aggregator (LDA)

Detector Interface (DIF)

Detector Unit
Detector Interface (DIF) status

- Two halves – Generic DAQ and Specific Detector
  - 3 detectors: ECAL, AHCAL, DHCAL
  - 1 DAQ Interface!
- Transmits configuration data to the Detector Unit and transfers data to downstream DAQ
- Designed with redundancies for readout
- Signal transmission along ECAL test slab and ECAL slab interconnects being tested
Link Data Aggregator (LDA)

Hardware:
- PCBs designed and manufactured
- Carrier BD2 board likely to be constrained to at least a Spartan3 2000 model
- Gigabit links as shown below, 1 Ethernet and a TI TLK chipset
- USB used as a testbench interface when debugging
Link Data Aggregator (LDA)

Firmware:
- Ethernet interface based on Xilinx IP cores
- DIF interface based on custom SERDES with state machines for link control. Self contained, with a design for the DIF partner SERDES as well
- Possible to reuse parts from previous Virtex4 network tests
- No work done on TLK interface as of yet

1 Link Data Aggregator can serve 8 Detector Interfaces
Off Detector Receiver (ODR)

- Receives module data from Link Data Aggregator
  - PCI-Express card, hosted in PC.
  - 1-4 links/card (or more), 1-2 cards/PC
  - Buffers and transfers to store as fast as possible
- Sends controls and config to the Link Data Aggregator for distribution to the Detector Interfaces
- Performance studies & optimisation on-going

**Hardware:**
- Using commercial FPGA dev-board:
  - PLDA XPressFX100
  - Xilinx Virtex 4, 8xPCIe, 2x SFP (3 more with expansion board)
Off Detector Receiver - data access rate

transfer of the data from ODR memory to the user-program memory

=> >500 MByte/sec

All measurements: single requester thread, no disk write, data copied To the host memory.
Clock and Control (C&C) board

- C&C unit provides machine clock and fast signals to 8x Off Detector Receiver/Link Data Aggregator.

- Logic control (FPGA, connected via USB)

- Link Data Aggregator provides next stage fanout to Detector Interfaces
  - Eg C&C unit -> 8 LDAs -> 8 DIFs = 64 DUs.

- Signalling over same HDMI type cabling

- Facility to generate optical link clock (~125-250MHz from ~50MHz machine clock)

Board is already designed, will be built soon
Single Event Upset (SEU) Study

finalised, accepted by NIM

SEU cross section depending on
• FPGA type
• traversing particle (n,p,π)
• energy of traversing particle
=> need to study particle spectra
Single Event Upset (SEU) Study

Main backgrounds: (tt, WW and bhabha scattering also studied)
$\gamma\gamma$ (from beamstrahlung) -> hadrons

$\Rightarrow$ SEU rate of 14 min-12hours depending on FPGA type for the whole ECAL, needs to be taken into account in control software
$\Rightarrow$ fluence of $2\times10^6$/cm per year, not critical
$\Rightarrow$ radiation of 0.16Rad/year, not critical
$\Rightarrow$ occupancy of 0.003/bunch train (not including noise)

V.B, M.W. UCL
DAQ software

• Chose the DOOCS framework (http://tesla.desy.de/doocs/doocs.html), a distributed control system

• ENS naming service:
  Facility (F)/device (D)/location (L)/property (P)
  e.g. CALICE/ODR/ODR1/LDAX

• starting point:
  Off Detector Receiver Interface

• event builder needs to be modified

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Summary

- testbeam for the EUDET module in 2009

- prototypes of all hardware components (Detector Interface, Link Data Aggregator and Off Detector Receiver) built and tests started

⇒ Debugging and improving of each component before putting the components together

- Off detector software is in design phase
DAQ architecture

**Detector Unit**: Sensors & ASICs

**DIF**: Detector InterFace - connects generic DAQ and services

**LDA**: Link/Data Aggregator – fanout/in DIFs & drive link to ODR

**ODR**: Off Detector Receiver – PC interface for system.

**C&C**: Clock & Control: Fanout to ODRs (or LDAs)
backup slides
Overview

**Classic Design**
- Front-ends read out into on-detector data concentrators
- Data concentrators drive long links off detector
- Off detector assembly of complete bunch train data and event storage

**Points to note**
- Triggerless operation
- Inter-bunch-train gaps used to send data off detector
- Bunch train data processed/assembled near online asynchronously from readout
Link Data Aggregator (LDA)

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