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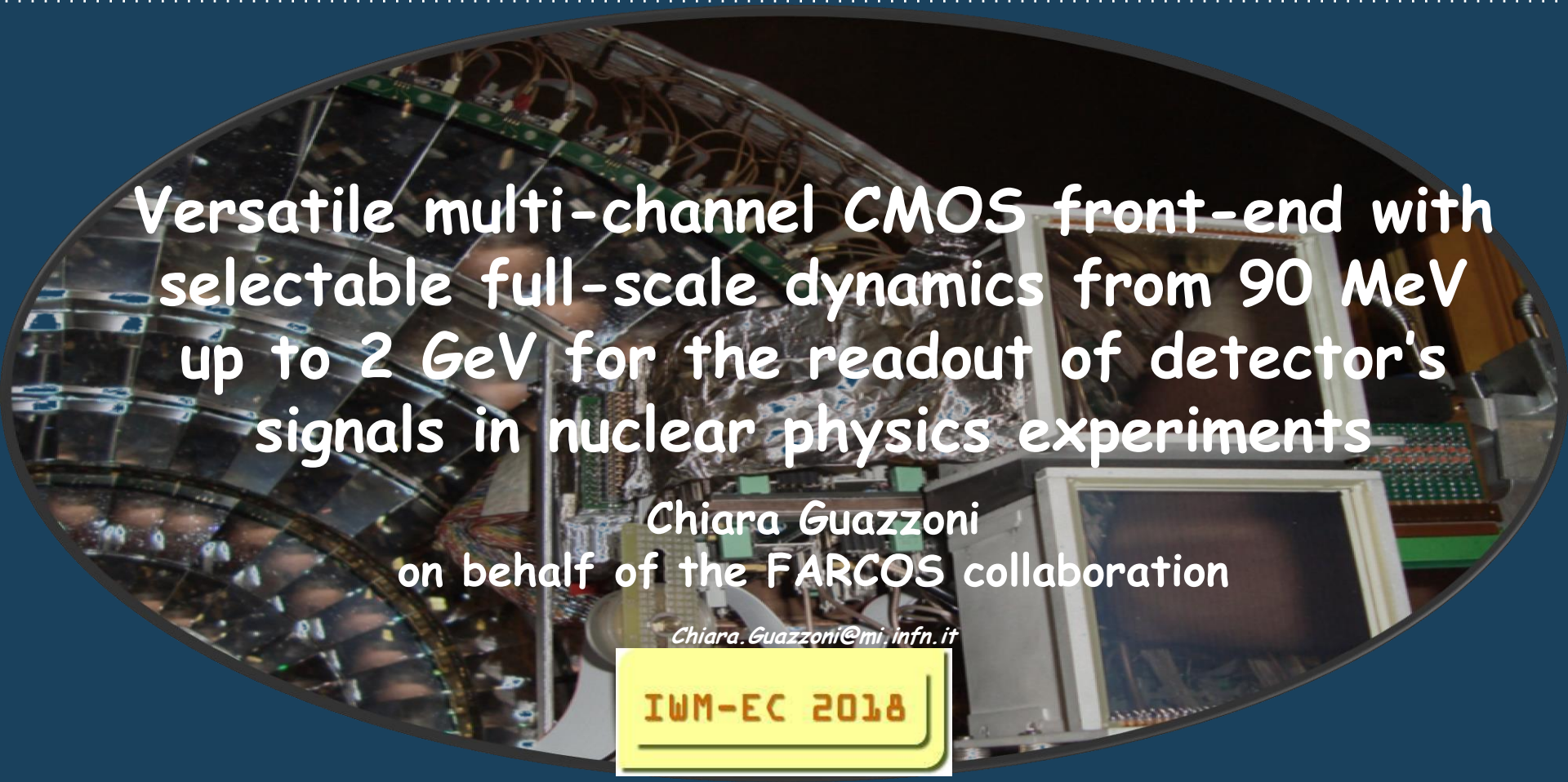

Versatile multi-channel CMOS front-end with selectable full-scale dynamics from 90 MeV up to 2 GeV for the readout of detector's signals in nuclear physics experiments

Chiara Guazzoni
on behalf of the FARCOS collaboration

Chiara.Guazzoni@mi.infn.it

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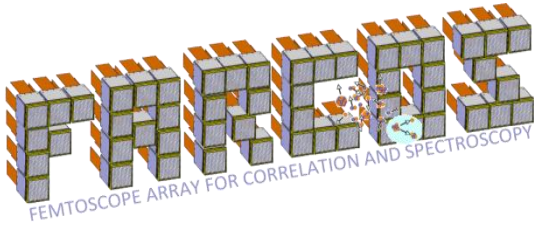
The FARCOS collaboration



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Universidad de Huelva
Univ. de Huelva

L. Acosta[b,a], L. Auditore[g], C. Boiano[c], G. Cardella[a], A. Castoldi[d,c], M. D'Andrea[a], E. De Filippo[a], D. Dell' Aquila[i], S. De Luca[g], F.Favela[a], F. Fichera[a], N. Giudice[a,f], B. Gnoffo[a,f], A. Grimaldi[a], C. Guazzoni[d,c], G. Lanzalone[h,e], F. Librizzi[a], I. Lombardo[i], C. Maiolino[e], S. Maffessanti[d,c], N. S. Martorana[f,a], S. Norella[g], A. Pagano[a], E. V. Pagano[f,e], M. Papa[a], T. Parsani[d,c], G. Passaro[e], S. Pirrone[a], G. Politi[f,a], F. Previdi[l,c], L. Quattrocchi[f,a], F. Rizzo[f,e], P. Russotto[e], G. Saccà[a], G. Salemi[a], D. Sciliberto[a], A. Trifirò[g], M. Trimarchi[g], M. Vigilante[i]

a. INFN, Sezione di Catania - Catania, Italy
b. Instituto de Física, Universidad Nacional Autónoma de México - Mexico City, Mexico
c. INFN, Sezione di Milano, Milano, Italy
d. Politecnico di Milano, Dip. Elettronica, Informazione e Bioingegneria
e. LNS-INFN - Catania, Italy
f. Dipartimento di Fisica e Astronomia, Universita' di Catania - Catania, Italy
g. INFN, Gr. coll. di Messina e Dip. di Scienze MIFT Universita' di Messina - Messina, Italy
h. Facolta' di Ingegneria e Architettura, Universita' Kore - Enna, Italy
i. INFN, Sezione di Napoli e Dip. di Fisica Universita' di Napoli Federico II - Napoli, Italy
l. Universita' degli Studi di Bergamo, Dip. Ingegneria gestionale, dell'informazione e della produzione, Bergamo, Italy

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Outline

- Motivation of the work
- The designed front-end:
  - architecture
  - designed ASIC
  - front-end board
  - slow control
- ASIC experimental qualification
- Use as FARCOS frontend electronics and coupling with the GET DAQ
- On-beam tests
- Conclusions and outlook

Motivation of the work

- With the advent of radioactive beams the nuclear physics community is active in developing **novel experimental methods and instruments** coping with beam characteristics to extract **spectroscopic information and** study **novel nuclear reaction mechanisms**.

- Nuclear particle physics instrumentation today require a **full cover of the available phase space** with good efficiency, angular, energy and particle identification capabilities.

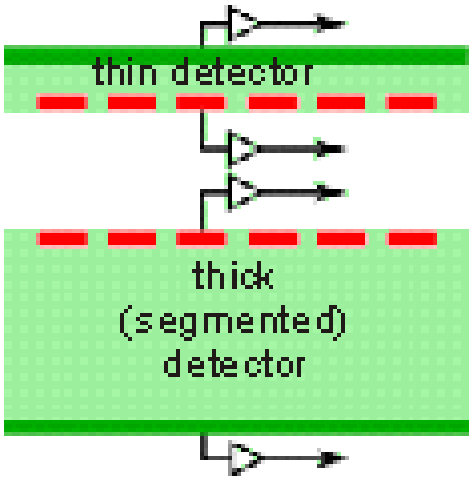
- From the **detector standpoint** this fact pushes towards the **use of multi-channel detectors** with moderately fine pitches. In addition **different types of detectors in very close geometry** around the target are required, often operating in vacuum.

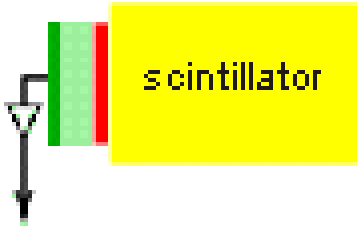
- The **tendency** is **towards Digital Pulse Shape Acquisition** – a powerful technique that opens the way to fully exploit the information encoded in the detector output response.

multi-channel, low-power, compact readout electronics is mandatory, pushing towards the integration of the front-end electronics in CMOS technology

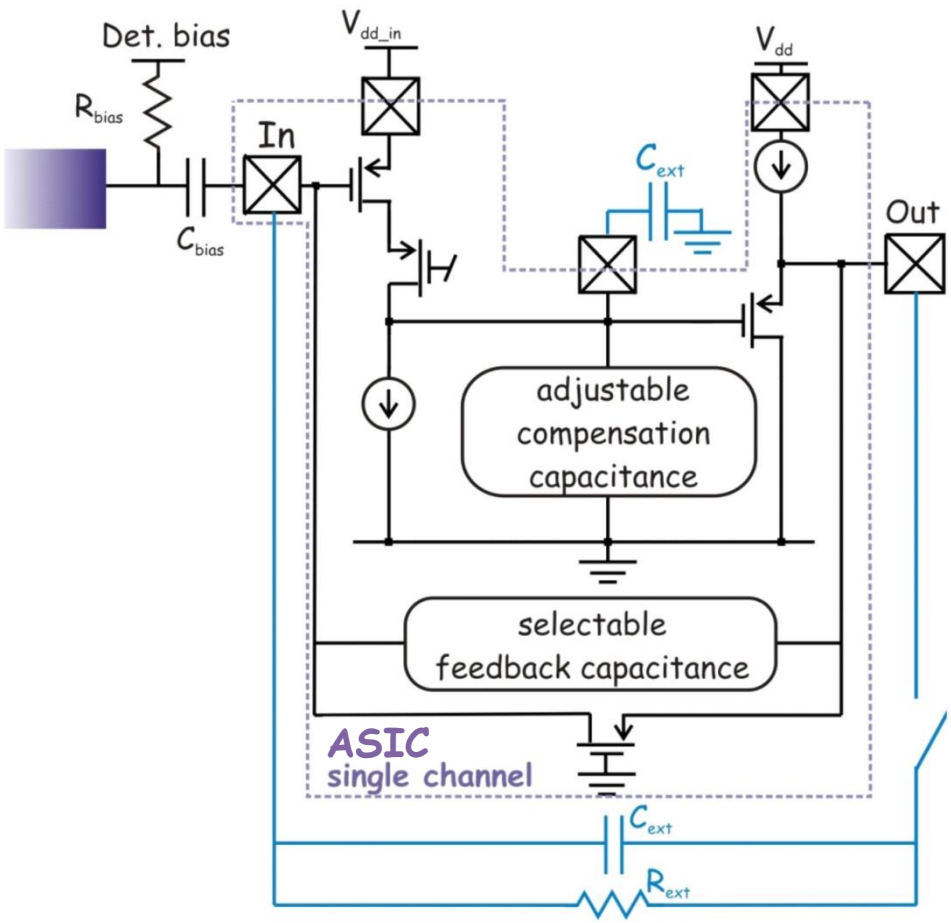
Design specifications

- **one design "fits-all"**, suitable to readout:
  - a **large variety of detectors** with **output capacitance in the range 10 pF - 200 pF**
  - **signals of both polarities** to ease spare management and reduce costs.
- **suitable for pulse shape technique:** front-end amplifies the whole signal waveform without amplitude and shape distortion.
- **digitally selectable full-scale energy range** at 0.5% INL: **90 MeV, 200 MeV, 350 MeV, 500 MeV and 2 GeV** to cope with different experimental requirements.
- **static power consumption** of about **10 mW/channel**.
- **single-channel** ASIC **or multi-channel** ASIC of 8 or 16 channels to cope with different detector types.
- zero-capacitance 20%-80% rise time below 10 ns to cope even with fast charge collection times.



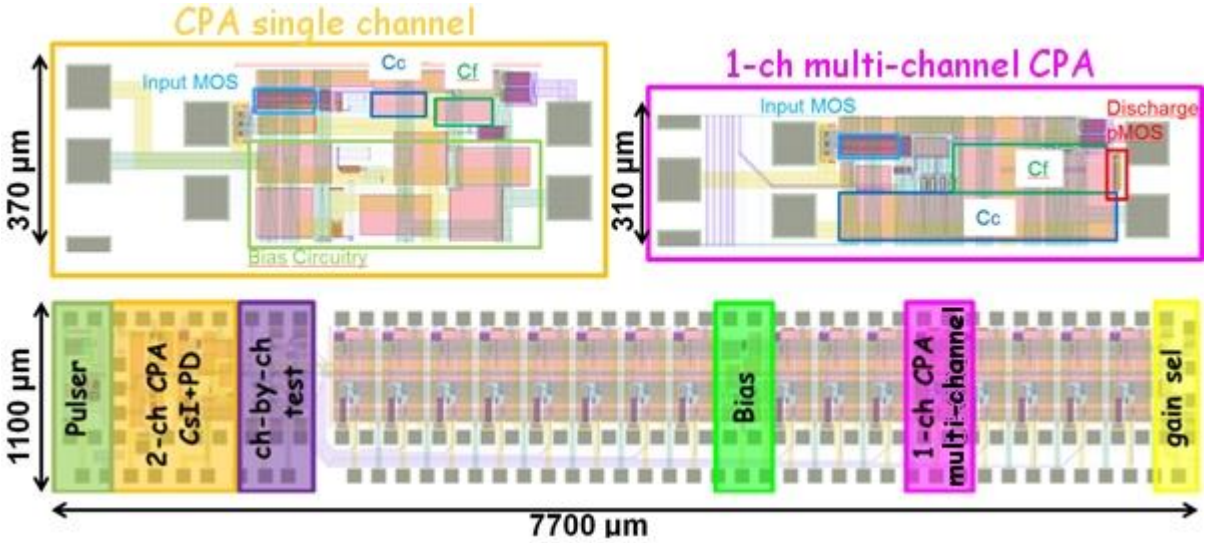


Architecture of the designed frontend



- **charge preamplifier** configuration
- **DC** coupled **or AC coupled**, with external capacitor and biasing resistor
- **telescopic cascode** architecture
- independent biasing of the first branch to cope with the requirement of a single chip to readout both signal polarities
- different feedback networks:
  - external feedback resistor
  - on-chip MOS transistor
- **selectable feedback capacitance** & adjustable compensation network
- **limited power dissipation** (<10mW/ch): first transistor in moderate-weak inversion

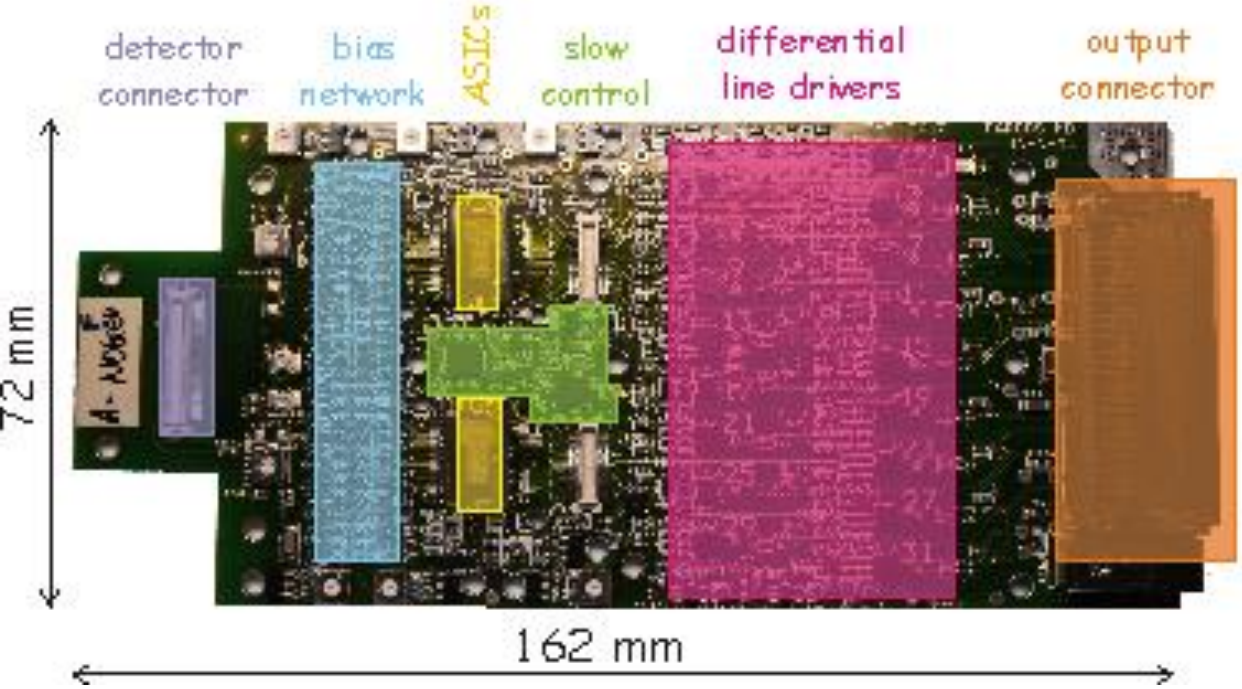
Designed multi-channel ASIC



G	FSR (MeV)	Sensitivity (mV/MeV)	Sensitivity (mV/pC)	Feedback cap. (pF)
0	**90**	**11.11**	250	4
1	**200**	**4.44**	100	10
2	**350**	**2.78**	62.50	16
3	**500**	**2.02**	45.45	22
4	**2000**	**0.49**	11.11	90

- The chosen **technology** is the **ams CMOS C35B4C3** (3.3 V supply voltage, 0.35 µm minimum feature size, 4 metal layers, high resistivity poly, poly precision capacitors)
- A complete stand-alone channel is 1000 µm wide and 370 µm long, including all needed services.
- The designed preamplifier can be used to assemble **multi-channel chips**, at present **up to 16-channel ASICs** have been designed and tested with an occupied area that can be as low as 5270 µm × 1000 µm.
- Each chip foresees **additional services**, like an **on-chip pulser**, a channel-by-channel **test signal injection system** and a **temperature monitor**.

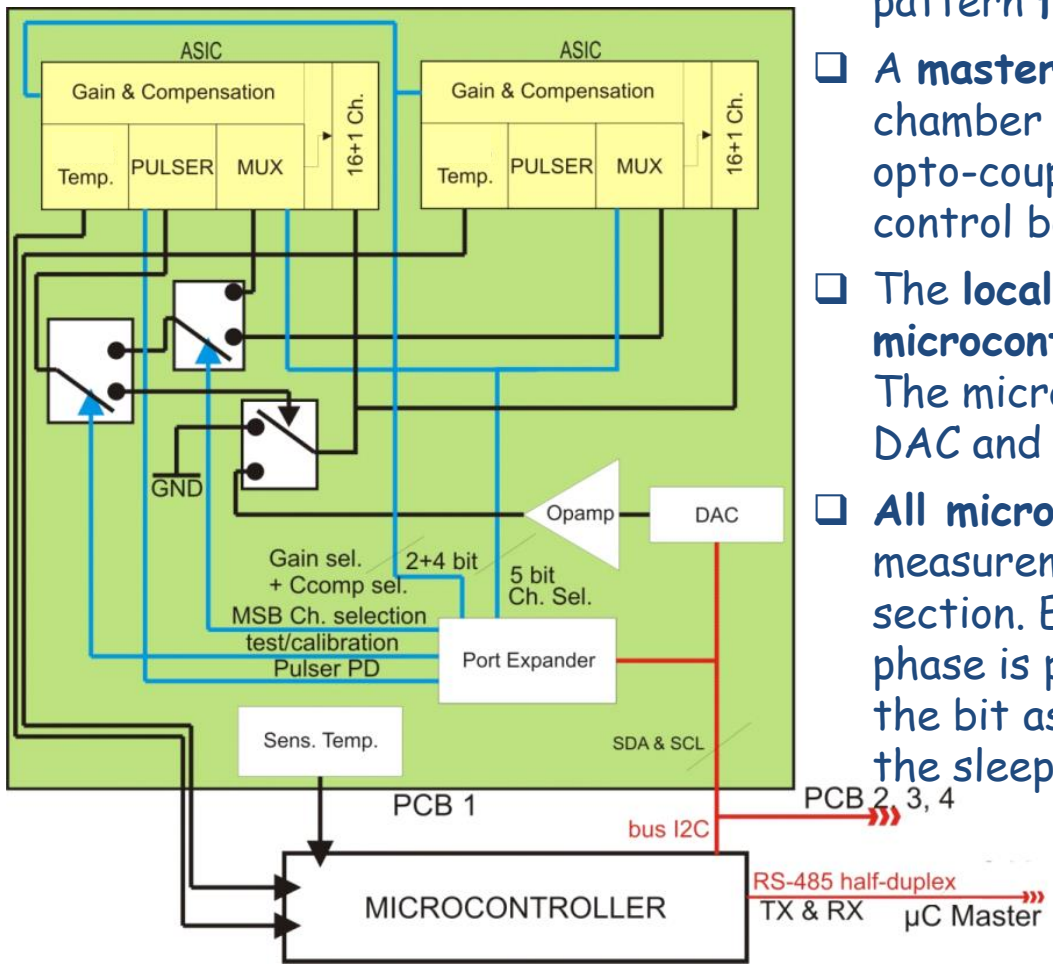
Front-end board



- A **custom** designed 8-layer **PCB** houses two (16 + 1) channel ASICs and **reads out 32+2 detector channels** (e.g. one DSSSD side and of one/two CsI(Tl) in the case of the FARCOS telescopes).
- **Differential line drivers** (ADA 4940) drive the signals coming from the ASIC towards the output of the vacuum chamber.

- Hi-Density right-angle open-pin-field connectors (Samtec SEAF-30-01-L-06-1-RA-TR) interconnect the motherboard with the slow control board. Other input/output connectors are possible.
- A **dedicated calibration circuitry** is placed on the front-end board in order to ease the debug and the calibration of the full system during mounting and data taking. The full calibration routine as well as the telescope slow control is handled by a microcontroller placed on the slow-control board.
- The ASIC supply voltages are generated locally on board to minimize disturbances.

Front-end Slow Control

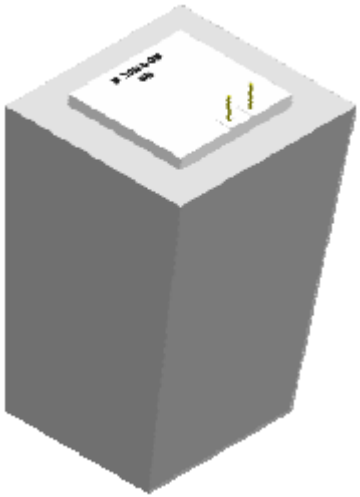


- **Monitor** ASIC and board **temperature**.
- **Sets** all the ASIC **control bits**.
- Provides **input** test **signals** according to a given pattern **for system calibration**.
- A **master microcontroller outside** the **vacuum** chamber and communicating via IEEE 485 (through opto-couplers) to the host PC and to each slow control board oversees the slow control system.
- The **local** cluster slow control is based on the **microcontroller** housed on the slow control board. The microcontroller communicates via I^2C to the DAC and the port expander present on each PCB.
- **All microcontrollers** are **in sleep mode** during measurement to prevent pick-ups from the digital section. Each DAC at the end of the calibration phase is powered down. The port expander keeps the bit assignment when the microcontroller enters the sleep mode.

ASIC experimental qualification

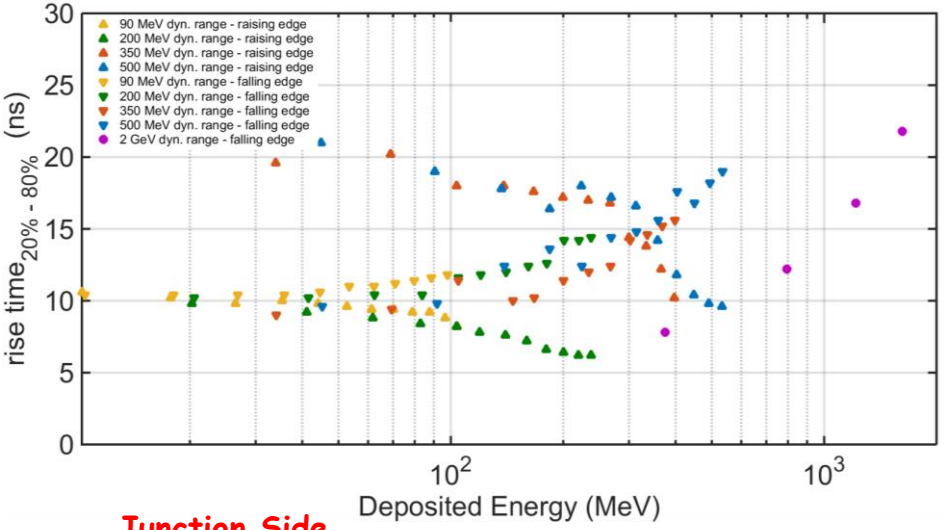
- We fully characterized different versions of the chip standalone, with a detector-like input load capacitance and coupled with different detectors prototypes:
  - 300 μm thick DSSSDs - BB7 design provided by Micron Semiconductor Ltd.
  - 1500 μm thick DSSSDs - BB7 design provided by Micron Semiconductor Ltd
  - 1.8 × 1.8 cm^2, 300 μm thick Silicon PIN diode provided by Hamamatsu (S3204-08), optically coupled with a 3.2 × 3.2 cm^2, 6 cm thick CsI(Tl) scintillator crystal.
  - 1 cm^2, 300 μm thick Silicon PIN diode provided by Hamamatsu (S3590-09)

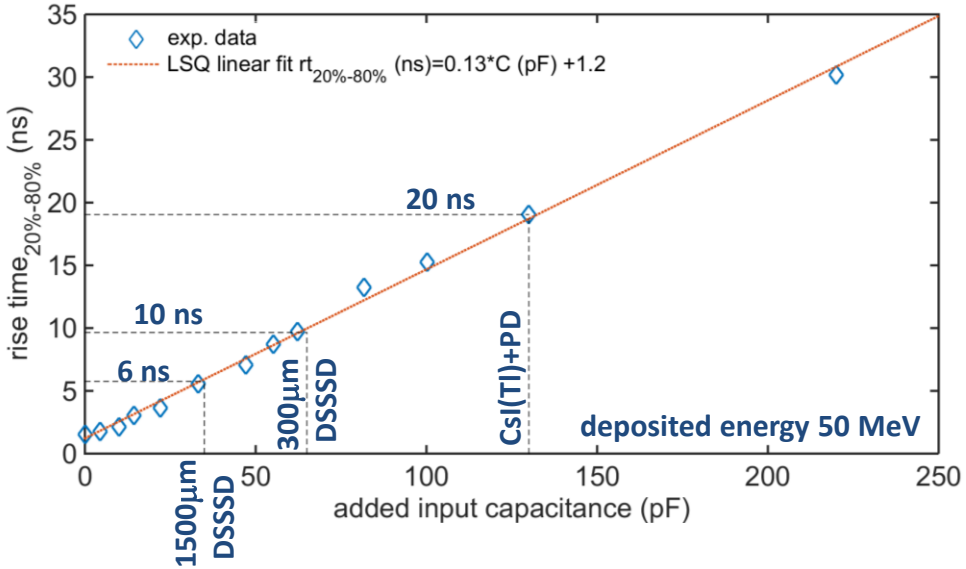
Photograph of one 300 μm thick DSSSD – BB7 design.



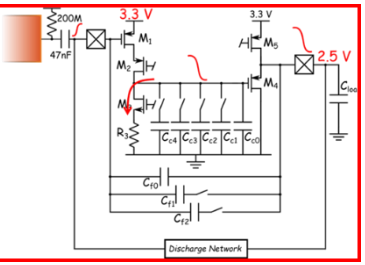
3D rendering of a CsI(Tl) scintillator crystal.

ASIC experimental qualification – Rise/Fall Time



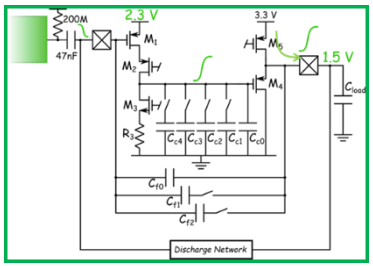


Junction Side



input transconductance decreases as signal amplitude is increased

Ohmic Side

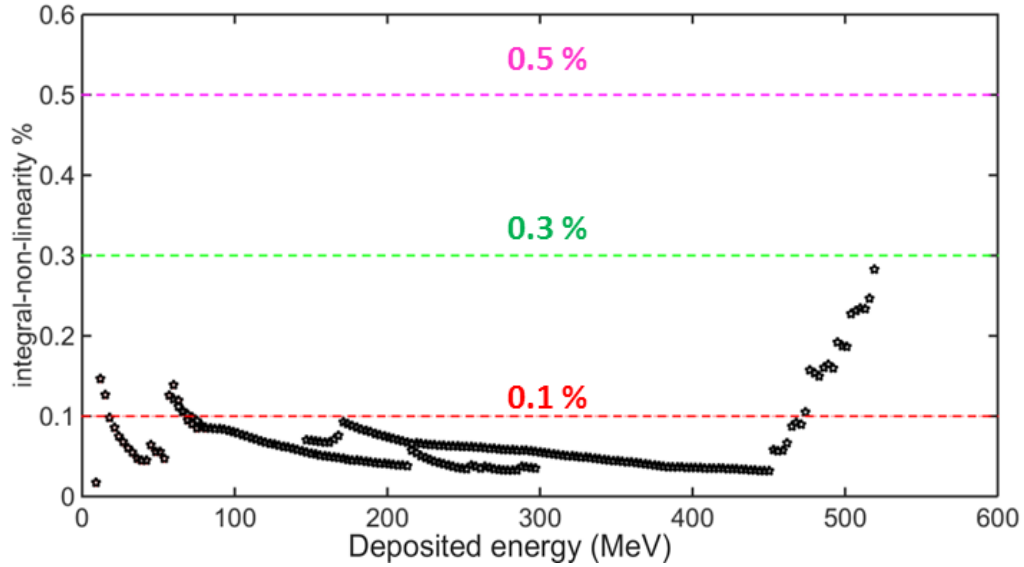


input transconductance increases as signal amplitude is increased

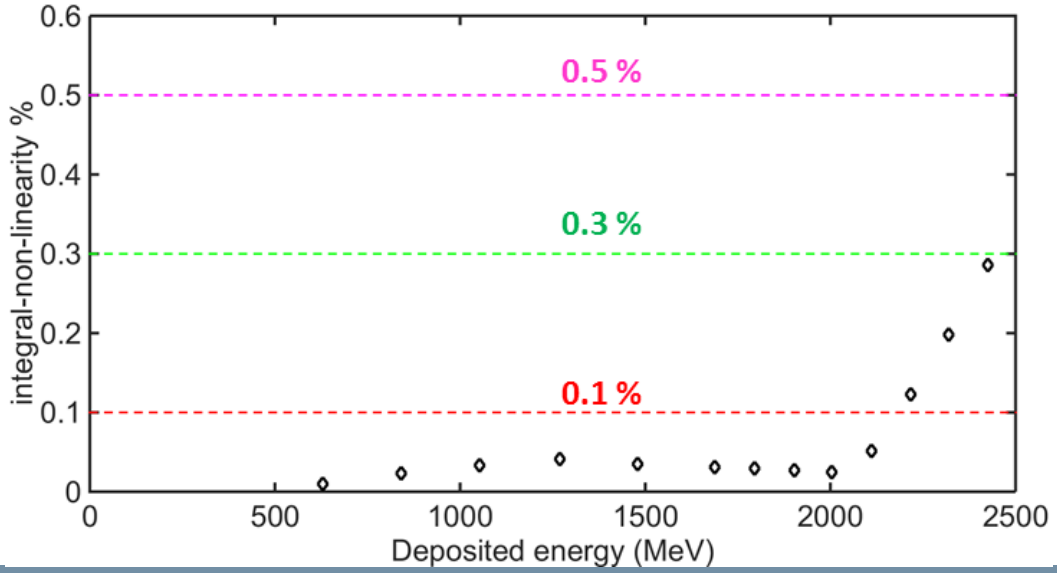
- measured with 65 pF input capacitance (300 µm DSSSD – BB7 design)
- up to 500 MeV dynamic range rise time below 20 ns & no slew rate limitation
- at 2 GeV (falling edge) rise time below 30 ns
- slope dependent on level of compensation capacitance needed
- versatile frontend for input capacitances in the range 10pF - 220pF

ASIC qualification – Integral-Non-Linearity

500 MeV Range



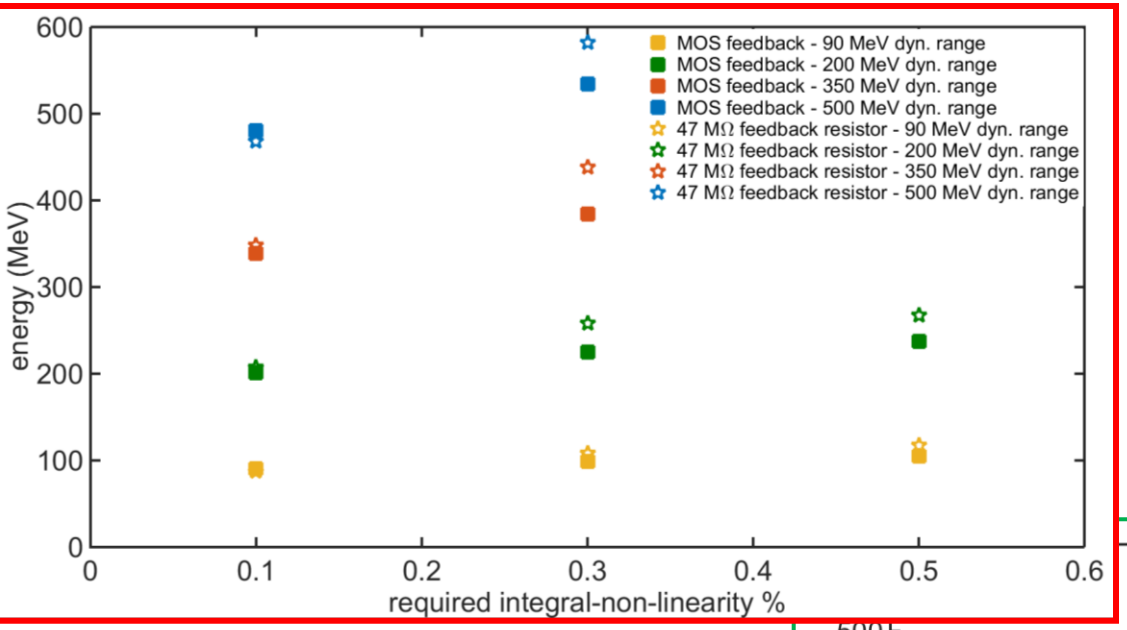
2 GeV Range



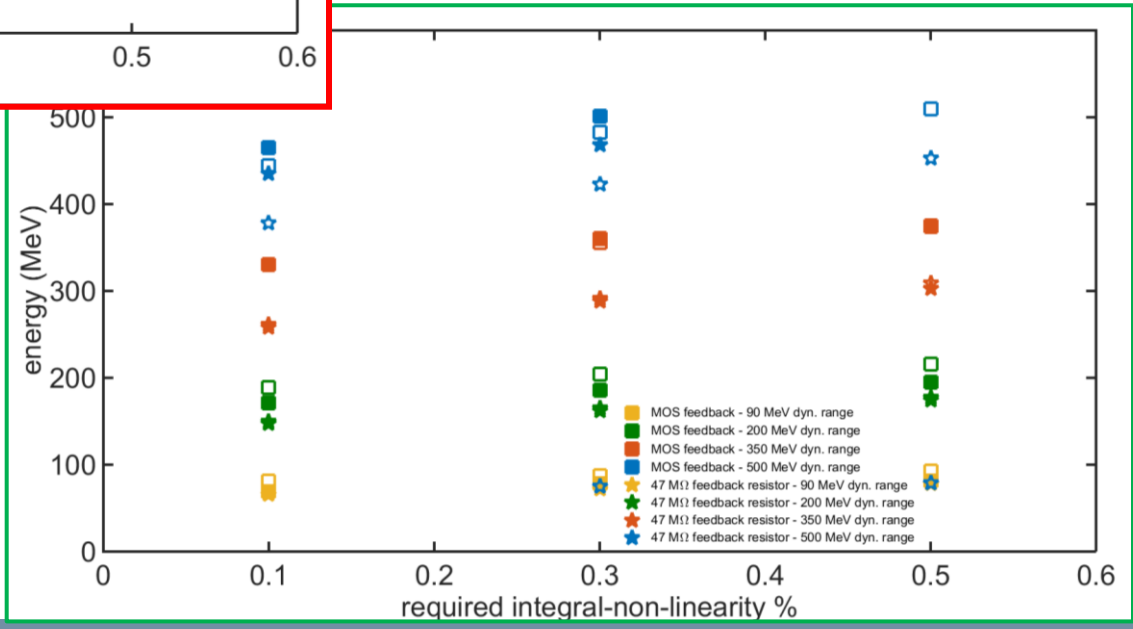
- for every input signal amplitude, the integral-non-linearity is computed as the maximum deviation from the linear LSQ fit up to the considered amplitude
- integral-non-linearity assessed both via electrical injection and verified up to more than 500 MeV with a pulsed 3 MeV proton beam with variable bunch multiplicity (from 1 proton up to more than 200 protons) at the DeFEL beamline of LaBeC, INFN, Firenze (Italy).

ASIC qualification – Integral-Non-Linearity

Junction Side

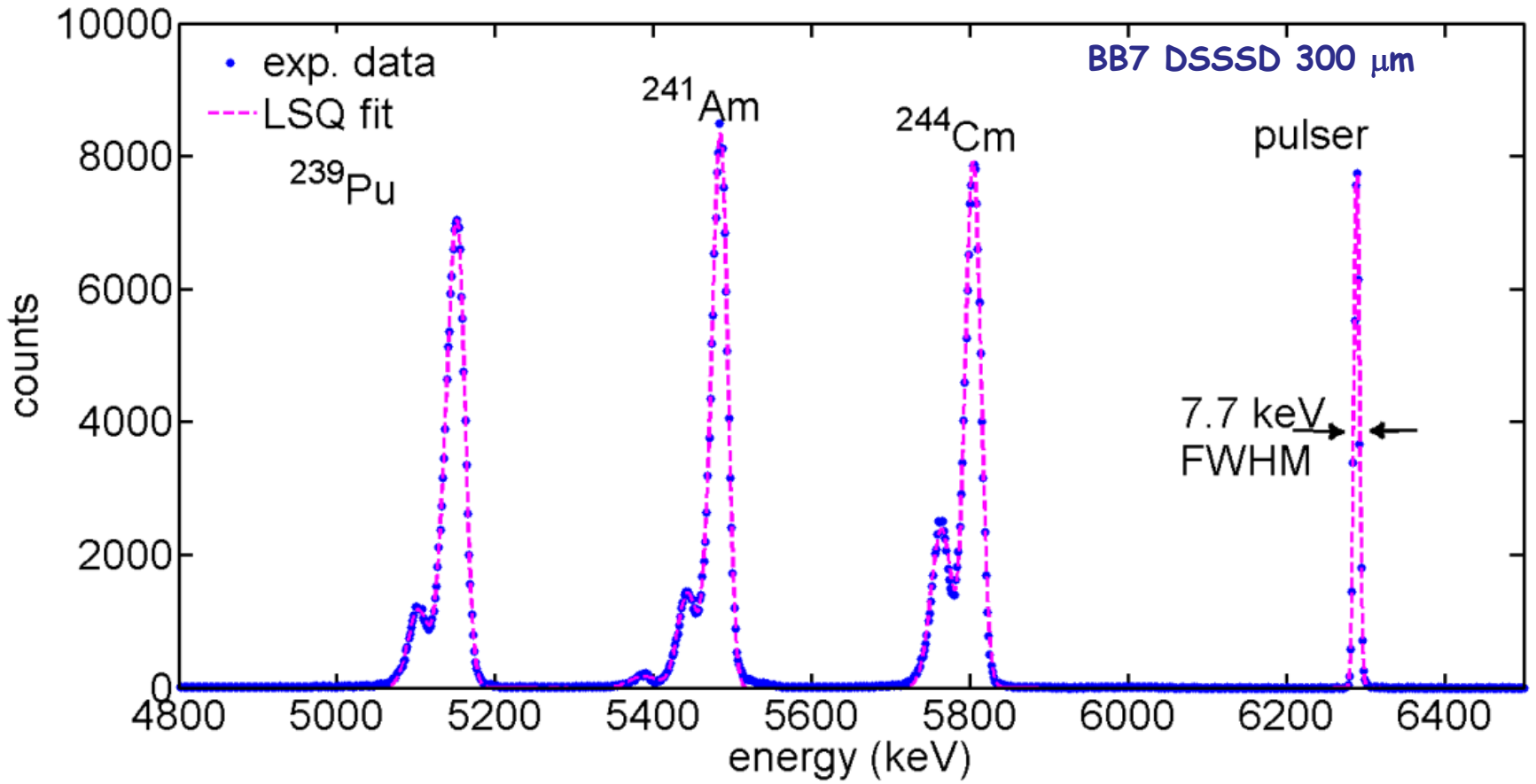


Ohmic Side



- INL < 0.5% over all the designed energy ranges for both signal polarities and all detectors

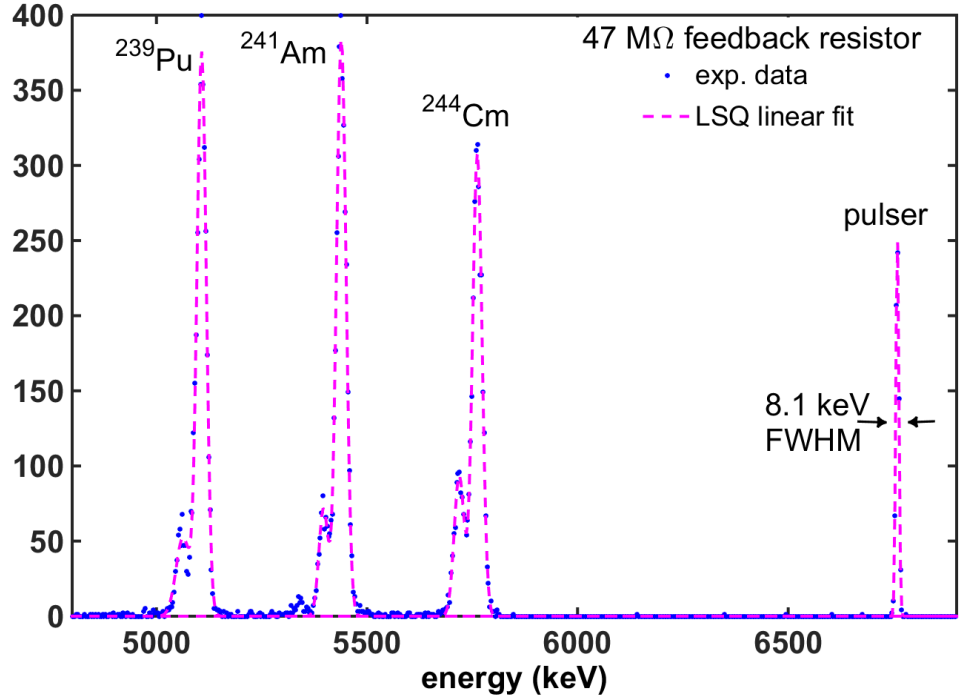
ASIC experimental qualification – Energy Resolution



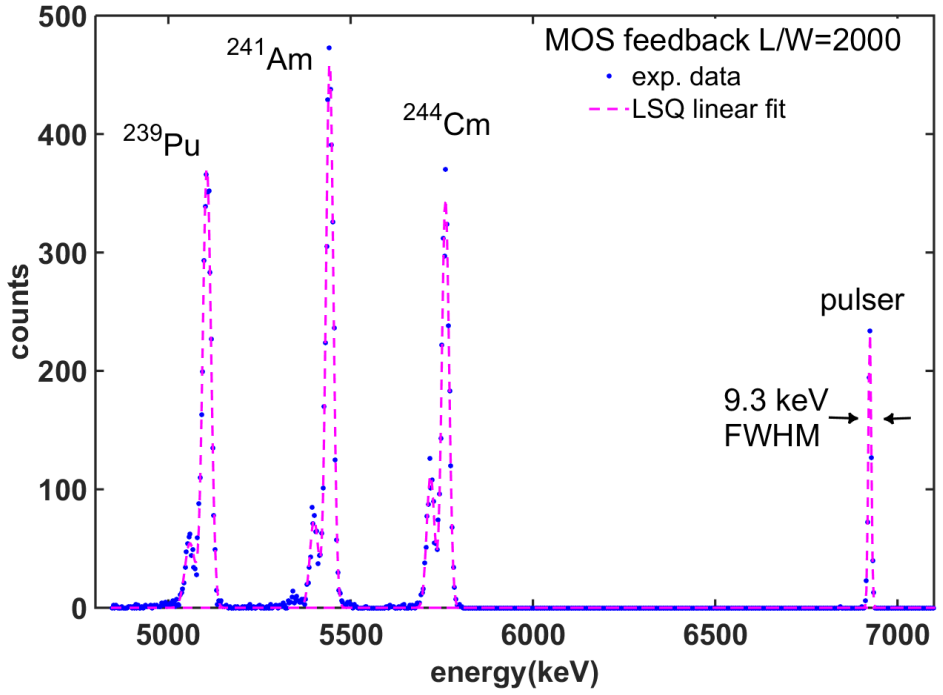
- **7.7 keV FWHM** (pulser) measured in the lab with **300 μm BB7 DSSSD** (junction side strips, ext. resistor feedback, 90 MeV dynamic range)

ASIC experimental qualification – Energy Resolution

- resistive feedback (junction side)



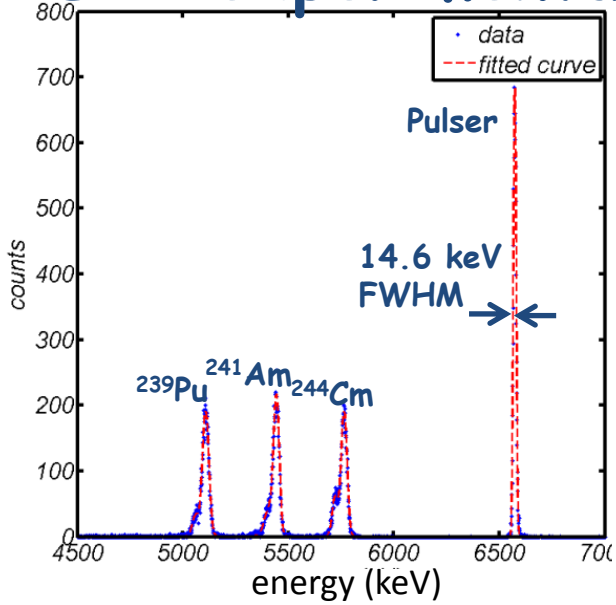
- MOS feedback (junction side)



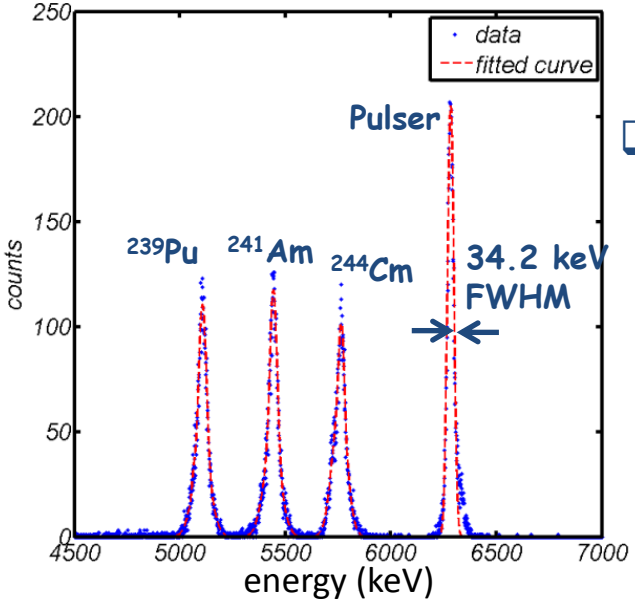
- 300 μm BB7 DSSSD illuminated with a mixed nuclei α source at the DEFEL beamline at LaBeC, INFN, Firenze, Italy.
- all channels in operation (4 × 16 channels ASICs).

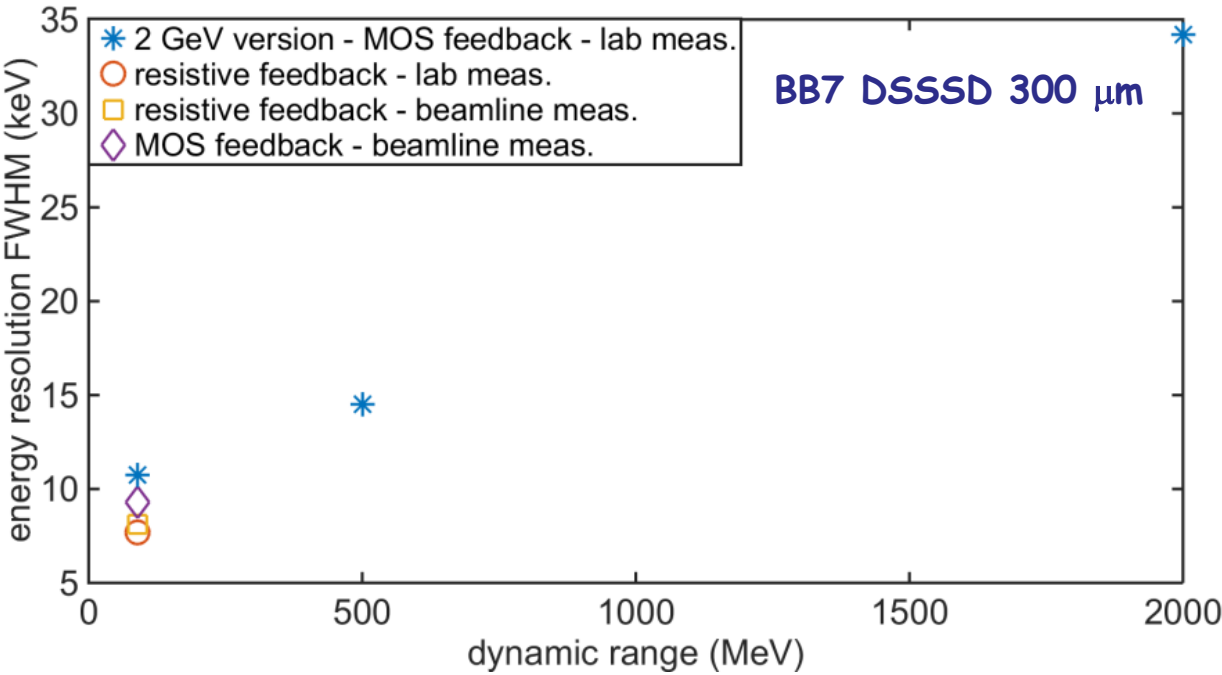
ASIC experimental qualification – Energy Resolution

500 MeV Range – T_{sh} = 6 µs



2 GeV Range – T_{sh} = 12 µs

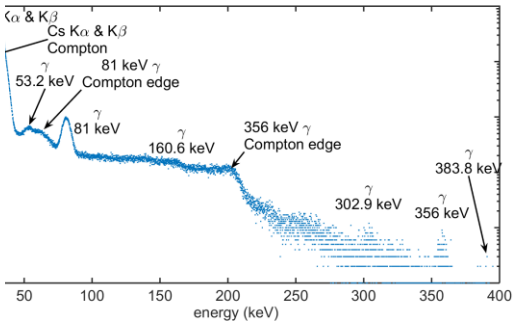




- energy resolution (coupled with the BB7 300µm thick DSSSD):
  - ≤ 10 keV FWHM at 90 MeV full-scale energy range
  - ≤ 15 keV FWHM at 500 MeV full-scale energy range
  - ≤ 35 keV FWHM at 2 GeV full-scale energy range

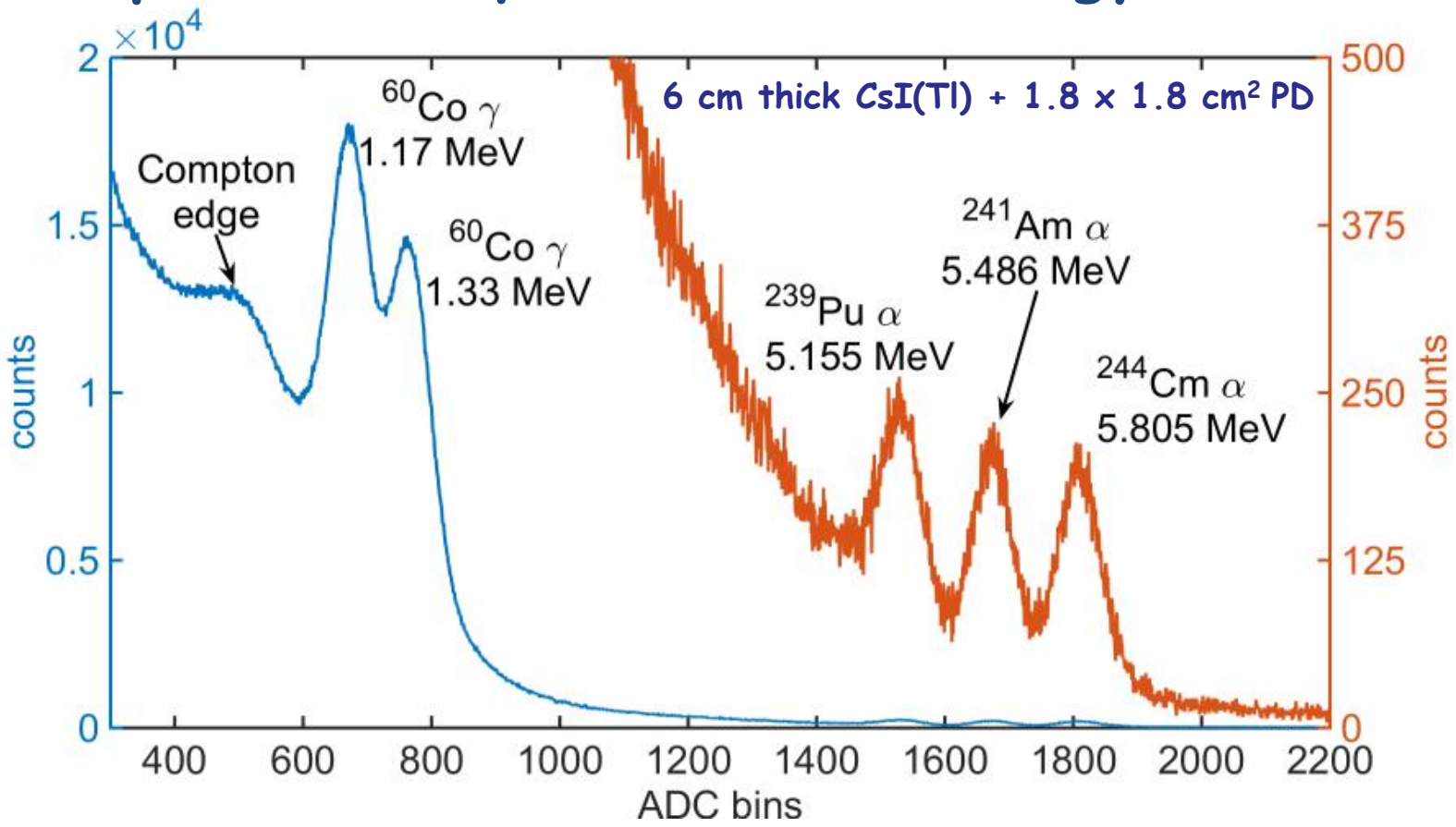
ASIC experimental qualification – Energy Resolution

1cm² 300μm thick Si photodiode



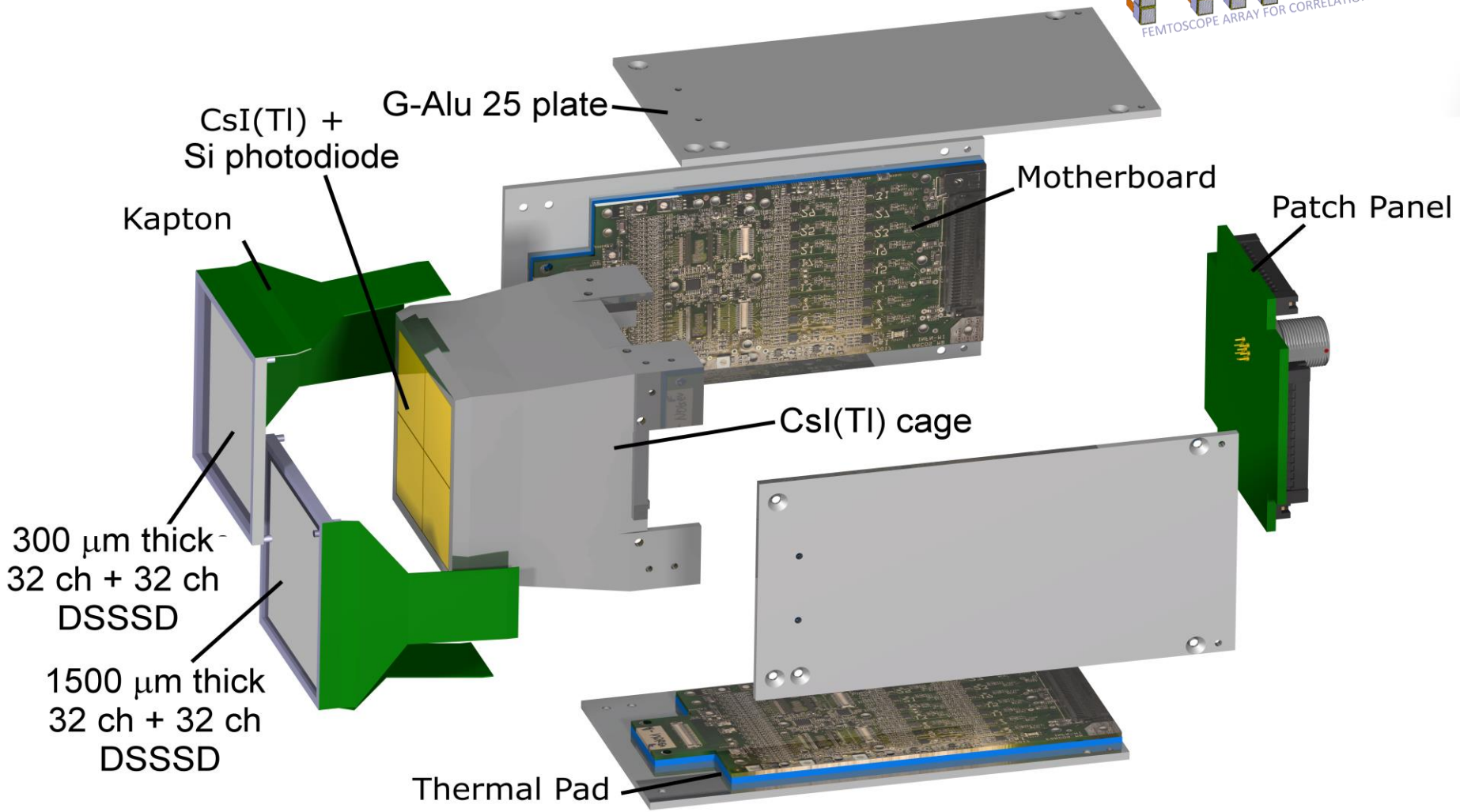
- Collected spectrum of a ^{133}Ba source measured with the proposed frontend and a **1 cm² photodiode** (Hamamatsu S3590-09) **at room temperature**. The output signal is shaped with a 5th order pseudo-Gaussian shaper at 1 μs shaping time.
- The **achieved energy resolution** at the **Cs-Ka line** is **7.8 keV FWHM**.

ASIC experimental qualification – Energy Resolution



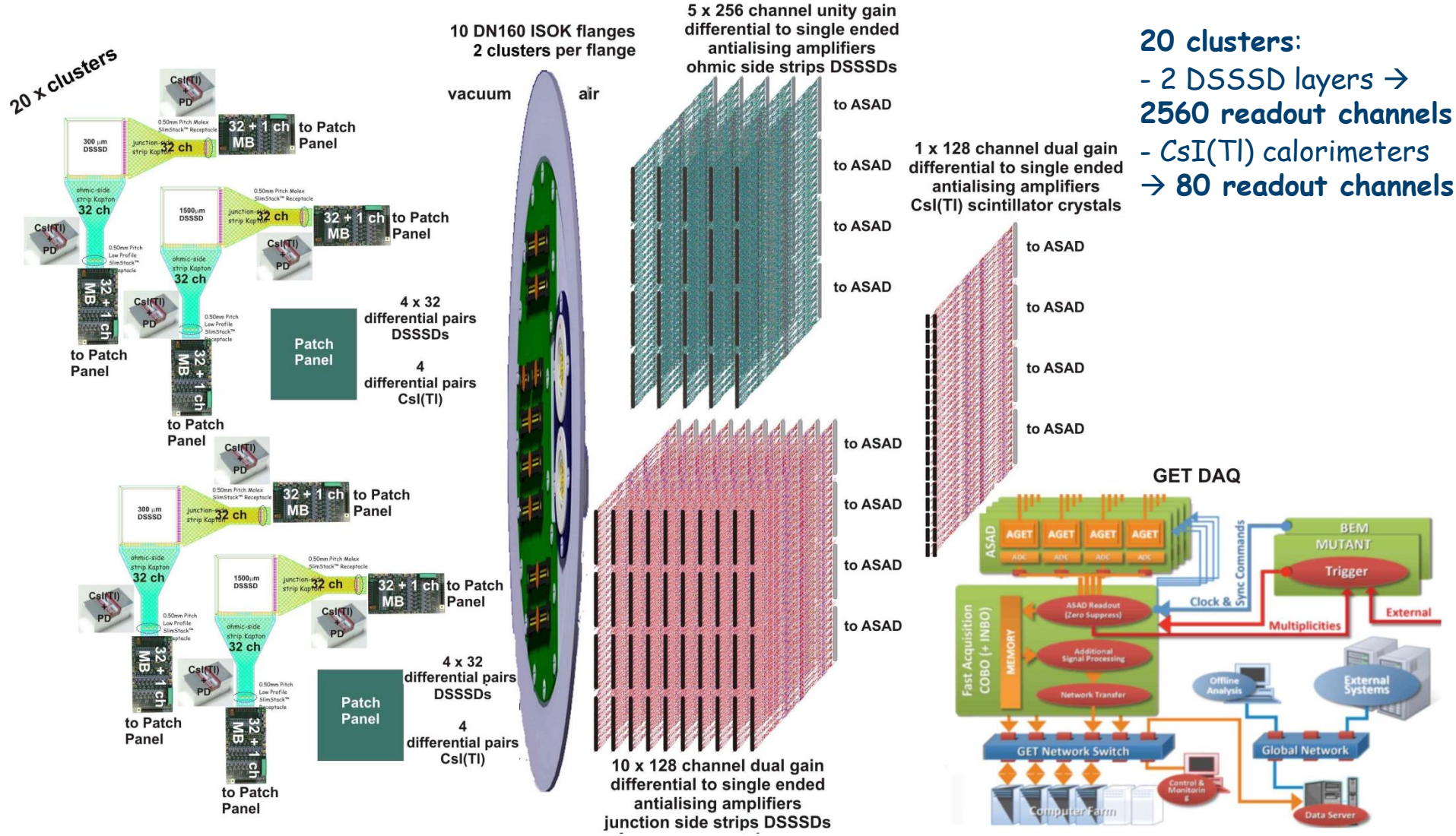
- **179 keV FWHM** measured in the lab at the ^{241}Am α line with **CsI(Tl) scintillator 6 cm thick coupled with 1.8 cm x 1.8 cm PD**
  (ext. resistor feedback, 90 MeV dynamic range)

The FARCOS frontend electronics



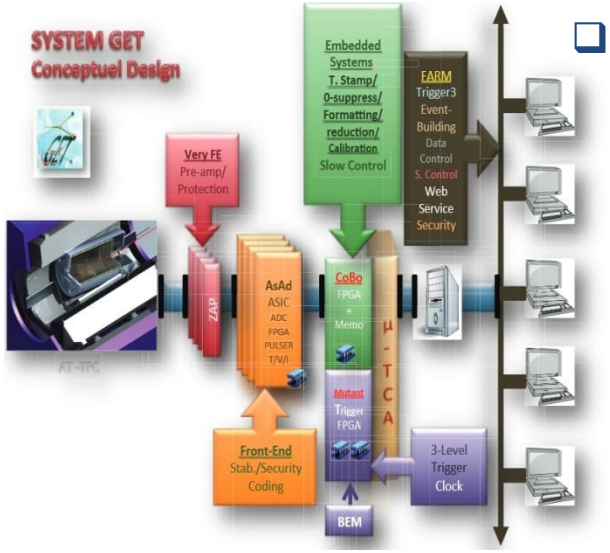
The FARCOS frontend electronics

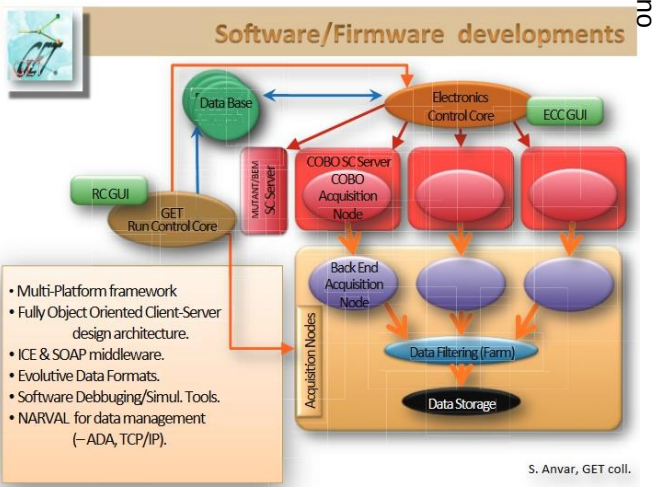
FARCOS
FEMTOSCOPE ARRAY FOR CORRELATION AND SPECTROSCOPY



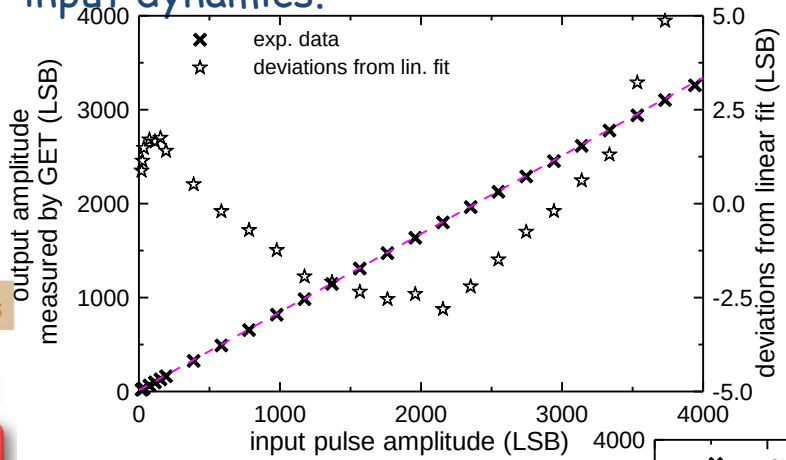
20 clusters:
- 2 DSSSD layers →
2560 readout channels
- CsI(Tl) calorimeters
→ **80 readout channels**

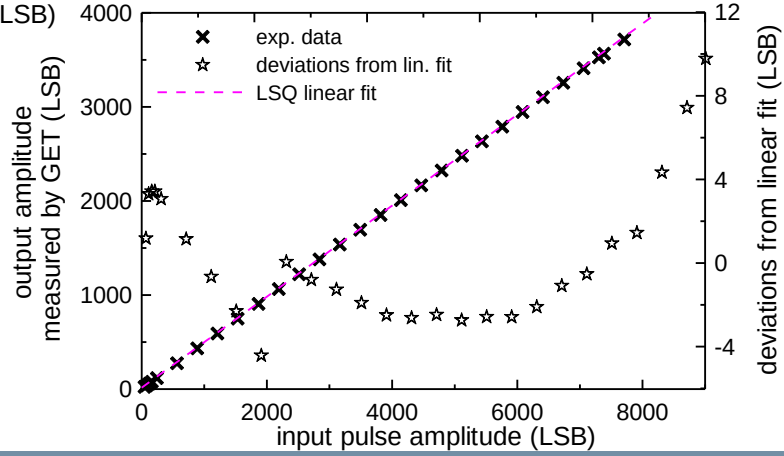
Coupling with the GET backend electronics





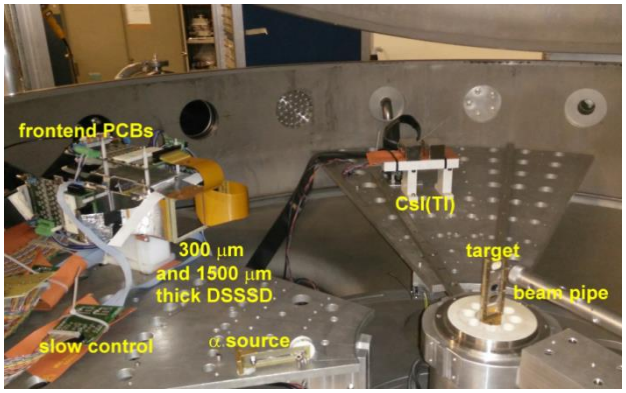
- We probed the performance of the developed frontend when coupled to the GET backend electronics (0.75V input dynamics) by means of a custom antialiasing module that provides 256 channel antialiasing filter with selectable parameters and differential input responsible also of adapting with the GET input dynamics.

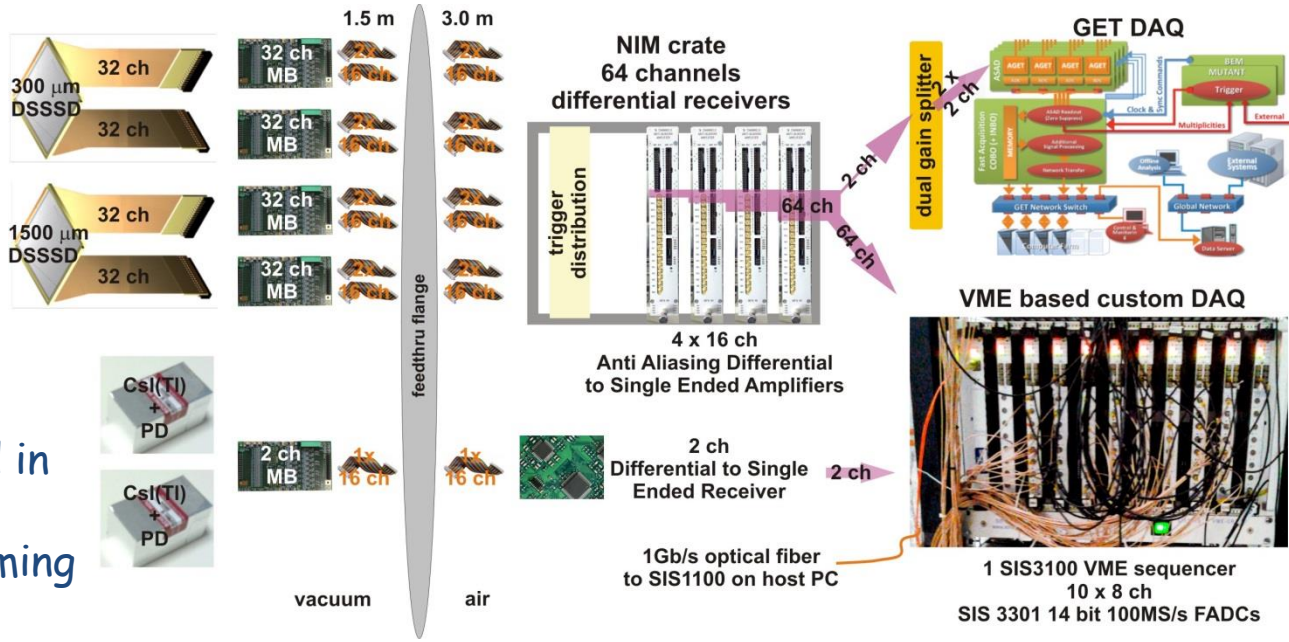




E. Pollacco e al., «GET: A Generic Electronic System for TPCs for nuclear physics experiments,» *Physics Procedia*, vol. 37, pp. 1799-1804, 2012.

On-beam tests: experimental setup w/ FARCOS



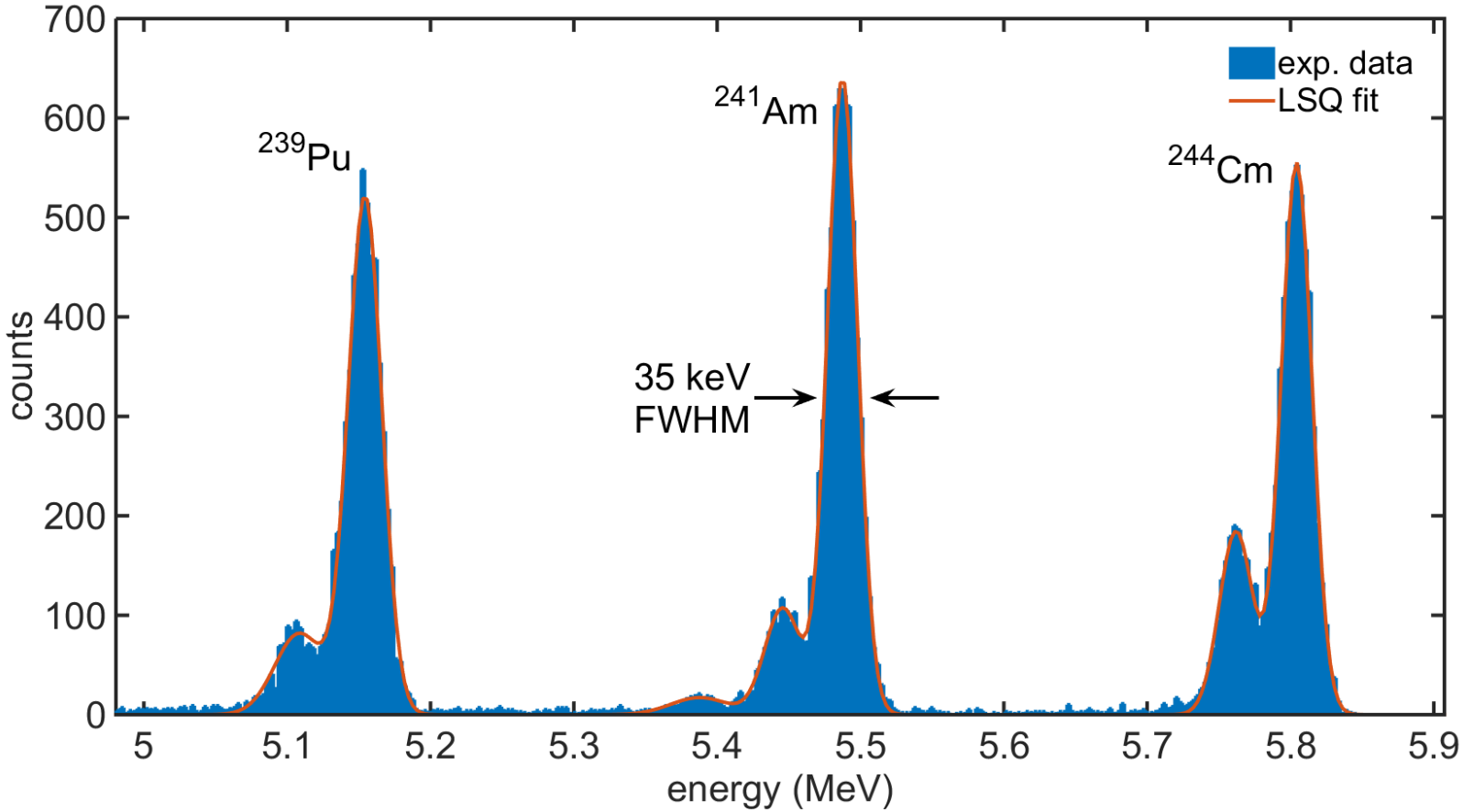


- 300 μm and 1500μm thick FARCOS DSSSD assembled in telescope configuration and located at 30° wrt the incoming beam
- CsI(Tl) crystals located at the same angle on the opposite side.
- February 2017, test beam at the Laboratori Nazionali del Sud in Catania.
- Setup in CT-2000 chamber, placed at the end of the 60 degree beamline.
- Tandem ^{16}O beam at 88 MeV impinged on different targets: LiF, Au, C, Ni.
- mixed nuclei radioactive α source permanently located inside the vacuum chamber

Sketch of the experimental configuration with the different detectors, the frontend electronics and the two different DAQs.

- End of May 2018, parasitic data taking with one FARCOS telescope during EQUIL2 beamtime.
- Setup in the CHIMERA chamber
- Tandem ^{12}C beam at 55 MeV and ^{40}Ca & ^{48}Ca CS beams at 40AMeV

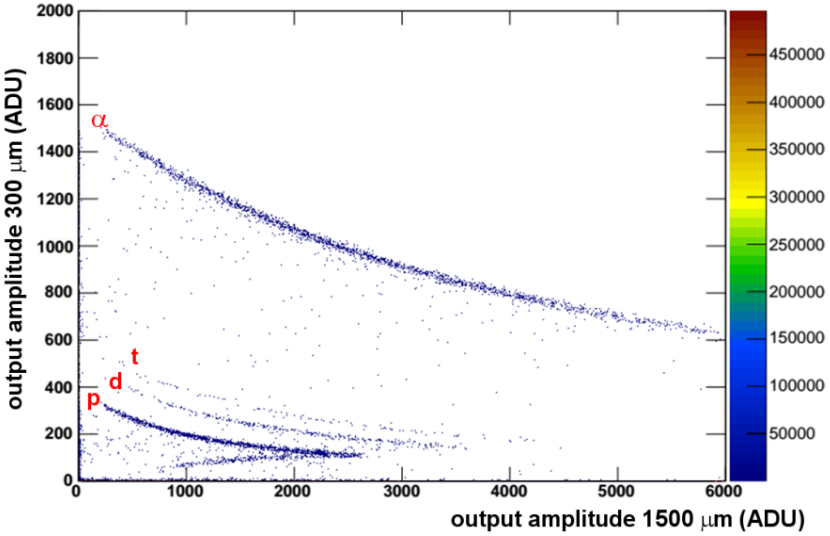
On-beam tests: Energy Resolution



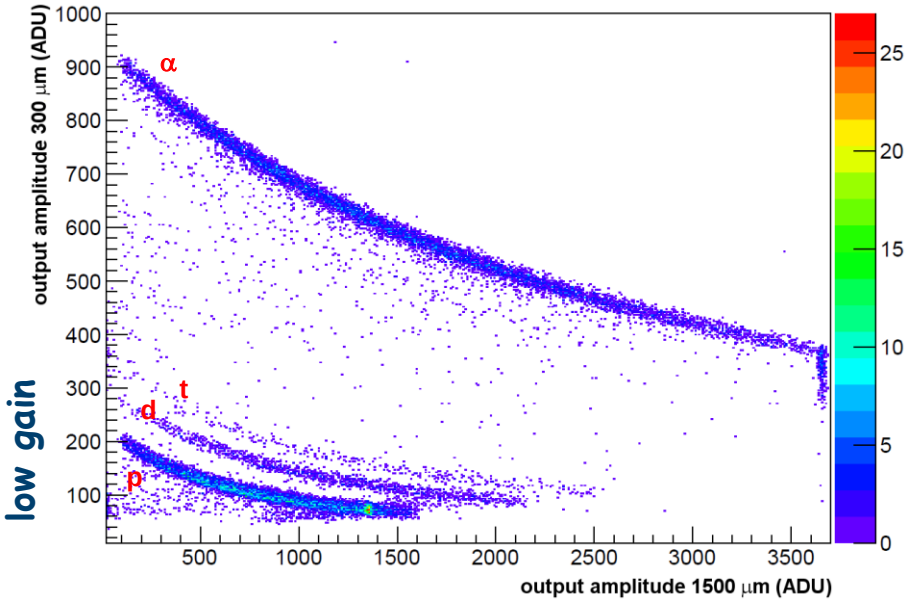
- measured mixed nuclei α source energy spectrum at one of the 300 μm thick DSSSD channel as acquired with the 14 bits DAQ.
- energy resolution mainly limited by the line broadening within the radioactive source.

On-beam tests: ΔE-E

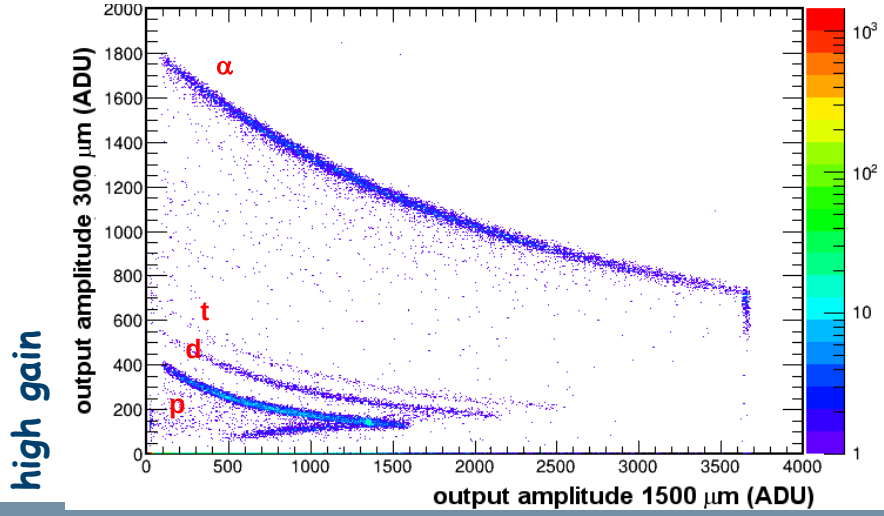
- 14-bit DAQ



- GET DAQ 12-bit

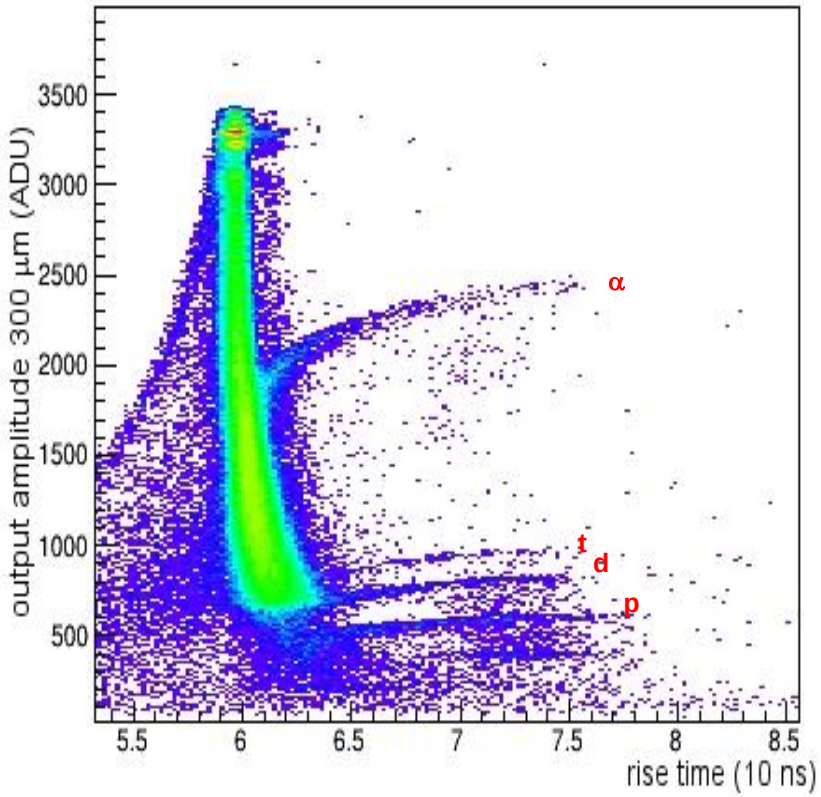


- ΔE-E (300 μm and 1500 μm thick FARCOS DSSSDs) identification plot as acquired with the two DAQ in the case of a LiF target.
- protons, deuterons, tritons and α nicely gather as expected
- punching through used for calibration.

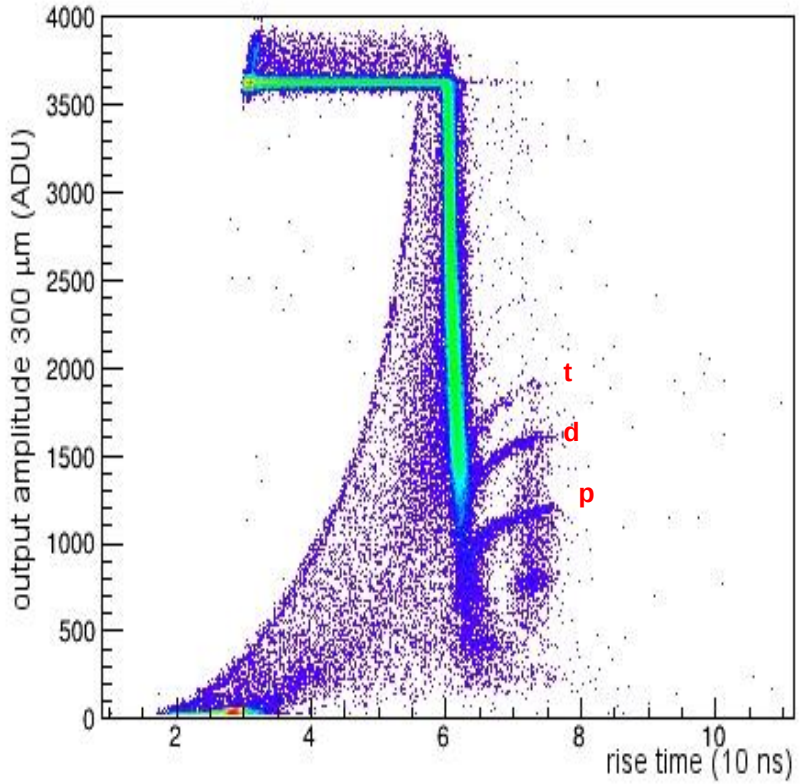


On-beam tests: Energy – Rise Time

low gain



high gain



- Preliminary Energy – Rise Time identification plot for one strip of the 300 µm thick DSSSD (front injection) in the case of a 88 MeV ^{16}O beam impinging on a LiF target
- The output of the charge preamplifier has been fast (100 MSps) digitized at 12/bit with the GET electronics and digitally filtered.
- Performance limited by non adequate filter shape.

Conclusions and outlook

- ✓ We developed a **compact** and **versatile multichannel CMOS front-end** with **electronically selectable** full-scale **energy range** from **90 MeV up to 2 GeV** for the readout of detector's signals in nuclear physics experiments.
- ✓ A **built-in pulser** accounts **for** system **debugging and calibration**.
- ✓ A **single ASIC design** reads out **signals of both polarities**, from **different detector types** (pn diodes, DSSSDs of different thicknesses, scintillators coupled with photodiodes…) with output **capacitances** in the range **10pF - 220pF**.
- ✓ Measured performance:
  - **rise-time 20%-80% ≤ 20ns up to 500 MeV** full-scale energy range,
    ≤ 30 ns up to 2 GeV full-scale energy range
  - **INL < 0.5%** over different energy full scale ranges **up to 2 GeV**
  - **energy resolution (coupled with the BB7 300μm thick DSSSD)**
    ≤ 10 keV FWHM at 90 MeV full-scale energy range
    ≤ 15 keV FWHM at 500 MeV full-scale energy range
    ≤ 34 keV FWHM at 2 GeV full-scale energy range
  - **power consumption ≤ 10mW/ch**
- ✓ **32-channel front-end board** ready to use
- ✓ The designed frontend will readout all the FARCOS channels:
  - **DSSSD**: (20 telescopes × 2 layers × 32 channels/side × 2 sides) = **2560 channels**
  - **CsI(Tl)**: (20 telescopes × 4 CsI(Tl)) = **80 channels**

Acnowledgement

- Andrea Capsoni and mechanical workshops of INFN, Sezione di Milano and Sezione di Catania
- Luca Carraresi for the collaboration at the DeFEL beamline
- Federica Chiodaroli for the 2 GeV dynamics qualification
- Mauro Citterio, Fabio Manca and Fabrizio Sabatini for the bonding of the motherboard batch
- Federico De Benedetti for the flange design and the interconnections and biasing
- Pengfei Chang and Francesco Pinzin for the 256 differential to single ended antialiasing amplifiers
- Sergio Masci for the careful bonding of many detector/ASIC prototypes
- Filippo Riccio for the 14-bit DAQ development
- Dario Romeri for the slow control system development
- Andrea Rossetti for the integral-non linearity measurements
- Vincenzo Sicari for the patchPanel design
- Pietro Zambon for the detector qualification

- ….. And many others


Thank you for your attention !

Backup slides

Motivation of the work

- With the advent of radioactive beams the nuclear physics community is active in developing novel experimental methods and instruments coping with beam characteristics to extract spectroscopic information and study novel nuclear reaction mechanisms.

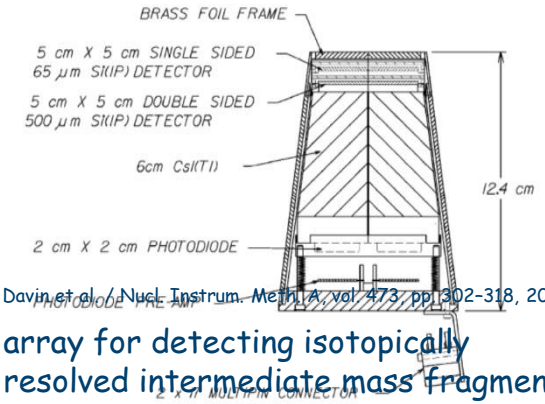
- Nuclear particle physics instrumentation today require a full cover of the available phase space with good efficiency, angular, energy and particle identification capabilities. From the detector standpoint this fact pushes towards the use of highly-segmented detectors with moderately fine pitches. In addition different types of detectors in very close geometry around the target are required, often operating in vacuum. Therefore multichannel, low-power, compact readout electronics is mandatory, pushing towards the integration of the frontend electronics in CMOS technology.

- The tendency is towards Digital Pulse Shape Acquisition – a powerful technique that opens the way to fully exploit the information encoded in the detector output response. The resolution in charge and mass separation and the energy threshold achievable with a chosen pulse-shape processing technique are strictly related to the physical properties and to the topology of the detector, to the experimental setup (i.e. front-side or reverse-side mounting) as well as to the type (i.e. charge-sensing or current-sensing) and performance of the analogue front-end.

- The key feature to preserve the fast rise time of the preamplifier output and the signal integrity over meter long connections from inside the vacuum chamber to the backend electronics is to feed a differential output to shielded differential pairs.

Existing competitors:

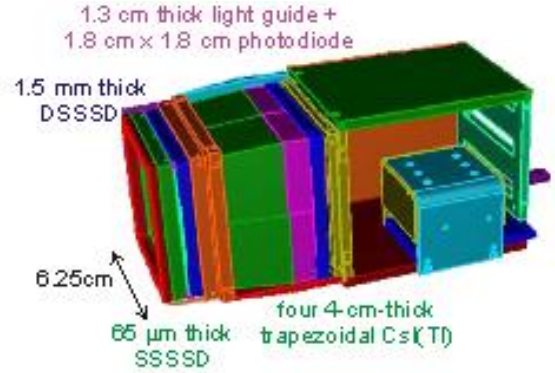
- **LASSA**



B. Davin et al. / Nucl. Instrum. Meth. A vol. 473, pp. 302–318, 2001.

- array for detecting isotopically resolved intermediate mass fragments (IMF: 3<=Z<=10) and light charged particles (LCP: Z<=2).
- 5 cm x 5 cm 65 μm passivated silicon detector (16 strips), backed by a 500 μm detector (16 front strips and 16 back strips) of the same area and by 4 x 6 cm thick CsI(Tl) crystals with photodiode readout.
- nine telescopes in a 3x3 arrangement

- **HiRA**



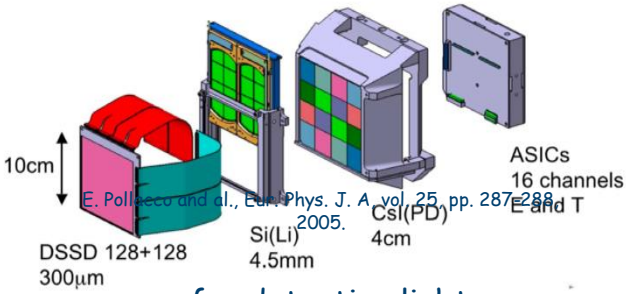
, 2007.

lved

3<=Z<=10) and light charged particles (LCP: Z<=2).

- 6.2 cm x 6.2 cm 65 μm silicon detector (32 front strips + 32 back strips), backed by a 1500 μm detector (32 front strips and 32 back strips) of the same area and by 4 x 4 cm thick CsI(Tl) crystals with photodiode readout.
- 20 telescopes in a modular arrangement

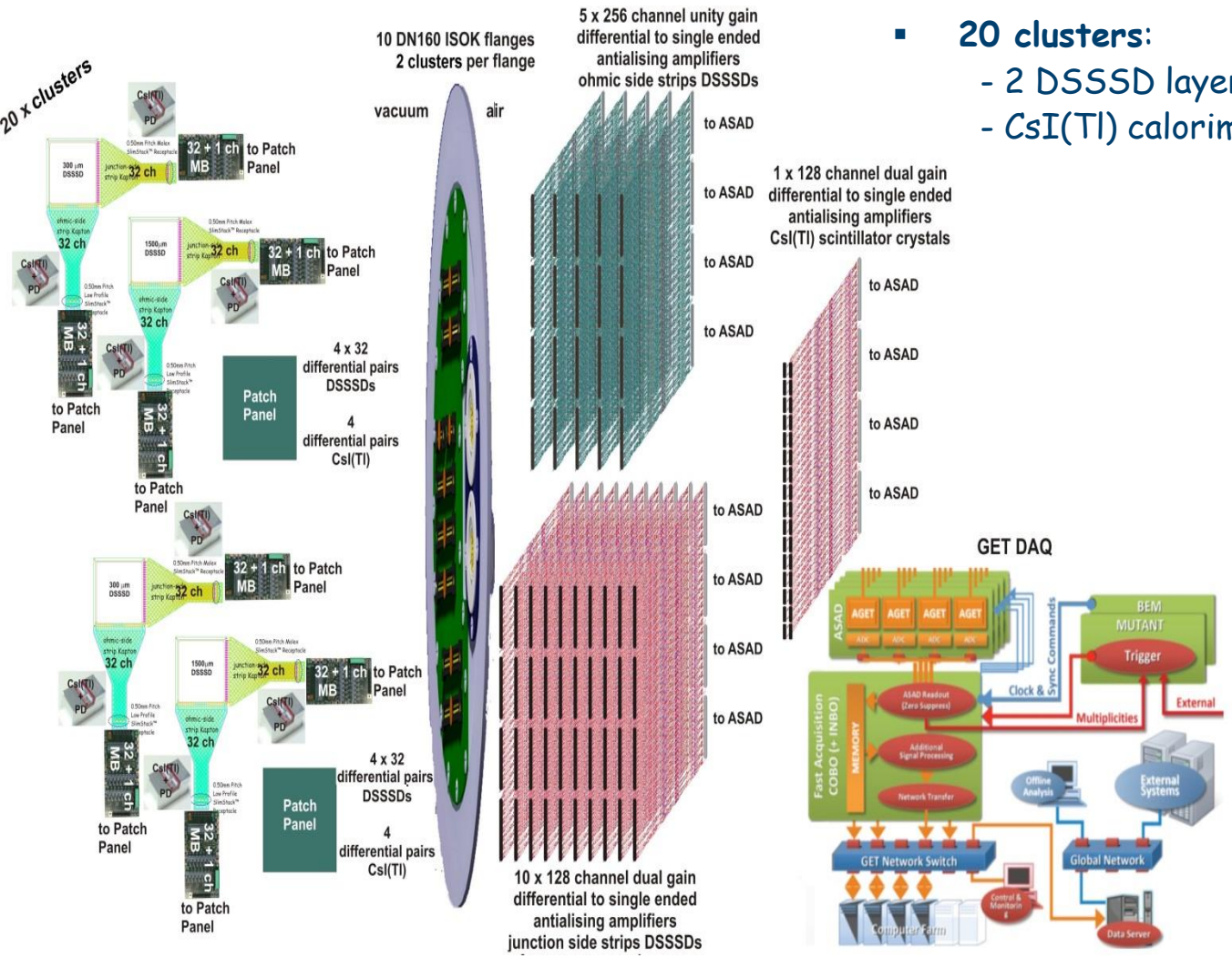
- **MUST & MUST II**



E. Pollacco and al., Eur. Phys. J. A, vol. 25, pp. 287–288, 2005.

- array for detecting light charged particles (LCP: Z<=2).
- 100 mm x 100 mm 300 μm silicon detector (128 front strips + 128 back strips), backed by a 4.5 mm Si(Li)detector (2 pads of 2 mm x 4 mm) and by 16 x 4 cm thick CsI(Tl) crystals with photodiode readout.

Our goal: the final FARCOS system

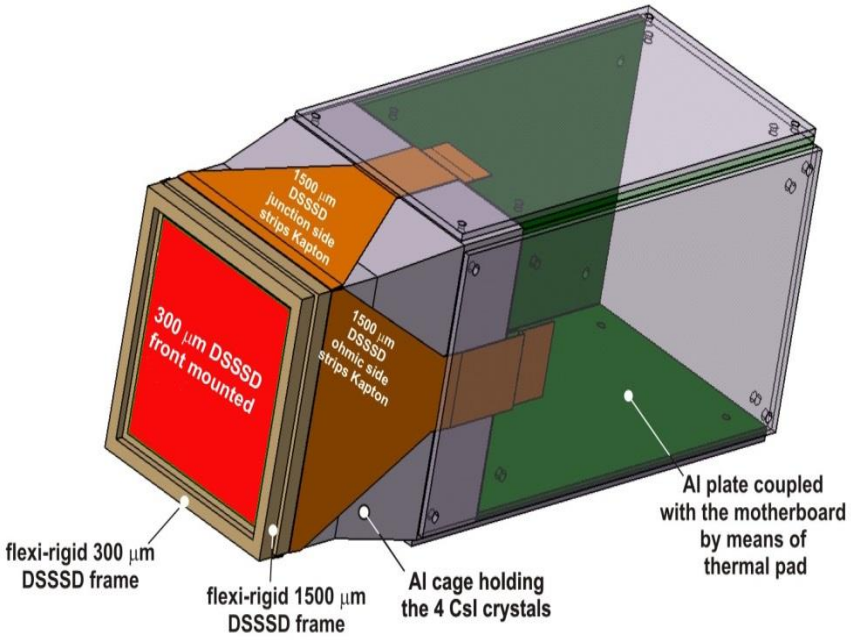


- **20 clusters**:
  - 2 DSSSD layers → 2560 readout channels
  - CsI(Tl) calorimeters → 80 readout channels

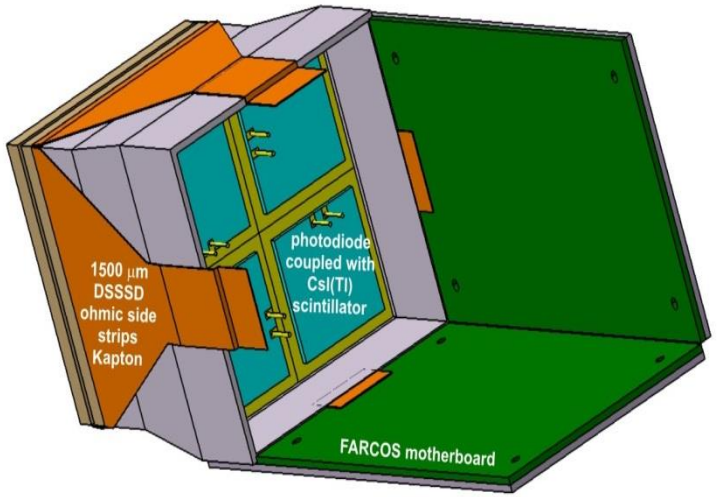
- High energy- and angular-resolution
- Wide solid angular coverage,
- Low identification thresholds
- Wide dynamic range
- High stopping power
- Simple, versatile, modular and transportable geometry
- LCPs and IMF identification in A, Z, E, T also for fragments stopping in the 1st stage

FARCOS cluster

- front view

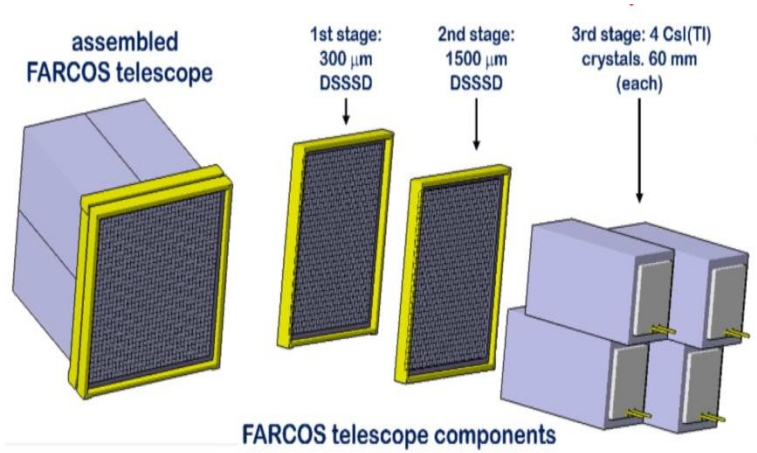


- back view



- custom designed flexi-rigid frame houses each DSSSD
- 4 custom motherboards – coupled with Al plates by means of thermal pad – form the mechanical walls of the cluster and house the frontend ASICs, the line drivers and the local slow control.
- patch panel acting as the rear side of the cluster hosts the output connectors

FARCOS Detection Layers



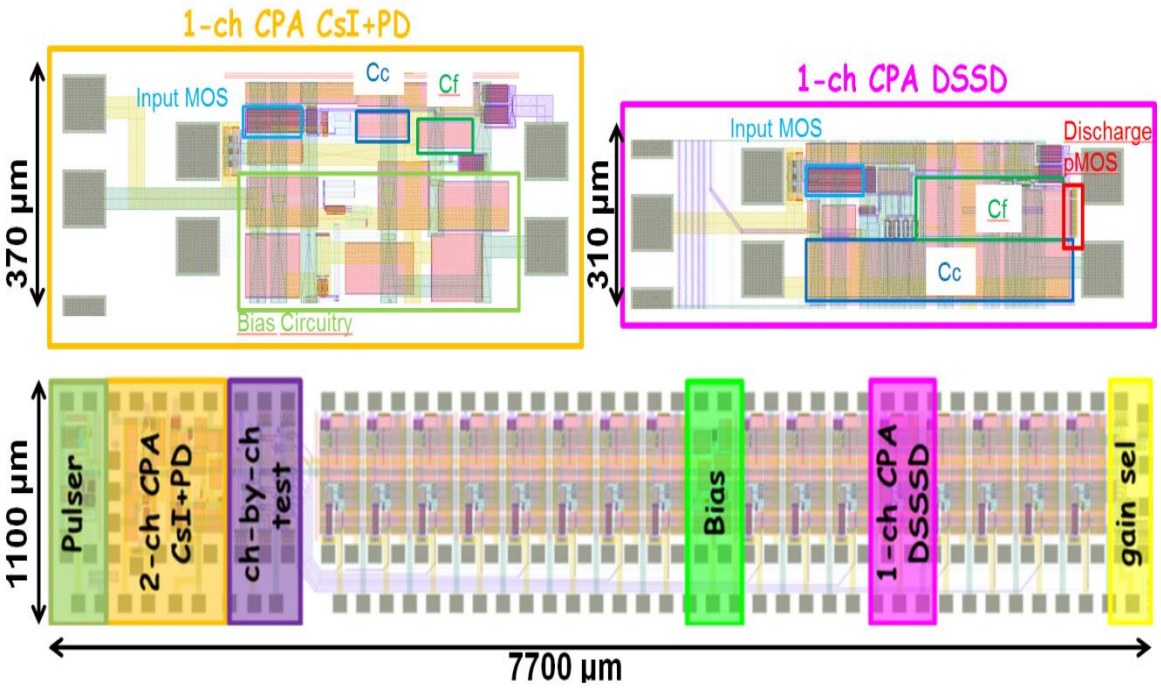
- **2 x DSSSD**

- ✓ DSSSD, made by MICRON Semiconductor Ltd on a standard design (BB7)
- ✓ mounted on a custom flexi-rigid carrier to minimize dead are and improve signal integrity.
- ✓ 2 mm strips – 32 strips on the front side and 32 strips on the back side.
- ✓ Front-side gap: 25 μm, back-side gap 40 μm
- ✓ Kapton cables directly attached to the flexi-rigid carrier.

- **4 x CsI(Tl)**

- ✓ highly homogeneous CsI(Tl) crystals, made by SCIONIX, with Tl concentration of the order of 1200 to 1500 ppm with a tronco-pyramidal shape
- ✓ each crystal wrapped with 0.12 mm thick white reflector including 50 micron of aluminized Mylar
- ✓ entrance window composed by 2 μm thick aluminized Mylar with a density of 0.29 g/cm^2
- ✓ output light read out by a Hamamatsu 18x18 mm PIN diode S3204-08, attached to the rear face of each crystal.

FARCOS Frontend Electronics - ASIC



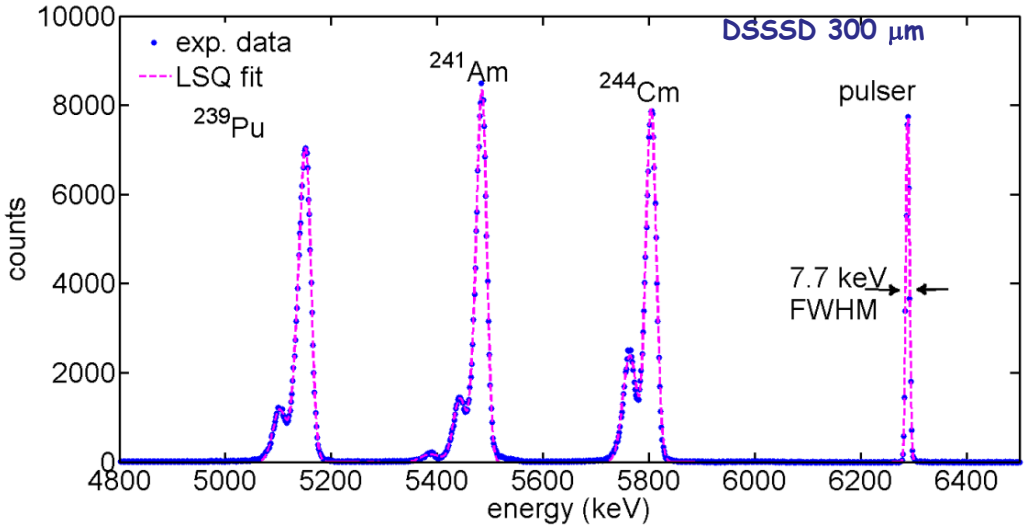
- ams 0.35 µm C35B4C3 technology
- one design fits all: single core topology reads out signals from all FARCOS detectors
- **16-ch CSA for DSSSD** readout
- **2-ch CSA for CsI(Tl)+PD** readout
- **on-chip pulser**
- **channel-by-channel test signal injection**
- temperature monitor

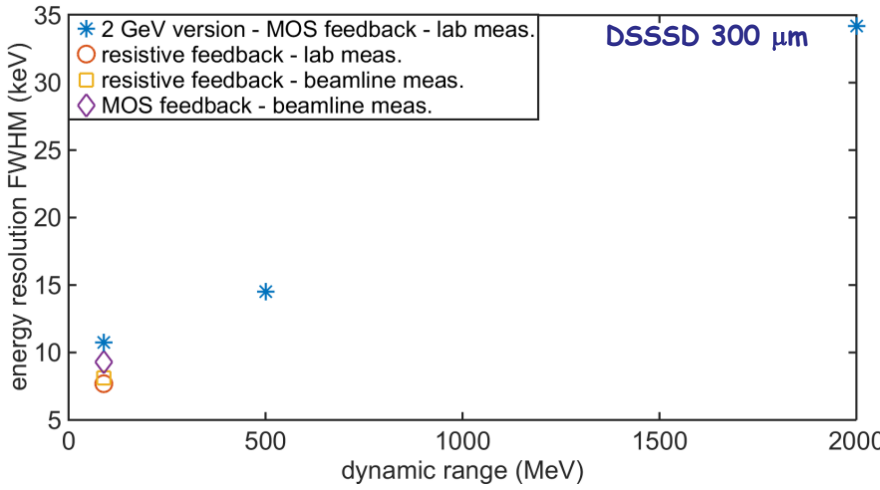
G	FSR (MeV)	Sensitivity (mV/MeV)	Sensitivity (mV/pC)	Feedback capacitance (pF)
0	90	11.11	250	4
1	200	4.44	100	10
2	350	2.78	62.50	16
3	500	2.02	45.45	22
4	2000	0.49	11.11	90

Front-end Slow Control – ASIC Control Bits

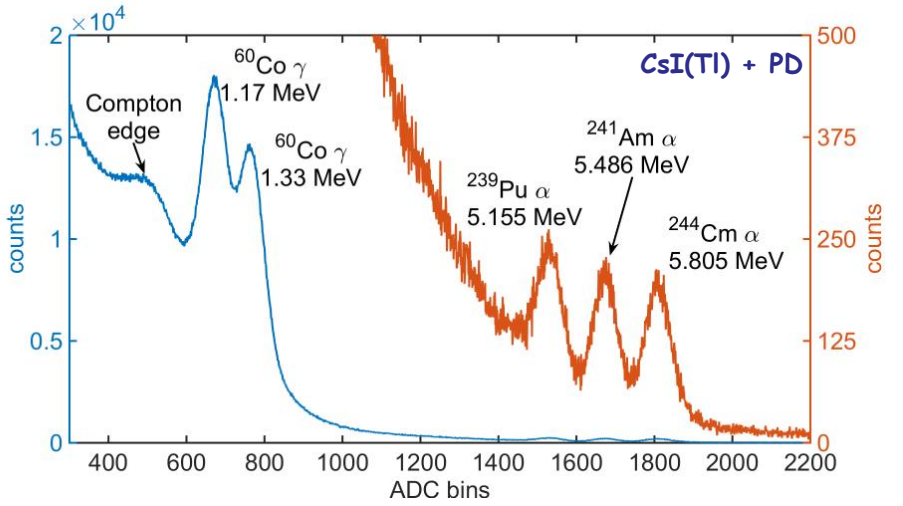
Bit Name	*Action*	*Description*
G0	sensitivity selection, bit 0	selection of the ASIC sensitivity for 5 different dynamic ranges.
G1	sensitivity selection, bit 1	
G2	sensitivity selection, bit 2	
C0	compensation selection, bit 0	selection of the ASIC compensation configuration for all channels.
C1	compensation selection, bit 1	
C2	compensation selection, bit 2	
C3	compensation selection, bit 3	
C4	compensation selection, bit 4	
pulser_PD	pulser circuit power down	pulser circuit power down signal
Test/Calibration	test or calibration mode selection	selection between TEST MODE (test signal fed to the integrated analog demux to pulse on a channel-by-channel basis, with fixed amplitude) and CALIBRATION MODE (on-chip pulser output fed to the external pulsing network with selectable amplitudes)
ch_sel0	test channel selection, bit 0	TEST MODE, ASIC channel selection
ch_sel1	test channel selection, bit 1	
ch_sel2	test channel selection, bit 2	
ch_sel3	test channel selection, bit 3	
ch_sel4	test channel selection, bit 4	
ch_sel5	test channel selection, bit 5	

ASIC experimental qualification – Energy Resolution



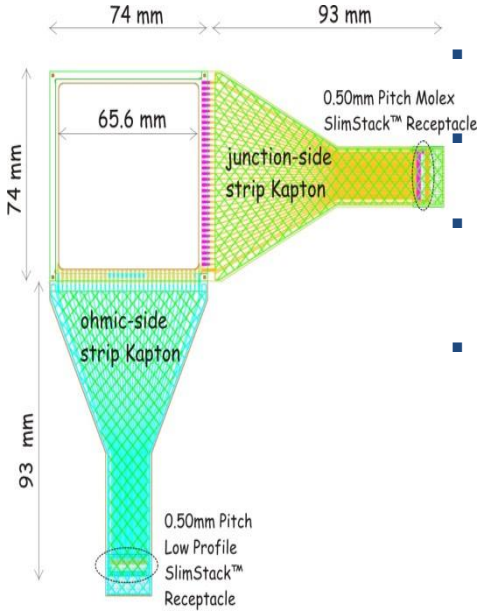


- **7.7 keV FWHM** (pulser) measured in the lab with **300 μm DSSSD** (junction side strips, ext. resistor feedback, 90 MeV dynamic range)
- **179 keV FWHM** measured in the lab at the ^{241}Am α line with **CsI(Tl) scintillator 6cm thick coupled with 1.8 cm x 1.8 cm PD** (ext. resistor feedback, 90 MeV dynamic range)
- excellent γ ray sensitivity



FARCOS Interconnections

Detector - Motherboard

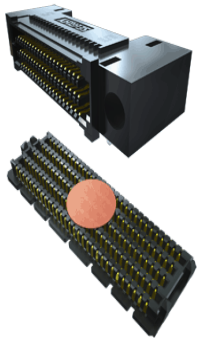


- DSSSD custom-designed flexi-rigid frame
- Kapton featuring ground plane for shielding
- Molex 52991-0708 connectors on the flexi-rigid frame
- Molex 52991-0708 connectors on the motherboard

PatchPanel - Backend

- 5m long + 5m long Samtec 0.80 mm Edge Rate® Edge Card Twinax Cable Assembly:
  - ECDP-32-190.0-L1-L2-1-3 32 differential pairs for DSSSDs
  - ECDP-08-190.0-L1-L2-1-3 8 differential pairs for CsI(Tl)
- FischerConnectors 105 CoreSeries cables and connectors for power (one cable for cluster) and slow control
- Custom-designed vacuum flange with interconnections for two clusters

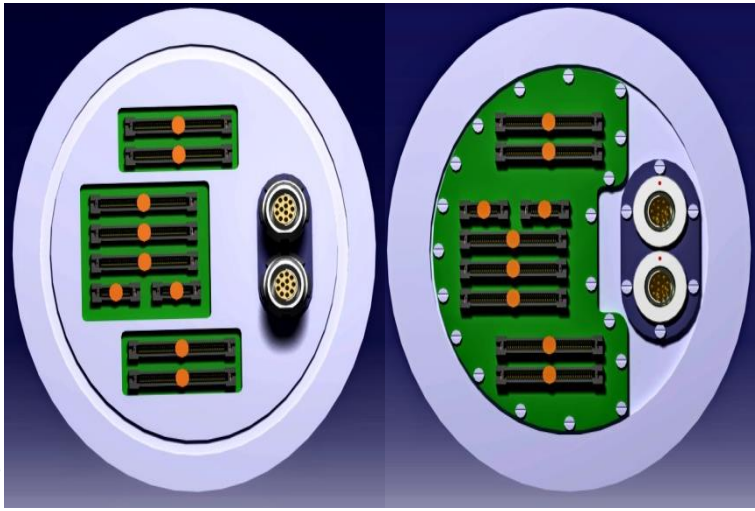
Motherboard – PatchPanel



- Samtec SEAF-30-01-L-06-1-RA-TR High-Speed High-Density Open-Pin-Field Array Socket on the motherboard
- Samtec SEAM-30-02.0-L-06-1-A-K-TR High-Speed High-Density Open-Pin-Field Array Terminal on the patchPanel

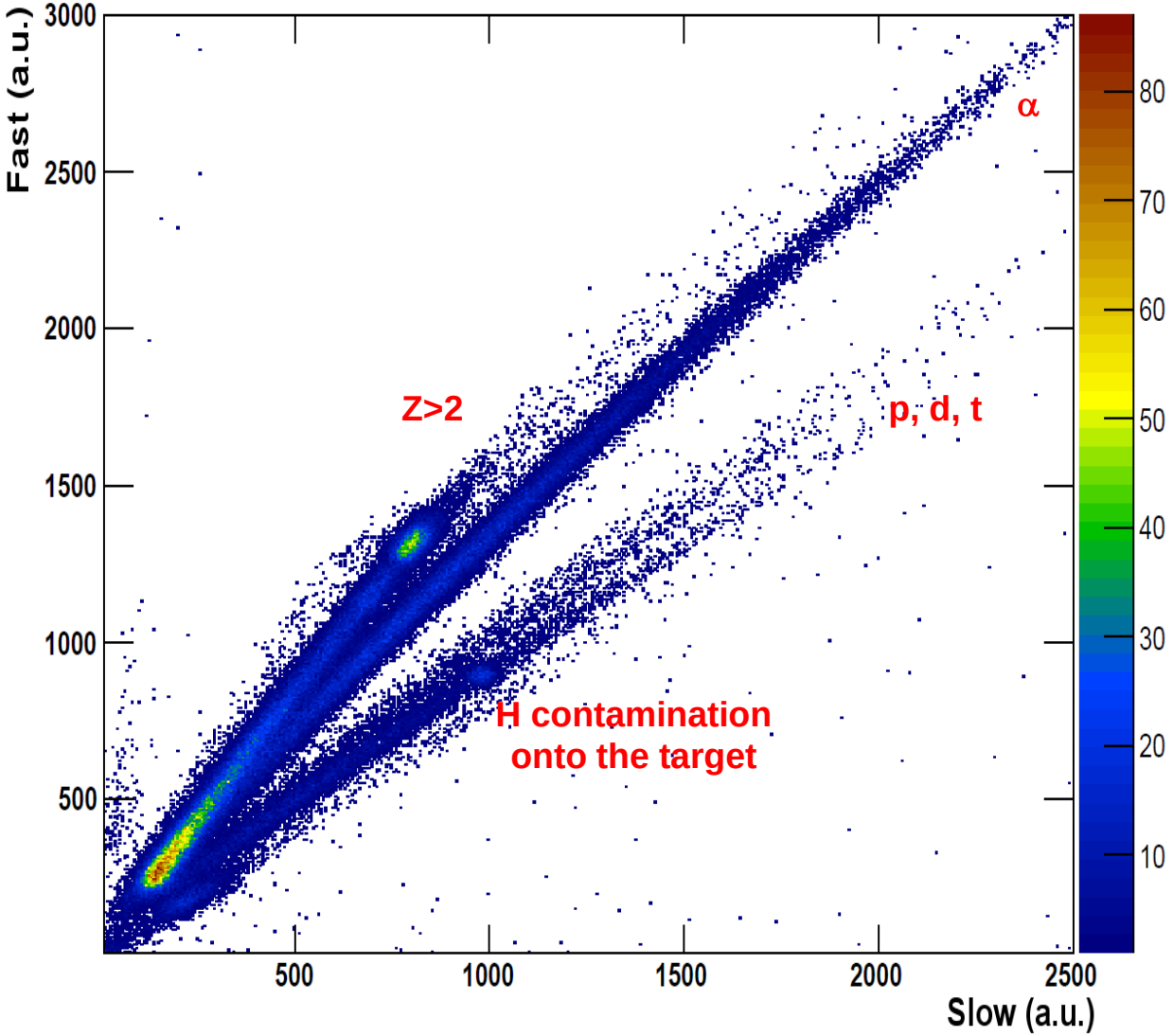
ECDP differential pairs

FischerConnectors 105 CoreSeries



vacuum side air side

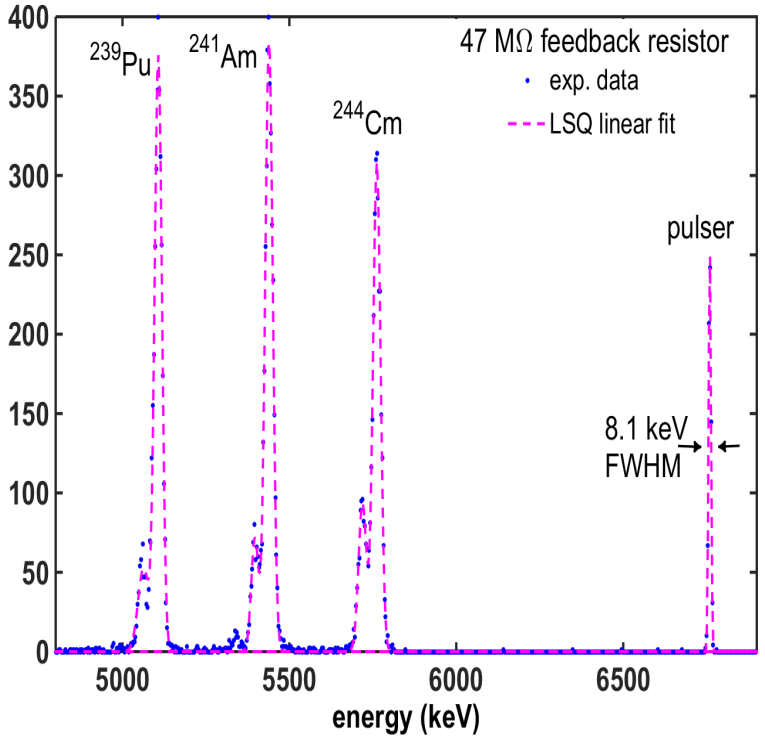
On-beam tests: Fast - Slow



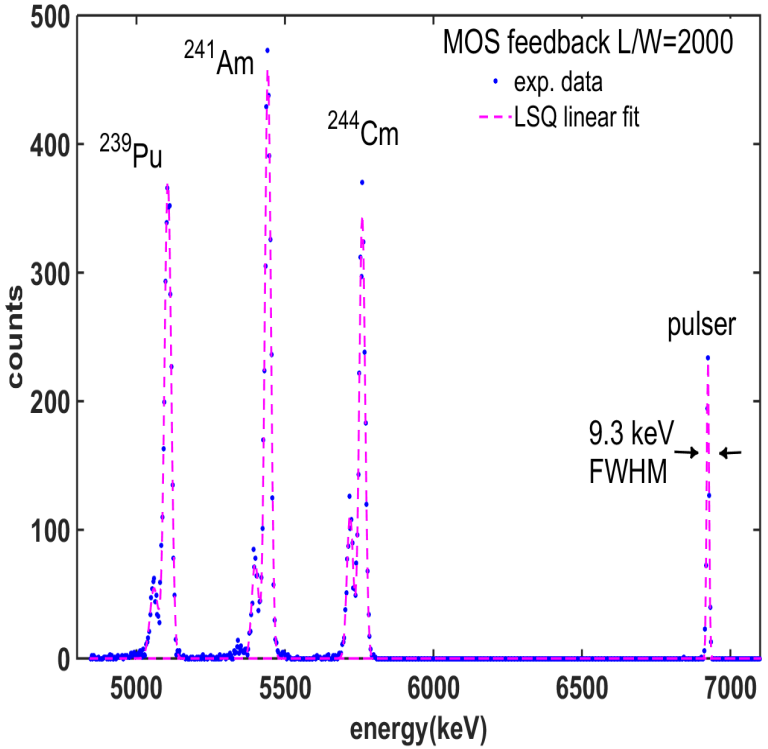
- Preliminary Fast - Slow identification plot for one CsI(Tl) scintillator crystal in the case of a LiF target as acquired with the 14 bits DAQ.
- Resolution limited by the non optimized differential to single ended receiver used for the CsI(Tl) + PD readout.

FARCOS Frontend Electronics – Energy Resolution

resistive feedback (junction side)



MOS feedback (junction side)

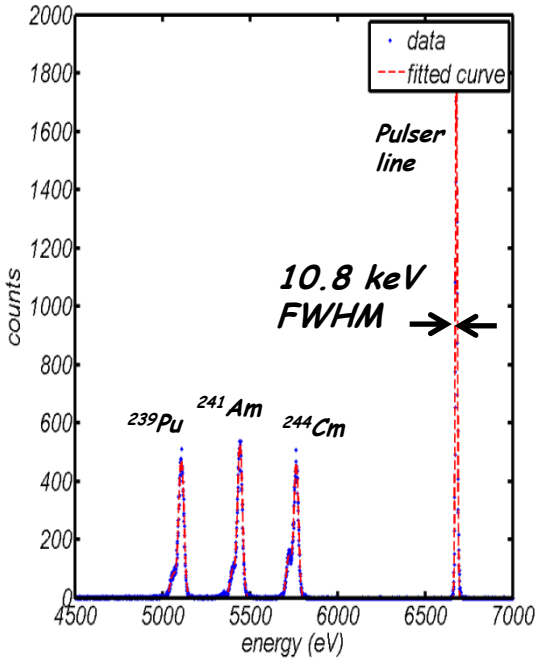


- ✓ 300 μm DSSSD illuminated with a mixed nuclei α source at the beamline
- ✓ all channels in operation (4 ASICs)
- ✓ 7.7 keV FWHM (pulser) measured in the lab with 300 μm DSSSD

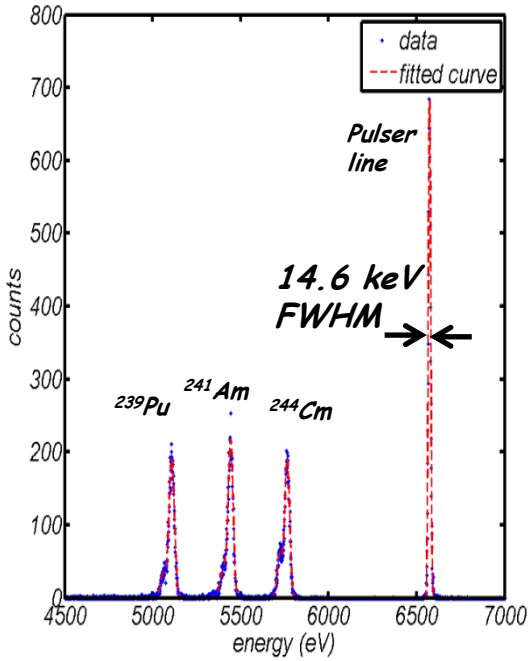
FARCOS Frontend Electronics – Energy Resolution

300µm DSSSD - Junction Side Strips

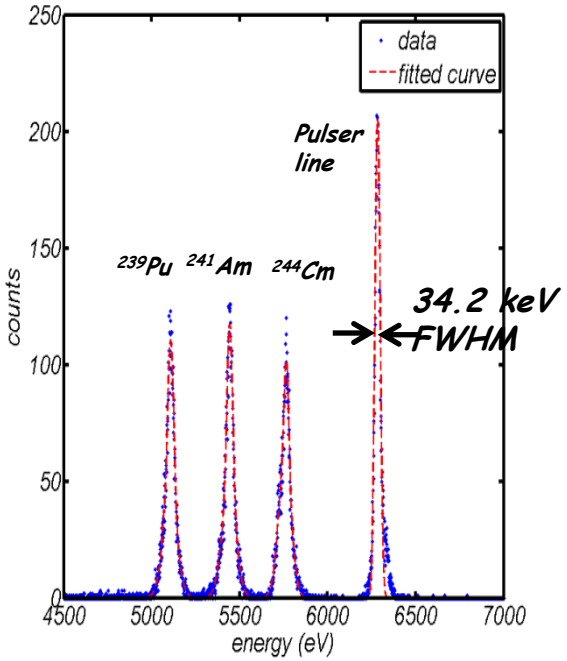
90 MeV Range – τ_{sh}= 6 µs



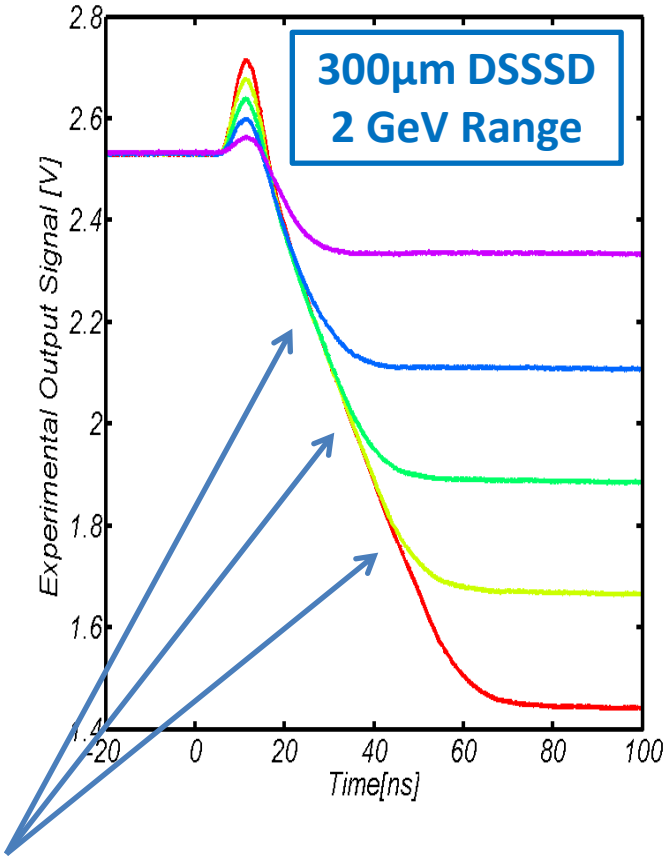
500 MeV Range – τ_{sh}= 6 µs

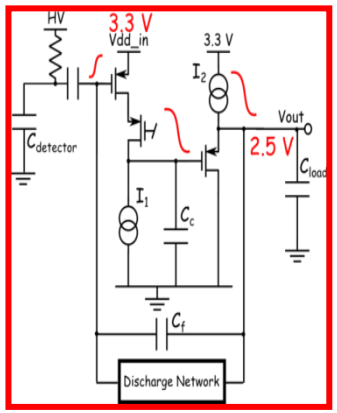


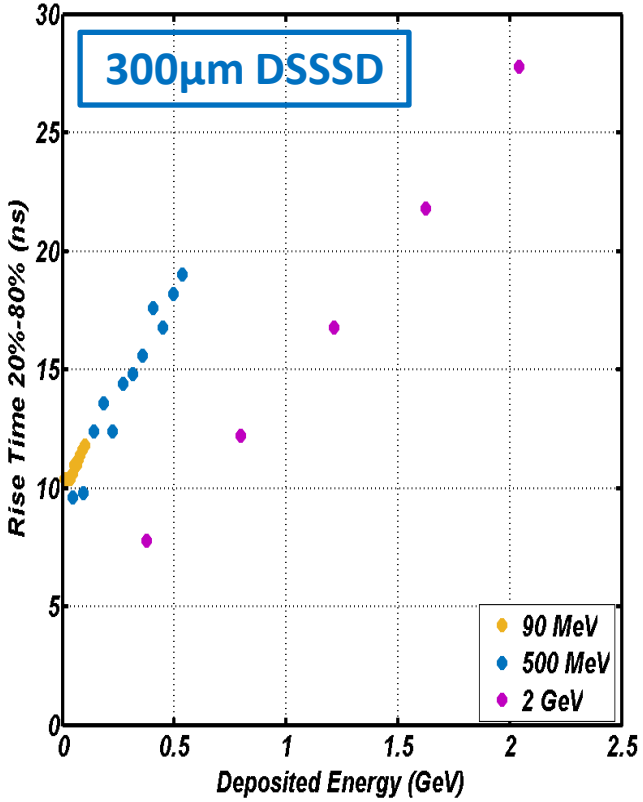
2 GeV Range – τ_{sh}= 12 µs



Exp qualification – RiseTime, Negative polarity





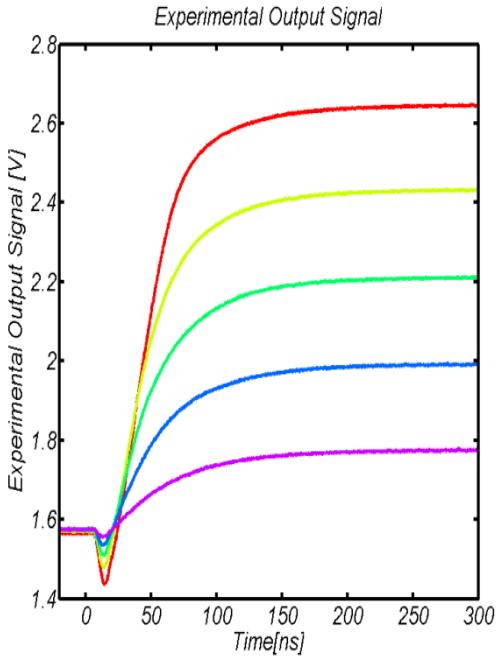


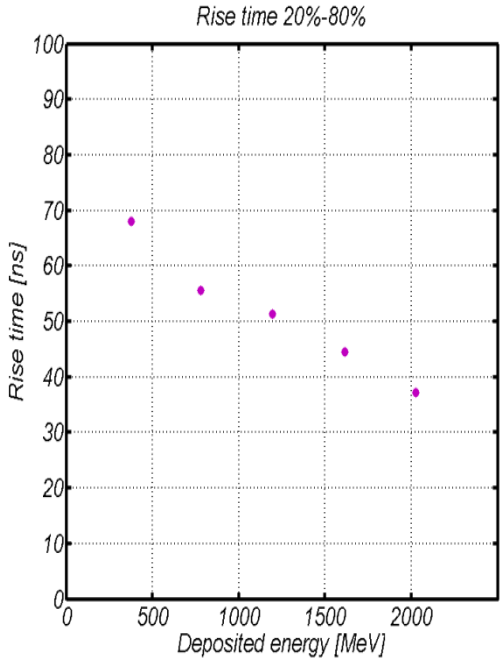
$$SR^{-} = \frac{I_1}{C_C + C_{stray}} = \frac{550\mu A}{19p + 3p} = 25\,\frac{V}{\mu s}$$

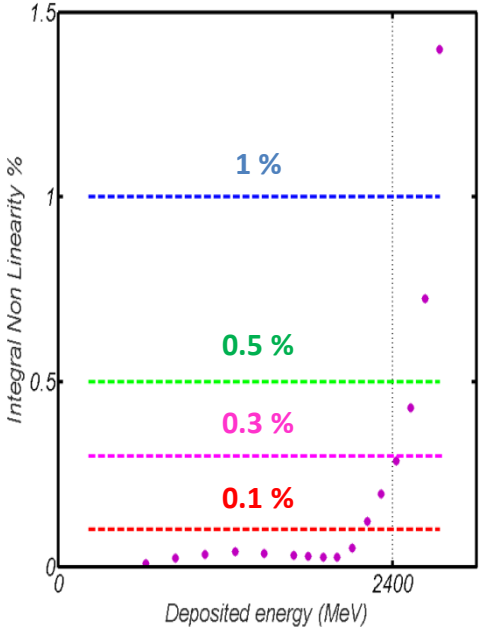
ΡισεΤιμε βελοω 20νσ φορ δψναμιχ ρανγεσ υπ
500 Μες
ΡισεΤιμε βελοω 30νσ φορ δψναμιχ ρανγε 2 Γ

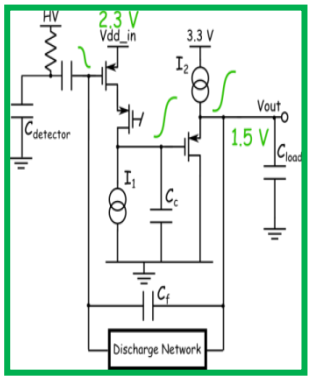
Exp qualification – Positive Output Polarity

300µm DSSSD - 2 GeV Range









- **RiseTime below 70ns for dynamic range 2 GeV**
- **No SR limitation in the time response**
- **Integral Non Linearity <0.5% up to 2.4 GeV**