R&D Track Triggers fase-2 parte di RDfase2

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Phase-II motivations

- HL-LHC is a Higgs factory
  - 3000 fb^{-1} / exp. @ 14 TeV
  - ~170M Higgs in total

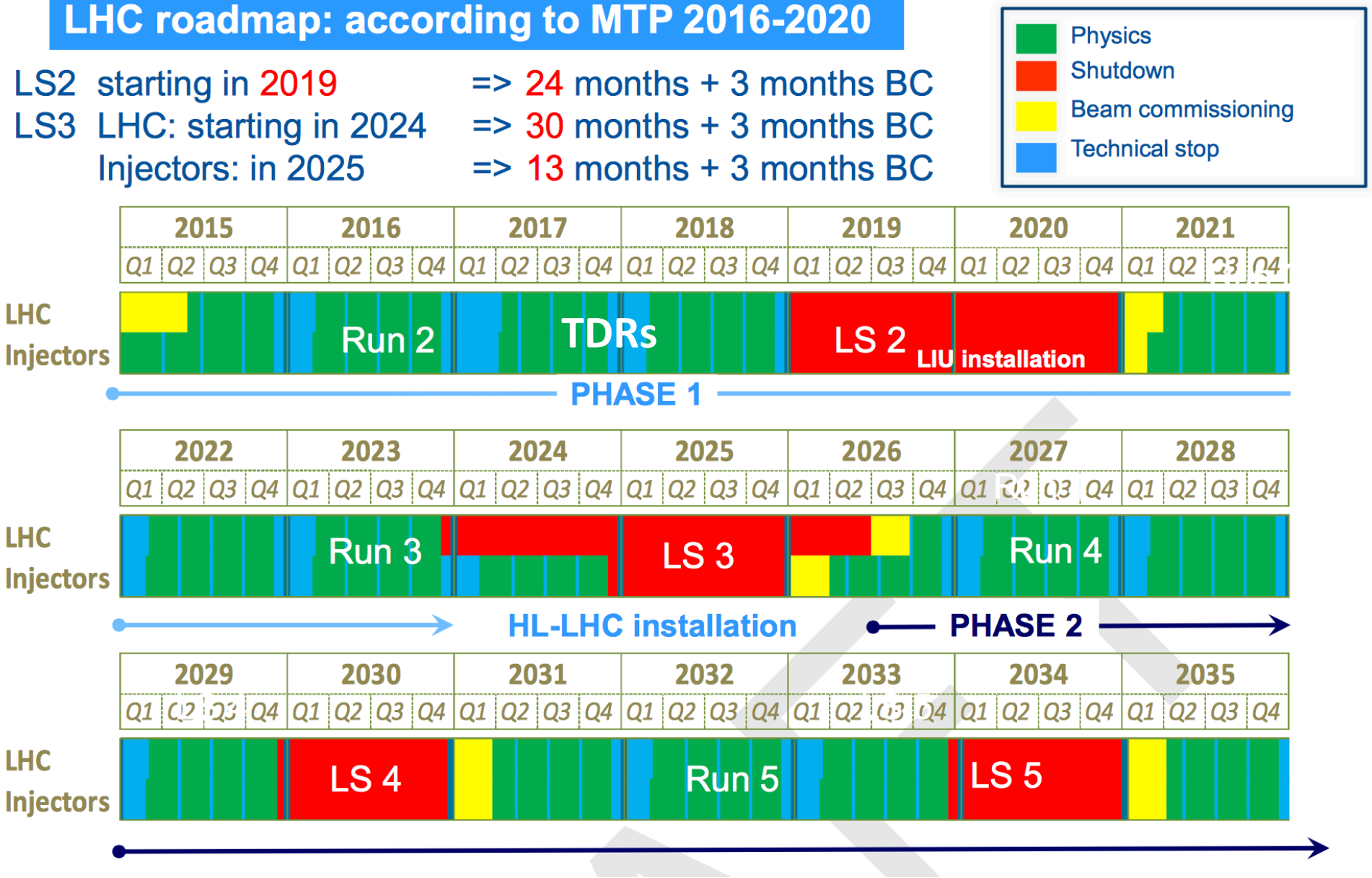
Process	Value	Now	300 fb-1	3000 fb-1
H->γγ	Δμ/μ	20%	13%	9%
H->ZZ		27%	11%	9%
H->WW		30%	13%	11%
H->ττ	Z	4.1 σ	6.9 σ	
	Δμ/μ	31%	21%	19%
H→bb	Z	-	3.9 σ	8.8 σ
	Δμ/μ	100%	26%	14%

- Precision of the measurements of the Higgs couplings
- Extend high-mass and extra dimensions searches well into the multi-TeV region

- Need triggering and reconstruction of low *pT* leptons and identification of heavy flavours

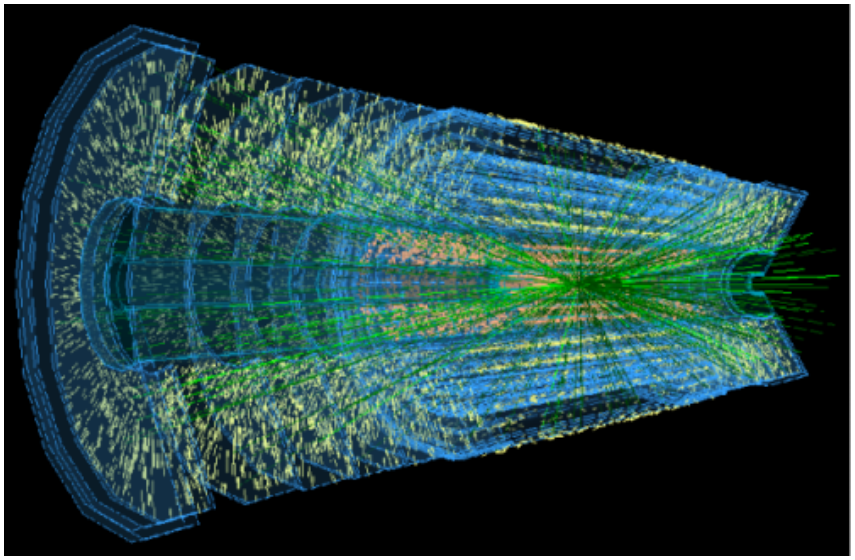
LHC roadmap: according to MTP 2016-2020

LS2 starting in 2019 => 24 months + 3 months BC
LS3 LHC: starting in 2024 => 30 months + 3 months BC
Injectors: in 2025 => 13 months + 3 months BC



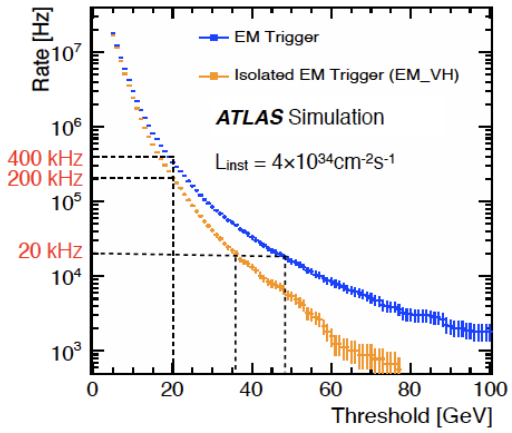
Track Trigger motivations & goals

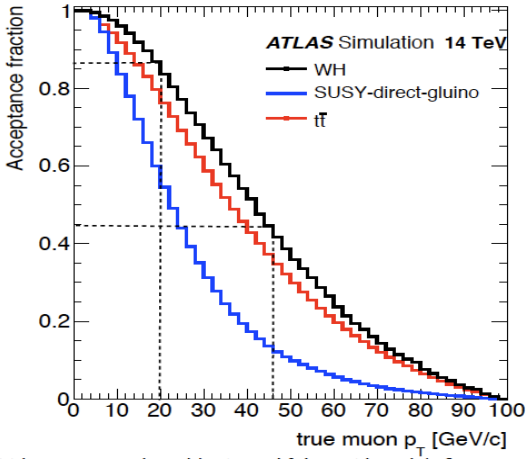
- Big challenges from phase-II conditions
  - Goal 7e34 Hz/cm2
  - Pileup 200
  - Move part of HLT including Traking to L1
- R&D for a feasible design
  - ATLAS TDAQ IDR (end 2015 / begin 2016)
  - ATLAS TDAQ TDR (2017)
  - CMS TDR (2017)



- Goal: extrapolate/evolve FTK design to phase-II environment
  - AM chip R&D
  - Fully exploit ATCA potentialities

Need a L1Track
to save EM pt>20 GeV

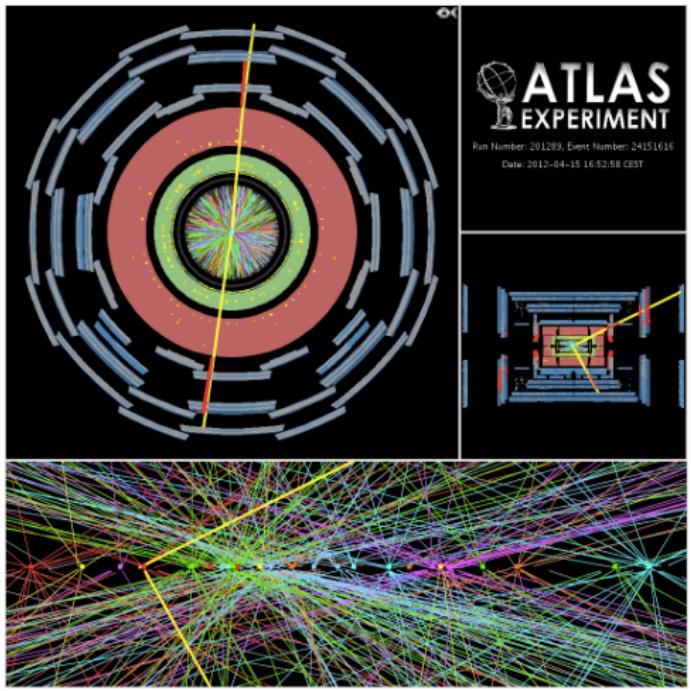




Tracking & processing power

- Current LHC (~2015):
  - 30 tracks per collision
  - 30 collisions per event
  - 1000 events/s
  - Need to find **1M tracks/s**
- Future LHC (~2025):
  - 30 tracks per collision
  - 200 collisions/event
  - 10000 events/s
  - Need to find **>60M tracks/s**

From connecting the dots (Berkely Feb 2015)



Current FTK: ~40 M track/s

- Tracking and offline processing in general **are an important challenge for Phase-II upgrades.**
- HW optimized solutions being planned considered (more) extensively:
  - track triggers can also be a offline co-processor.

ATLAS Track Triggers

Track Trigger R&D targets: L1Track and FTK++

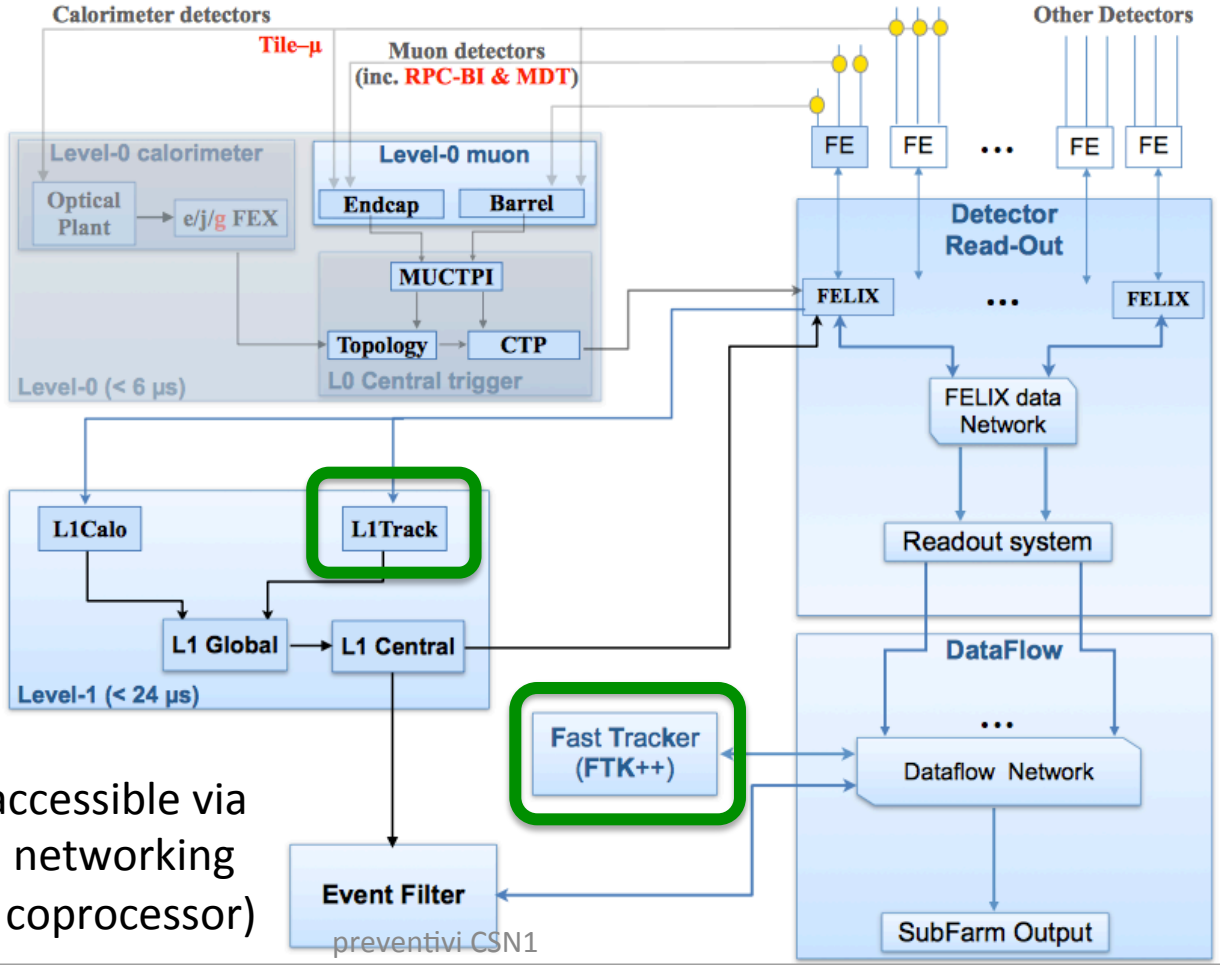
L1Track:
pT > 4 GeV
1 MHz input
regional

O(400 k) silicon hits / event

FTK++:
pT > 1 GeV
100 kHz input
full scan

TDAQ Phase-II costing

- Since LoI



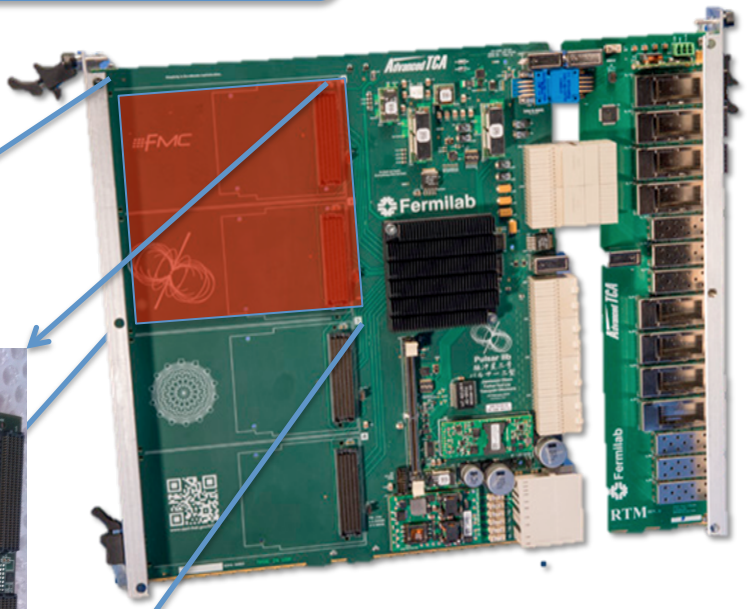
FTK++ accessible via general networking (offline coprocessor)

Common HW Model for Phase-II Track Triggers

ATCA

Proposed to ATLAS TDAQ (Annovi) used for L1Track and FTK++ costing

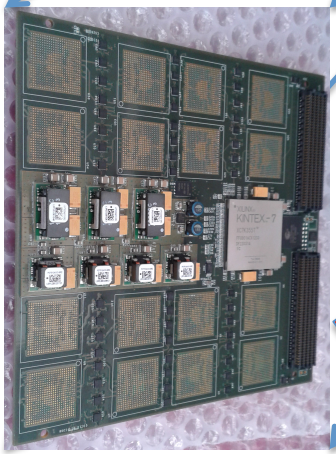
FTK Data Formatter



http://www-ppd.fnal.gov/ATCA/

future AM chip

x16



16 AM chips
1 FPGA
RAM
Power modules

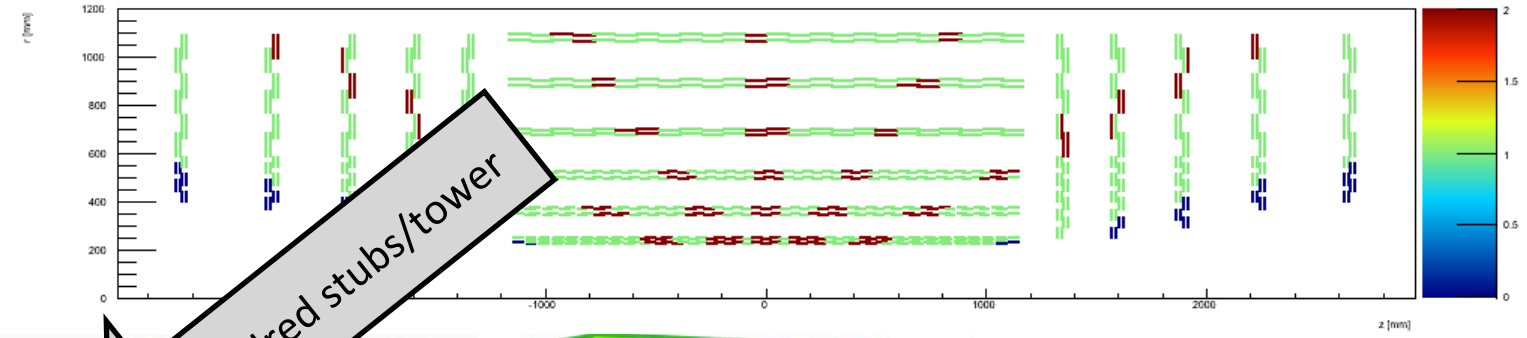
Pattern recognition mezzanine
D. Magalotti et al (RDfase2)

https://indico.cern.ch/event/299180/session/11/contribution/38/material/poster/0.pdf

ATLAS L1Track and FTK++

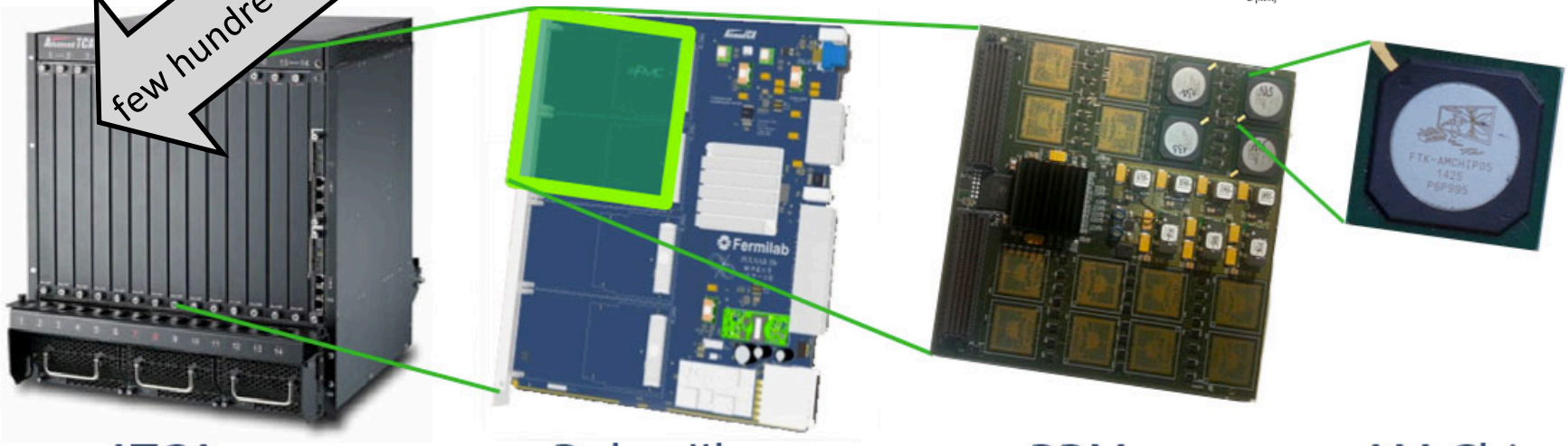
- Track Trigger upgrades are key part of Phase-II TDAQ upgrade plan
- L1Track and FTK++ part of all 3 costing scenarios
  - Cost (and processing power) for Track Triggers modulated depending on overall ATLAS budget
    - Reduce η range
    - Increase minimum pT
    - Reduce processing rate
  - L1Track first estimates of pattern needs 2-3 billions
  - FTK++ extrapolations from FTK to 3-10 billions
- Exploit FTK experience as much as possible
- Pisa has a leading role in this field
  - With FTK initial proposal, design, construction
  - With Phase-II R&D (phase-2 architecture, boards, AM chip 28nm)
- Sedi INFN: Frascati, Milano, Pisa

CMS L1 Tracking Trigger

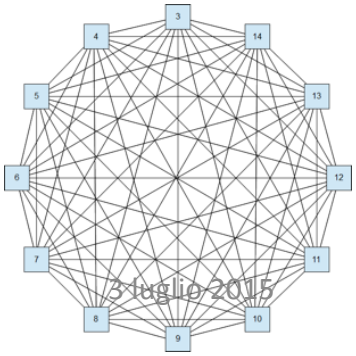


40MHz

p_T ~> 2 GeV filtering



ATCA Pulsarllb PRM AM Chip

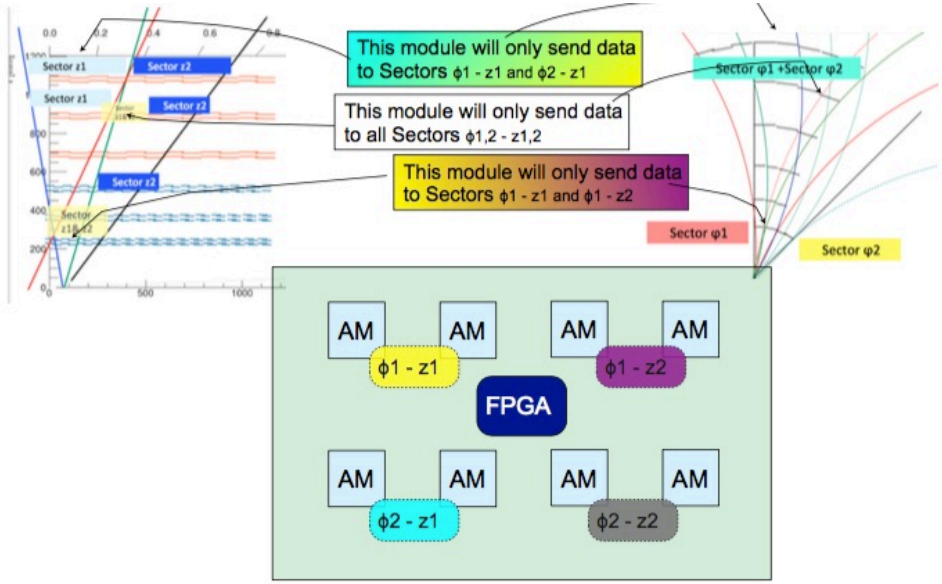


- Send data to Pattern Recognition Mezzanine in each ATCA blade
  - Data distributed to Pulsar boards in time multiplexed mode in round robin
  - Perform pattern recognition using several AM chips (120k Patterns/AM chip)
  - Track fit with FPGA inside the Mezzanine (~1 ns/fit)

CMS L1 Tracking Trigger

- Sviluppo di un "dimostratore" con tecnologie allo stato dell'arte per il TDR del Tracker (2017)
  - Data sharing, misure di latenza (<5 μs) e architetture di time-multiplexing
  - ATCA standards (fino a 40 Gbps) + AM chip sviluppati per FTK
  - Giustificazione delle scelte di disegno per il TDR del Tracker.
- Sviluppo di un nuovo chip di AM, in sinergia con ATLAS
  - Aumento della densità dei pattern e della velocità di clock in tecnologia 28 nm
  - R&D per il TDR del Track-Trigger a seguire (~2020?)
- Piano di spesa discusso e approvato in CSN1
  - Include chip 28 nm in sinergia con IMPART (FIRB CSN5) + Bicocca (nuovo) dal 2015
  - Sviluppo mezzanine, acquisto Pulsar boards e crates ATCA
- Sedi INFN: Fi (SW), Pd (SW), Pg (HW+SW), Pi (HW+SW), Ts (SW)
  - Bicocca (New Entry!) sul chip 28nm

CMS AM bank optimizations: sub-sectoring



L. Martini

patterns / trigger tower

Type0	normal	fountain
Total	1 295 185	2 139 272
$\phi_1 z_1$	339 857	523 509
$\phi_1 z_2$	339 184	560 681
$\phi_2 z_1$	307 298	508 367
$\phi_2 z_2$	332 245	546 715

- Latency due to I/O is not-negligible
- ➢ Divide banks in independent sub-banks depending on phi, zeta
- Such that modules in each layer are mostly linked only to fewer sub-banks as possible
- After preliminary studies, expected latency due to I/O reduced by a factor 2
- ➢ Trying this pattern splitting inside the official code to test the actual possible latency reduction
- ➢ Trying it on hardware: we have a mezzanine with 2 independent lines, we can split the bank in 2 (instead of 4) to demonstrate its actual feasibility

AMchip05, its Test Stand, and AMchip06

Design: INFN Frascati, Milano, Pisa + Paris (LPNHE)

TSMC 65nm

Big improvements in AMchip design

- AMchip05 power consumption / # of bit / MHz decreases of a **factor ~41** w.r.t. AMchip03
- AMchip05 memory density (patterns*layers/ area) increase of a **factor ~25** w.r.t. AMchip03
- High speed serial links (11 times 2 Gb/s)

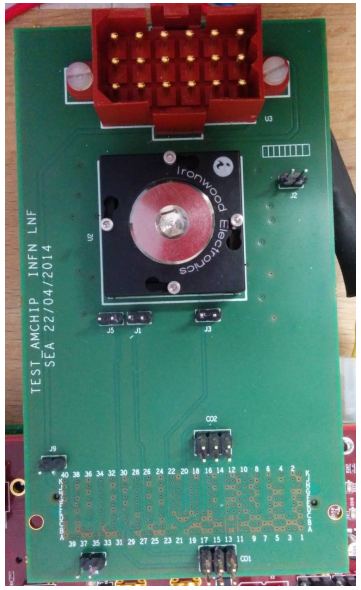
New **layout 128 kpatt**

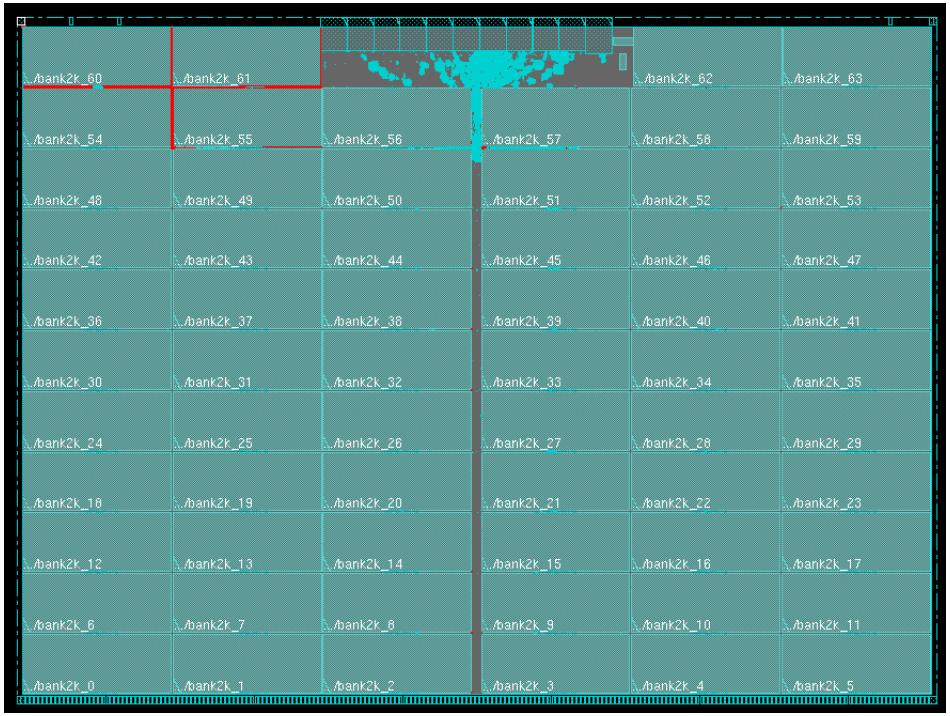
14.6 mm x 10.8 mm²

Sent to IMEC June 3rd

devices back end of September

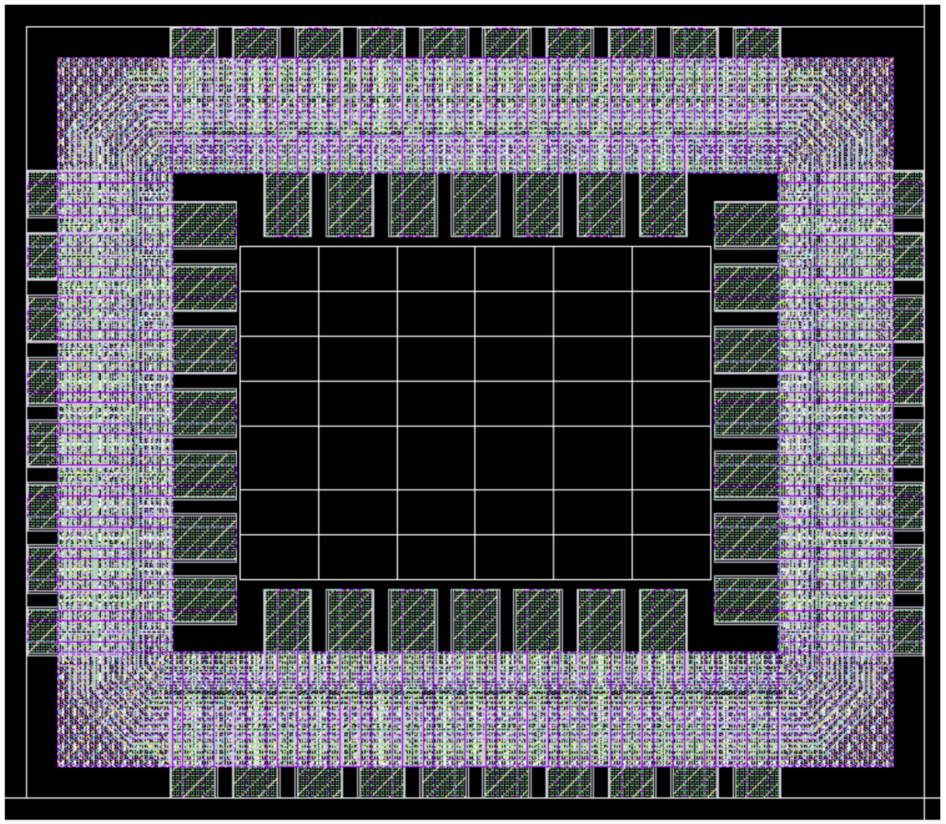
23x23 mm² BGA for AM05: 3k patterns and AM06: 128k patt.



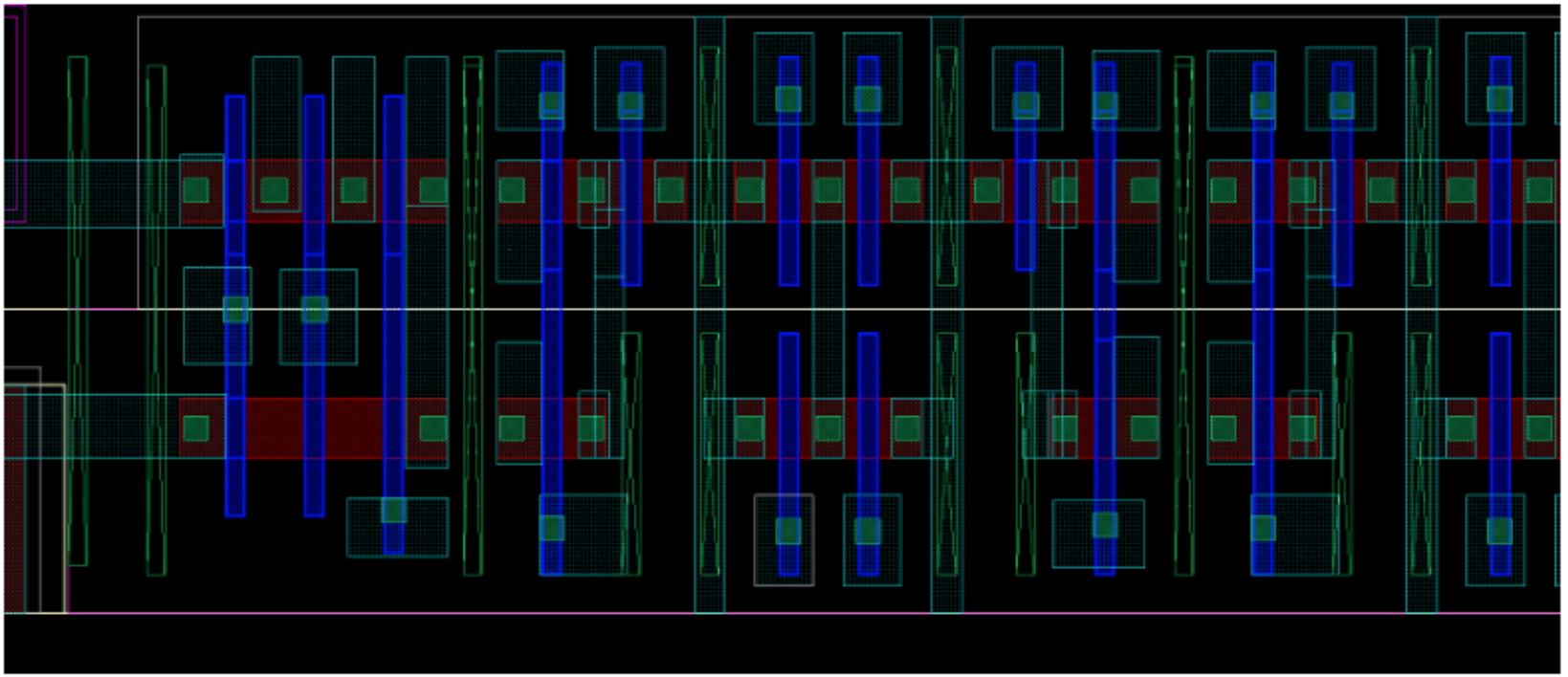


28 nm AM07a design just submitted

- A. Stabile (Mi Celoria) in collaboration with (Mi Bicocca)
- 0.6mm^2 including PAD/power ring
- 2688 single layers
  - 18 bits per layer
  - Eq. to 672 AM06 patterns
- Goals:
  - **Get experience on 28nm**
  - **First information on AM performance**



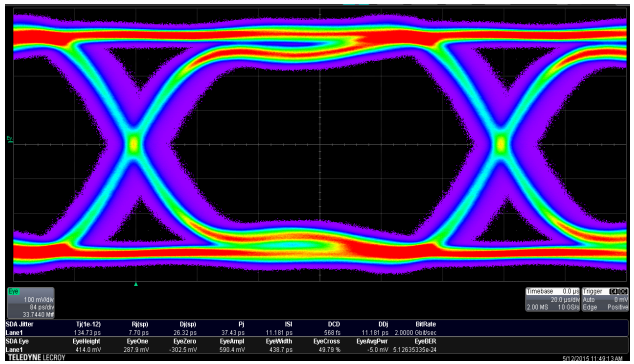
FULL CUSTOM CELLS



		AM04	AM05 miniasic	AM06	AM07	AM06 vs AM07
main block size	size (um^2)	27798	26388.72	21833.28	6925.896	**31.72%**
	length (um)	226	257.2	100.8	110.32	109.44%
	height (um)	123	102.6	216.6	62.78	28.98%
SIM power	uW/layer	1.07		1.91E-06	1.30E-06	**68.12%**
BL capacitance	pF/line	0.07	preventivi CSN1 0.06	0.027	0.018	**66.67%**

Stato Mezzanina

- Testati ~100 chips AM05 a Pisa (N. Biesuz, G. Fedi)
- Mezzanina AM05 + Kintex7 prodotta a Perugia
- Test e caratterizzazione (G. Fedi, G. Magazzu)
  - In collaborazione con Perugia
  - AM chip support from FTK



Test links @2 Gbps (verso i chip) e
@8 Gbps (verso Pulsar)
Nessun errore in 8 ore: BER<10^{-14}

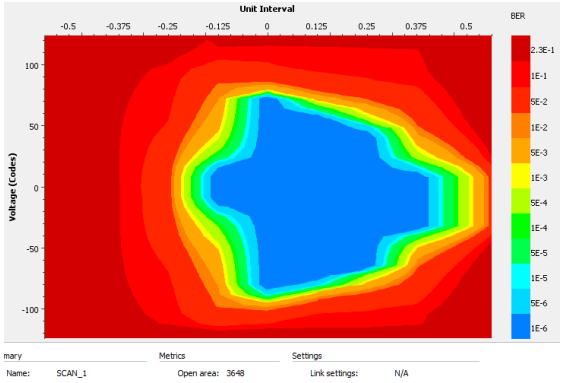
Sviluppo Firmware di test (G. Magazzu)
Sviluppo FW Track fit e Data Organizer
C++ (L. Martini) + Perugia
FW (G. Gentsos – IAPP / FTK)
NOW: Functionality tests in progress
Studio configurazione banche (L. Martini)

Realistic test - Test stand

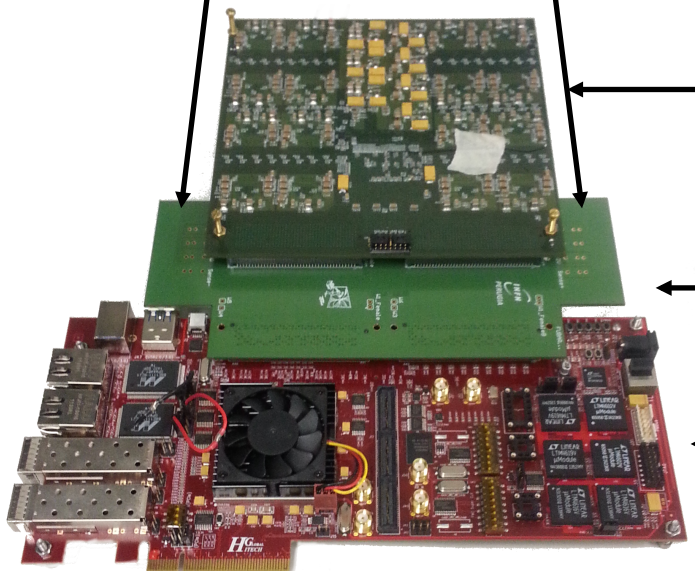
Aim: emulate the pulsar using the Virtex6 evaluation board
Limitations:

- Number of GTX links 4 (Evaluation board) Vs. 6 (Pulsar)
- FPGA Virtex6 (Evaluation board) Vs. Virtex7 (Pulsar)

Link0 @ 8 Gbps



Power connectors (3.3 & 12 Volt)



Kintex7 INFN mezzanine

INFN FMC connector adapter

Virtex6 evaluation board

Prossimi passi

- 2015
  - Ricezione e test AM06 e AM07a
  - Ricezione e test seconda mezzanina AM05
    - 16 chip – in produzione a Perugia
  - Test integrazione mezzanina nella Pulsar a FNAL
  - Acquisto crate ATCA e integrazione Pulsar a Pisa

- 2016
  - Sviluppo nuovo chip 28 nm (6 mm^2) AM07b (MI+)
    - Primo dispositivo da “utilizzare”
    - Ottimizzazione AM cella
  - Sviluppo (PG) e piccola produzione nuova mezzanina AM06

Richieste 2016

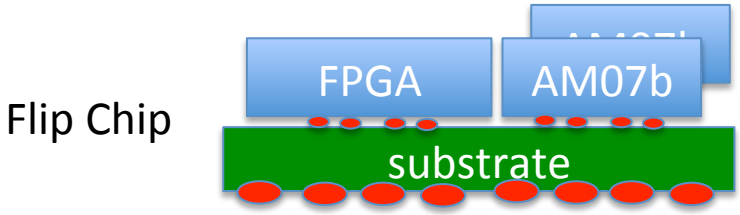
- 2 mezzanine con AM06 (11 k€)
  - per uso in “ATLAS”
  - mezzanine “CMS” finanziate a Perugia
- IPMC cards per le Pulsar (1k€)

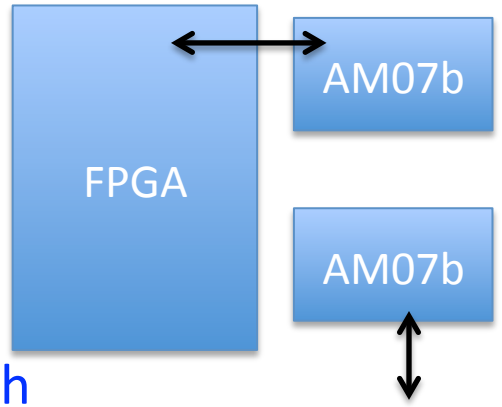
- Supporto del servizio di elettronica
  - G. Magazzu (5 mesi)

FPGA + AMchip system in package

In 2016/2017 exploring multipackaging

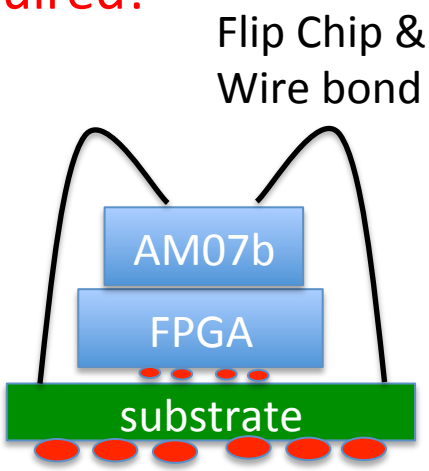
– 1 or 2 AM chip + 1 FPGA in the same package

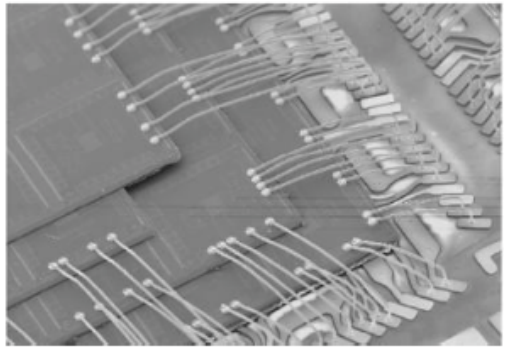




- Dramatically increases AM to Track Fitter bandwidth
  – "Through Silicon Vias not required!"

- No need to buy new SerDes IP
- Reduce FPGA-AM latency
- Simplify the AM development
- Increase fitting power/AMchip





Sommario

- Primo prototipo AM07a 28nm sottomesso
- Prima mezzanina fase2 con AM05 in funzione
- Preparazione
  - integrazione mezzanine e Pulsar
  - test AM chip
- L'attività è strategica per la realizzazione e l'efficacia degli upgrades di HL-LHC