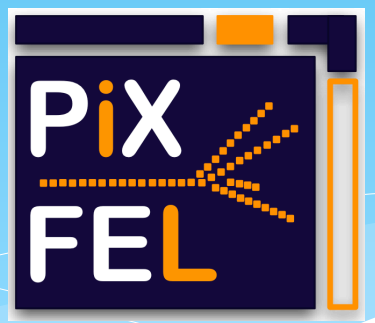
PixFEL

Enabling technologies, building blocks and architectures for advanced X-ray pixel cameras at FELs

Presentazioni preventivi CSN5 2016

INFN Sezione di Pisa, 9/7/2015



Outline

- The PixFEL project
- Motivation
- PixFEL Long Term Purpose & 3–years Activity Program:
  - Building blocks, Technologies, Architectures
  - Pisa contribution
- Present achievements
- Activity in 2016
  - Piani
  - Richieste finanziarie e ai Servizi di Sezione

The PixFEL Project

- Develop high performance X-ray imaging instrumentation for experiments at the next generation Free Electron Laser facilities
- Use innovative solutions & technology, now explored in HEP comunity, to improve performance of pixel device for photon science.
  - Key technologies: active edge sensors, 65 nm CMOS process, vertical integration
- Important synergy with other activities of the groups involved: LHC upgrade (65 nm, active edge sensor), AIDA (3D vertical integration).
- In the long term (+6 years) develop a four side buttable module for a large area X-ray camera for application at FELs. INFN 3-years project as a first step.

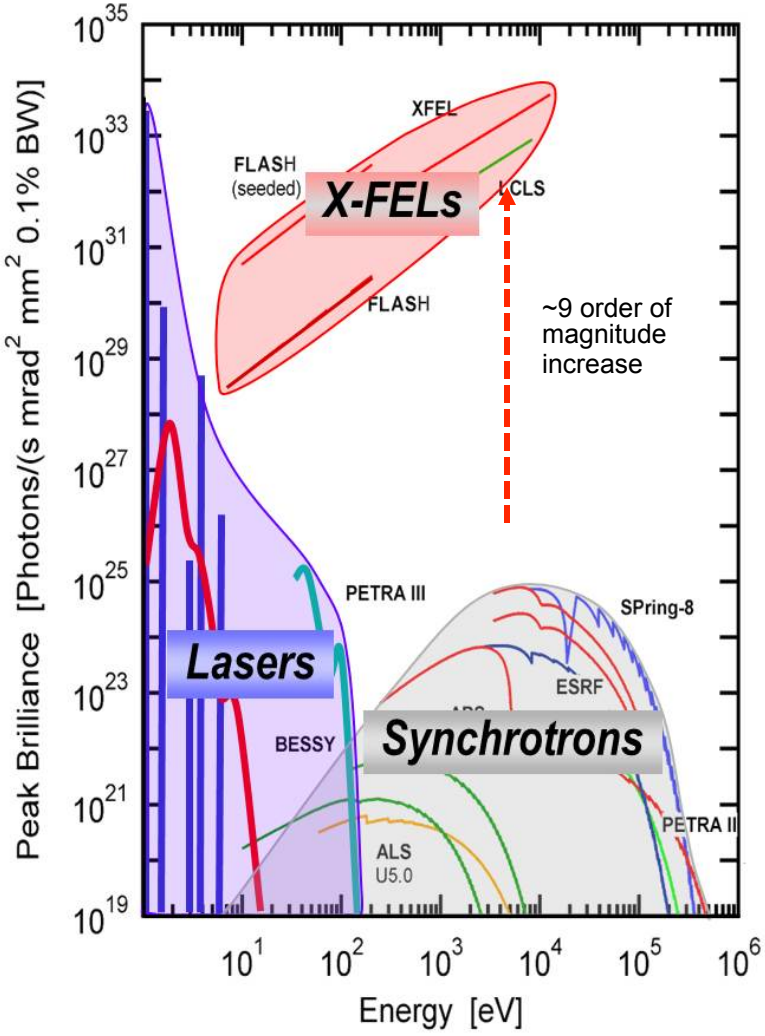
- WP1: Enabling technologies: L. Pancheri
- WP2: Building blocks: M. Manghisoni
- WP3: Architectures and testing: G. Rizzo

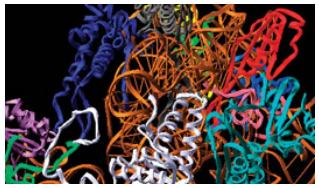
Participating groups

- INFN & University Pavia-Bergamo (3.3 FTE) (**Resp. Nazionale L. Ratti**, **Resp. Loc. M. Manghisoni**, V. Re, G. Traversi, D. Comotti, M. Grassi, P. Malcovati, L. Fabris, L. Lodola)
- INFN & University Pisa (2.5 FTE) (**Resp. Loc. G. Rizzo**, G. Batignani, S. Bettarini, G. Casarosa, F. Forti, M. Giorgi, F. Morsani, A. Paladino, E. Paoloni)
- INFN & University Trento (2.1 FTE) (**Resp. Loc. L. Pancheri**, G.F. Dalla Betta, R. Mendicino, H. Zu, G. Verzellesi, M. A. Benkechkache)

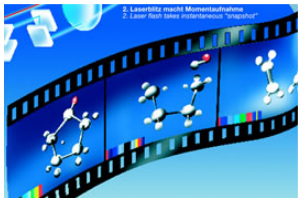
X-FELs as probing tool

- X-rays have been a fundamental probing tool in many fields since their discovery
- The advent of free electron laser (FEL) facilities opens up new possibilities to probe matter with X-ray beams of unique features:
  - very high intensity, coherent, ultrafast pulses, large energy range
- Broad science program accessible at FELs:
  - Structural biology, Chemistry, Material science Atomic and molecular science (AMO)
- A number of facilities already operational (LCLS, FLASH, SACLA, FERMI), other being built (Eu-XFEL, SwissFEL) or upgraded (LCLS!LCLSII)

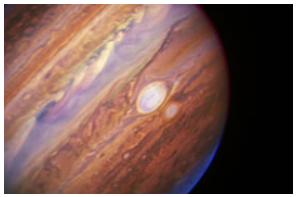




Deciphering the structure of biomolecules…



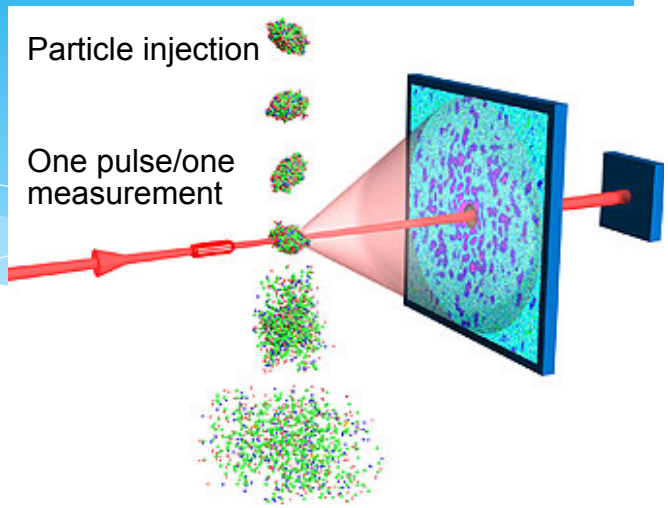
Filming chemical reactions…



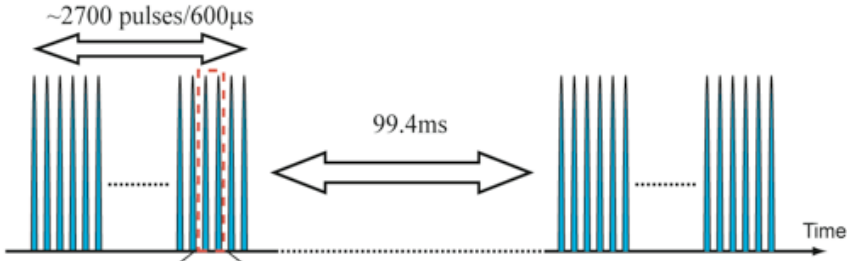
Investigating extreme states of matter…

2D Imaging X-ray FEL detector challenges

- Many measurements based on scattering of coherent X-ray pulses and detection of diffraction pattern with a large pixel camera.



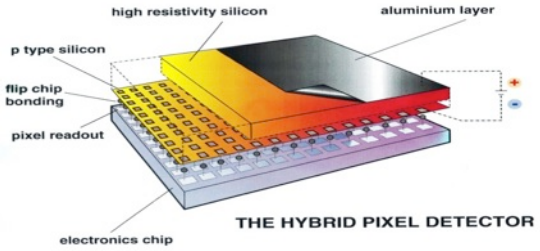
Eu-XFEL-Pulse structure



- FEL Pulse Structure
  - Single shot imaging within 220 ns (4.5MHz-pulse repetition rate Eu-XFEL)
  - Burst operation mode (Eu-XFEL)
  - Continous operation mode (LCLSII up to 1MHz!)
- Dynamic Range
  - Single photon counting
  - Up to 10^4 ph/pixel/pulse

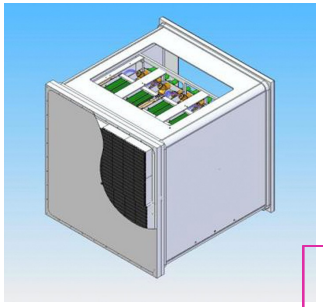
- Sensitive Energy Range
  - 0.25-25 keV ideally with the same system
- Radiation Hardness
  - 10 MGy-1 GGy over 3 years operation
- Pixel size:
  - 700-20 μm, depending on distance & angular resolution required
- Large area coverage:
  - multiple tiles with no dead area

Overview of Eu-XFEL 2D imaging detectors



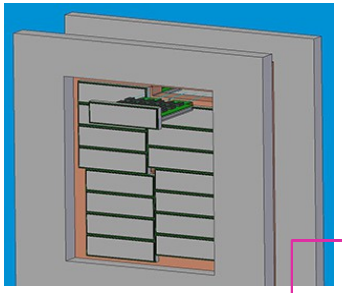
- Well advanced projects based on highΩ hybrid pixels
- Modular detectors with dead area ~ 15%
- PixFEL aims to improve on dead area, pixel size, storage cells with new technologies & adopts an innovative solution for a dynamic signal compression in the front-end

Large Pixel Detector (LPD)



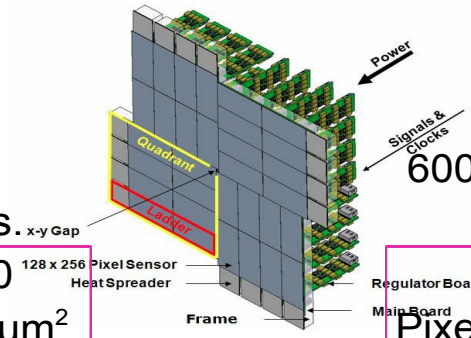
Energy range
5 (1) - 20 keV (25 keV)
Dynamic range
10^5@12 keV
Single Photon Sens.
Storage Cells ≈ 512
Pixel Size 500 x 500 μm^2

AGIPD Adaptive Gain Integrating Pixel Detector (AGIPD)



Energy range
3 - 13 keV
Dynamic range
10^4@12 keV
Single Photon Sens.
Storage Cells ≈ 300
Pixel Size 200 x 200 μm^2

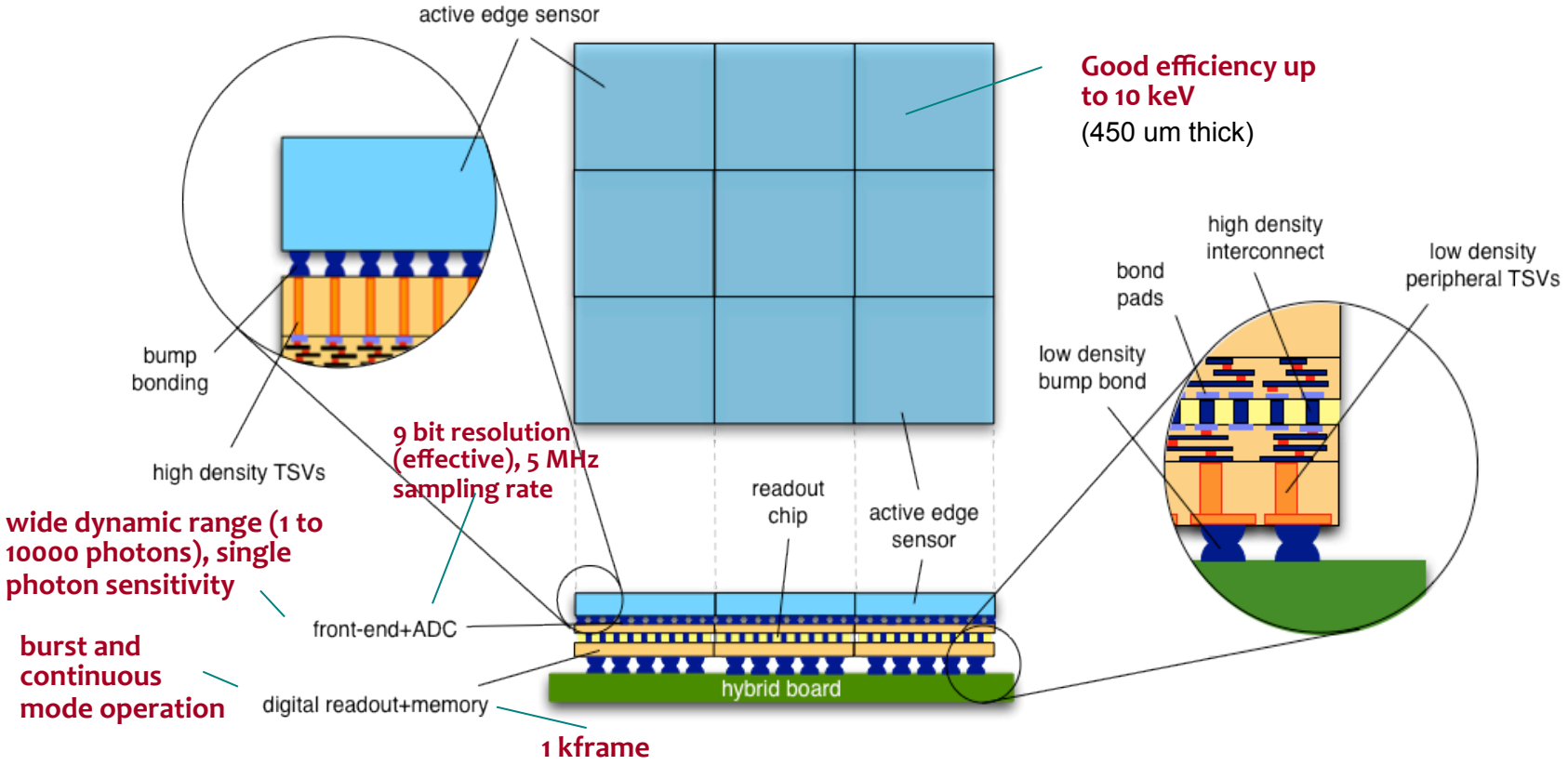
DEPFET Sensor with Signal Compression (DSSC)



Energy range
0.5 - 6 keV (25 keV)
Dynamic range
6000 ph/pix/pulse@1 keV
Single Photon Sens.
Storage Cells ≈ 640
Pixel Size ≈236 x 236 μm^2

Long term goal of PixFEL

- Develop a four side buttable, multi-layer module for the assembly of a large area X-ray detector with minimum dead area
  - active edge thick pixel sensor, two tiers CMOS readout chip (analog+digital/ memory), low/high density TSV, 65 nm to increase memory and functionality, smaller pixel pitch of 100 μm.



PixFEL target specifications

Single tile (2014-2016)

Time, complexity

- Pitch: 100x100 μm^2
- Tiling "without" dead area
  - → active edge sensors ~ 2% dead area
  - → low density TSV to connect I/O chip PAD to hybrid board
- Single photon counting & Wide dynamic range, 1-10^4 photons (1-10 keV)
  - →Preamplifier with dynamic signal compression
- A/D conversion in 200 ns (Eu-XFEL)
  - → Successive approximation 10 bit ADC (SAR ADC)
- Memory: 1k frame depth
- Readout:
  - Burst mode: Eu-XFEL 4.5 MHz frame rate, 1% duty cycle
  - Continuous mode: 15 kHz frame rate or better?

Not covered in presentation

System (>2016, still to be optimized)

- Tot. area ~20x20 cm^2
- Chip 64x64 pixel, ladder=sensor=2.56x5.12 cm^2, 4x8 chips/ladder
- Bandwidth: 0.6 Gb/s/chip & 20 Gb/s/ladder

PixFEL 3-years activities

2014

- define chip specifications.
- design of test structures with single blocks (analog front-end, ADC, circuits for gain calibration, single MOS capacitors, I/O circuits), CMOS 65 nm
- design of a 8x8 matrix, 100 um pitch
- design of 1st batch active edge pixel sensors
- start investigation on readout electronics

Costruzione e test di un dimostratore 32x32 (sensore active edge + readout chip) che verifichi alcuni degli elementi piu' innovativi del progetto.

2015

- test the structures from the first run
- Radiation hardness studies (sensors & front end)
- start investigation on 3D integration processes, including low density TSVs
- design of the 32x32 matrix (accounting for low density TSVs)
- start organizing the test beam

2016

- design 2nd batch active edge pixel sensors
- test the 32x32 front-end chip
- test the chip after interconnection with the the active pixel sensor
- VHDL design of the readout electronics fro a full size chip prototype
- test the chip with beam

Attività a Pisa (2014-15-16)

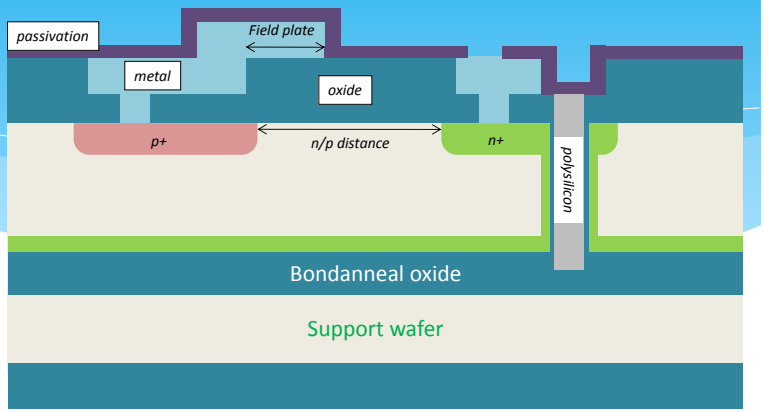
- Collaborazione alla definizione delle specifiche
- Contatti con le facilities FEL
- Progetto logica in-pixel e architettura readout per i 2 chip prototipo singolo layer (8x8→2014 , 32x32→2016)
- Collaborazione progetto ADC SAR con PV
- Progetto e costruzione schede di test
- Caratterizzazione in lab dei vari chip prototipo
- Interconnessione e test chip-sensore
- Contributo al progetto del chip digitale per chip 2 layers (3D)
- Test su fascio

Dove siamo arrivati

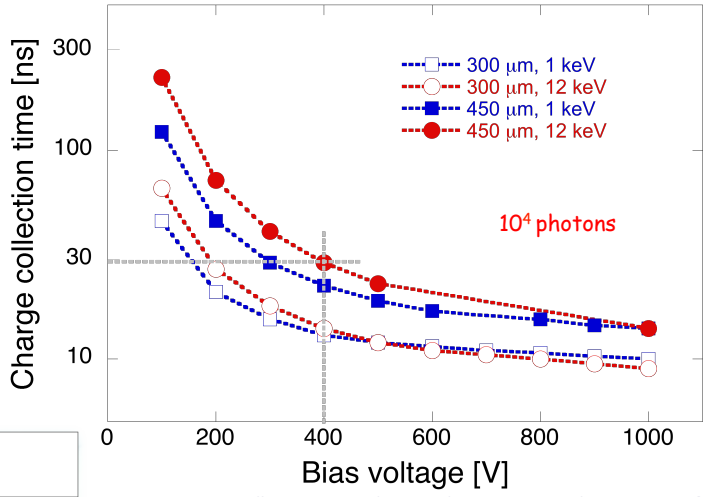
Active edge sensors (TN)

- Active edge to minimize the gap between the last active element and edge of the sensor but avoid high leakage current injection from the damaged cut region.

  → Cut lines not sawed but etched with DRIE & doped to act as electrodes



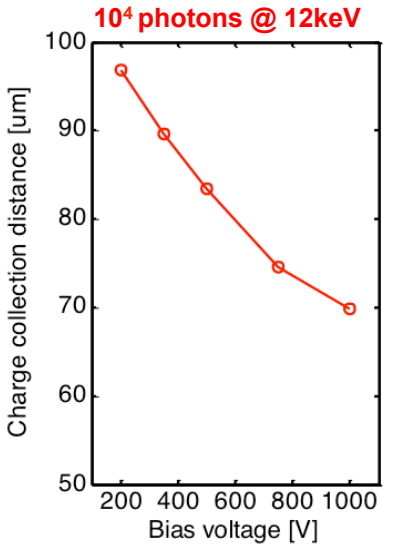
- **Main issues for FEL applications**
- Plasma effect: high charge concentration from huge signal (10^4 photons 1 keV → $2.8x10^6$ e-/h > 100 MIP), reduces collection field & deteriorate charge Collection Distance (CD) and Collection Time (CT)
- Thick sensor (450 μm) for good efficiency @ 10 keV
- Thin entrance window for good efficiency @ 1 keV



TCAD simulation campaign

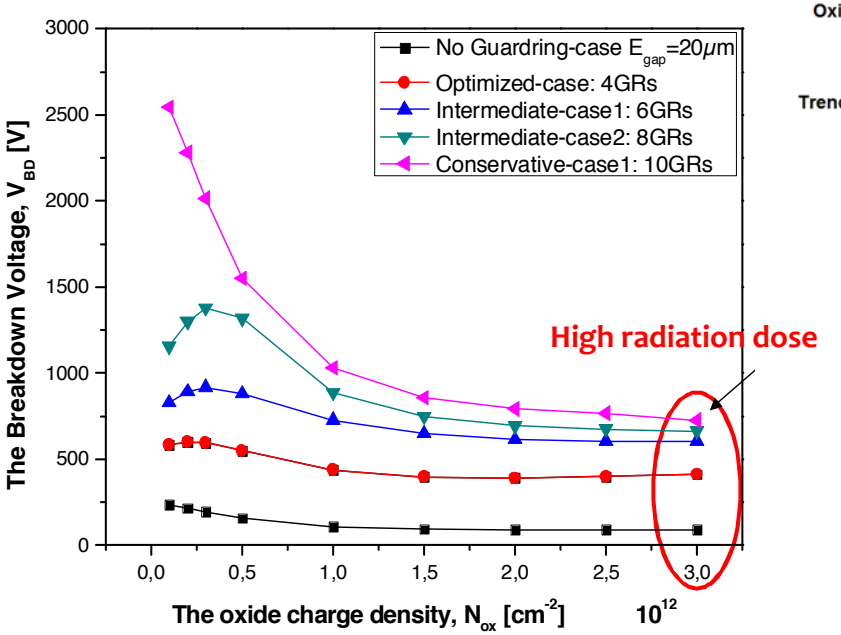
→ High Bias voltage mitigates plasma effect: with Vbias=400 V fast collection time (<30 ns) & collection distance < 100 μm

→ Edge geometry optimized to increase breakdown voltage

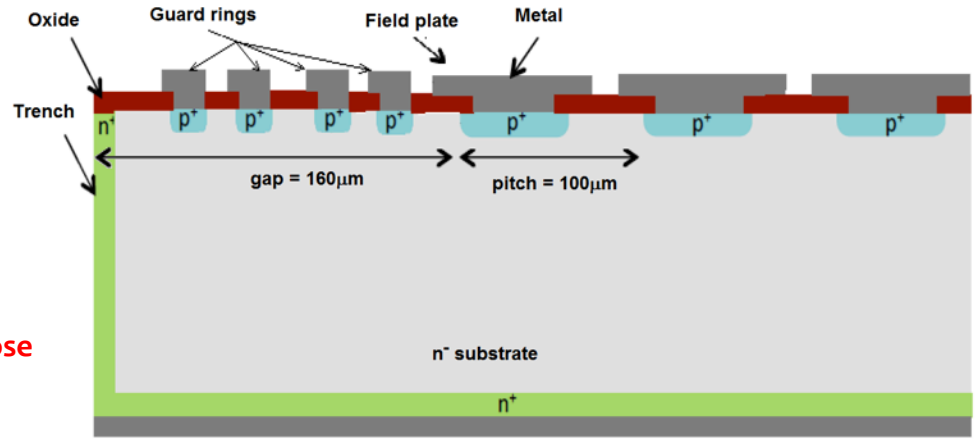


Sensor optimization for FELs

- Edge geometry optimized to increase breakdown voltage:
  - Edge distance, floating guard rings, field plate
  - Oxide thickness, junction depth
- With present optimization $V_{breakdown}$ > 400V for entire operation lifetime:
  - 4 guard rings with external field plate
  - 2.4 μm junction depth
  - 300 nm oxide thickness
  - max Q_{OX}=3e12 cm^{-2} (=high radiation dose)

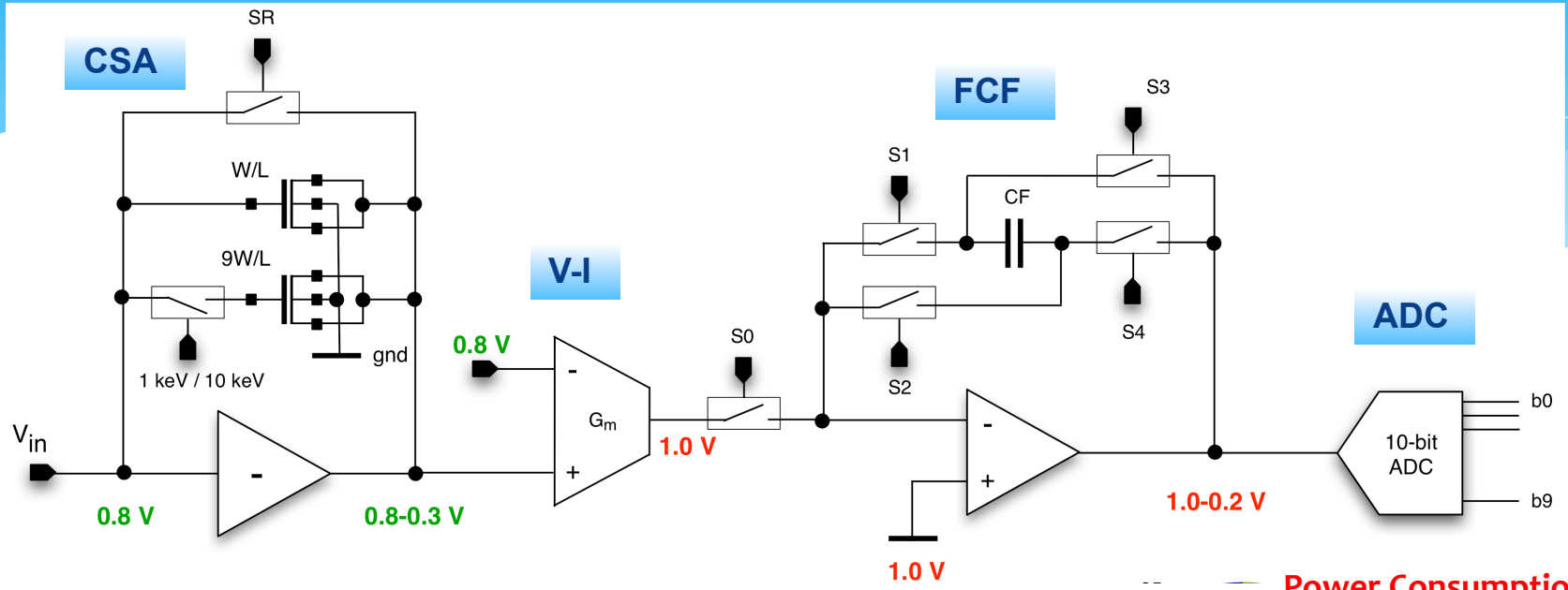


- First pixel at 160 um from the edge ~2% dead area

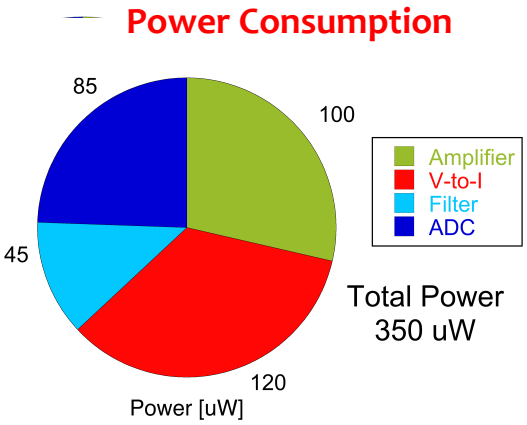


- The first PixFEL sensor batch is now in fabrication @ FBK (Trento, Italy)

Readout Channel (PV/BG)



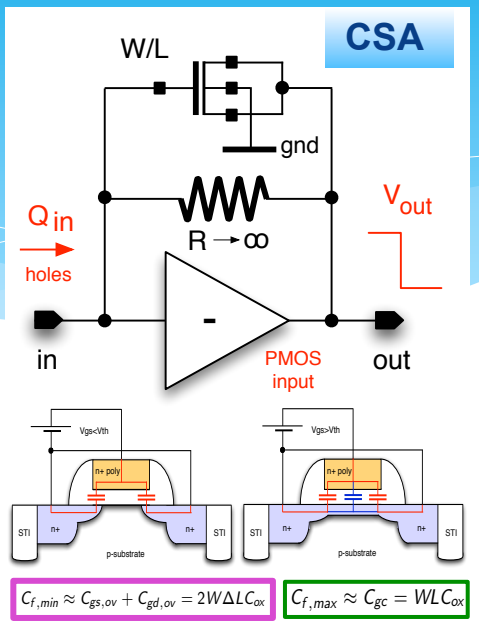
- Charge Sensitive Amplifier – dynamic signal compression
- Transconductor – voltage to current convertion
- Flipped Capacitor Filter – variable gain and integration time
- Analog-to-digital conversion – 10 bit SAR ADC
- Technology – 65 nm CMOS (TSMC)
- Two test chips realized now under test:
  - single blocks + 8x8 matrix with 110 um pixel cell
- Post Layout Simulation ENC=60 e- rms → SNR=4.7 for 1 keV (280 e-)

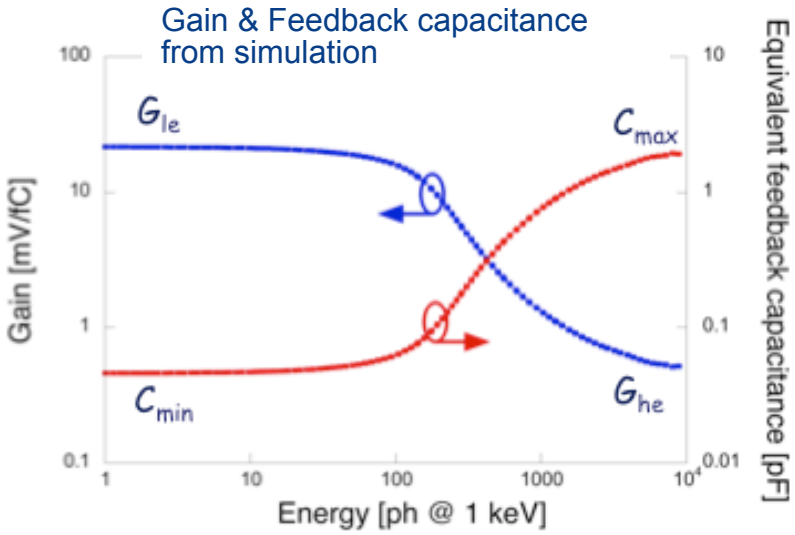


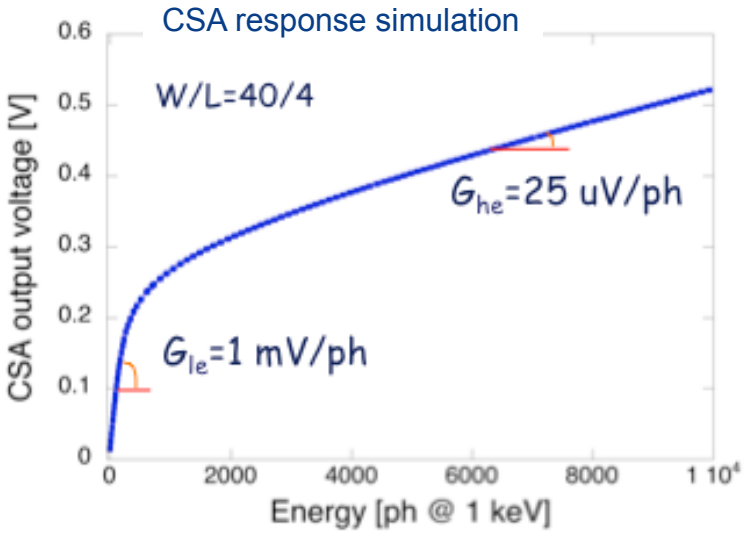
Dynamic Compression

- Wide dynamic range front-end channel
- 1-10^4 photons between 1-10 keV
- Bilinear Amplifier: use the non-linear features of MOSFET capacitor, in inversion mode, to dynamically change the gain with the input signal amplitude
  - For low energy → High gain & For high energy → Low gain

$|\Delta V_{OUT}| << V_{TH} \rightarrow C_f = C_{min}$, Gain=$1/C_f = G_{le}$ $|\Delta V_{OUT}| >> V_{TH} \rightarrow C_f = C_{max}$, Gain=$1/C_f = G_{he}$

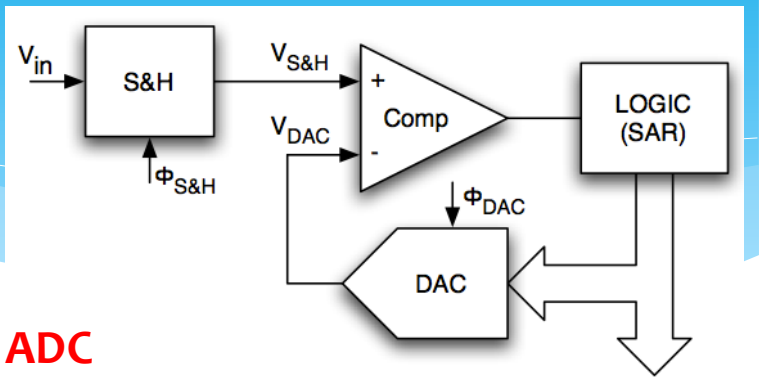




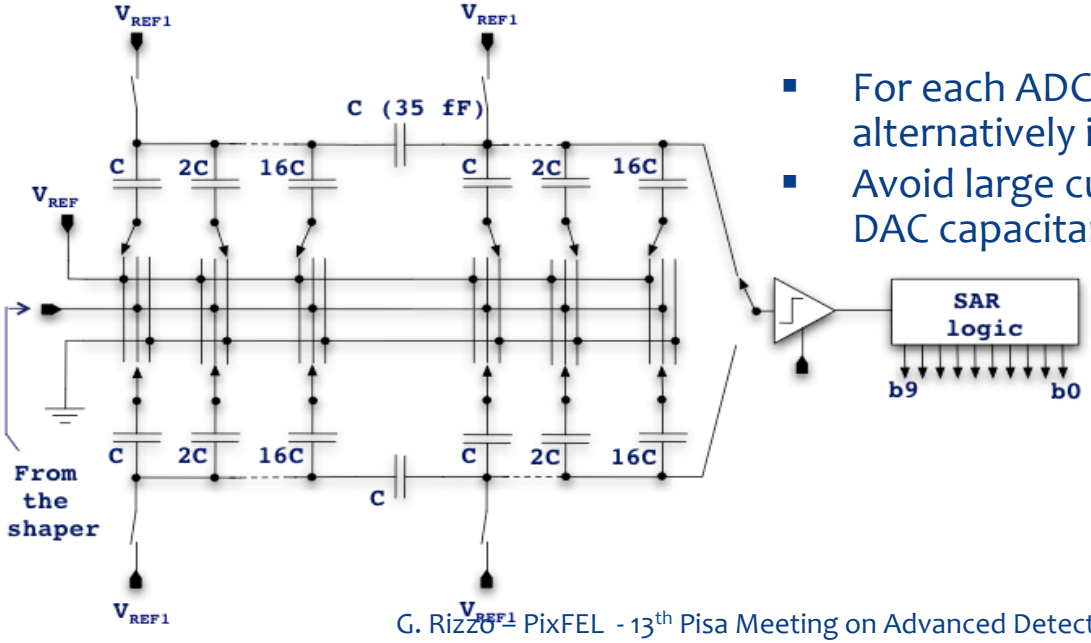


In pixel ADC

- **Requirements:**
  - Wide dynamic
  - Large number of bits
    - guarantee single photon resolution at small signal
    - small quantization noise in Poisson-limited regime
  - 5 MHz sampling rate (for Eu-XFEL)
- **10 bit SAR (Successive Approximation Register) ADC**
  - good compromise between clock frequency and resolution.
  - Clockfrequency=5MHz×11=55MHz



$$V_{in} = b_1 \frac{V_{ref}}{2} + b_2 \frac{V_{ref}}{4} + b_3 \frac{V_{ref}}{16} + \cdots$$



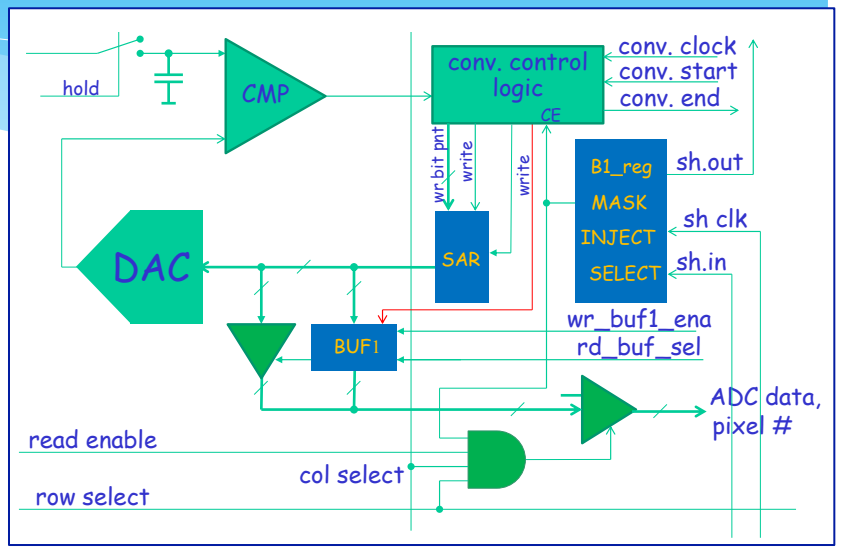
- For each ADC use **2** split capacitive DACs that work alternatively in a time interleaved structure
- Avoid large current peaks due to fast charge of the DAC capacitance (~2.5 pF)
  - Precharge of the DAC input capacitance during one entire sampling period
  - Conversion during the following sampling period

In pixel logic & readout for test chip (PI)

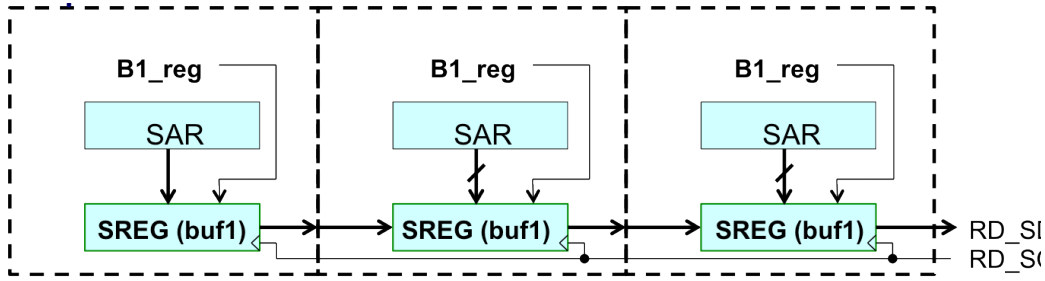
Readout designed for first test chip with flexibility to study performance of the front-end and possible cross talk effects.

- 2 sets of commands available: different timing among various pixels of the matrix possible.
- 2 in-pixel buffers available; study cross talk inside the pixel itself among various phases of two successive events.

Pixel cell logic



Concept for Matrix readout

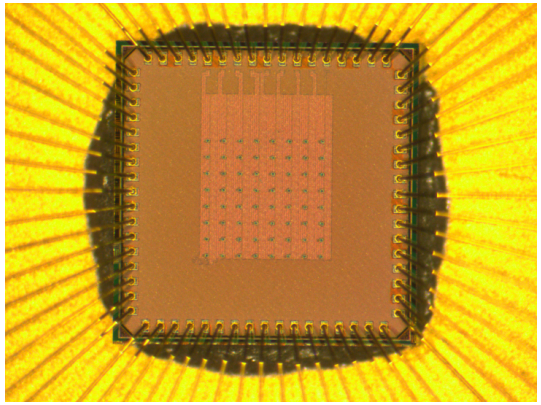


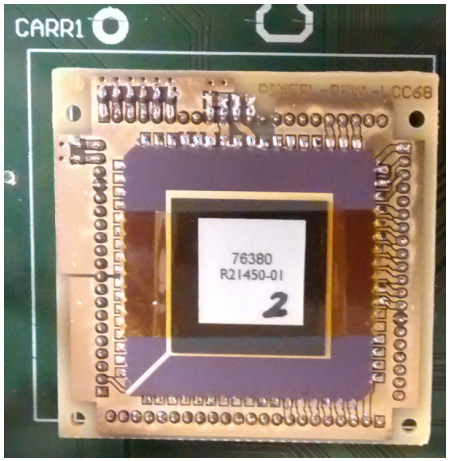
First concept for fast matrix readout will be explored:

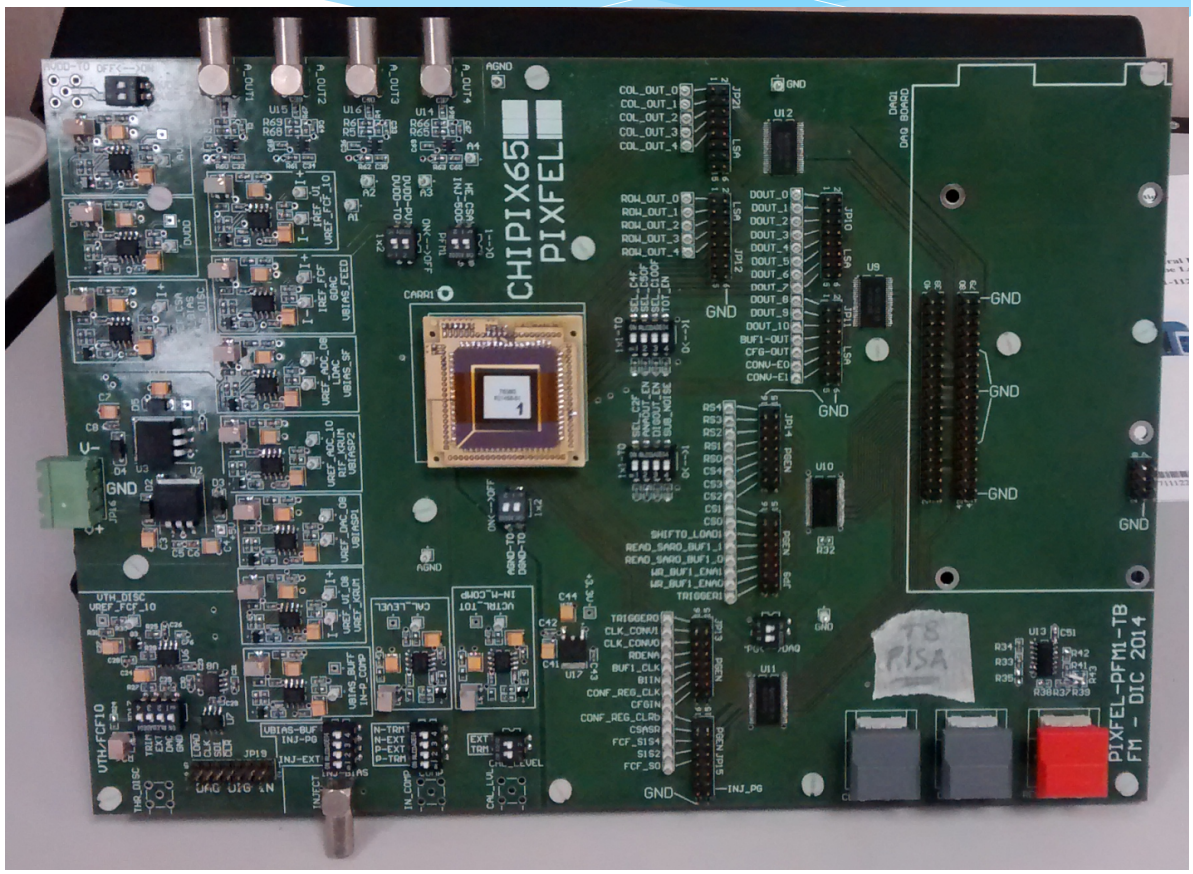
- for fast sequential readout the in-pixel buffer can be configured as a shift register to serialize output data on a single line.

Test board (PI)

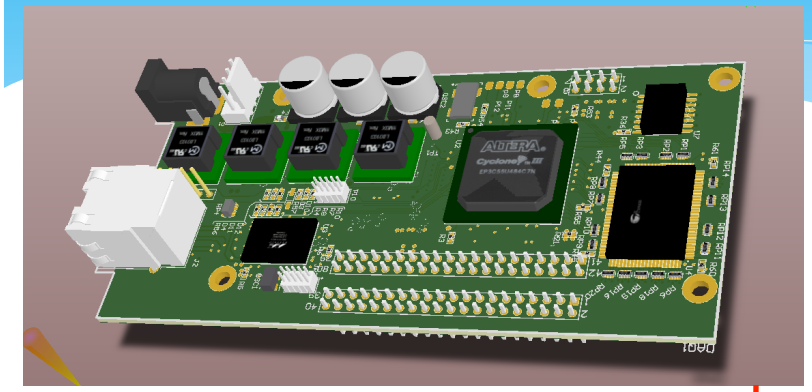
- Realizzate le schede di test dei chip PixFEL da Morsani ed esportate nei vari lab (Pisa PV/BG TO-CHIPX65) per I test dei vari chips
  - Progetto usato in sinergia anche per schede per CHIPIX65





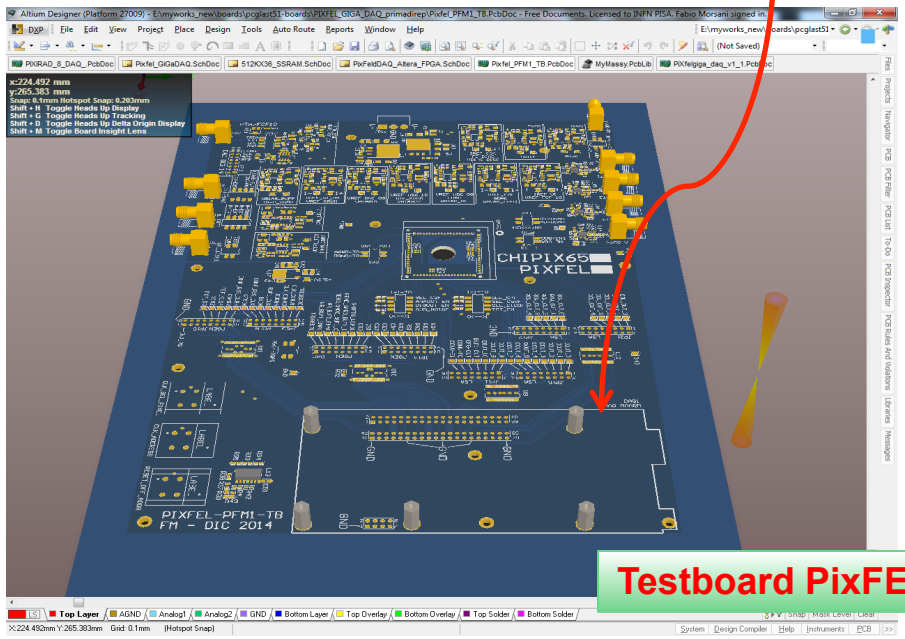


GiGa DAQ a general purpose FPGA based DAQ Board (PI)



- Schede di DAQ realizzate in passato da INFN-Pisa (Minuti) per l'acquisizione dati da sensori per Imaging digitale
- Possibile riadattare GiGa DAQ per lo schede di test PixFEL (CHIPIX65) per sostituire il Pattern Generator ed il Logic State Analyzer.

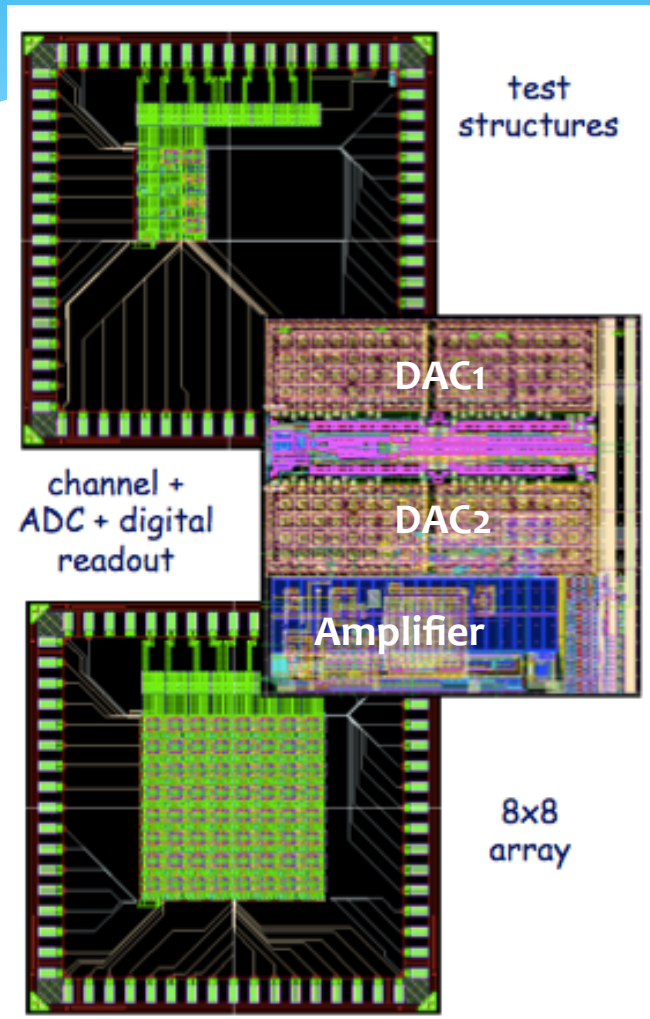
Sistema DAQ portatile per test su fascio !

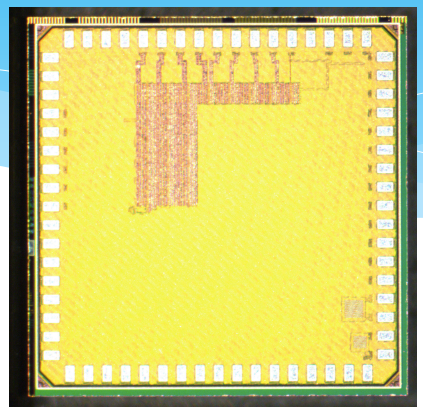


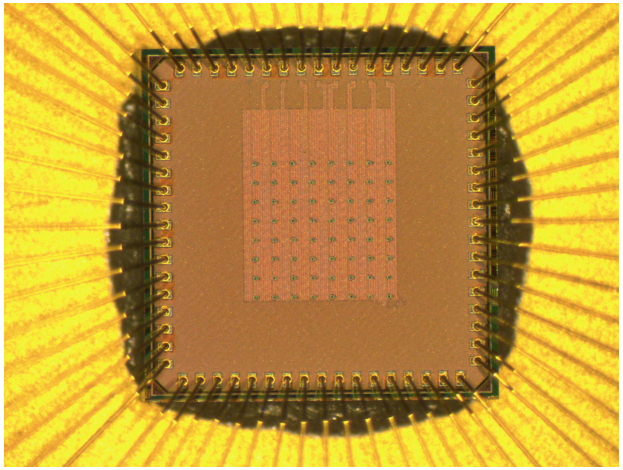
Testboard PixFEL

Dimensions:	6 cm X 12.5 cm
Supply:	12V 1.5A
Board Clock:	125MHz TTL
Interfaces:	1Gb Ethernet
FPGA Device:	Altera EP3C55
Memories:	64Mbit FLASH
	2MB SSRAM
GPIO:	60 X 3p3V TTL IOs

Misure sui chips prototipo (PV/PI)

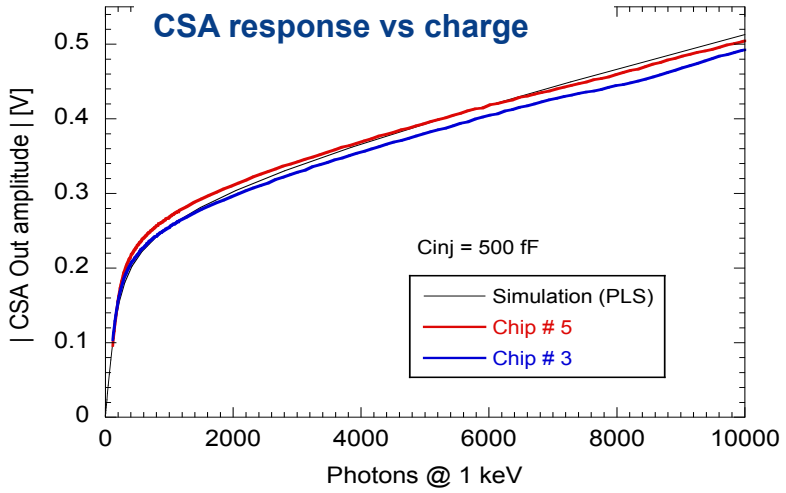


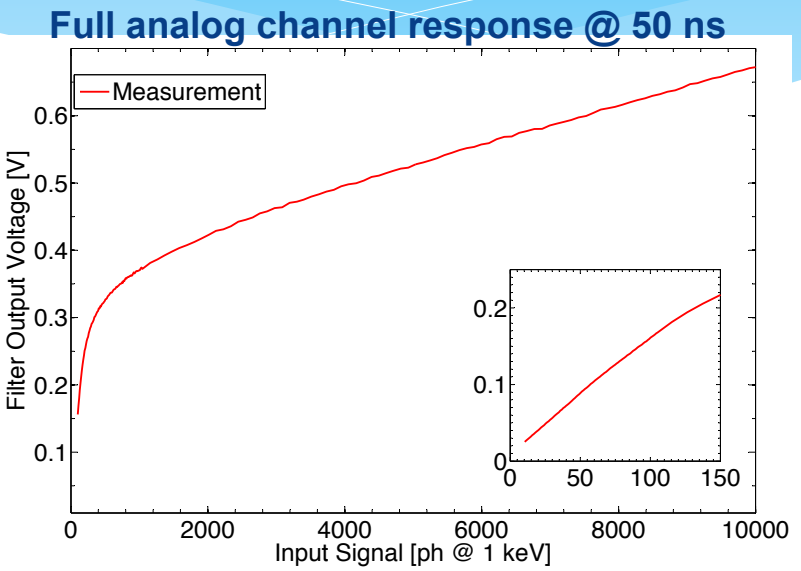


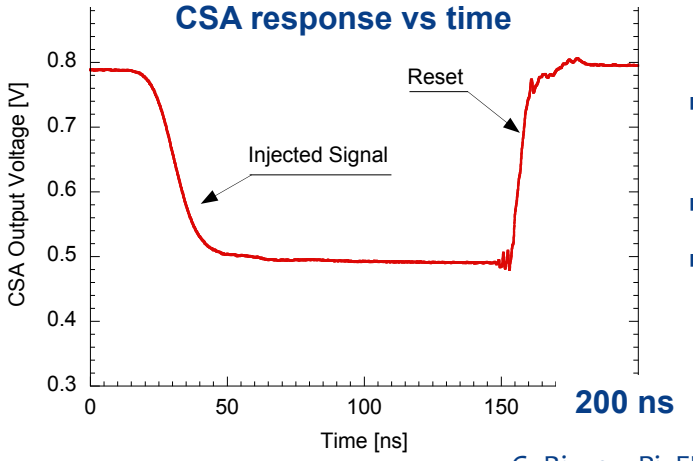


Preliminary Measurements on test chips

- Risultati molto positivi: primo chip a 65 nm con compressione dinamica del segnale ($10^4\,\gamma$), single photon capabilty, 50 ns integration time



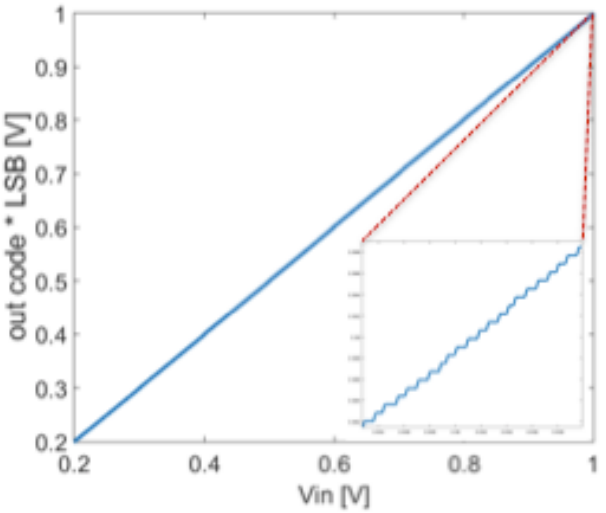


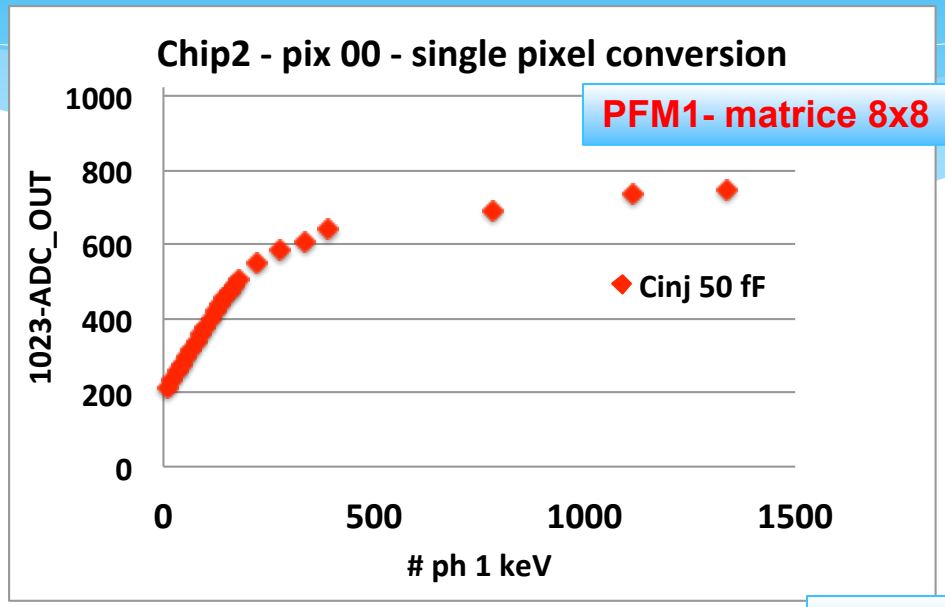


- Charge amplifier (CSA) shows the expected bilinear feature in the gain, in agreement with simulation (PLS).
- Fast transition and reset time measured (<30 ns),
- Full channel response measured with the filter operated successfully @ 50 ns integration time compatible with 4.5 MHz operation of Eu-XFEL

Preliminary Measurements on test chips

ADC measured response @ 20 MHz





Pisa-8x8 matrix

- Buona linearita' del 10-bit SAR ADC (in pixel) su tutto il range
- Confermata risposta bilineare anche nel canale completo (front-end + ADC) della matrice 8x8
- Gain low_energy =1.5 mV/ph, Gain high_energy=0.09 mV/ph
- Noise 0.4-0.9 ADC counts →60-140 e-
- Comportamenti anomali su alcuni pixel della matrice in corso di indagine

Pubblicazioni e Conferenze

- 3 articoli gia' pubblicati ed altri 3 in corso di pubblicazione
- 11 lavori gia' presentati a conferenze
  - Pixel2014, NSS2014, RESMDD14, Elba2015

PUBBLICAZIONI SU RIVISTA

1. M. Manghisoni, D. Comotti, L. Gaioni, L. Lodola, L. Ratti, V. Re, G. Traversia, and C. Vacchi, ``Novel active signal compression in low-noise analog readout at future X-ray FEL facilities", 2015 JINST 10 C04003. doi:10.1088/1748-0221/10/04/C04003.

2. G. Rizzo et al., ``The PixFEL Project: development of advanced X-ray pixel detectors for application at future X-FEL facilities", 2015 JINST 10 C02024, doi:10.1088/1748-0221/10/02/C02024.

3. L. Ratti et al., ``PixFEL: developing a fine pitch, fast 2D X-ray imager for the next generation X-FELs'', Nucl Instrum. Methods A, doi:10.1016/j.nima.2015.03.022.

PRESENTAZIONI A CONGRESSI

1. M. Manghisoni, L. Ratti et al., ``Novel Active Signal Compression in Low-noise Analog Readout at Future XFEL Facilities", presented at the International Workshop on Semiconductor Pixel Detectors for Particles and Imaging (PIXEL2014), Niagara Falls, Canada, 1-5 September 2014.

2. V. Re, ``The PixFEL project: advanced fine-pitch X-ray pixel detectors for the next generation FEL facilities'', Workshop on Research Opportunities at the European X-ray Free Electron Laser, Bologna, July 4 2014.

3. G. Rizzo, L. Ratti et al., ``The PixFEL Project: development of advanced X-ray pixel detectors for application at future X-FEL facilities", presented at the International Workshop on Semiconductor Pixel Detectors for Particles and Imaging (PIXEL2014), Niagara Falls, Canada, 1-5 September 2014.

4. L. Ratti et al., "The PixFEL project: developing a fine pitch, fast 2D X-ray imager for the next generation X-FELs", presented at the 10th International Conference on Radiation Effects on Semiconductor Materials, Detectors and Devices (RESMDD14), Florence, Italy, 8-10 October 2014.

5. L. Ratti et al., "PixFEL: Enabling Technologies, Building Blocks and Architectures for Advanced X-Ray Pixel Cameras at the Next Generation FELs", presented at the 2014 IEEE Nuclear Science Symposium, Seattle, USA, November 8-15 2014.

6. D. Comotti, et al., "Low-Noise Readout Channel with a Novel Dynamic Signal Compression for Future X-FEL Applications", 2014 IEEE Nuclear Science Symposium, Seattle, USA, November 8-15 2014.

7. G.F Dalla Betta, "Design and TCAD Simulations of Planar Active- Edge Pixel Sensors for Future XFEL Applications", 2014 IEEE Nuclear Science Symposium, Seattle, USA, November 8-15 2014.

Attivita' a Pisa 2016

- Sottomissione prototipo 32x32 (fine 2015 o feb 2016)
- Disegno/fabbricazione delle schede di test ed integrazione del DAQ per test beam (giugno)
- Inizio progetto chip digitale per prototipo 2 layers (3D)
- Caratterizzazione chip 32x32 in lab: (maggio-sett)
  - Scheda DAQ testabile gia' con il chip senza sensore
- Interconnessione chip 32x32 su matrice active edge del primo batch
- Caratterizzazione in lab del chip interconnesso con sensore
  - Test di funzionalita' e con sorgenti (Fe55, 5.9 keV, con Sr90 e-)
- Testbeam ~ Nov 2016

Richieste servizi di Sezione 2015

- Sviluppi del chip di elettronica e schede di test/DAQ
  - Morsani: 35%
  - Minuti: 20%
- Assemblaggi di chip
  - Supporto del servizio A.T., per incollaggi, microsaldatura

Richieste Pisa 2016

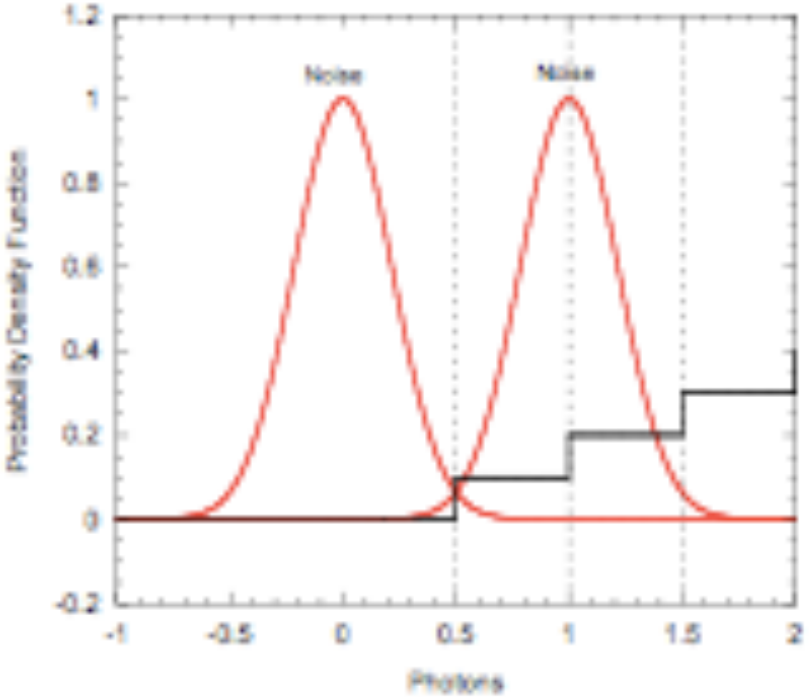
	2016		
		Richieste	commenti
Missioni	partecipazione a test beam	7500	
	trasporto materiale	1500	
	riunioni di collaborazione	1000	
	test congiunti	1000	
	TOTALE MISSIONI	**11000**	
Consumo	materiale per schede di test per prototipo 32x32 (PCB+carriers+componenti)	2000	
	interconnessione chip e sensore con bump bonding a IZM: preparazione 2 wafer sensori e assottgliamento (9kE) + 10 chip RO (23kE)	32000	
	meccanica per test su fascio	2000	
	shipping box per traporti	1000	
	schede per acquisizione (FPGA+1Gbit Ethernet + connectors + LVDS, PCB, Assembly)	2500	
	TOTALE CONSUMO	**39500**	
Inventariabile			
totale	Totale	50500	

Personale a Pisa 2016

NOME	Qualifica	Percentuale PixFEL
Bettarini	RU	30%
Casarosa	Assegnista	20%
Forti	PA	30%
Paladino	Assegnista	30%
Paoloni	RU	20%
Rizzo	RU	50%
Morsani	Tecnologo	35%
Minuti	CTER	
PERSONALE FULL TIME		**2.2**

backup

Single photon detection



Assume

- Gaussian distribution for the electronic noise with

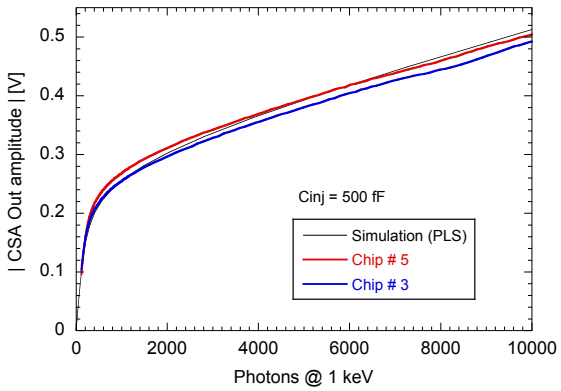
$$ENC = 60e - rms$$

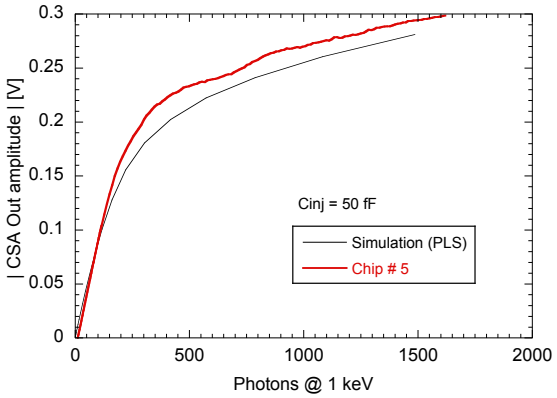
- ADC threshold of the 2nd bin placed @ 1st photon

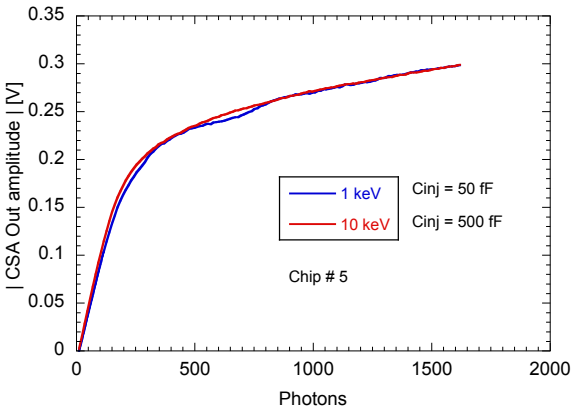
- The probability that a zero signal is misinterpreted as a one photon signal is 1%
- The probability that 1 photon signal is correctly attributed to the first 2 bins is 98%

Preliminary Measurements on test chips

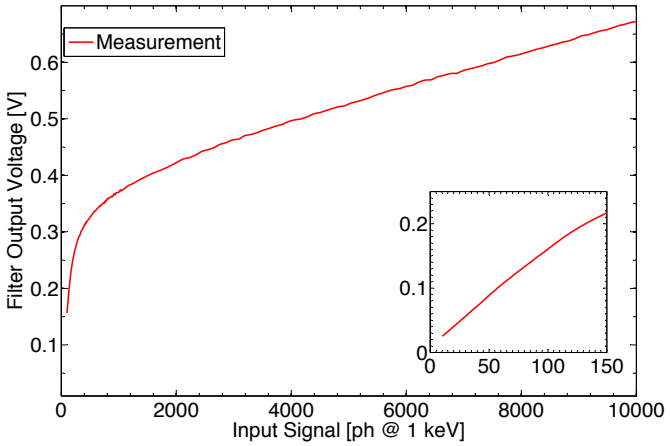
CSA response

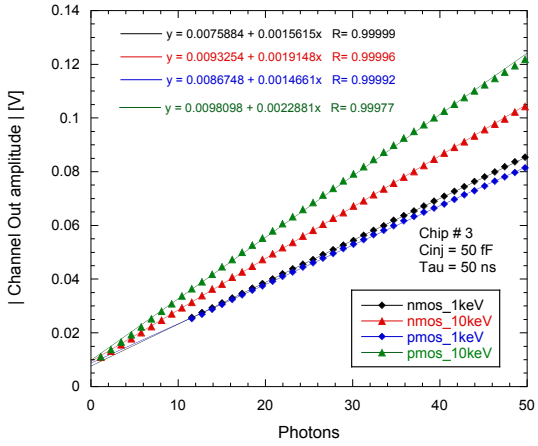






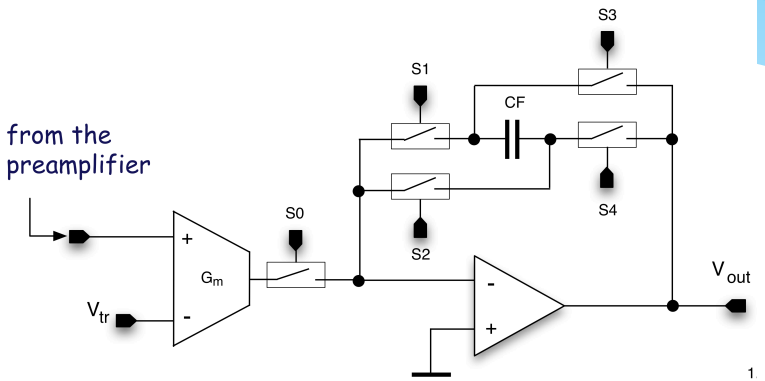
Full channel response with 50 ns integration time



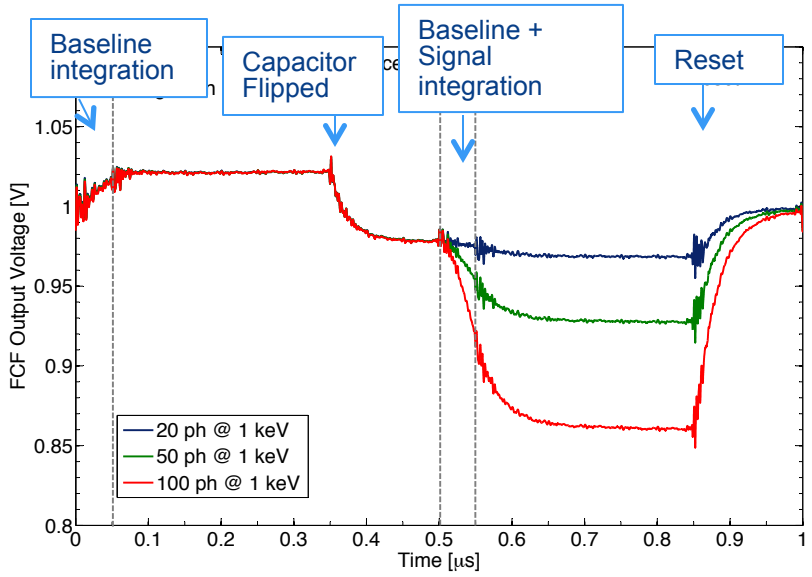


Preliminary Measurements on test chips

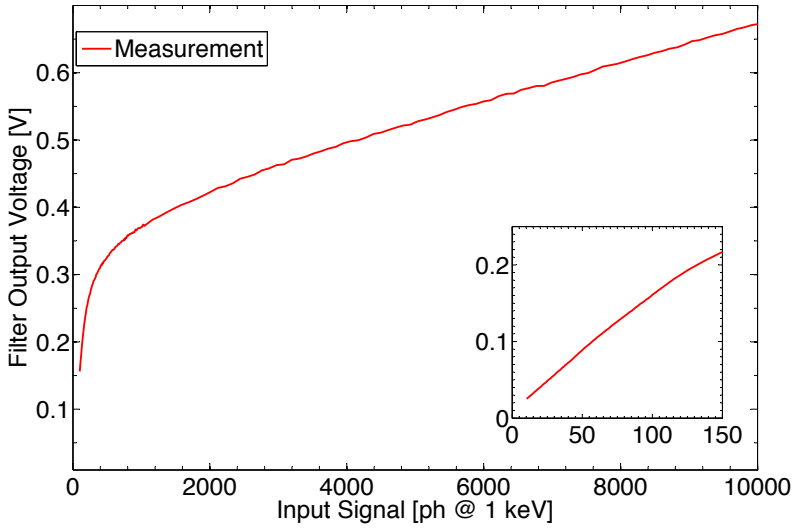
- **Full analog channel operated successfully with 50 ns integration time compatible with Eu-XFEL time structure**



- Flipped Capacitor Filter (FCF) performs correlated double sampling (CDS)
  - X-ray pulse arrives after first integration (Baseline)
  - During second integration (Baseline + signal) filter capacitor has been flipped and baseline is subtracted

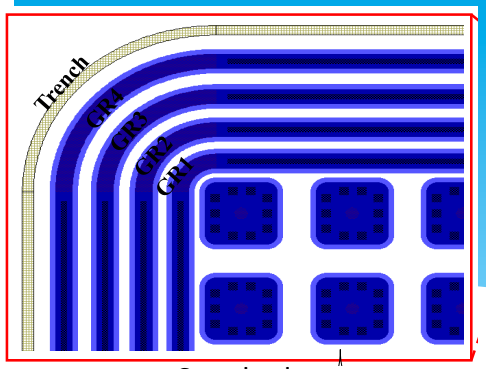


Full channel response @ 50 ns



PixFEL wafer layout

6-inch wafer including active edge & slim edge pixel sensors & test devices, to be fabricated at FBK (Trento, Italy)



Standard test structures

15x15 arrays for capacitance extraction

Large diode w/o Active Edge (6GRs)

8x8 arrays with Active Edge

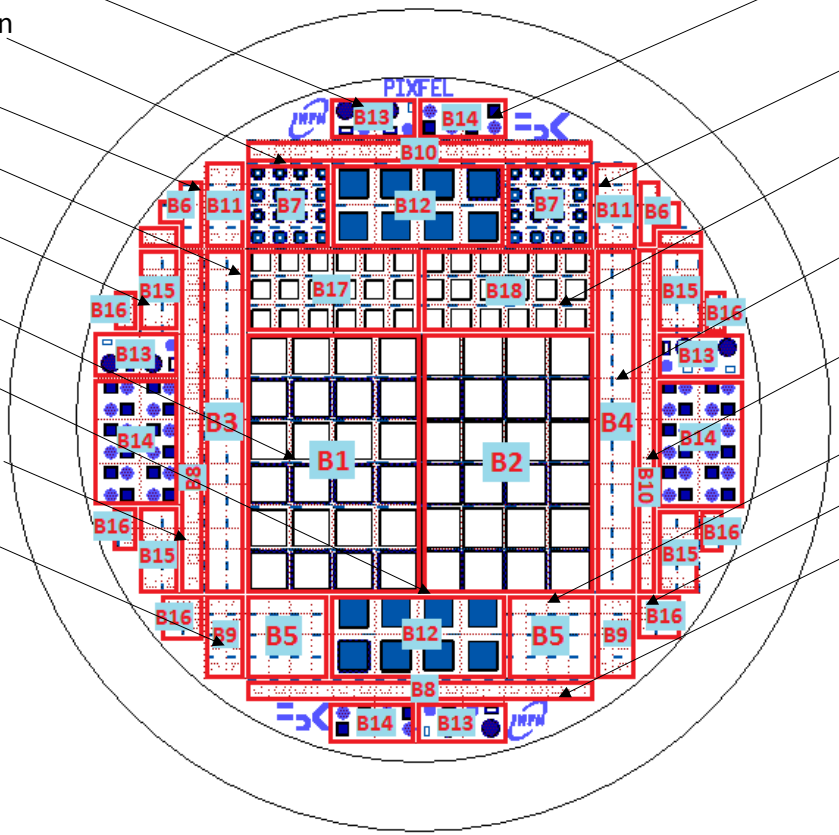
8x8 arrays with column trenches

64x64 Pixel array

Strip Sensors with Active Edge

Large diodes with column trenches

8x8 arrays with Slim Edge



Test structures for irradiation

8x8 arrays with overlapped slim Edge

32x32 Pixel array

8x8 arrays with Active Edge

Large diodes with overlapped Slim Edge

Large diodes with Active Edge

8x8 arrays with Slim Edge

Large diodes with Slim Edge

Problem of missing data

Modules of limited size and gaps between modules

➔ lots of missing data ➔reconstruction may become ambiguous

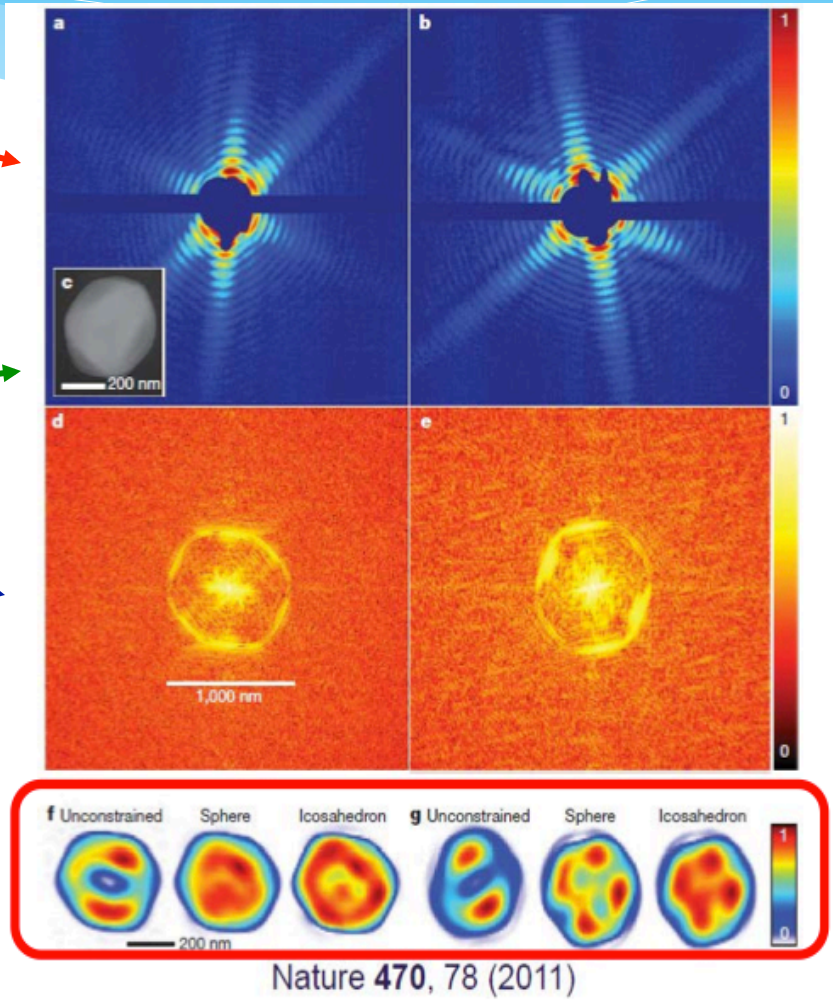
2 single shot diffraction pattern images of a large virus, 0.75 μm diameter, taken with pnCCD detector at LCLS.

As a comparison the virus picture taken with a transmission electron microscope (30000 images averaged)

Autocorrelation function for the 2 diffration patterns

Possible reconstructed images of the virus with ambiguities coming from missing data:

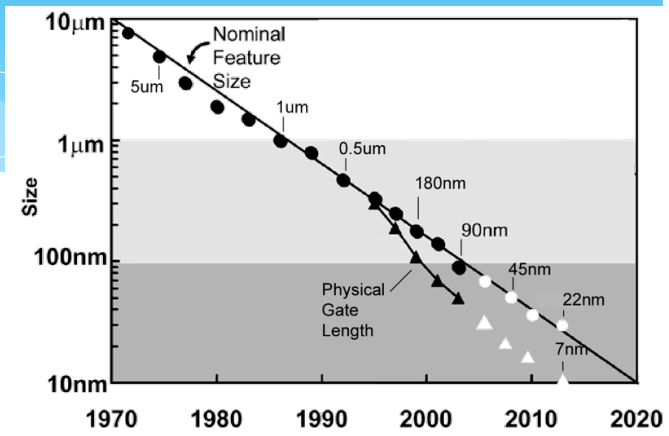
- dead area
- saturation of pixel in the central region.

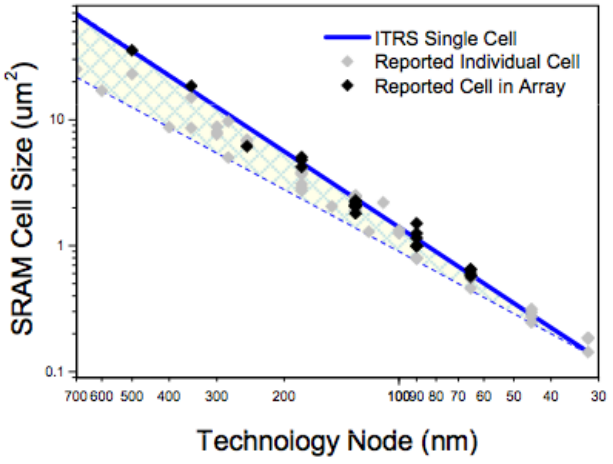


Nature **470**, 78 (2011)

PixFEL technologies: 65 nm CMOS readout electronics

- Mature technology:
  - available since 2007
- High density and low power
  - High density vital for smaller pixel and increased data buffering during bunch trains
  - Low power tech critical to maintain acceptable power for higher pixel density and much higher data rates
- Long term availability
  - Strong technology node used extensively for industrial/automotive
- Significantly increased density, speed and complexity compared to previous generations
- Important sinergy with R&D activities for LHC upgrade





Readout architectures

- No sparsification possible for these imaging detectors
  - large amount of data to be read out in a relatively short amount of time, also depending on the structure of the X-ray beam
- Burst mode operation: data need to be stored locally and read out in the interval between two bursts;
  - 65 nm CMOS technology to increase storage capacity
  - Bandwidth needs for XFEL: 4.5 MHz frame rate, 1% duty cycle, 1k frames stored over 3k frames → 0.6 Gb/s/chip & 20 Gb/s/ladder
- Continuous operation: data are read out as soon as they are collected, frame by frame;
  - With low repetition rate (i.e. 120 Hz @ LCLS) continuous readout within reach of present technology: 5 Mb/s/chip & 160 Mb/s/ladder.

    → XFEL bandwidth needs much higher: equivalent to continuous operation @ 15 kHz frame rate
  - Readout for future LCLS II at high repetition rates (up to 1 MHz) very challenging!
- Capability of switching from one mode of operation to the other may be an important asset for a 2D imager

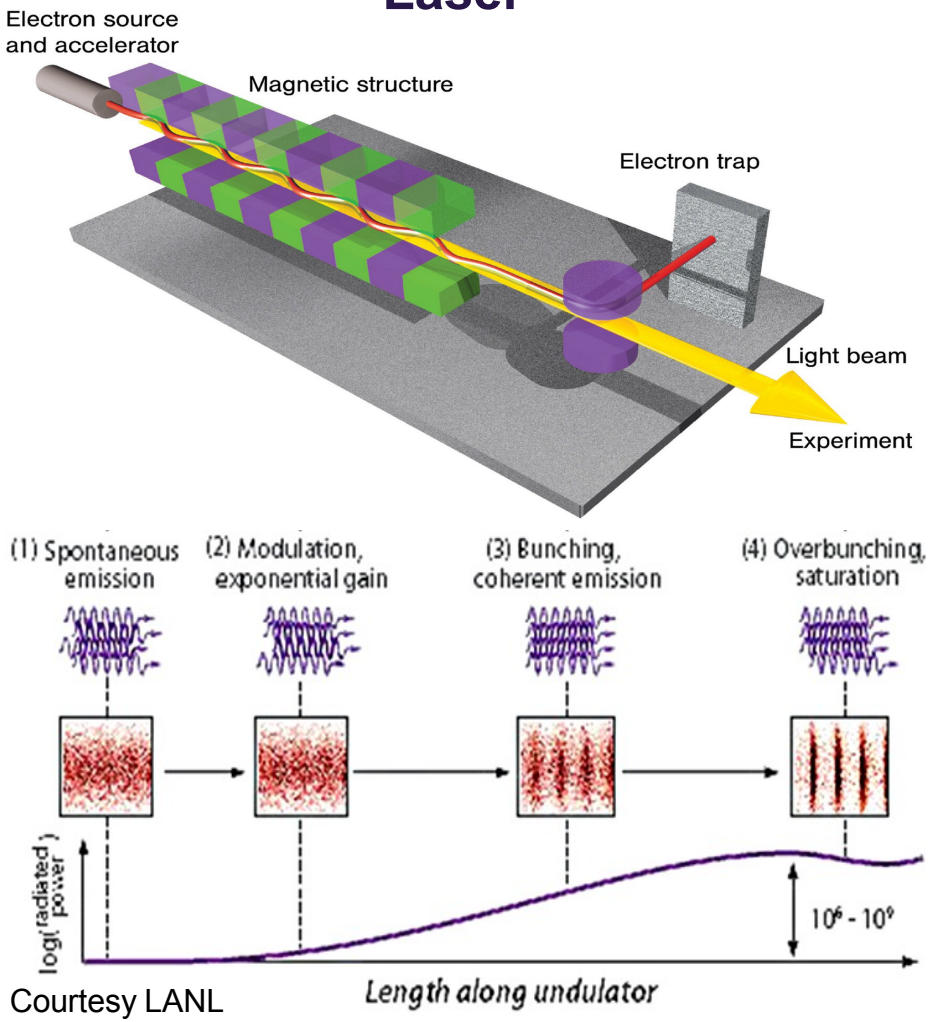
FELs in operation or under construction

Project	Start of operation	Electron beam energy [GeV]	Photon energy [keV]	Frame/Burst repetition rate [Hz]	Number X pulses/burst
FLASH@DESY	2005	1.25	0.03-0.3	5	800@1us
LCLS@SLAC	2009	14.5	0.3-10	120	1
SACLA@RINKEN	2011	8	4.5-15	60	1
Fermi@ELETTRA	2010	2.4	0.01-0.06	10	1
European-XFEL	2016	17.5	0.4-20	10	2700@220 ns
SwissFEL	2016	5.8	1/12	100	2@50 ns
LCLS II	>2020	4-14.5	0.2-25	120 - 10^6	1

After the success of first FELs, new facilities & upgrades are in design phase in many countries (i.e. LCLS II)

Free Electron Laser – How does it work?

Principle of an X-ray Free Electron Laser



Courtesy LANL

Wiggler

- No constructive interference of out-going radiation
- Broad spectrum
- Intensity proportional to N (N: Period)

SASE Undulator

- Longer, narrower emission cone
- Micro-bunching
  - Electrons interact with electro-magnetic field and reorganize to bunches
  - Constructive interference
    - → Sharp energy, coherent and high brilliance
  - Intensity proportional to N^2 and n_e^2

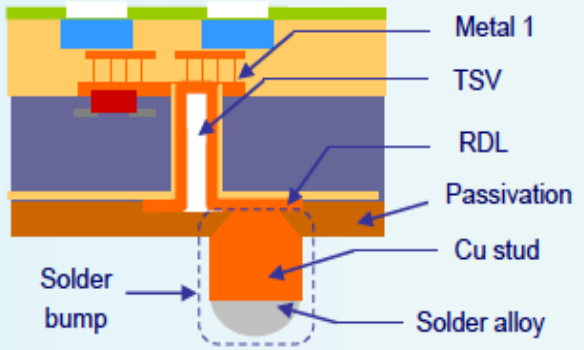
Enabling technologies for a 4-side buttable module

- Low density TSVs for chip to PCB bump-bonding

CEA-LETI

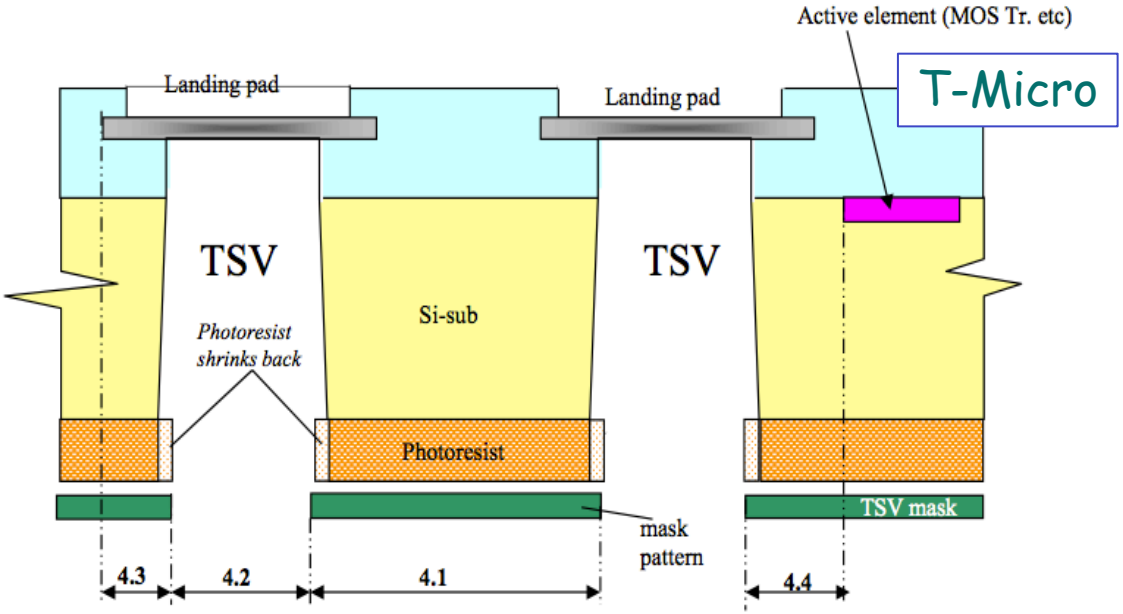
Solder bumps DRM & schematic

- Wafer size : **200 & 300 mm**
- Solder bumps material : **Cu stud / SnAg solder**
- Minimum pitch : **120 µm**
- Solder pillar diameter : **60-80 µm**
- Solder pillar thickness : **Cu 35-40 µm / SnAg 25-30 µm**



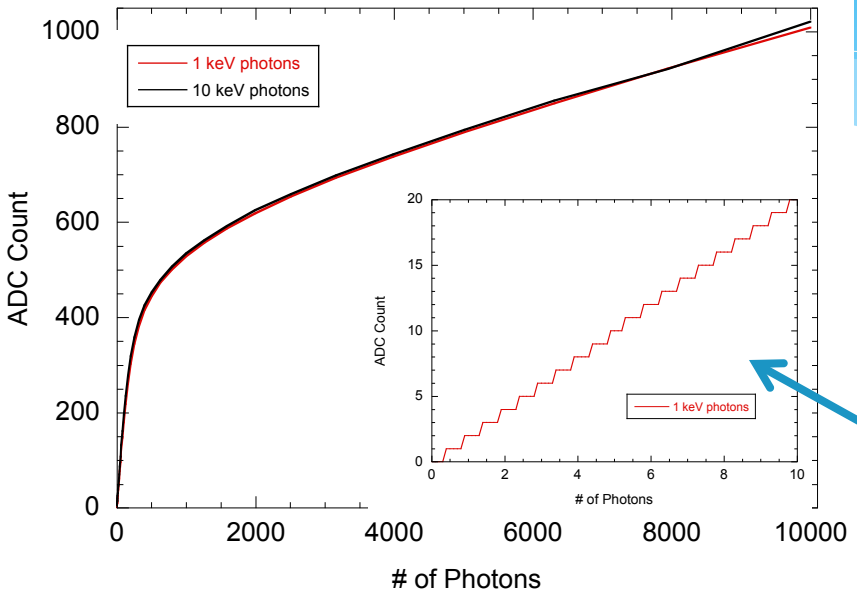
- No gaps, no need for complicate tiling (provided that the detector has minimum dead area)

T-Micro



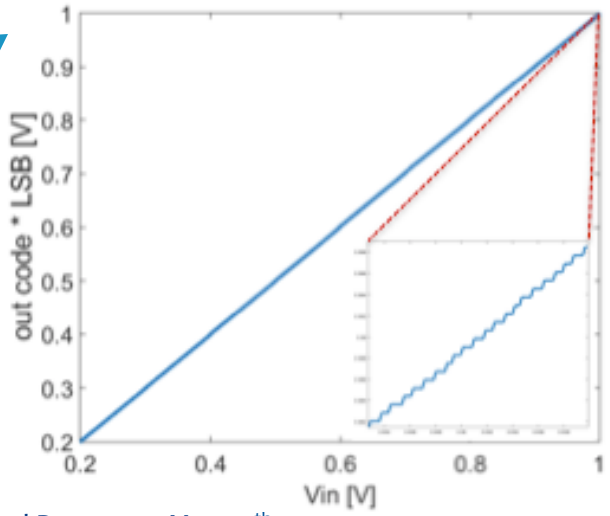
10-bit SAR ADC Performance

Full channel + ADC response - Simulation



- ADC Simulated performance
  - 0.2V-1V input dynamic range
  - INL and DNL < 0.5LSB
  - SNR 60 dB (ENOB=9.6)
  - Power ~ 70+15 μW
- ADC Area ~ 5000 μm²
- ADC dynamic range well covered
- Well detectable bilinear response of CSA
- First 10 photons well detectable

ADC measured response @ 20 MHz



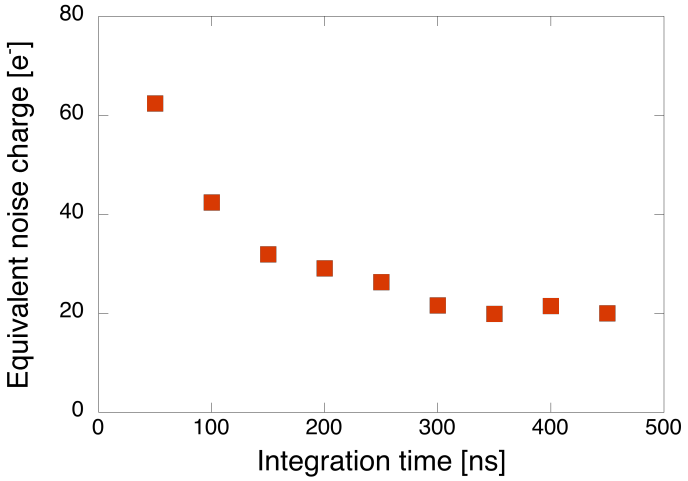
- Preliminary measurement of the ADC-only response shows good linearity over the full range (0.2V-1V)

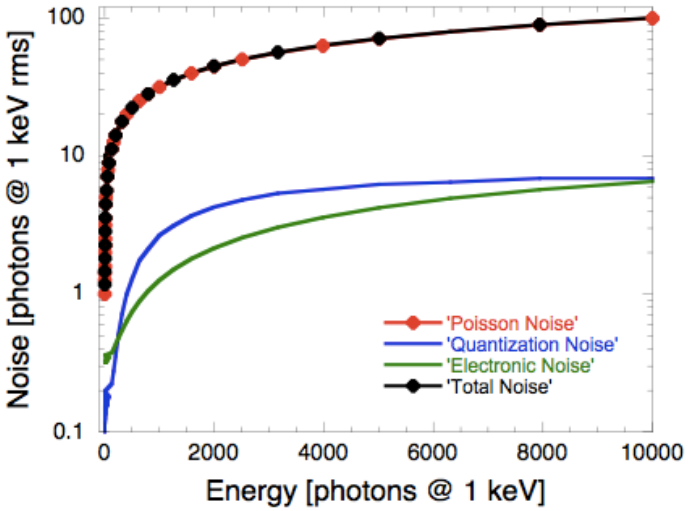
- See L. Lodola's Poster for details on ADC design & measurements

System Noise Analysis

- Electronic noise
  - due to analog front-end
  - ENC=60 e^- rms @ t=50ns (1 keV = 280e-)
  - Increases with increasing signal (Gain decreases)
- Quantization noise
  - due to ADC
  - negligible for small number of photons
  - #photons per bin/sqrt(12) for larger signal
  - Increases with increasing signal (Gain decreases)
- Poisson noise due to fluctuation of the number of photons that hit a pixel
  - irreducible

→ System performance dominated by the Poisson noise





Conclusions & Perspectives

- The PixFEL project is adopting several new technologies to build a fine pitch, rad tolerant, multi-layer, fast detector with minimum dead area for X-ray imaging at future at FELs
  - active edge sensors, 65 nm CMOS, TSV, 3D integration
- First prototypes (sensors and front-end chips) realized to evaluate the proposed innovative aspects
  - Encouraging results from preliminary tests on the front-end chips
  - Full characterization and rad tolerance test (sensor & electronics) in 2015
- In 2016 build a small module with sensor and front-end chip
- Longer term ambitious plan to develop full instrument