New service board

SYSTEM OVERVIEW AND nSB BOARD ARCHITECTURE

LHCb Italia Collaboration Meeting

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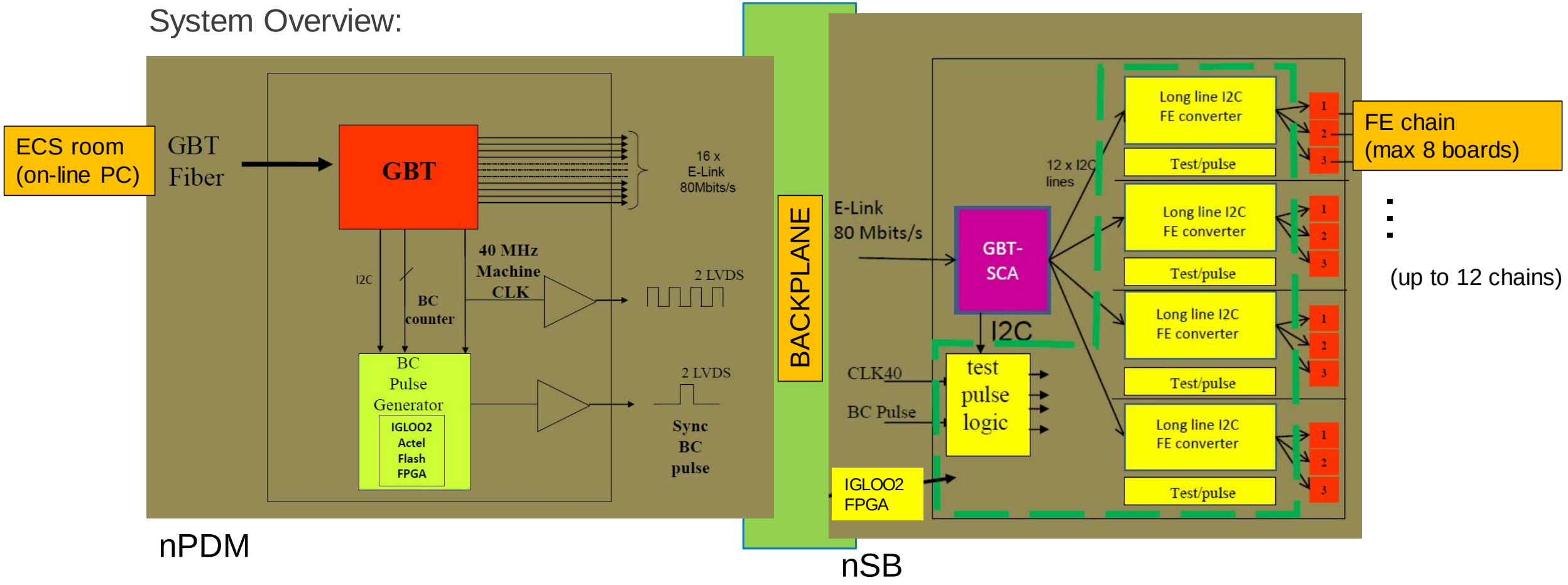
Introduction

System Overview:



Protocol converter

The communication between Service Board(s) and CARDIAC(s) device is made on a custom I2C bus. The distance greater than 10m forced to move toward a protocol derived from standard I2C:

- LVDS line (point-to-point connection)
- 3 wires (clock, output data and input data)

In the new Service Board system the CARDIAC (thus the DIALOG chips) are controlled directly from the ECS (no ELMB boards) through a standard I2C bus:

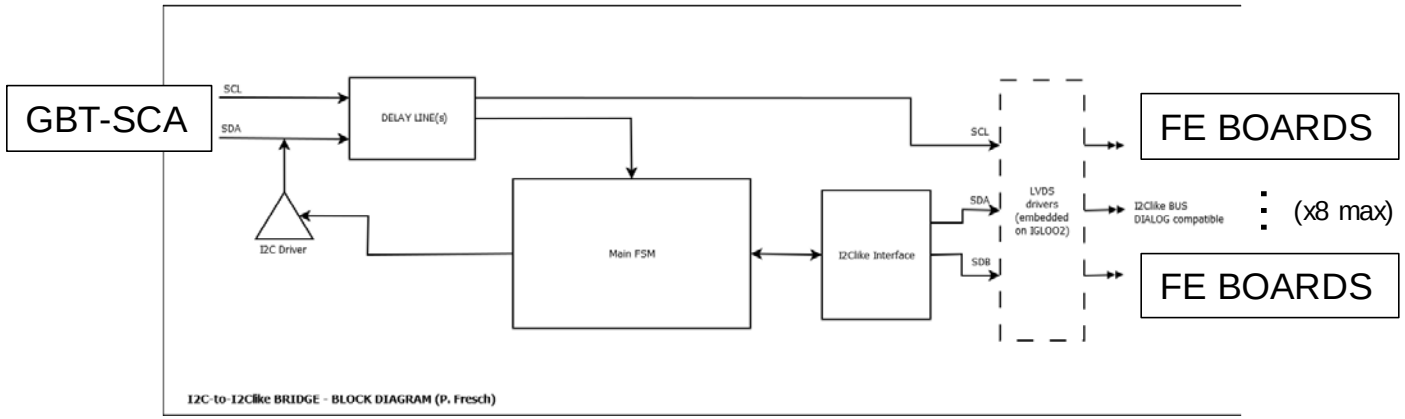
- Wired-OR line
- 2 wires (clock and bidirectional data)

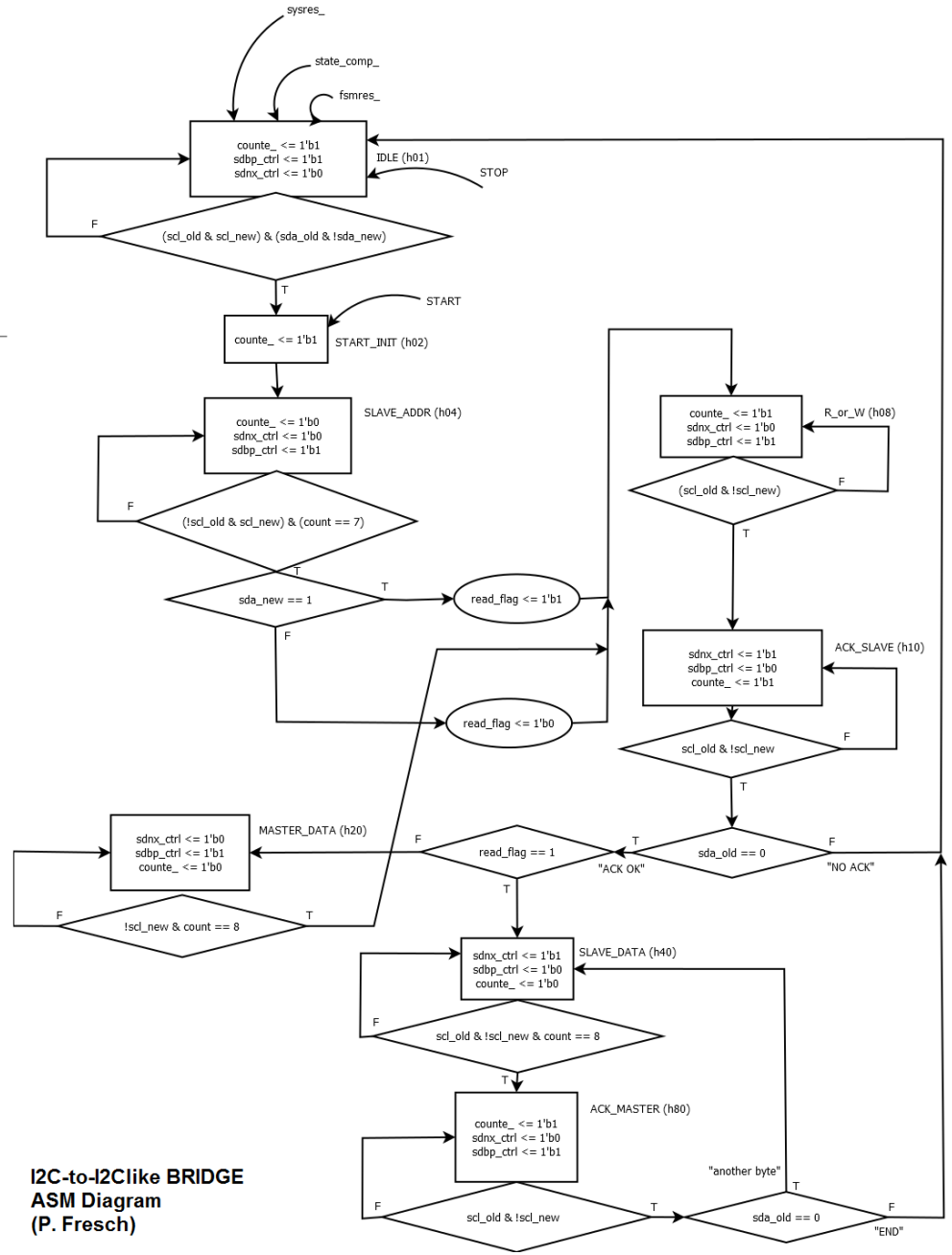
An I2C-to-I2CSB protocol converter is required

Protocol converter

Main features of the proposed protocol converter:

- Asynchronous start/stop detection
- On-the-fly action
- Completely transparent to the mastar and the slave
- Able to detect W ro R transaction
- Able to detect ACK or NACK

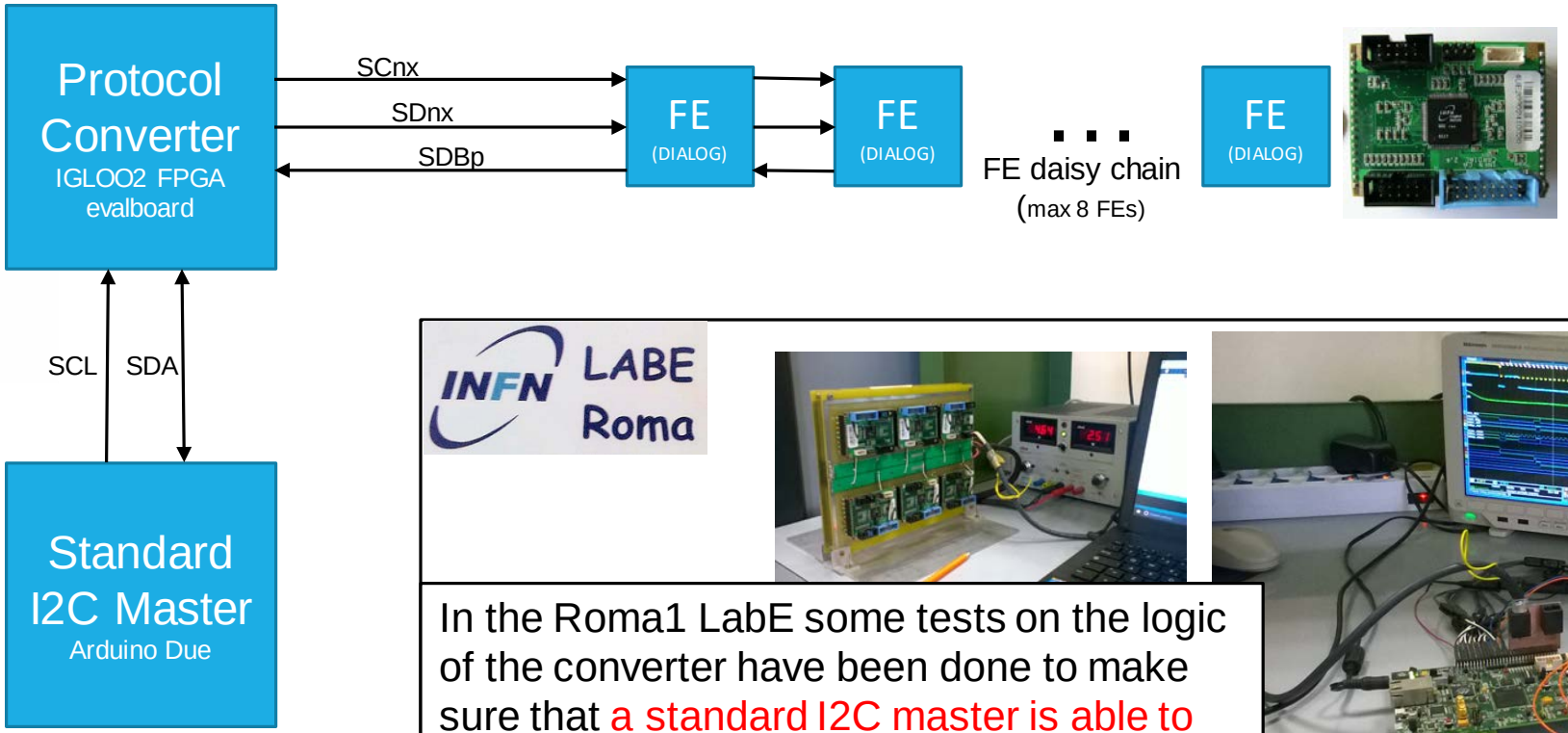




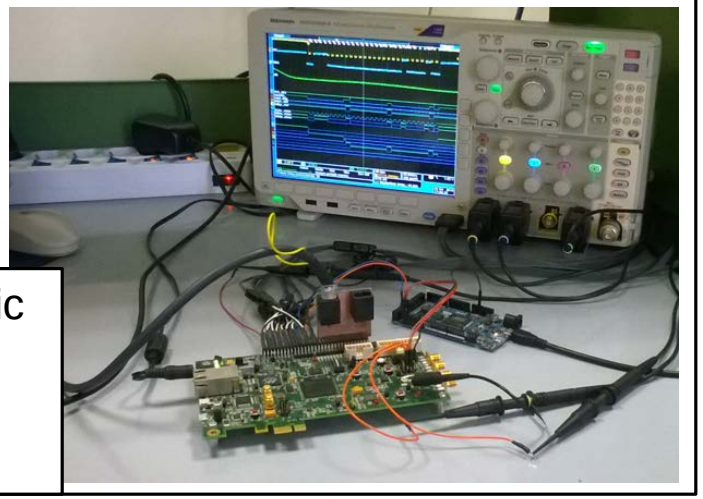
I2C-to-I2Clike BRIDGE ASM Diagram (P. Fresch)

Test summary

Test set-up:



INFN LABE Roma

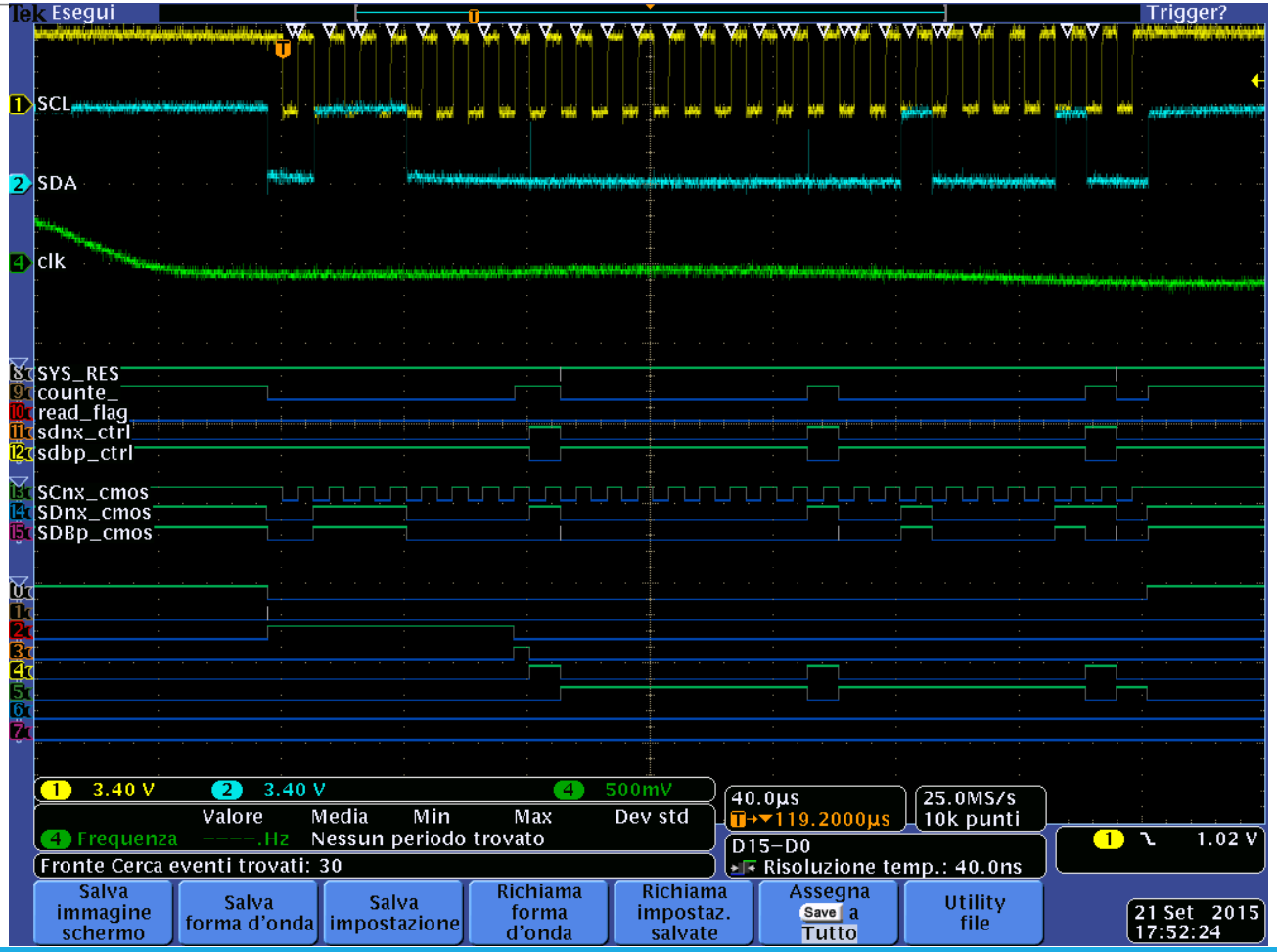


In the Roma1 LabE some tests on the logic of the converter have been done to make sure that a standard I2C master is able to write and read the DIALOG registers

Test summary

Write transaction:

- Slave address: 0x38
- Register address: 0x00 (PC0)
- Test data: 0x21 (ASCII «!»)

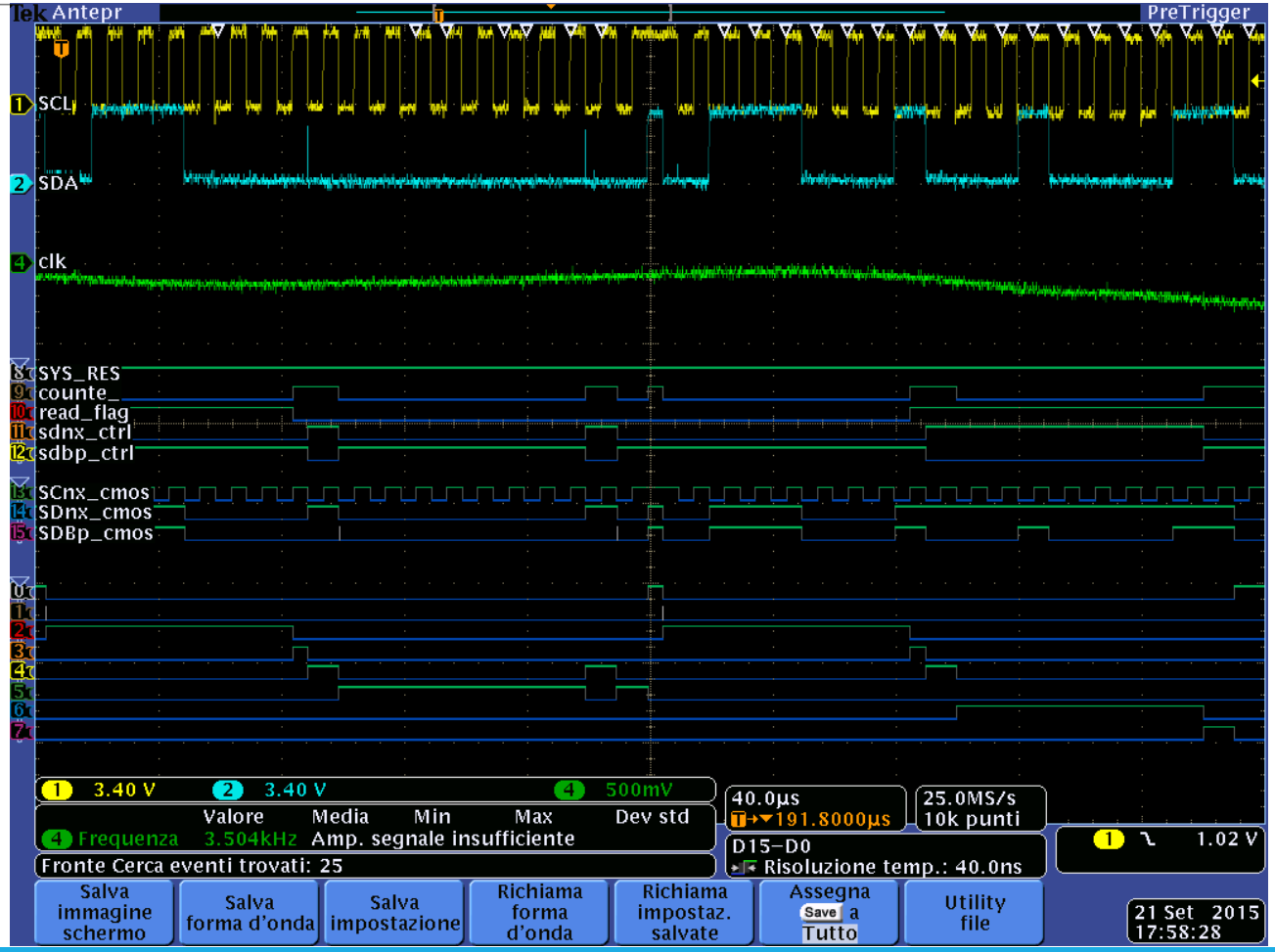


Test summary

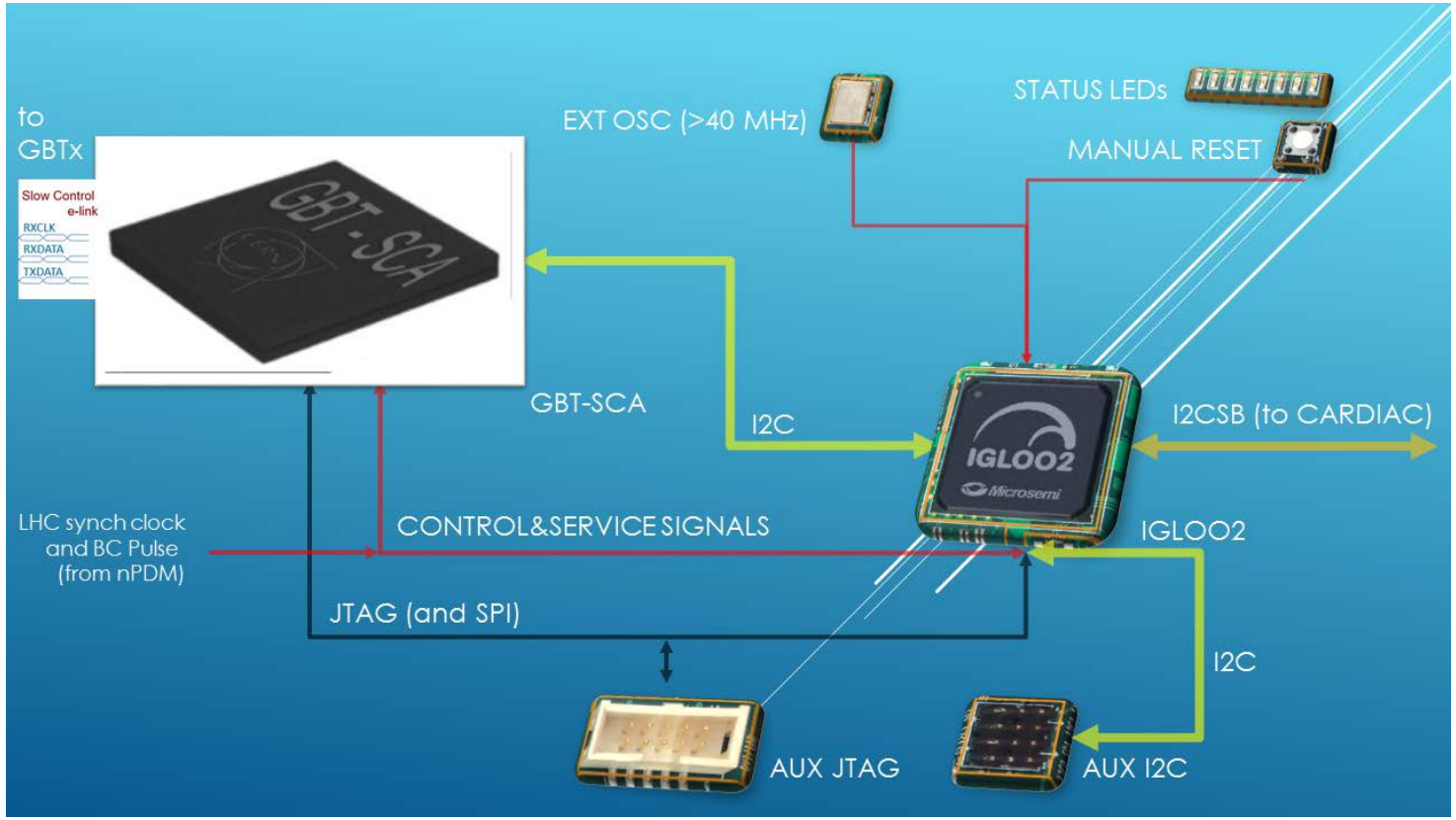
Read transaction:

- Slave address: 0x38
- Register address: 0x00 (PC0)

The tests ends with positive results ensuring that such solution is feasible



nSB: proposed architecture



- 16x I2C bus from SCA for communication and FPGA control
- Direct access to FPGA with specific purpose lines
- JTAG (and SPI if required) bus for microprogramming via GBT system
- Auxiliary I2C bus with full access to IGLOO2 for external devices
- Auxiliary JTAG

nSB: proposed features

- Complete and direct accesso to FE via GBT system
- Auxiliary external full access to FE
- Remote and local FPGA microprogramming on-board
- FPGA internal FF(s) protected by TMR redundancy (SEU tolerant)
- Possibility (if required) to activate built-in EDAC system (Microsemi® CoreEDAC)
- FE test_pulse generation configurable via I2C
- Possibility to add other features on the current fabric without replacing the component

What's next?

- Implement the proposed architecture in the FPGA and start complete tests
- Drawing the schematic for nSB prototyping (ongoing)
- Test the converter with the GBT module
- Post-P&R analysis and optimization (FPGA internal architecture)
- Implement the TMR on existing registers (FPGA internal architecture)

Thank you

FOR YOUR ATTENTION!