HVR_CCPD and CHIPIX65 chip design – Milano

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Outline

People and Expertise

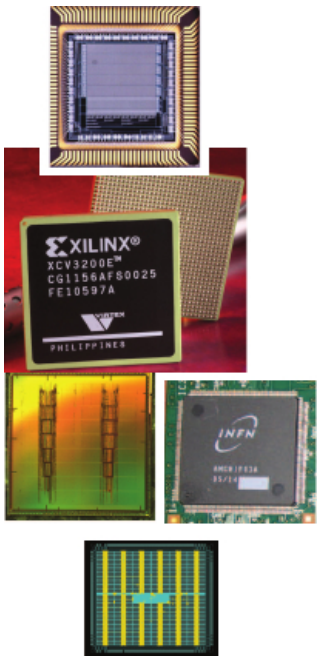
INFN-Milano design team:
Valentino Liberali, Alberto Stabile, Seyedruhollah Shojaii (chip design);
Mauro Citterio, Alessandro Andreani, Fabio Manca (PCB and chip assembling);
Alessandra Camplani (FPGA firmware and radiation tests);
Attilio Andreazza, Chiara Meroni, Francesco Ragusa (pixels)

Collaboration with Hitesh Shrimali, Indian institute of Technology, Mandi, India.

The Associative Memory chip (AMchip) for FTK

Since 2010, INFN-Milano in involved in the design of the **Associative Memory chip for the Fast TracKer (FTK) project in ATLAS, using TSMC 65 nm CMOS technology**

Several versions of the AMchip:

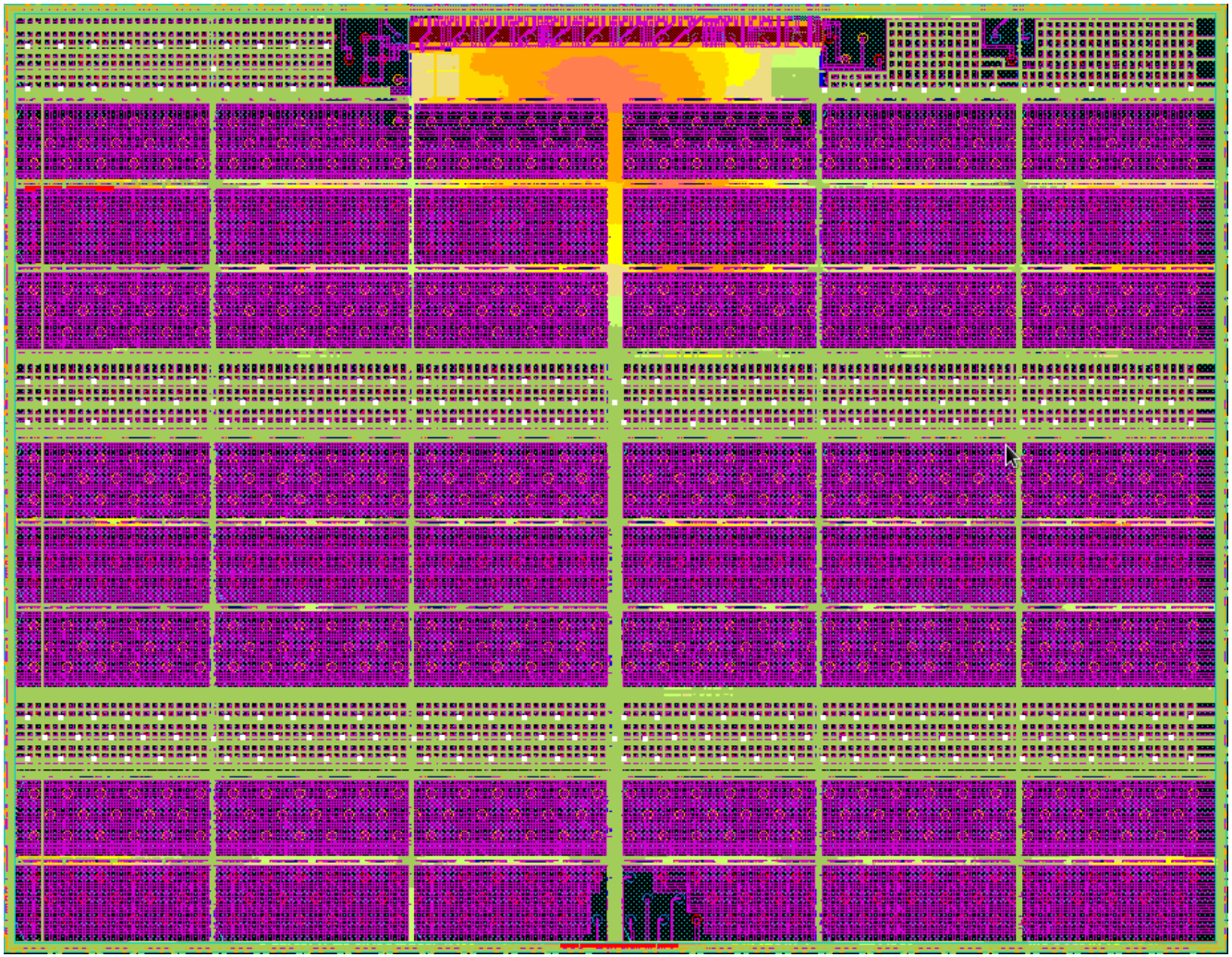


Vers.	*Design*	*Tech.*	*Area*	*Patterns*	*Package*
4	Std cells + Full custom	65 nm	14 mm^2	8 k	QFP
mini-5	**Std cells + Full custom + SERDES IP blocks**	**65 nm**	**4 mm^2**	**0,5 k**	**QFP**
5			**12 mm^2**	**3 k**	**BGA**
6	**Std cells + Full custom + SERDES IP blocks**	**65 nm**	**160 mm^2**	**128 k**	**BGA**

blue = under design

AMchip06

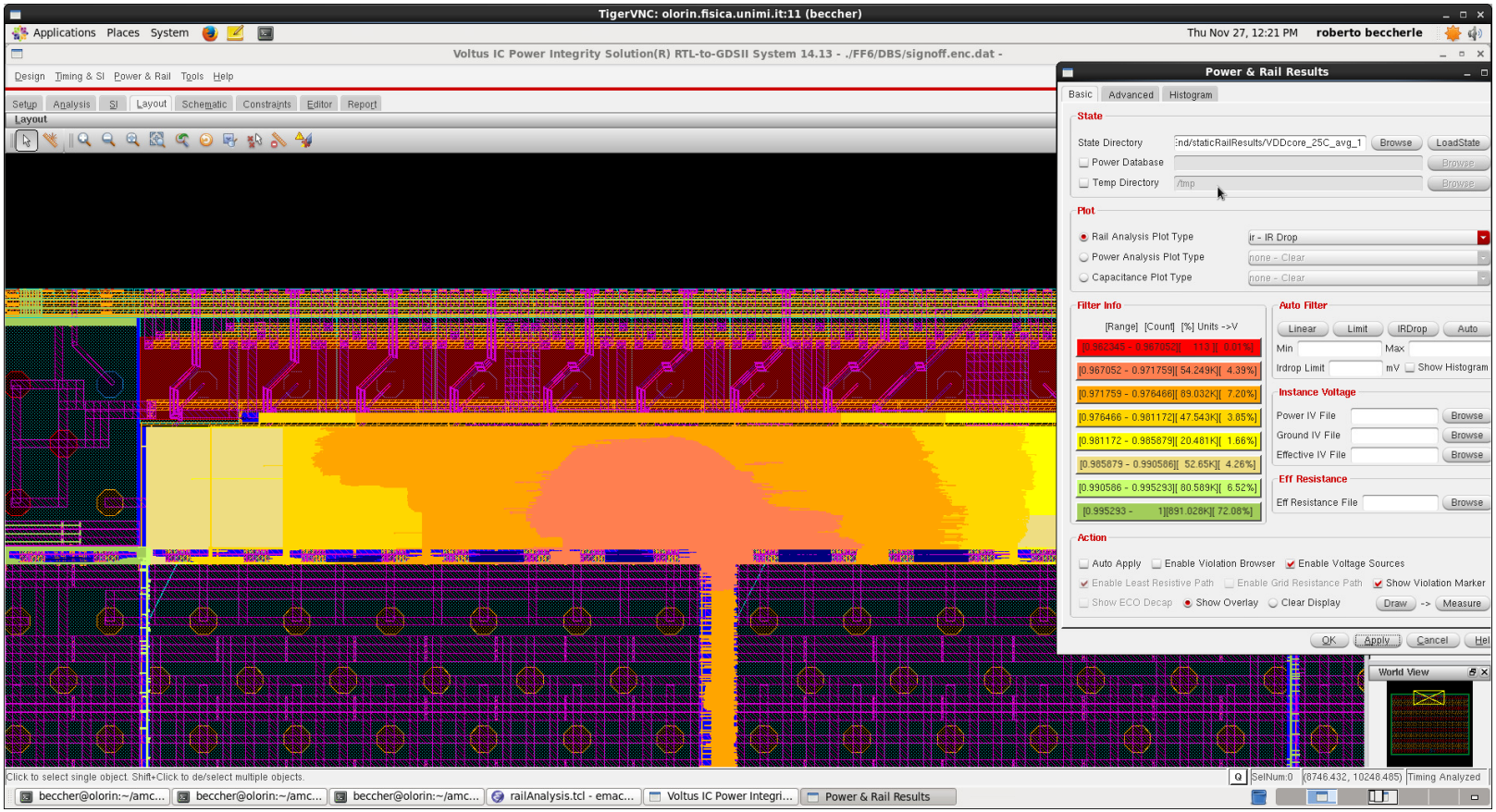
Last version: **AMchip06**
168 mm^2, 421 M transistors
Floorplan:



Expertise on Digital Design

Design of large IC's with Cadence Encounter
Mixed approach (full-custom, standard cells, IP blocks)
Use of timing analysis tools (Tempus) and *IR* drop analysis tools (Voltus)

Example: static *IR* drop for AMchip06 obtained from Voltus



Radiation Hardening Approach

Within RD53/CHIPIX65:

Digital IP blocks designed in 65 nm CMOS technology (TSMC) using RHBD (Radiation Hardening By Design) techniques.

REDUNDANCY technique has been used for:

- DICE SRAM
  - Array of 256 $\times$ 256 cells designed with three different layouts
  - Prototypes available
  - Test board designed
  - Test firmware under development
  - Radiation test planned in July
- D2RA logic
  - New logic family based on redundancy: each signal is propagated on two wires (bit and inverted bit)
  - Cells designed
  - Test chip under design; MPW submitted in May

Scopo e partecipanti

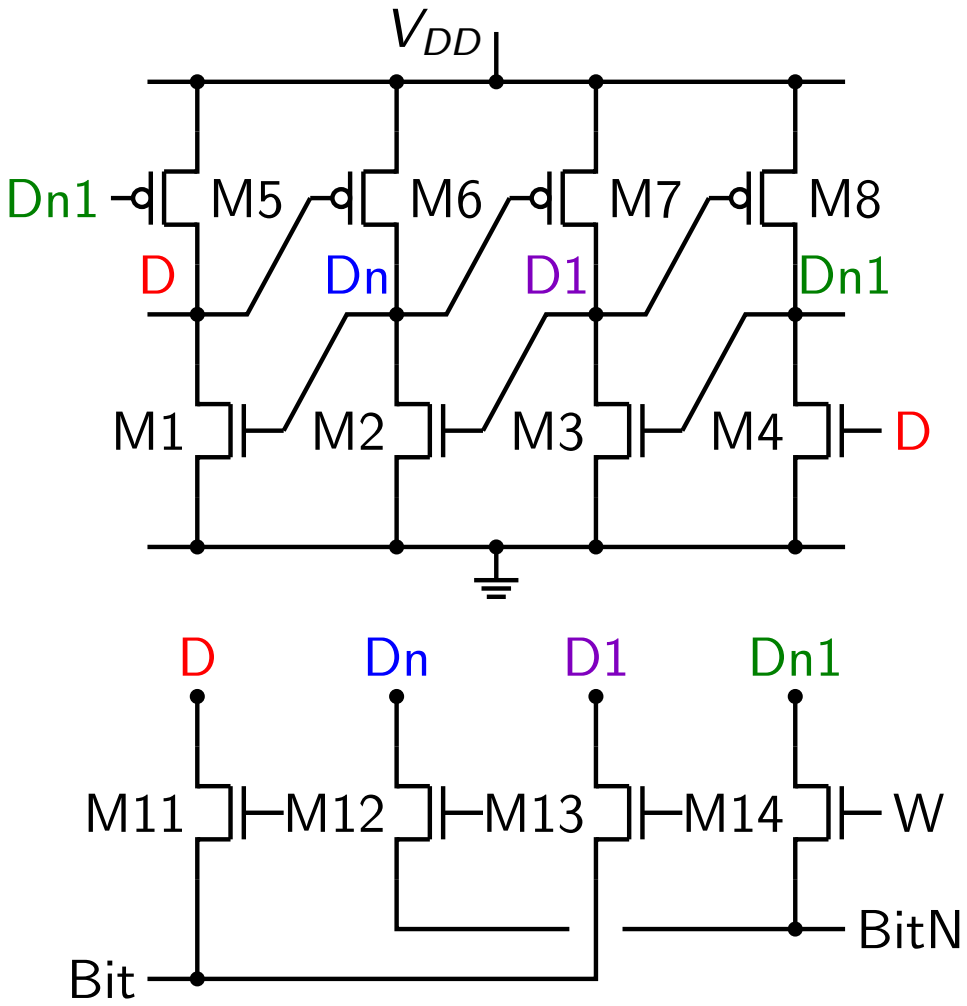
Scopo: Lo sviluppo di un pixel chip innovativo in tecnologia CMOS 65nm (TSMC) resistente a altissimi flussi di particelle e radiazione si inserisce nella partecipazione italiana al progetto CERN RD53, di cui CHIPIX65 è parte.

A RD53 (e a CHIPIX65) partecipano unità convolte nei progetti ATLAS e CMS. L'obiettivo finale è il progetto di un sensore a pixel, con relativa elettronica, adatto per la fase II di LHC.

Coordinatore: **N. Demaria (Torino)**
Unità partecipanti: **Bari** (CMS), **Bergamo + Pavia** (CMS), **Milano** (ATLAS), **Padova** (CMS), **Perugia** (CMS), **Pisa** (CMS + ATLAS), **Torino** (CMS)

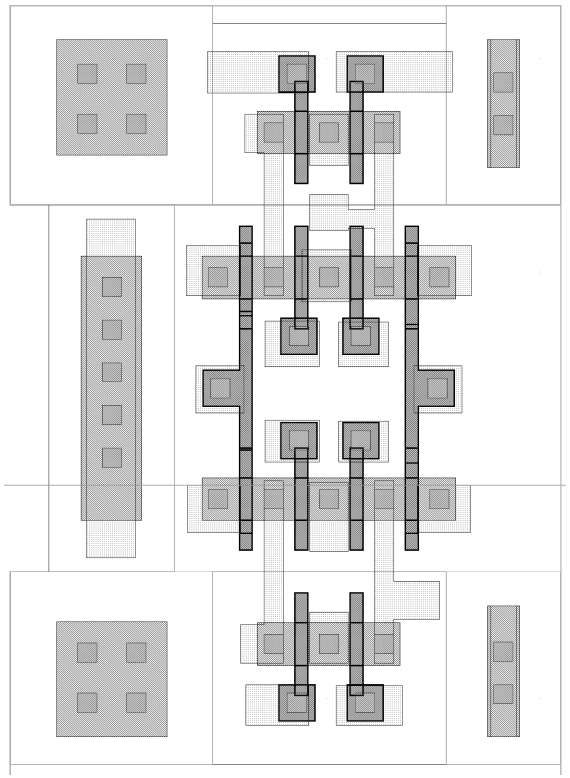
Partecipazione di Milano: **1 FTE**
Valentino Liberali, Seyeduhollah Shojaii, Alberto Stabile

DICE (Dual Interlocked CEll) SRAM: schematic



T. Calin, M. Nicolaidis, and R. Velazco, "Upset hardened memory design for submicron CMOS technology,", *IEEE Trans. Nucl. Sci.*, vol. 43, pp. 2874-2878, Dec. 1996.

DICE (Dual Interlocked CEll) SRAM: layout

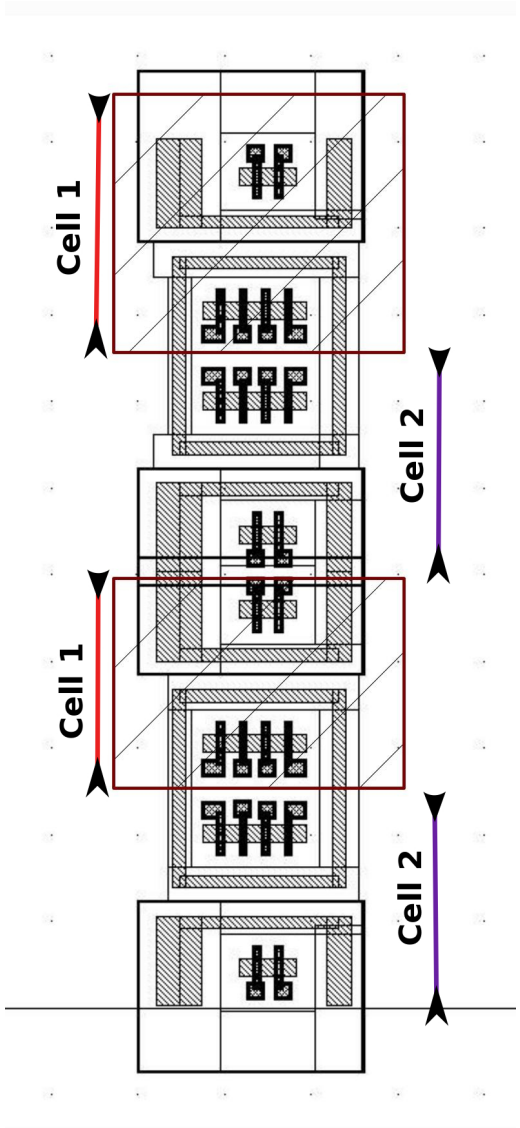


Simple layout

Minimum transistor size:
$W = 200$ nm, $L = 60$ nm

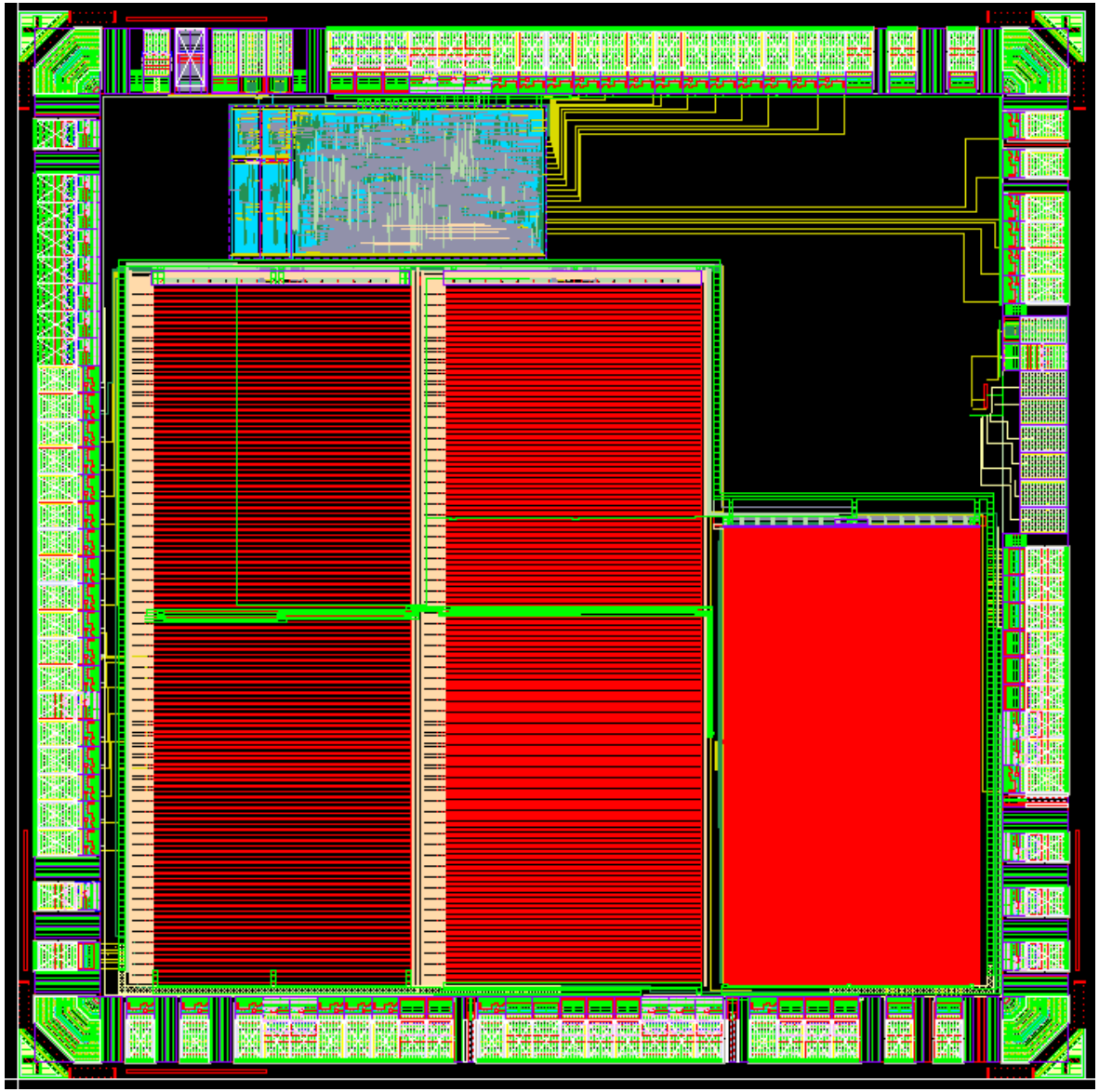
The cell has been designed in three different versions:

- "simple" layout
- with guard rings around transistors
- with both guard rings and interleaving



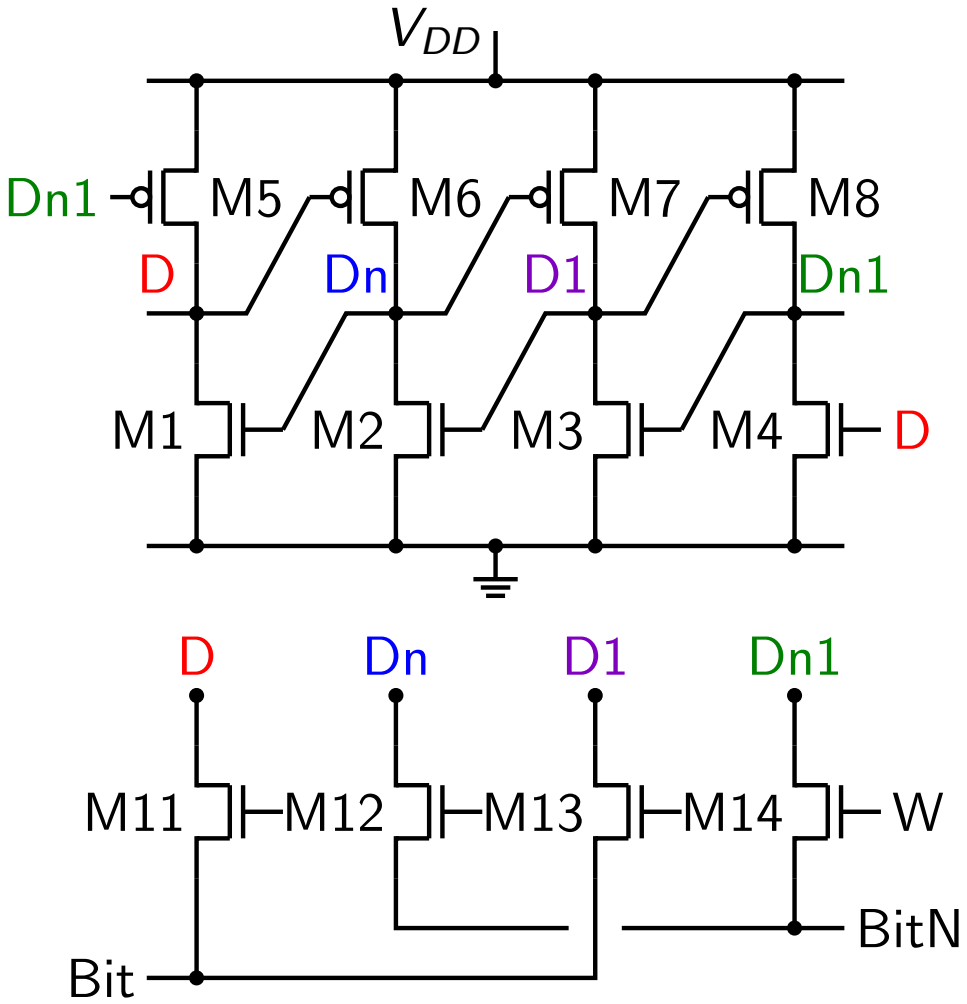
Interleaved layout

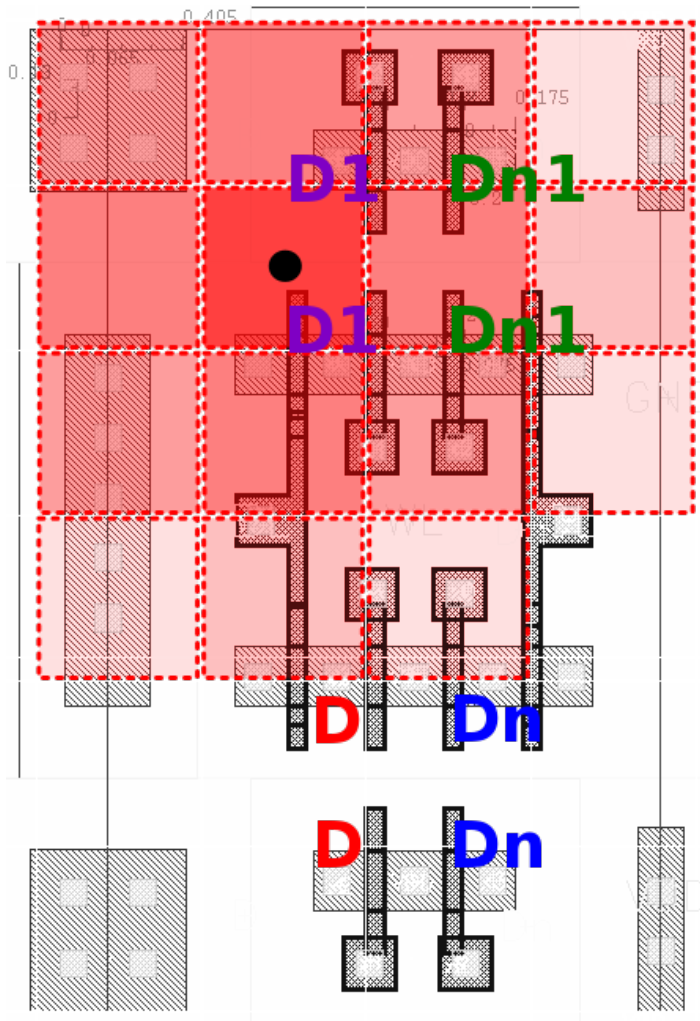
1st test chip: CHIPIX-SRAM-1



Layout:
3 256 $\times$ 256 SRAM arrays; SERDES; MOS transistors

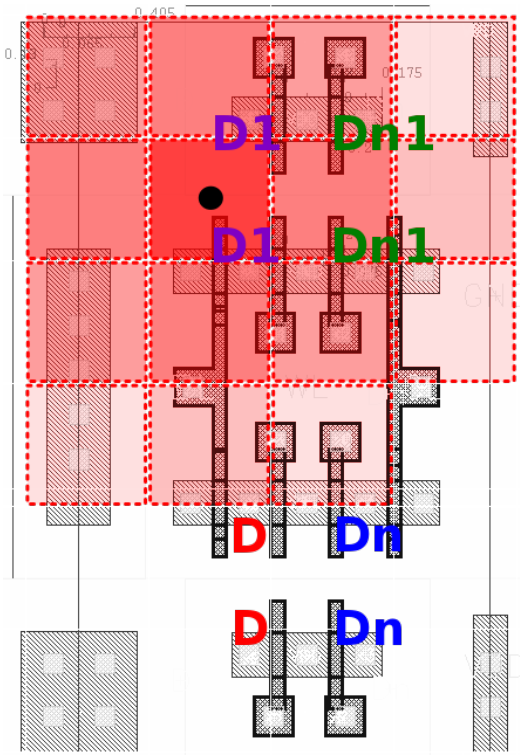
DICE Single Event Effect simulation

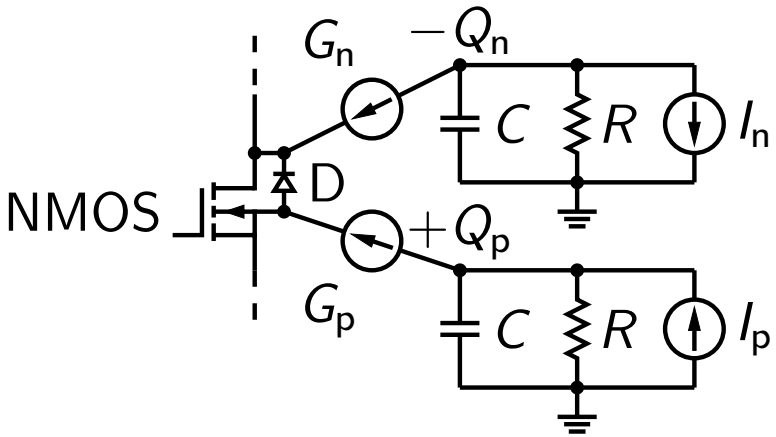




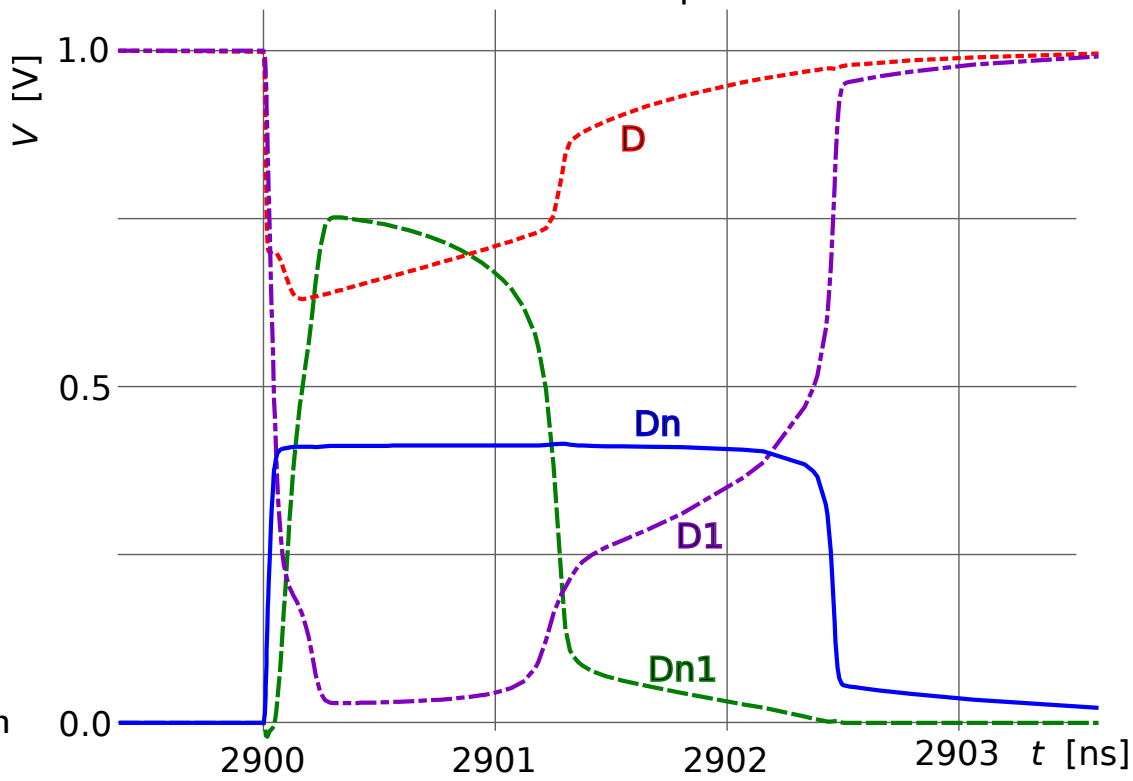
The area affected by a single particle is much larger than a single node!

DICE SEE simulation results





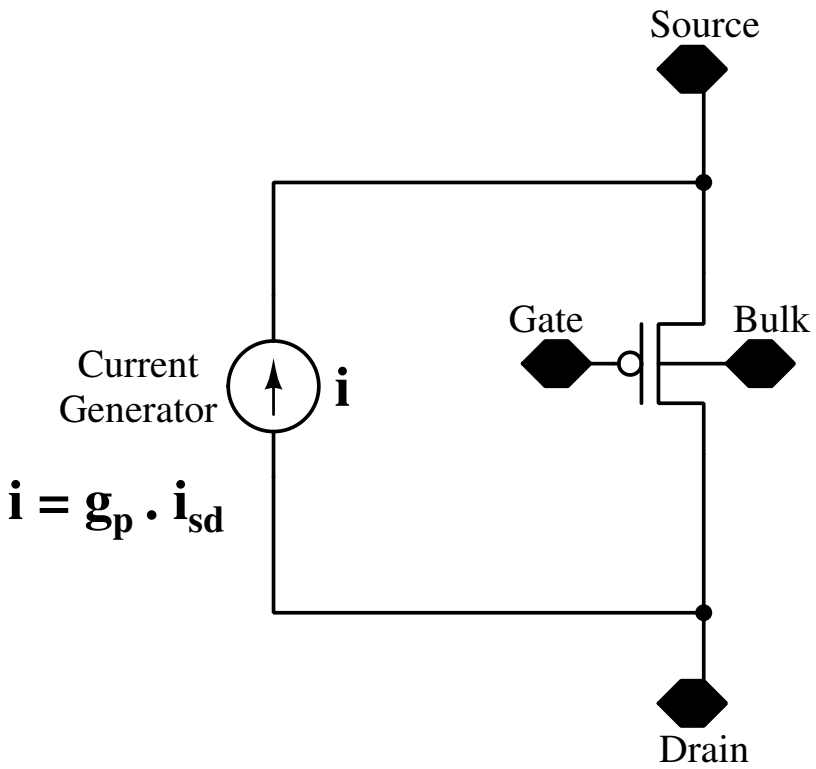
Total injected charge: $Q_p = Q_n = 1$ pC



After a 2.5 ns transient, the DICE memory reverts back to the correct value

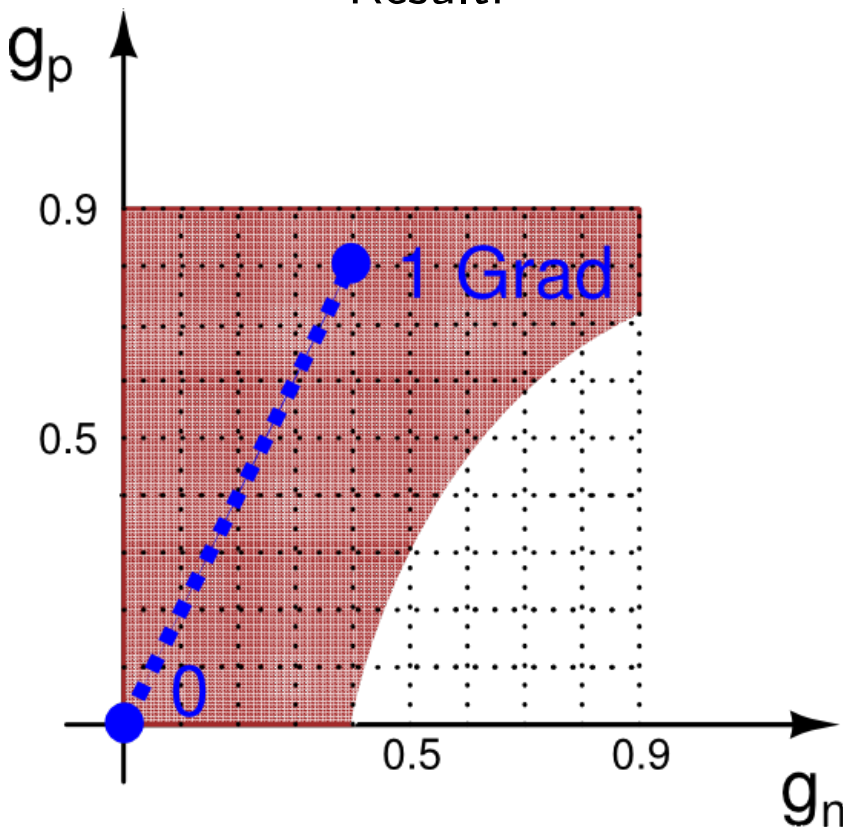
Total Dose simulation

Model:



The parameter g_p (g_n) accounts for the degradation of the PMOS (NMOS) transistor

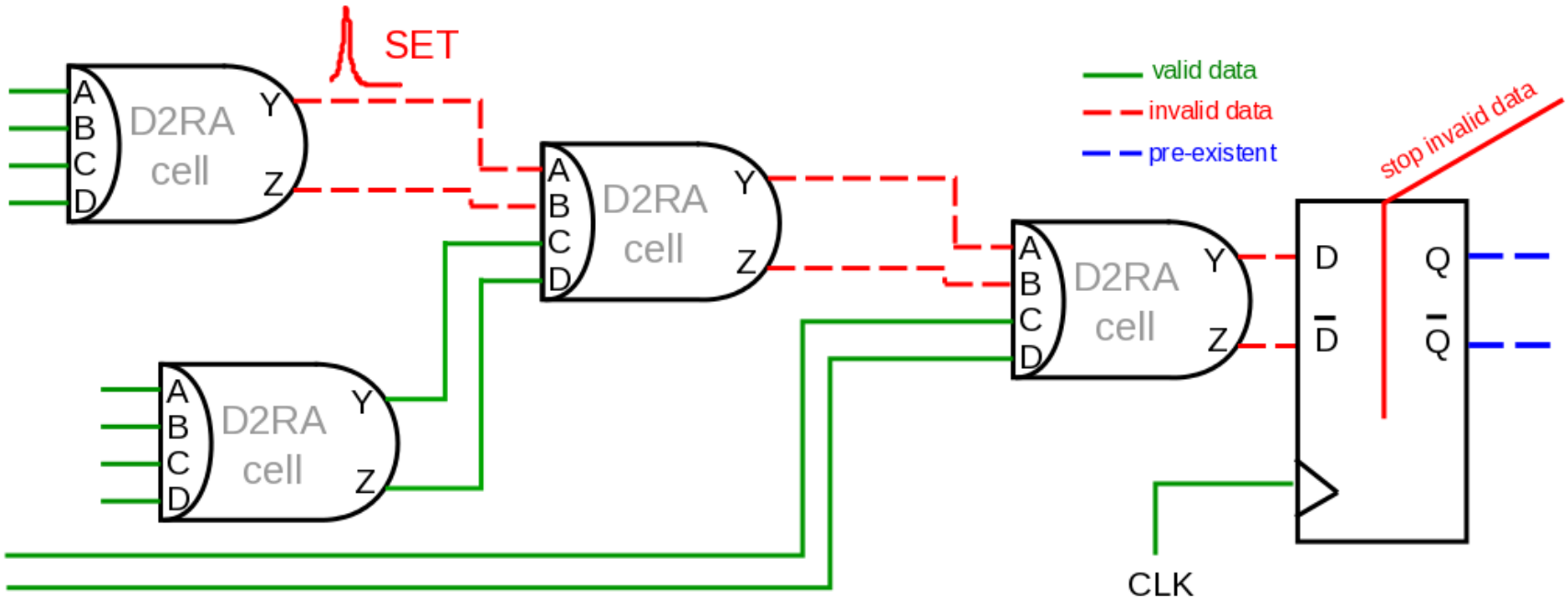
Result:



The DICE SRAM is less sensistive to PMOS conductance degradation

D2RA: Double-Rail Redundant Approach

Redundant logic which processes both the bit and the inverted bit
(01) and (10): valid data
(00) and (11): invalid data (Single Event Transient)



V. Ciriani, L. Frontini, V. Liberali, S. Shojaii, A. Stabile, and G. Trucco, "Radiation-tolerant standard cell synthesis using double-rail redundant approach," in *Proc. of Int. Conf. on Electronics, Circuits and Systems (ICECS)*, Sept. 2014, http://dx.doi.org/10.1109/ICECS.2014.7050063

D2RA Logic Gates

Combinational logic gates:

- AND / NAND
- OR / NOR (identical to AND / NAND with swapped inputs)
- XOR / XNOR (two identical "half-cells")
- MUX
- NOT (redundant inverter for single-ended signals)

Sequential logic gates:

- Edge-triggered delay flip-flop (D-FF)
- Clock edge detector

D2RA: Logic Constraints

Fully CMOS logic $\longrightarrow$ inverting logic gates

Correct points:
input valid data must give (**1**, **0**) or (**0**, **1**) at the outputs

Faulty points: **Invalid data** are represented by don't cares (-), which can be either (0, 0) or (1, 1)
Gravity points: 0000 and 1111 at the inputs must give (**1**, **1**) and (**0**, **0**) at the outputs, respectively

CD \ AB	00	01	11	10
00	**1**	-	-	-
01	-	**0**	-	**0**
11	-	-	**0**	-
10	-	**0**	-	**1**

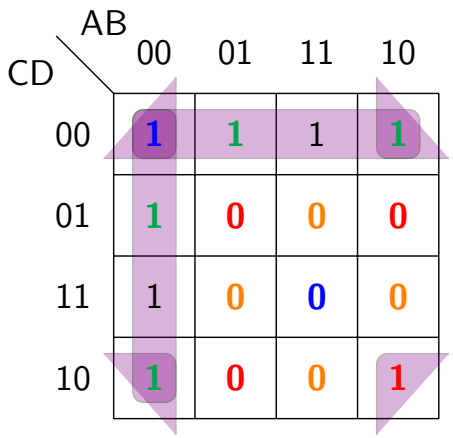
AND

CD \ AB	00	01	11	10
00	**1**	-	-	-
01	-	**1**	-	**1**
11	-	-	**0**	-
10	-	**1**	-	**0**

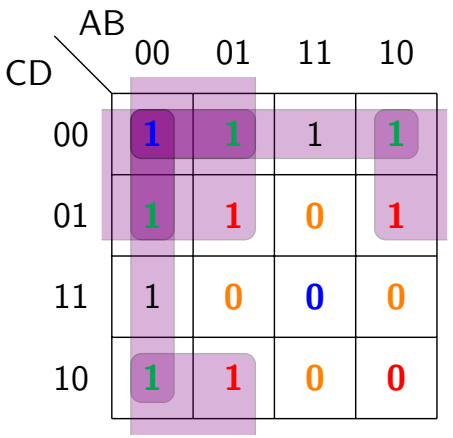
NAND

Synthesis of a 2-input D2RA AND-NAND

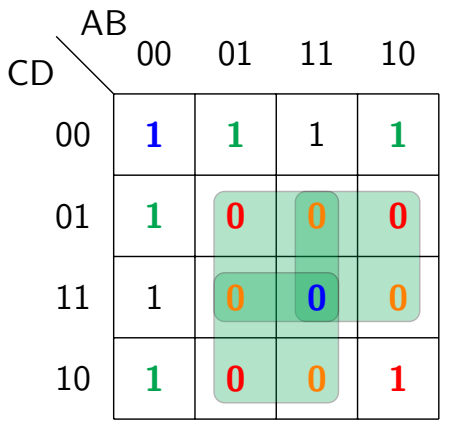
- For both gravity points find the square covers that include neighborhood
- Remaining don't care are filled with ones
- Find minimum covers



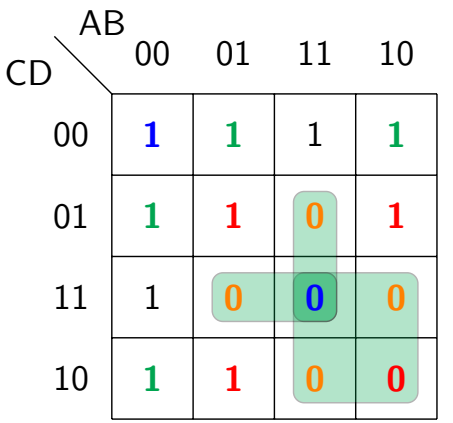
AND - Z output



NAND - Y output

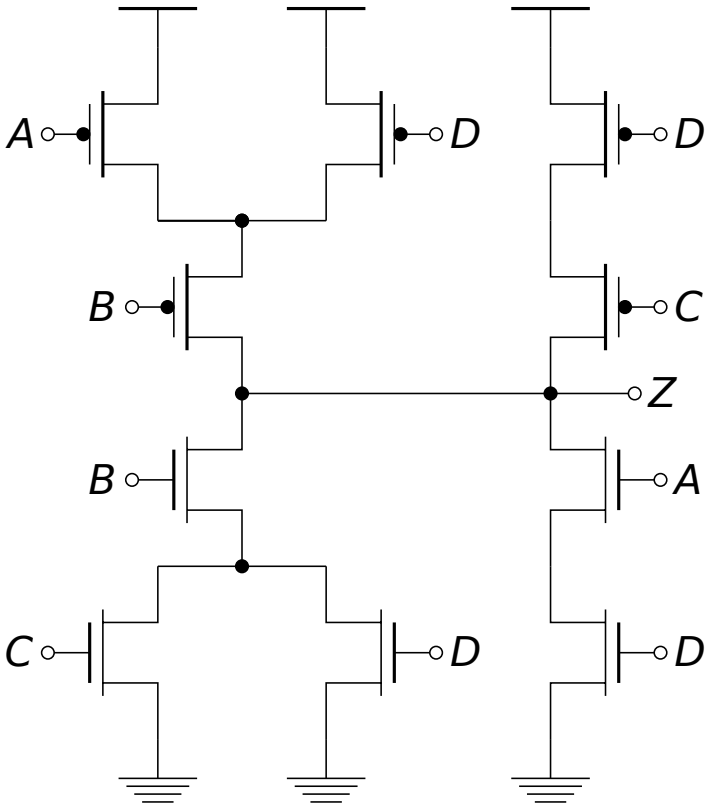


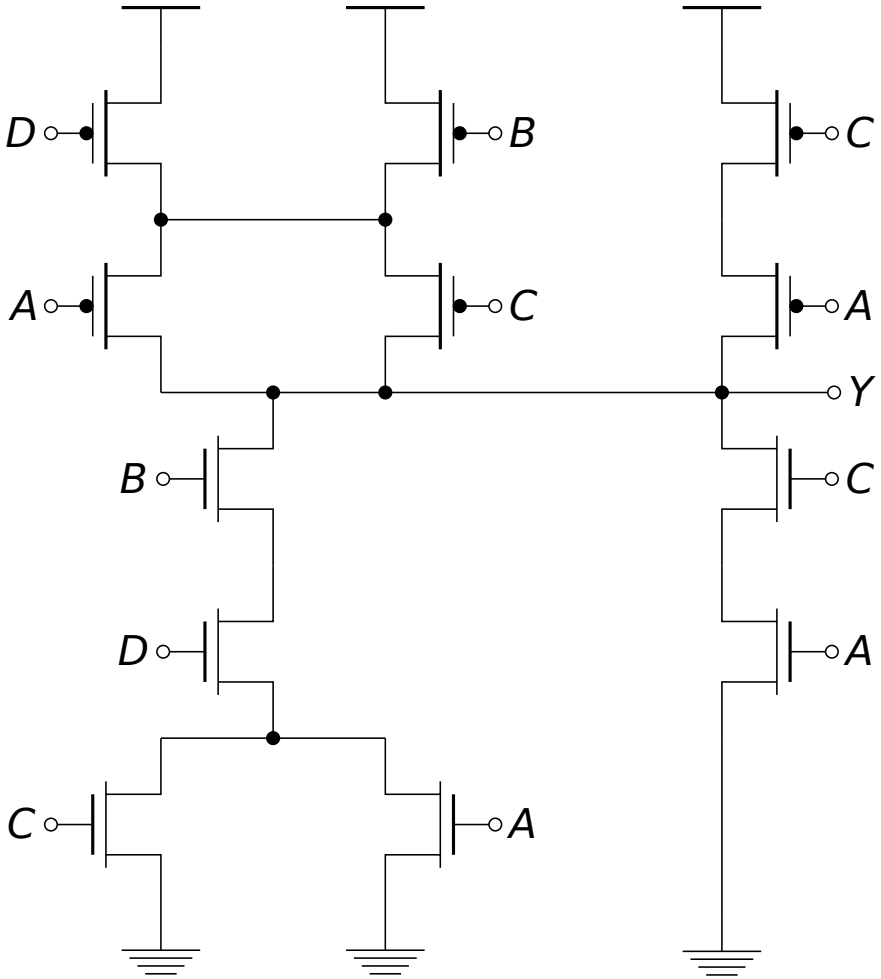
NAND - Z output



AND - Y output

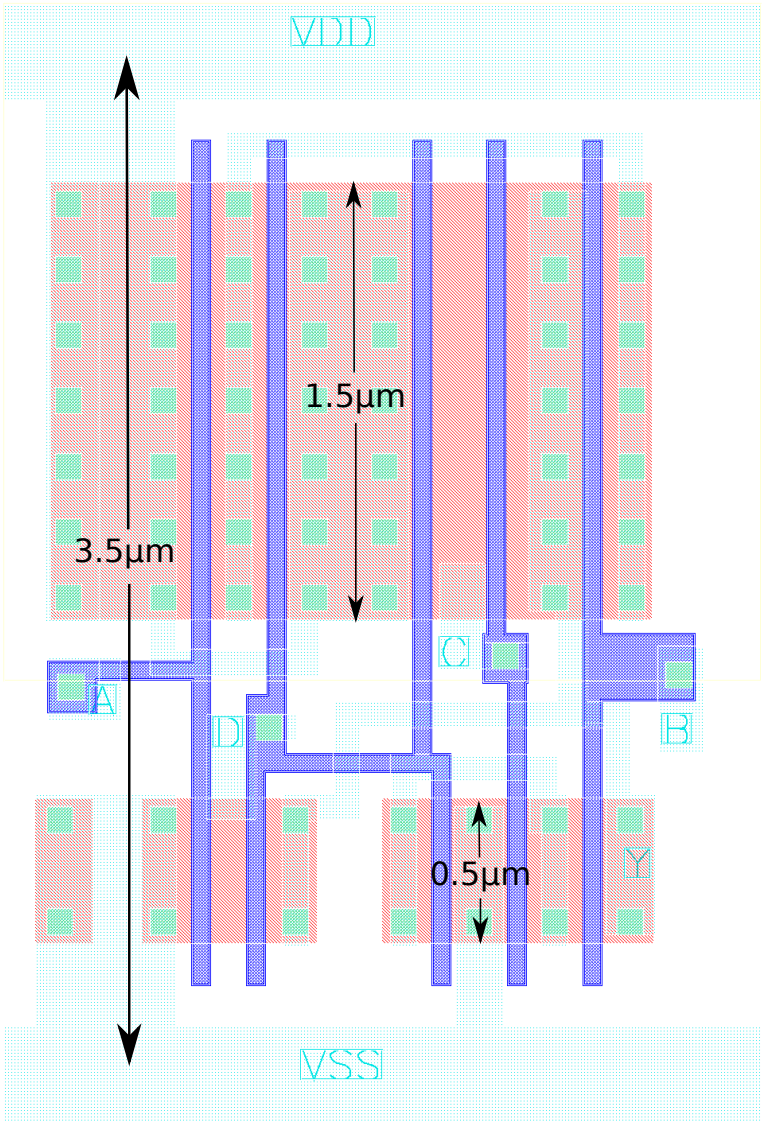
Schematic of a 2-input D2RA AND-NAND



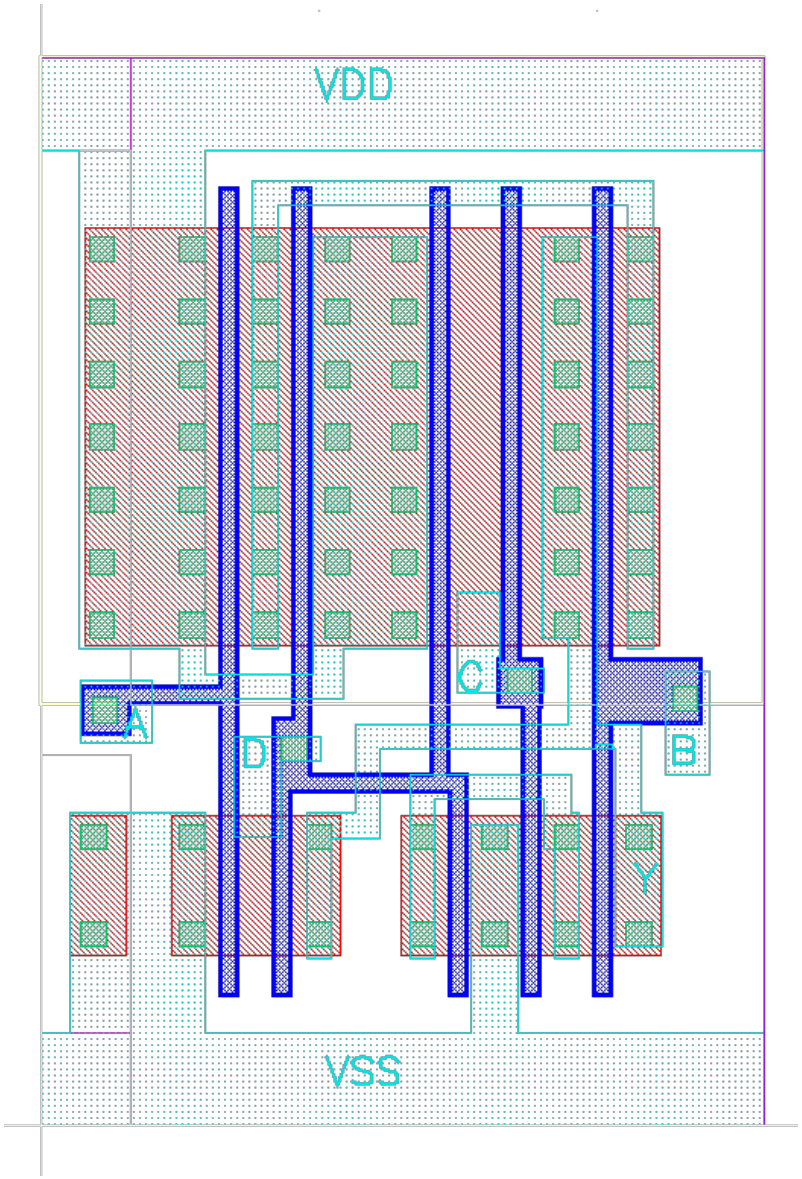


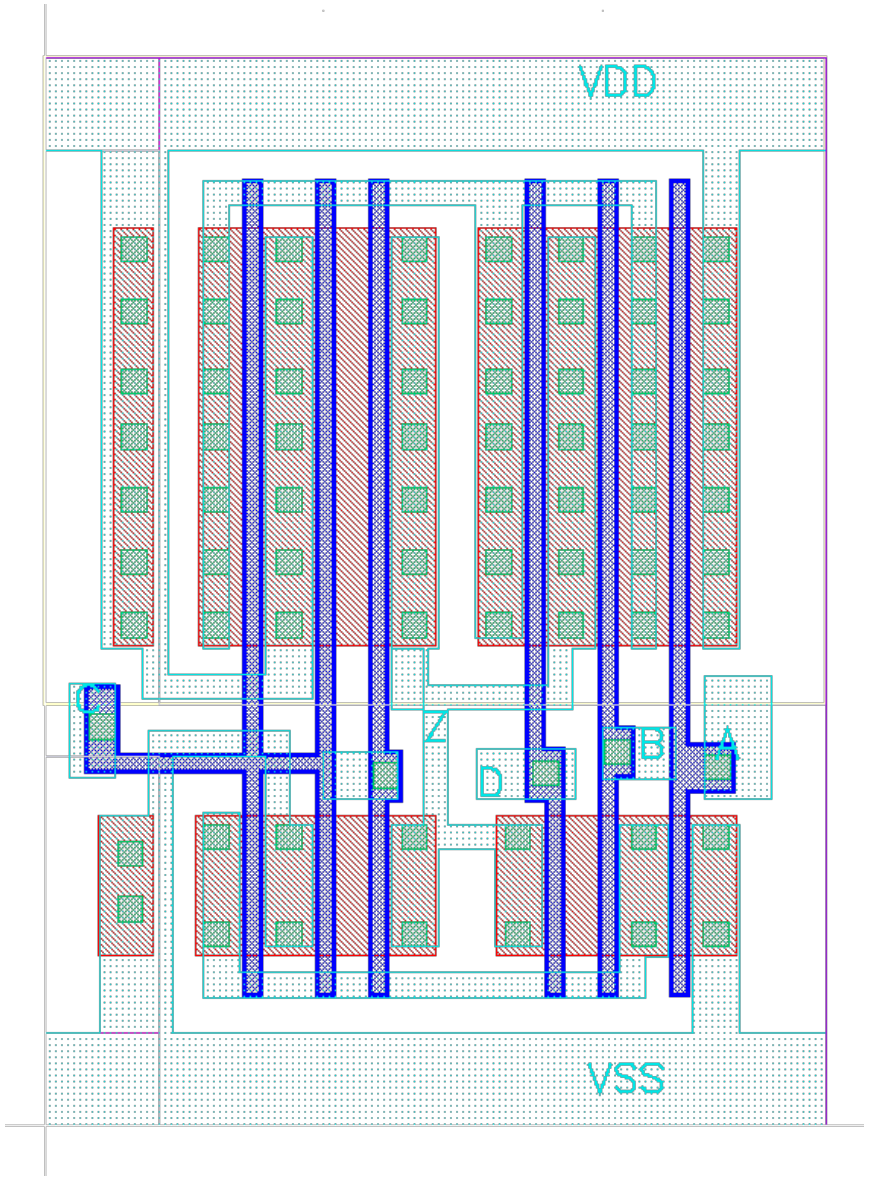
Layout approach for Standard Cells

- To reduce loss of transconductance at 10 MGy, transistors width is not minimum:
  $W_{\text{pmos}} = 1.5\,\mu\text{m}$
  $W_{\text{nmos}} = 0.5\,\mu\text{m}$
- Fixed cell height
- Power supply and ground nets at top and bottom of cells



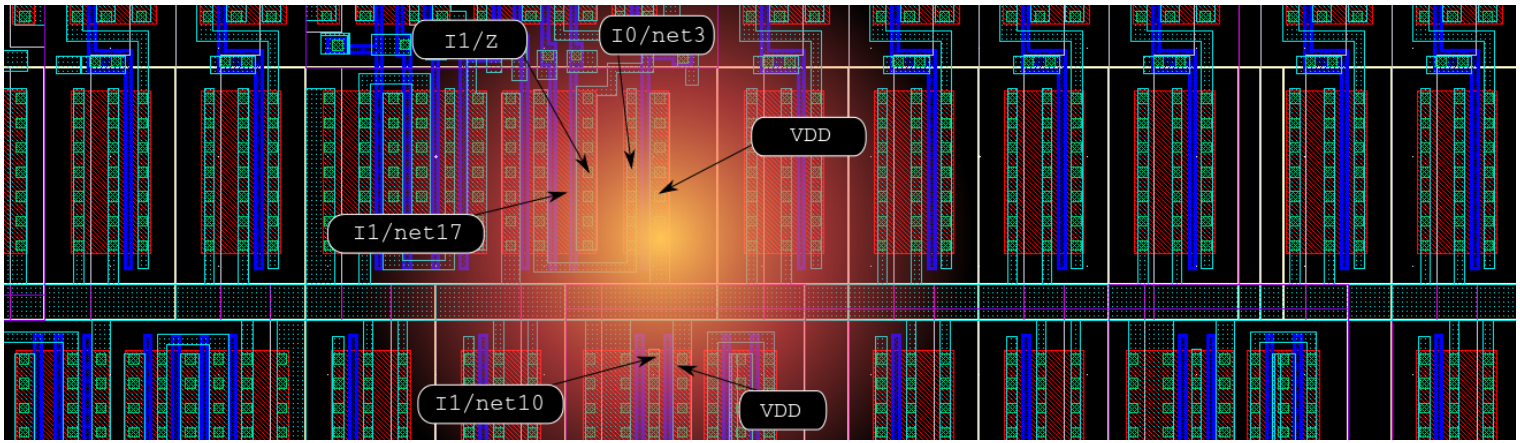
D2RA AND / NAND layout



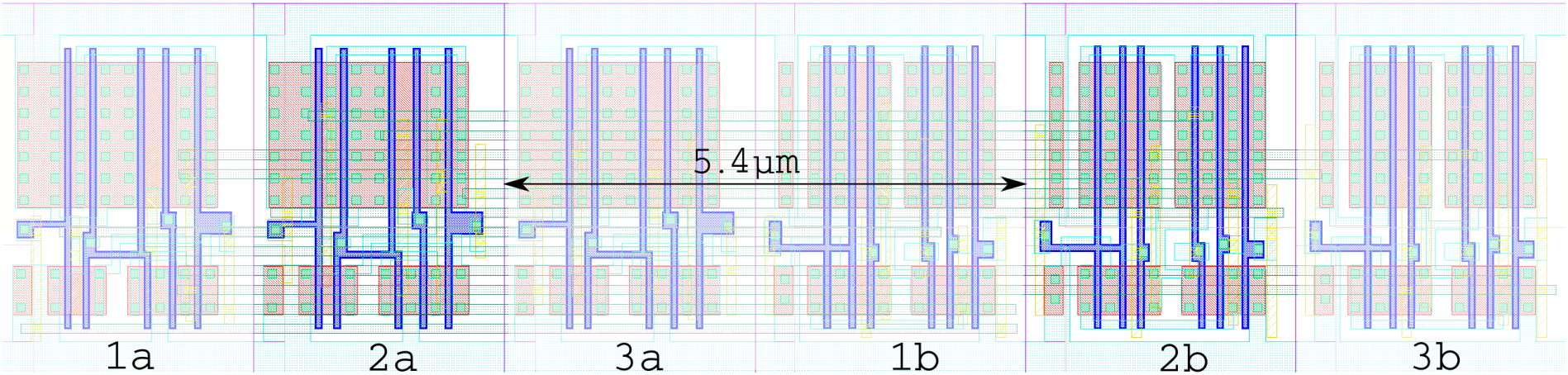


SET effect mitigation

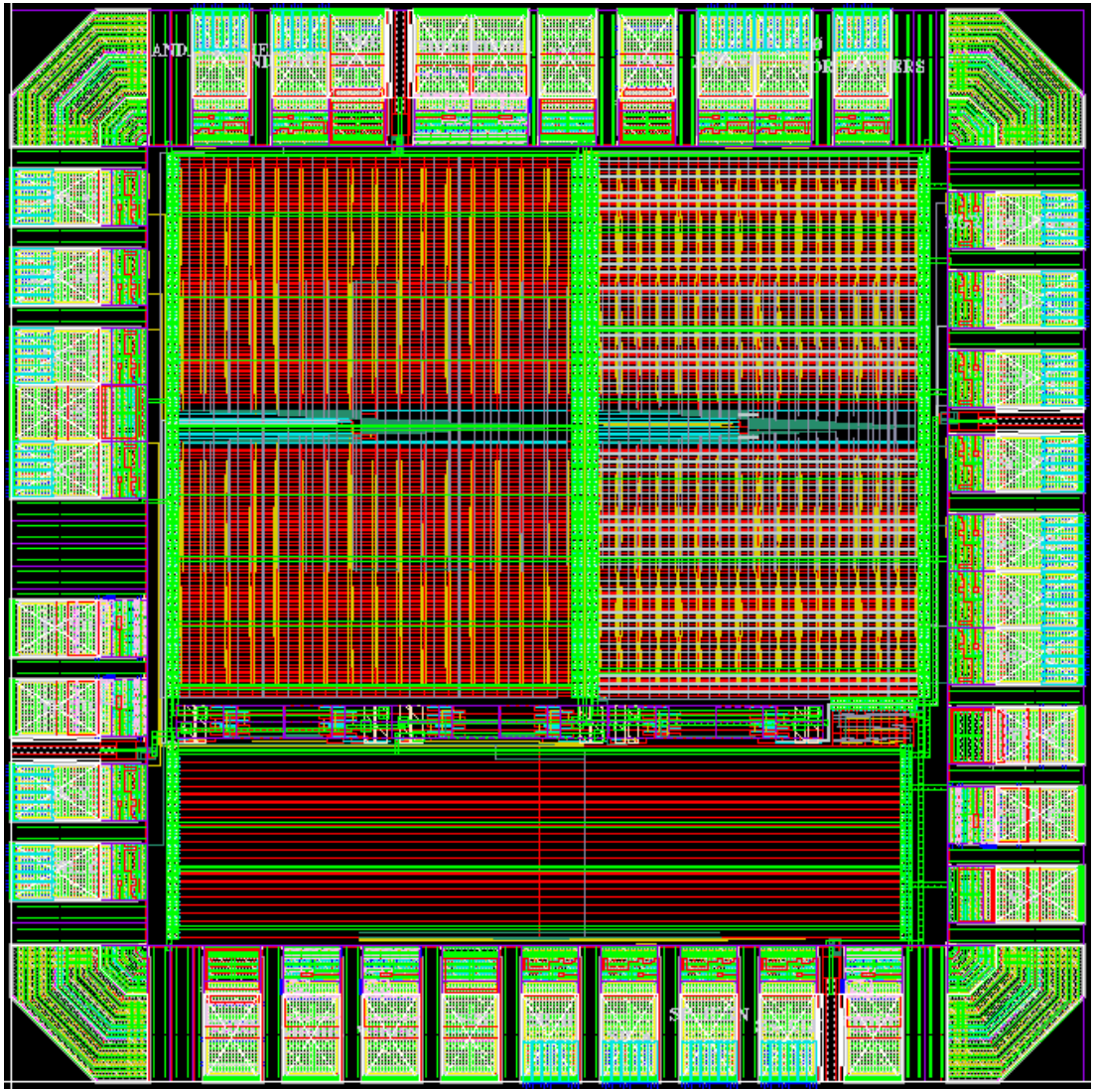
When radiation hits a circuit, the generated charge can affect several nodes causing SETs.



The two parts of a D2RA cell must be placed at a minimum distance of 5 µm:



2nd test chip: CHIPIX-D2RA-2



Layout:
AND/NAND and XOR/XNOR trees; shift register; ring oscillator
all designed with D2RA cells

HVR_CCPD summary

Purpose:
The **HVR_CCPD** project aims at prototyping an active **CCPD (Capacitively Coupled Pixel Detector)** by developing, testing and characterizing an **HV/HR (High-Voltage/High-Resistivity) CMOS** design and its integration with a pixel detector chip for readout.
Initially the readout chip will be the ATLAS FE-I4 and will be then moved to the RD53 design, when this will become available.

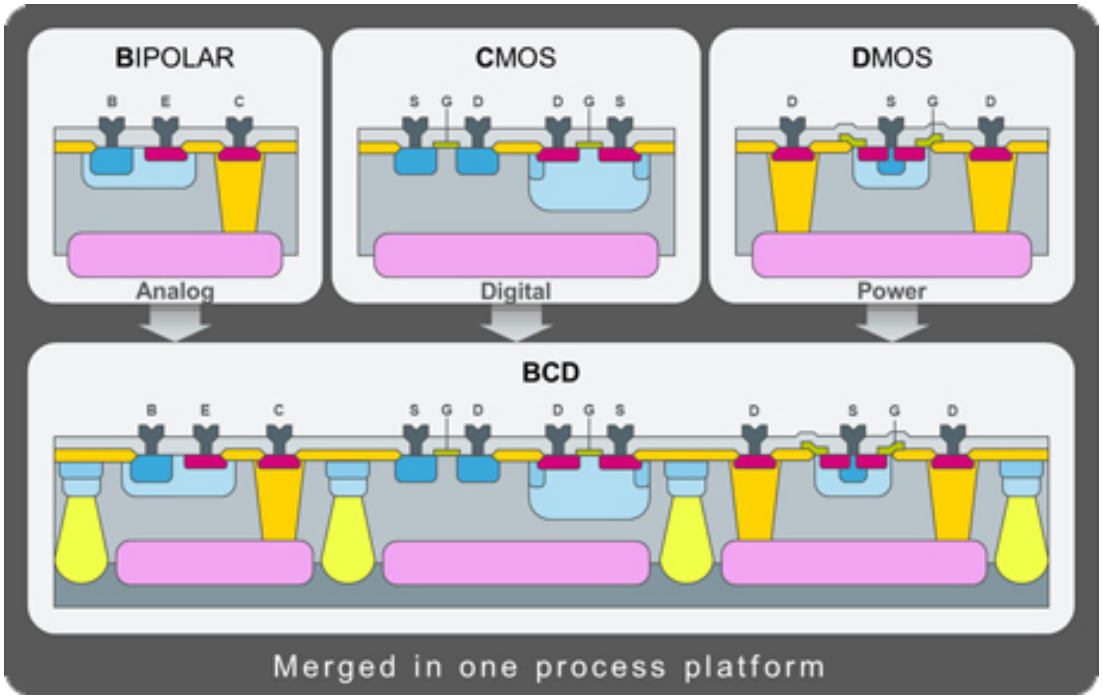
Units: INFN sections of Milano, Genova, Bologna.

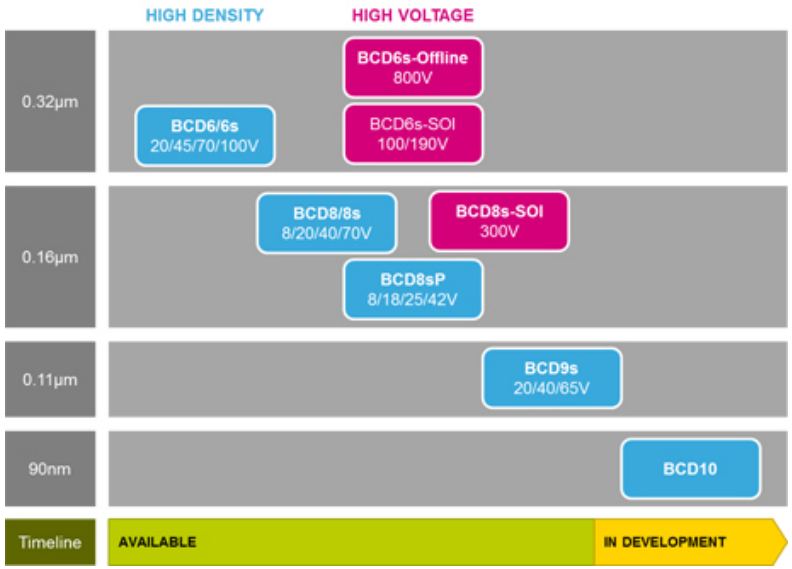
Project coordinator: Attilio Andreazza (Milano).

The Project involves electronic designers of three INFN Sections, with expertise in design of rad-hard electronics, and in manufacturing and operating silicon detectors.

BCD8 Technology (STMicroelectronics)

BCD = Bipolar + CMOS + DMOS





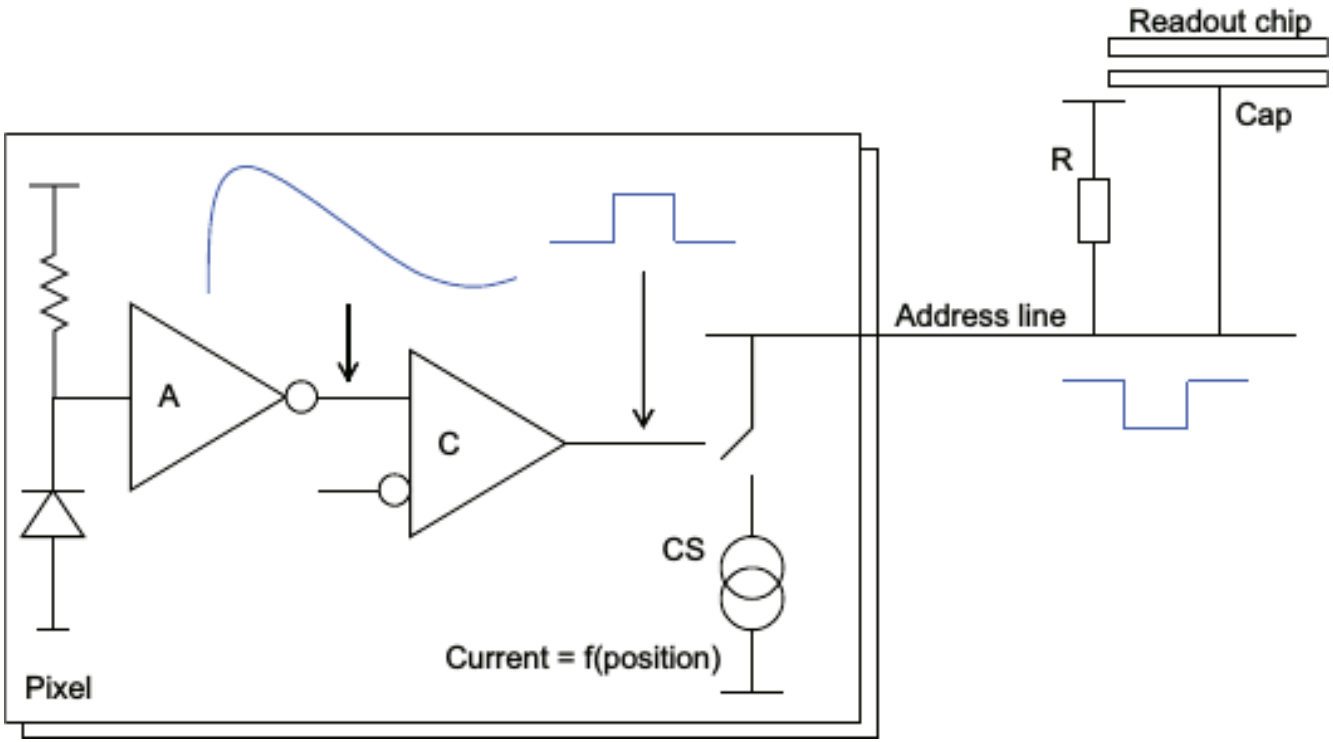
http://www.st.com/web/en/about_st/bcd.html

D. Riccardi, A. Causio, I. Filippi, A. Paleari, L. Vecchi, A. Pregnolato, P. Galbiati, C. Contiero, **BCD8 from 7V to 70V: a new 0.18 μm technology platform to address the evolution of applications towards smart power ICs with high logic contents**, in *Proc. 19th Int. Symp. Power Semiconductor Devices & ICs*, 2007. http://dx.doi.org/10.1109/ISPSD.2007.4294935

R. Roggero, G. Croce, P. Gattari, E. Castellana, A. Molfese, G. Marchesi, L. Atzeni, C. Buran, A. Paleari, G. Ballarin, S. Manzini, F. Alagi, G. Pizzo, **BCD8sP: An advanced 0.16 μm technology platform with state of the art power devices**, in *Proc. 25th Int. Symp. Power Semiconductor Devices & ICs*, 2013. http://dx.doi.org/10.1109/ISPSD.2013.6694422

Chip Design in BCD8

Front-end circuit based on the solution proposed by Ivan Perić et al.:



I. Perić, et al., **High-voltage pixel sensors for ATLAS upgrade**, *Nuclear Instruments and Methods in Physics Research* **A** (2014), in press. http://dx.doi.org/10.1016/j.nima.2014.06.035

I. Perić, C. Kreidl, P. Fischer, **Particle pixel detectors in high-voltage CMOS technology – New achievements**, *Nuclear Instruments and Methods in Physics Research* **A 650** (2011) 158–162. http://dx.doi.org/10.1016/j.nima.2010.11.090

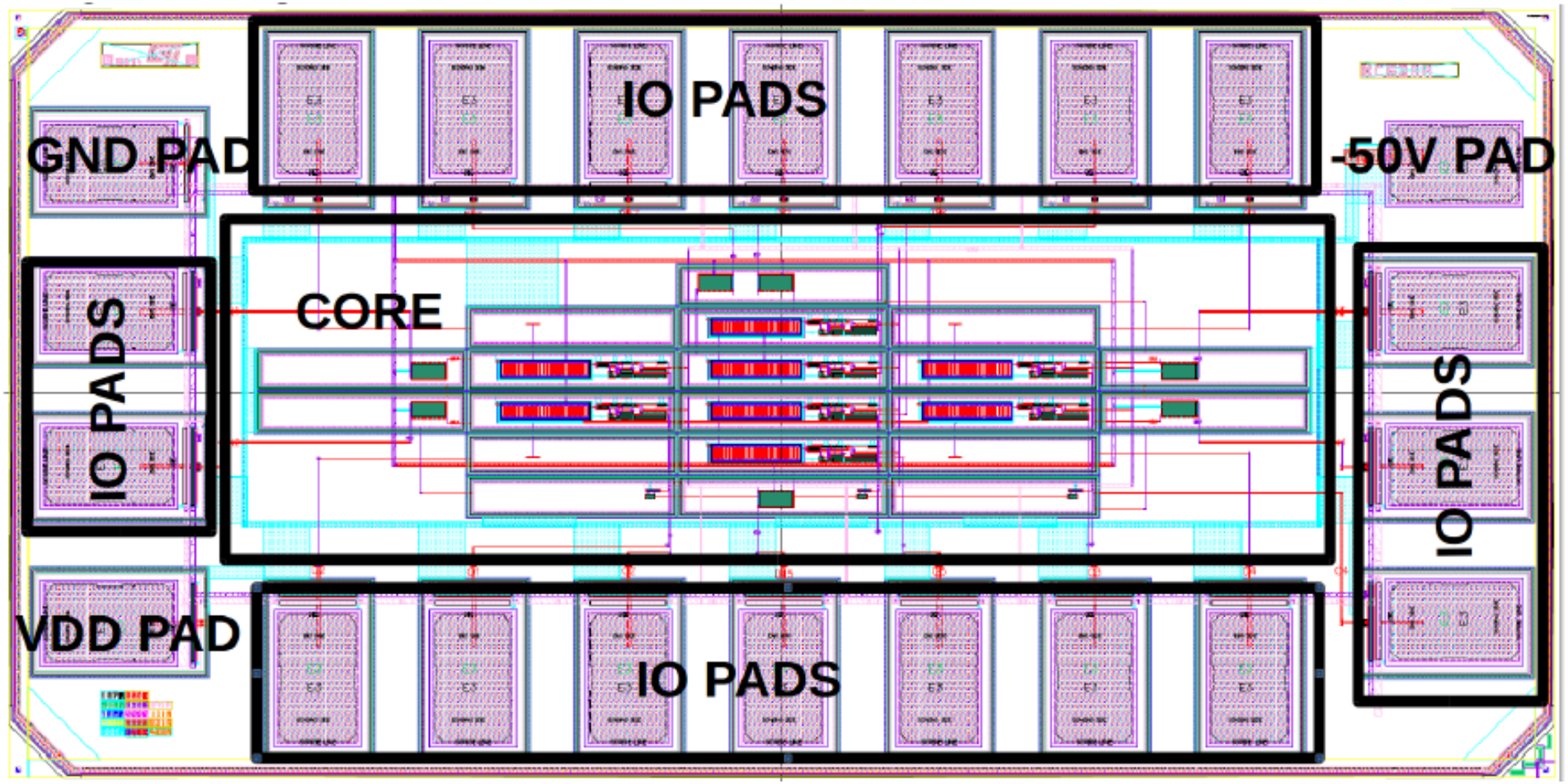
Preliminary Test Chip in BCD8

A preliminary test chip with simple structures was designed in a short time (3 weeks), to test some basic structures:

- passive diodes
- front-end amplifier
- isolation structures (for substrate bias at –50 V)
- ESD protection for signal pads

The "first" demonstrator in BCD8 will be designed in June 2015 (possibly compliant with the CPIX requirements).

Chip Layout

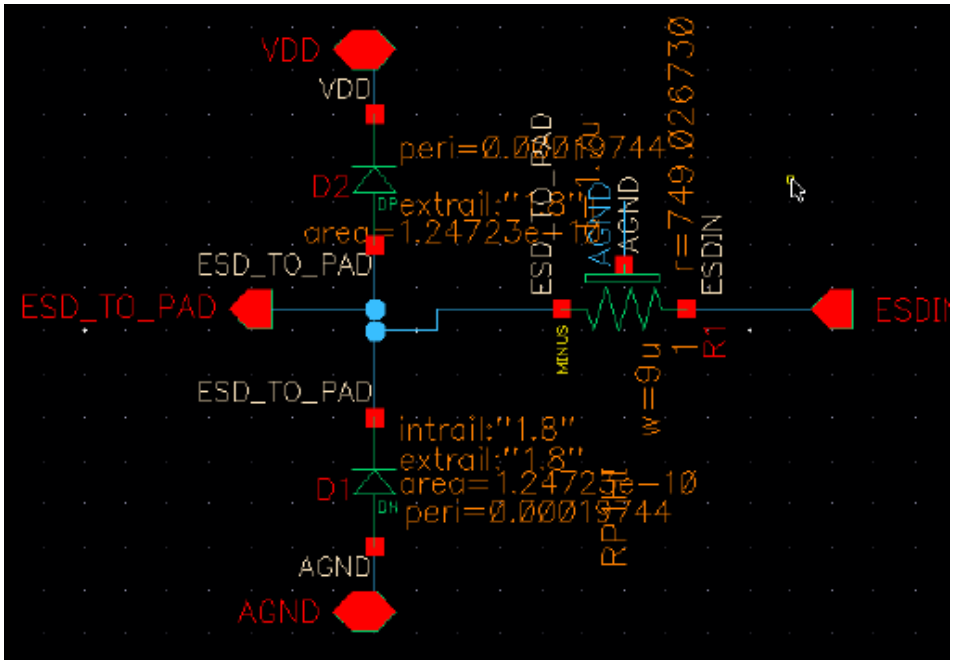


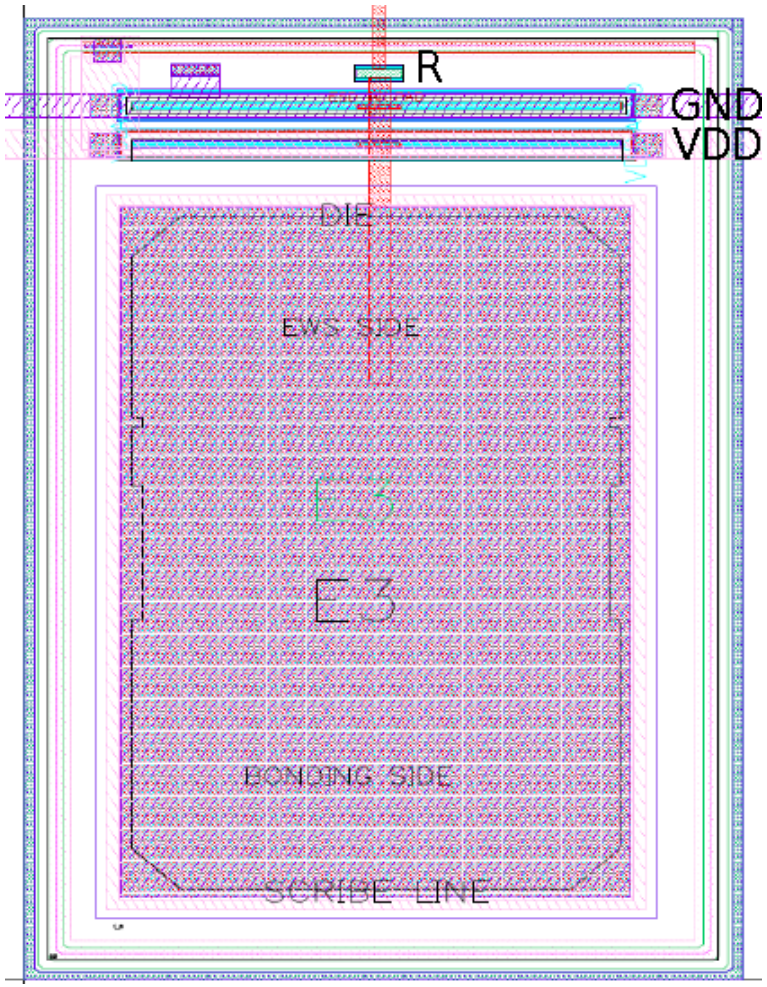
Chip size: 2 mm $\times$ 1 mm

Layout of the Array

4 Passive pixels (buried N-well to substrate diodes)
8 Active pixels (with the amplifier inside)
Pixel size: 250 μm $\times$ 50 μm

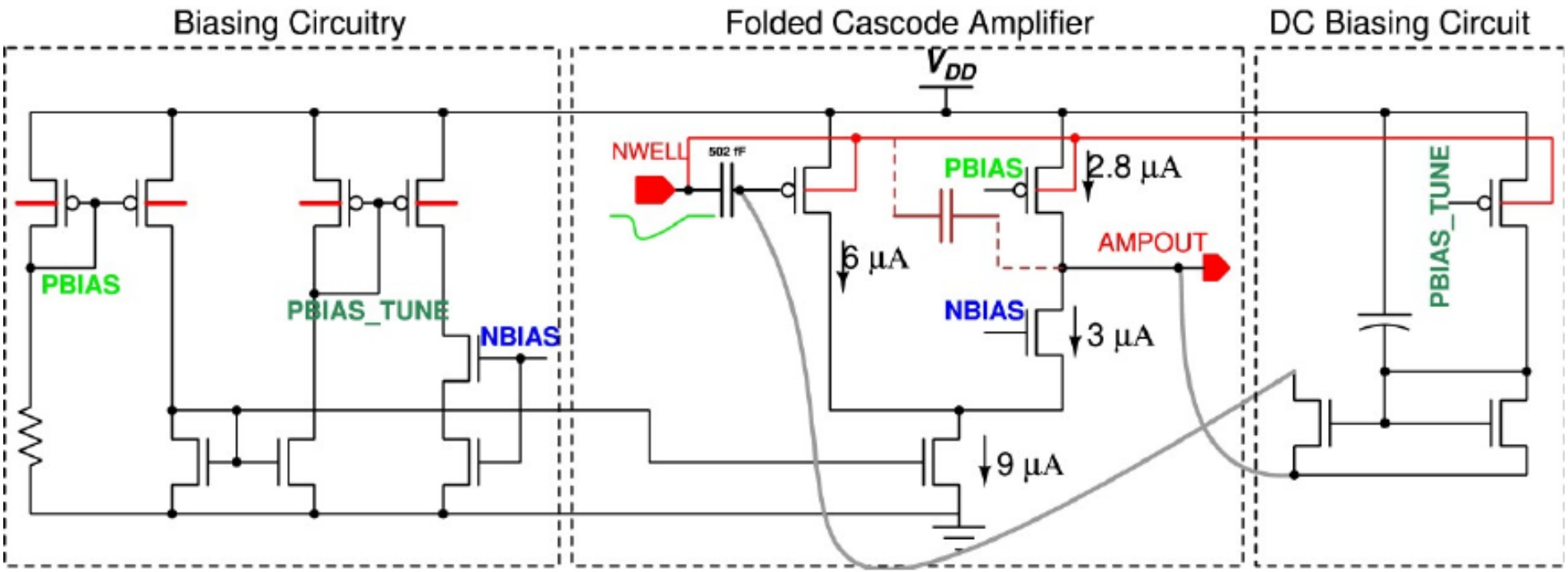
Layout of an I/O Cell



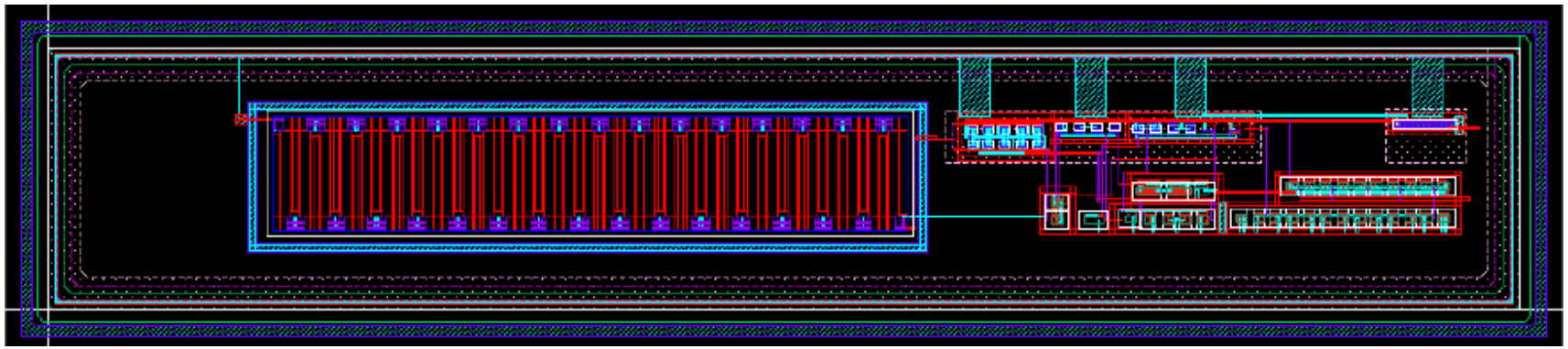


Shielded I/O pad with two protection diodes (towards VDD and GND) and series resistance (750 Ω) in high-resistivity polysilicon

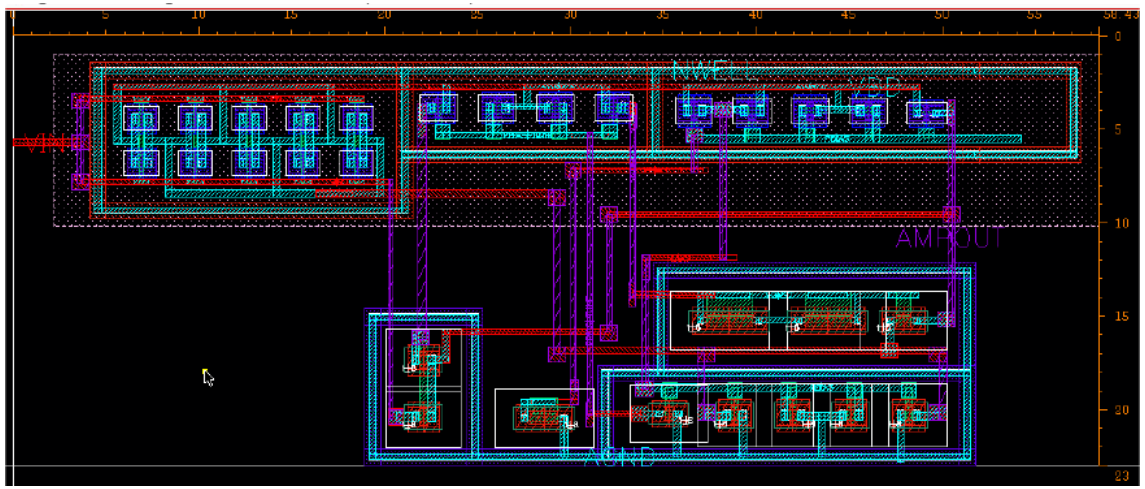
Amplifier schematic diagram



Layout of a single pixel

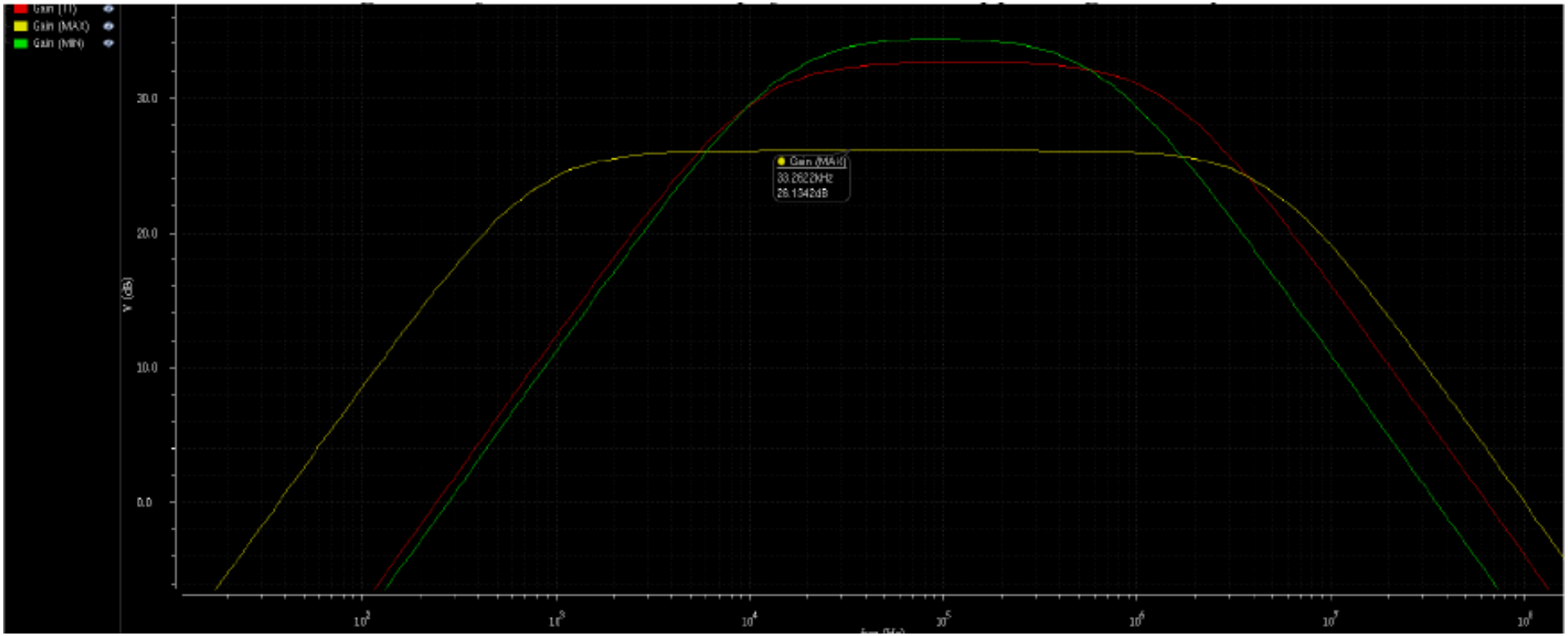


Size: 250 μm $\times$ 50 μm
Left: 0.5 pF capacitance; Right: amplifier + output buffer



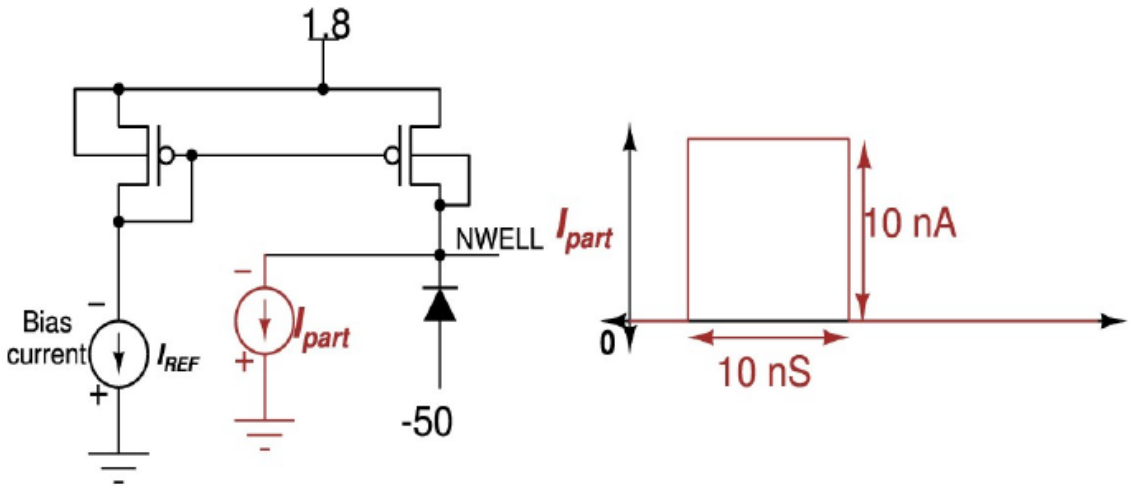
Detail of the folded cascode amplifier

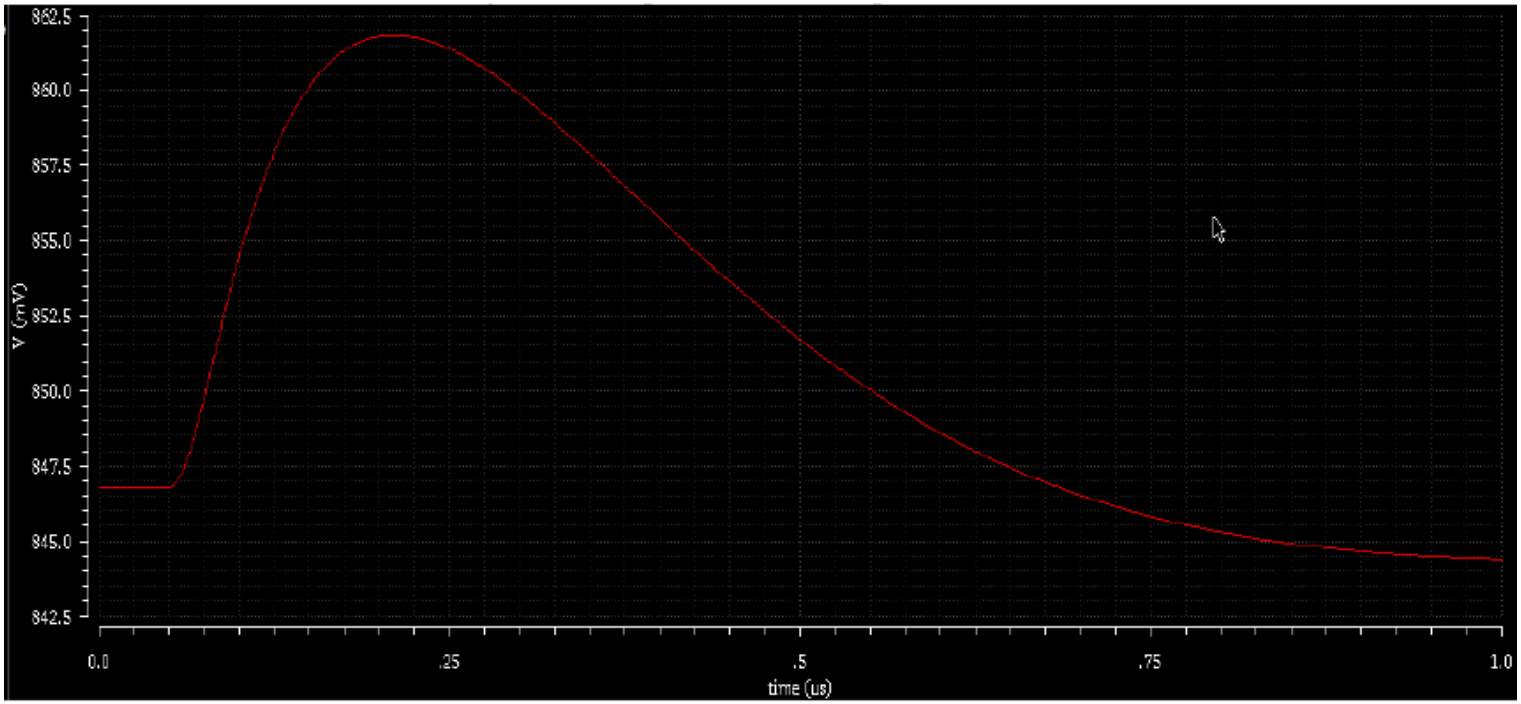
Simulation results: Amplifier gain



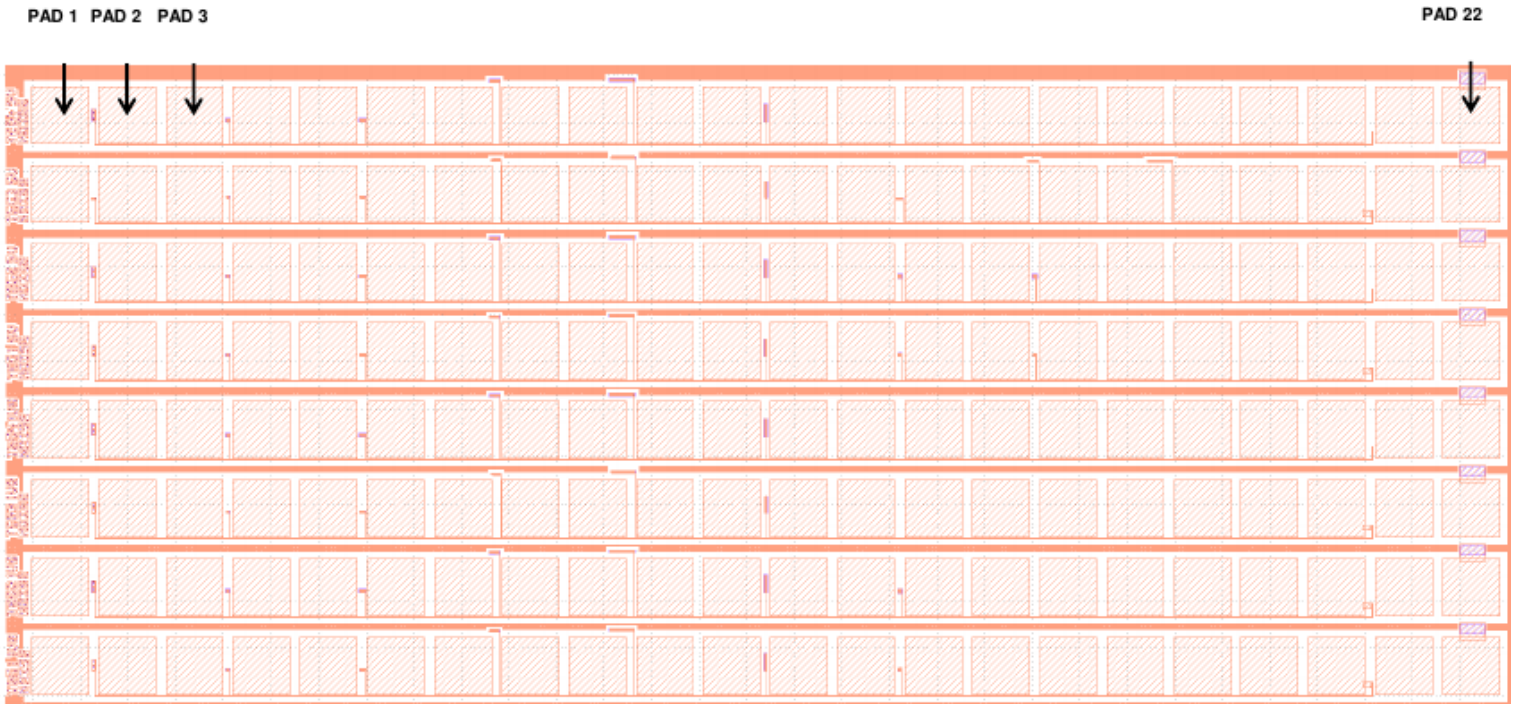
Gain: 26 dB $\div$ 34 dB
Bandwidth: from 10 kHz to 1 MHz

Simulation results: Amplifier output





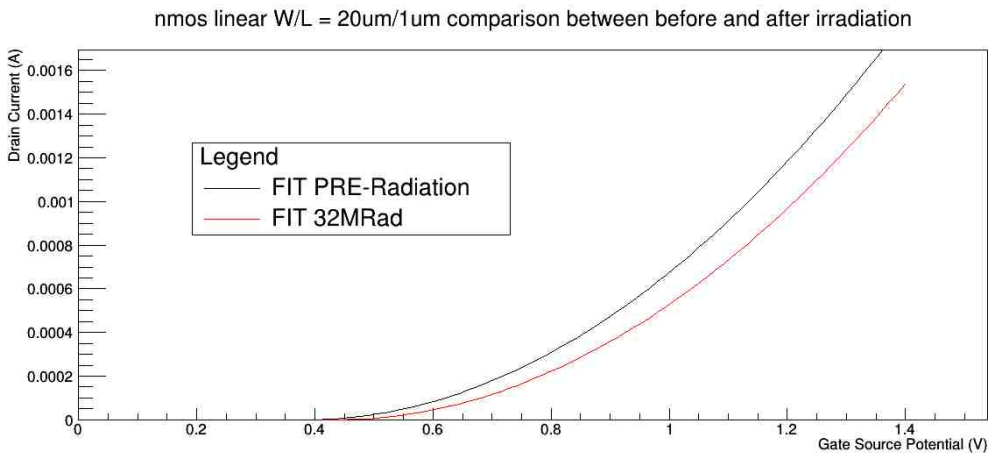
KC01: MOS Test Structures

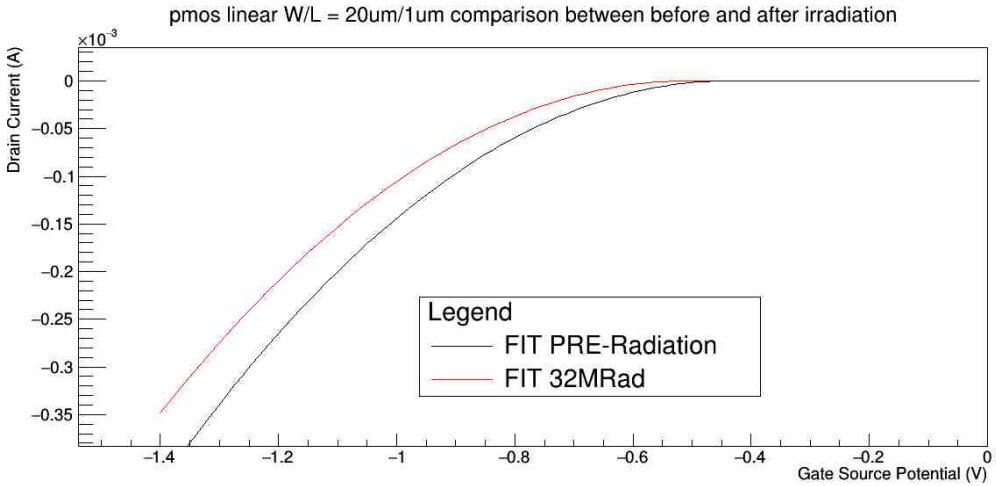


Each row contains single MOS transistors: 1.8 V / 5 V, NMOS / PMOS, standard / ELT
$W/L = 10\ \mu$m$/1\ \mu$m, $20\ \mu$m$/1\ \mu$m, $40\ \mu$m$/1\ \mu$m, $100\ \mu$m$/1\ \mu$m

Radiation test on KC01

LNS, Catania – May 17-20
TID: 32 Mrad





NMOS
$W/L = 20\ \mu\text{m}\ /\ 1\ \mu\text{m}$
black: TID $= 0$
red: TID $= 32$ Mrad
Threshold variation:
$\Delta V_{\text{th}}/V_{\text{th}} = +20\,\%$
Conductance variation:
$\Delta K/K = -7\,\%$

PMOS
$W/L = 20\ \mu\text{m}\ /\ 1\ \mu\text{m}$
black: TID $= 0$
red: TID $= 32$ Mrad
Threshold variation:
$\Delta V_{\text{th}}/V_{\text{th}} = +16\,\%$
Conductance variation:
$\Delta K/K = -4\,\%$

Conclusion

- CHIPIX65: DICE SRAM available for test
- CHIPIX65: D2RA new rad-hard logic family; test chip designed and submitted
- HVR_CCPD: KC53A submitted; 3-month delay in prototype delivery

Future activities:

- Design first chip in BCD8
- Laboratory characterization and radiation test of prototypes (CHIPIX65 and HVR_CCPD)
- Study of combined TID/SEE effects in 65 nm
- Study radiation effects in BCD8
- Improvement of models for radiation simulation at circuit level
- Develop a methodology for radiation hardness verification at layout level