RD_FASE2: INFN-FBK Sensors

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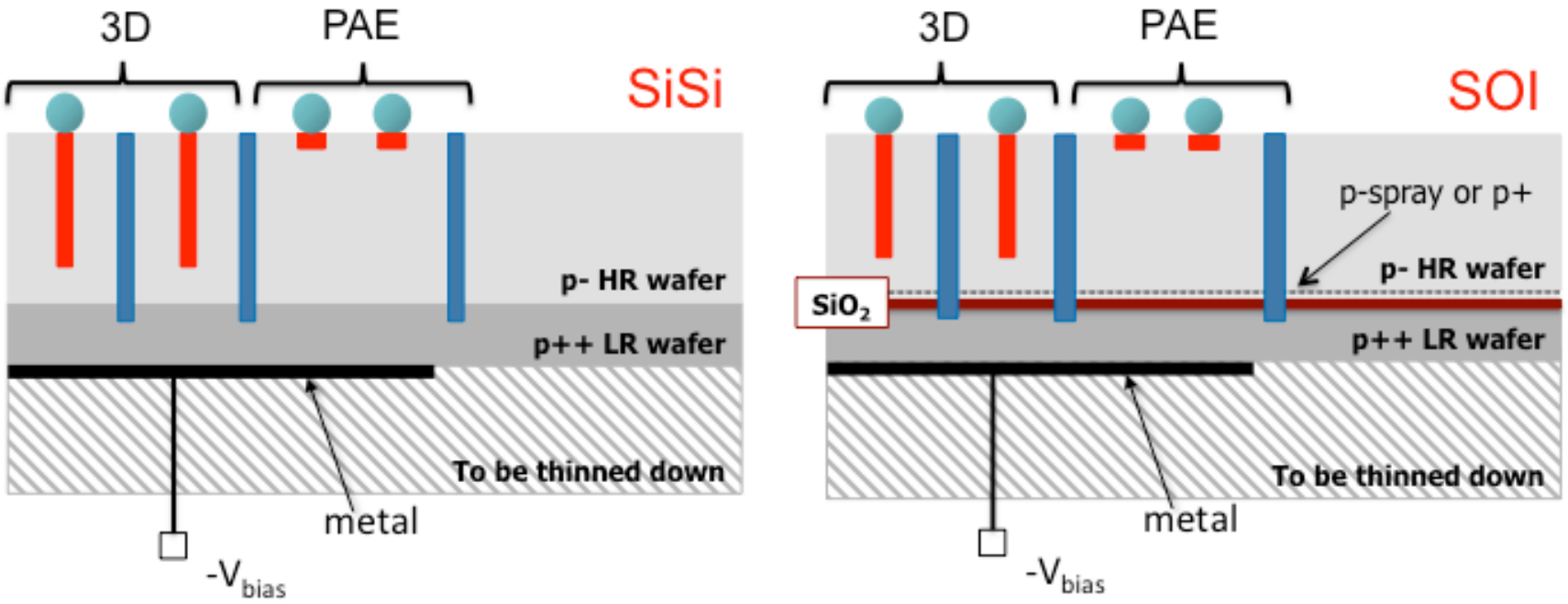
GOAL: development of new thin 3D and Planar Active Edge (PAE) pixel sensors on 6" p-type wafers at FBK:

- Technology and design to be optimized and qualified for extreme radiation hardness ($2x10^{16}$ n_{eq} cm^{-2})
- Pixel layouts compatible with present (for testing) and future (RD53 65nm) FE chips of ATLAS and CMS

Strong sinergy with WP7 of AIDA2020

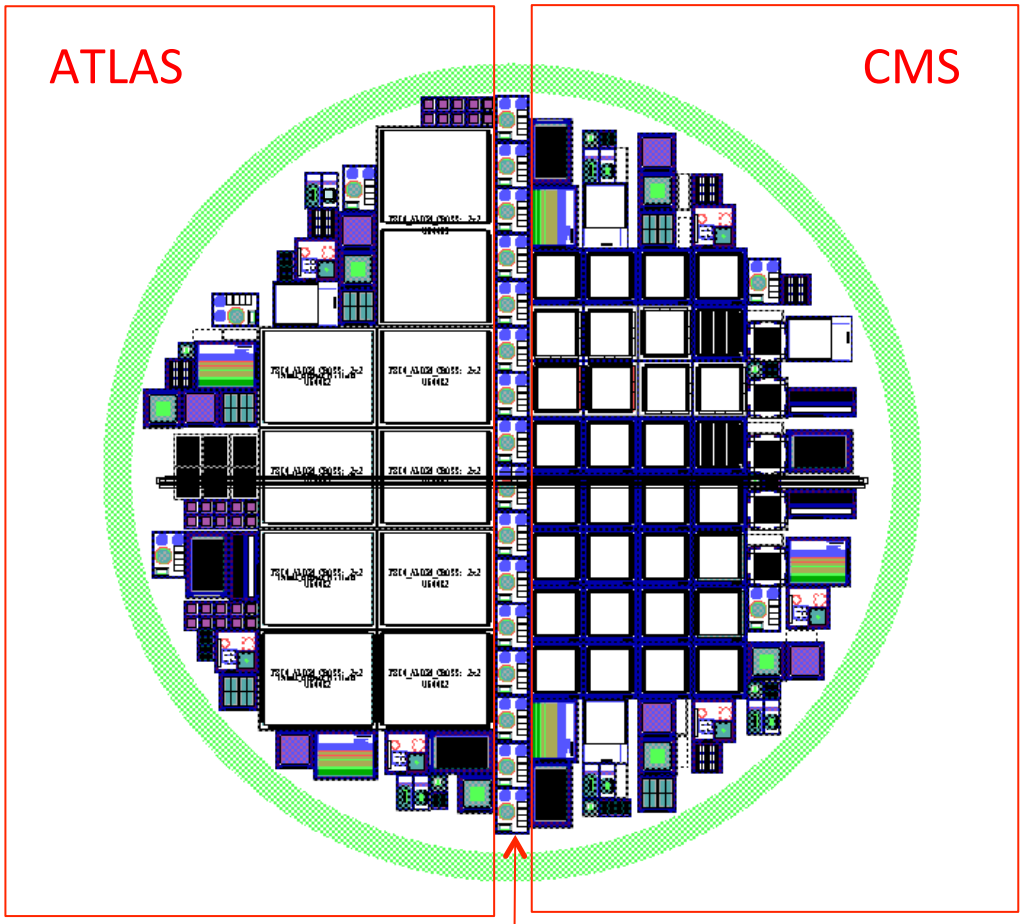
New single-side approach to 3D/PAE



- Thin sensors on support wafer: SiSi or SOI → Substrate qualification
- Ohmic columns/trenches depth > active layer depth (for bias)
- Junction columns depth < active layer depth (for high V_{bd})
- Reduction of hole diameters to ~5 um
- Holes (at least partially) filled with poly-Si

Process Tests

Planar test batch



Wafers

6” Si-Si silicon wafers (ICEMOS), 100±2μm and 130±2μm sensor layer thickness with ρ>3000 Ωcm (+500±10μm support wafer)

Process

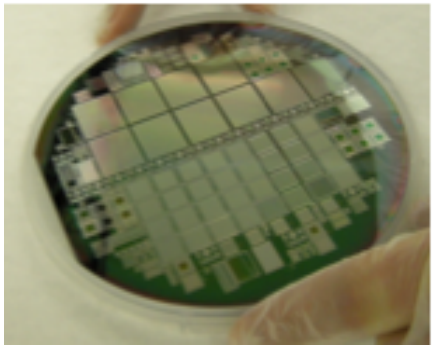
- n-on-p planar process
- three different p-spray doses

Layout

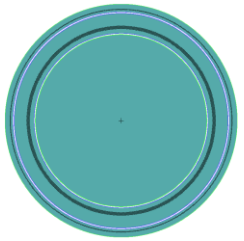
- 10 ATLAS pixels (FEI4)
- 32 CMS pixels (PSI46)
- Many test structures

Test structures for SiSi DWB substrate qualification

Batch completed at FBK in Dec. 2014

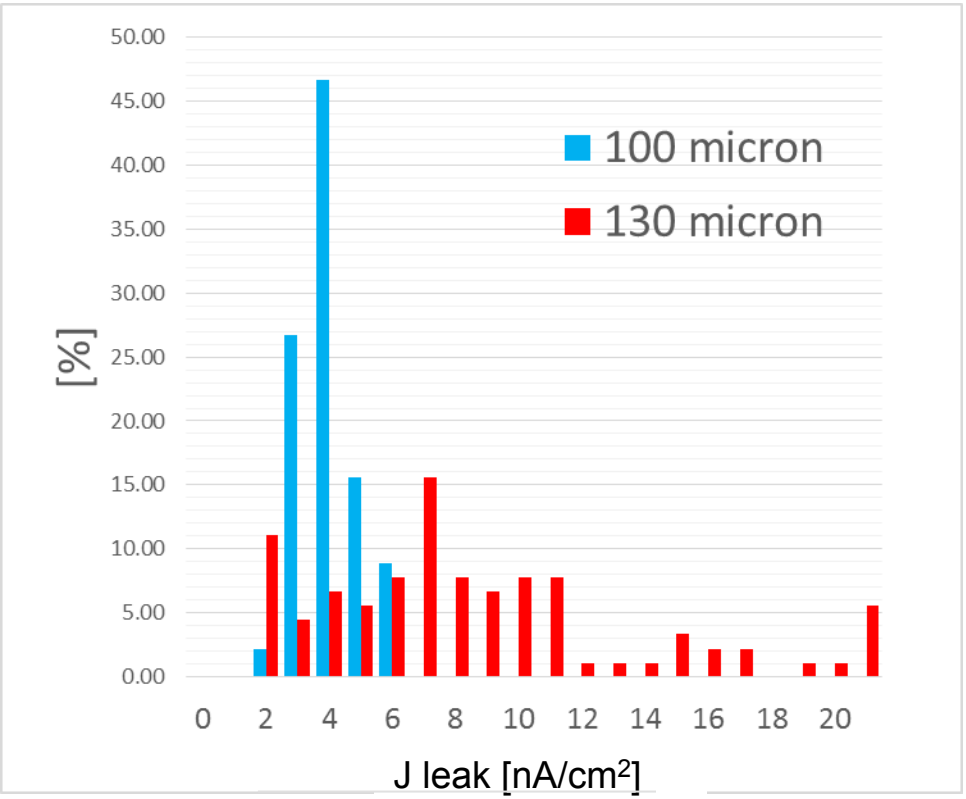


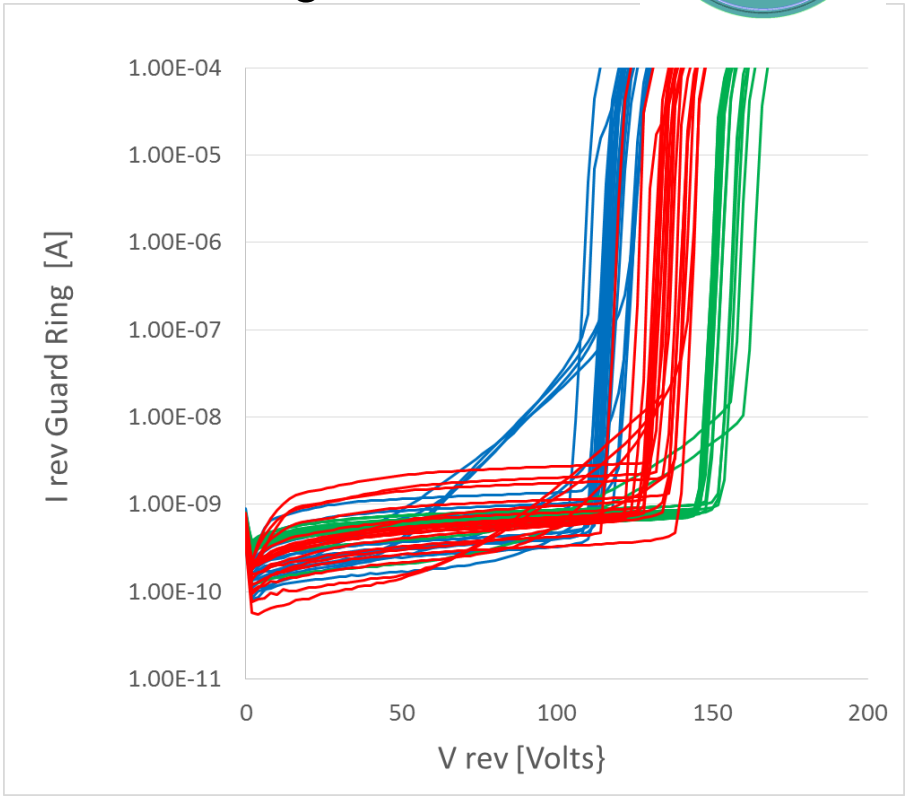
Test diode: I-V measurements



Measured at FBK up to 200 V

Circular diode, 4 mm^2, two Guard Rings





J_{leak} distribution on 135 diodes

→Different material quality ?

Guard Ring reverse currents on 3 wafers with 3 p-spray doses: Low Medium High (correct V_{bd} trend)

Test diode: C-V measurements

Measured at FBK

Depletion voltages:

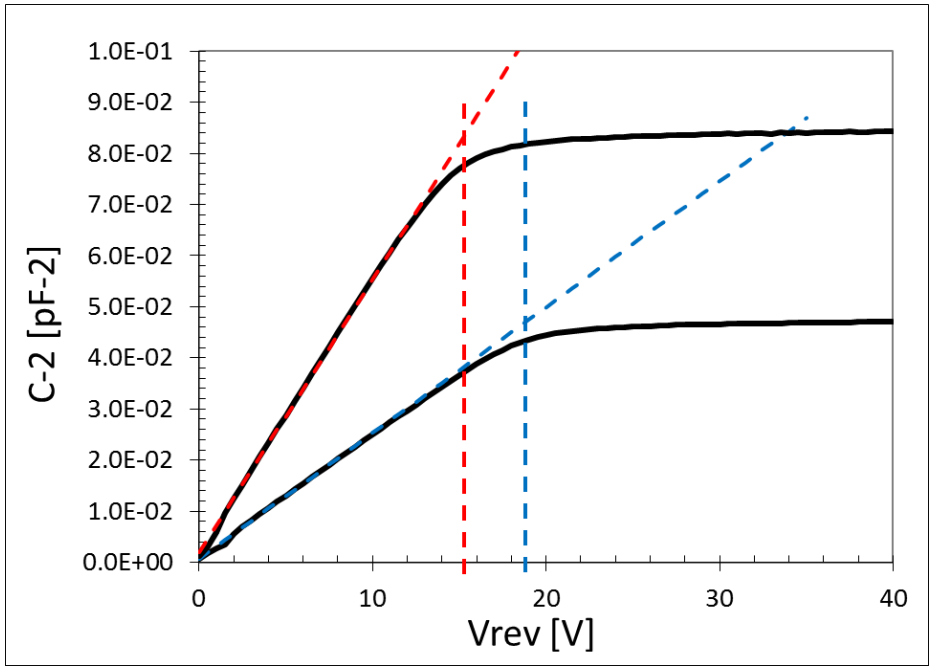
- V_{depl} ~ 16V for 100 μm thick.
- V_{depl} ~ 20V for 130 μm thick.

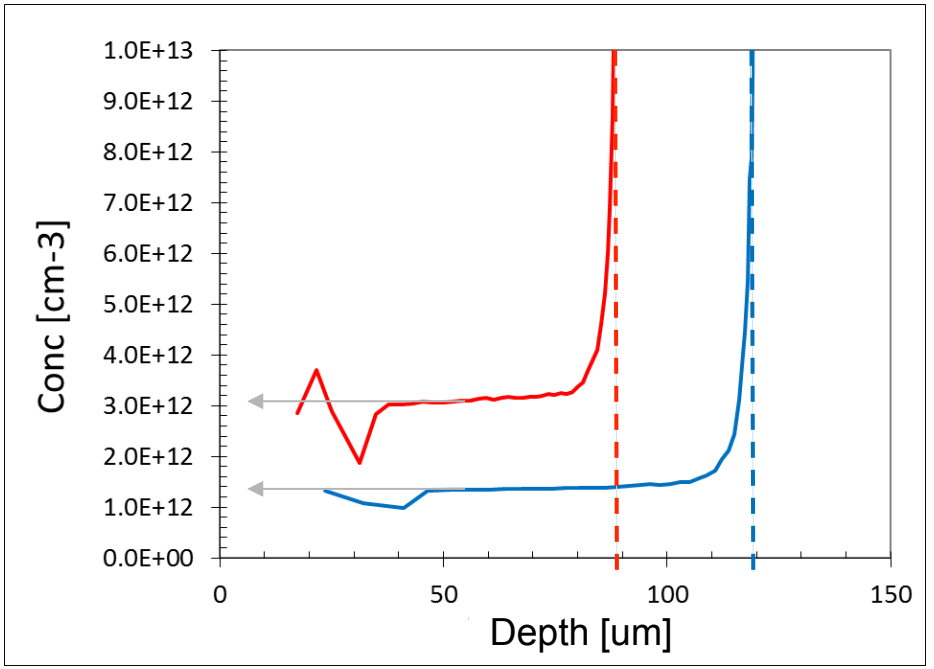
do not scale with square of thickness

→ Different resistivities …

Concentration profiles

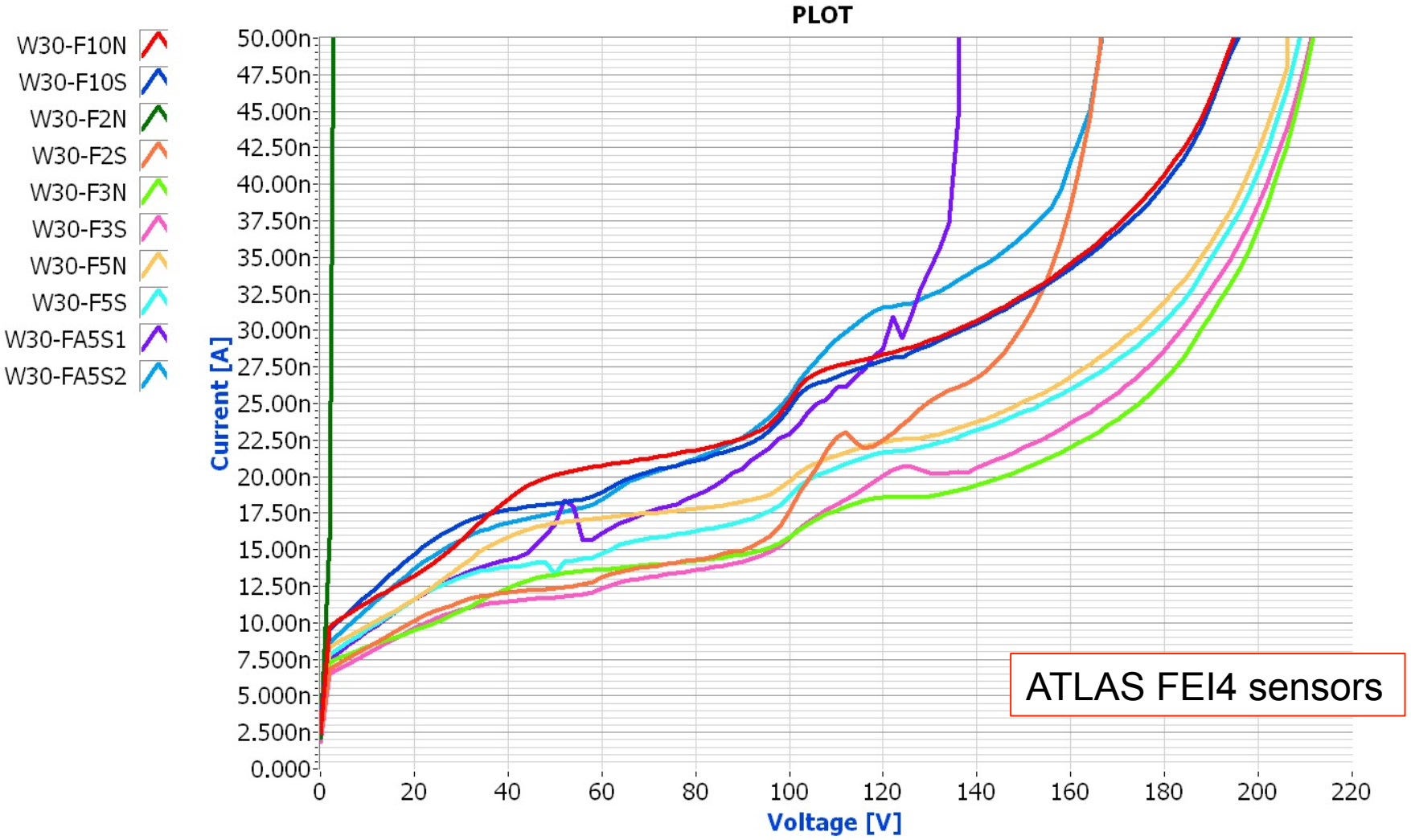
- Doping 1 – 3 x 10^{12} cm^{-3}
- Thicknesses about 10 μm lower than the nominal values, compatible with Boron diffusion from support wafer and measurement limit (L_{debye})



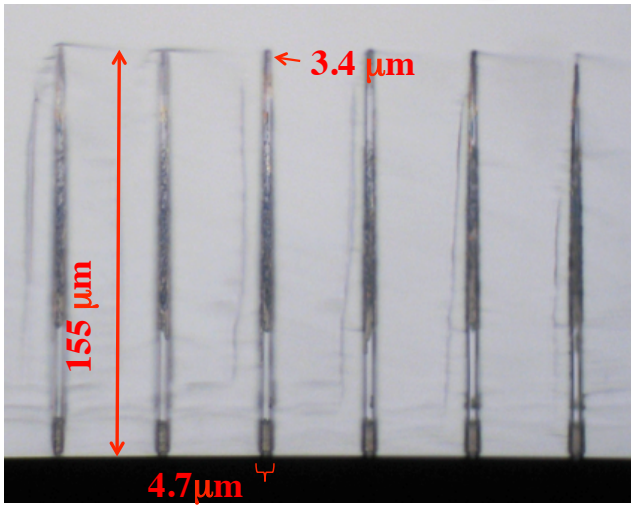


Pixel sensors I-V measurements

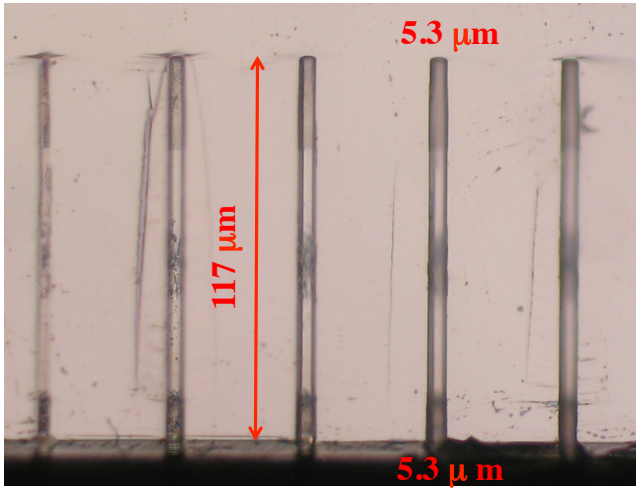
Measured at INFN Firenze up to high voltage



Etching narrow columns by DRIE

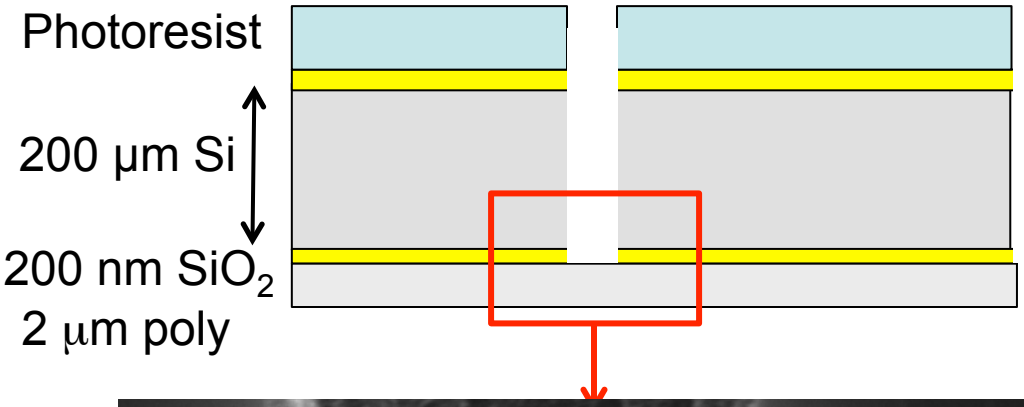


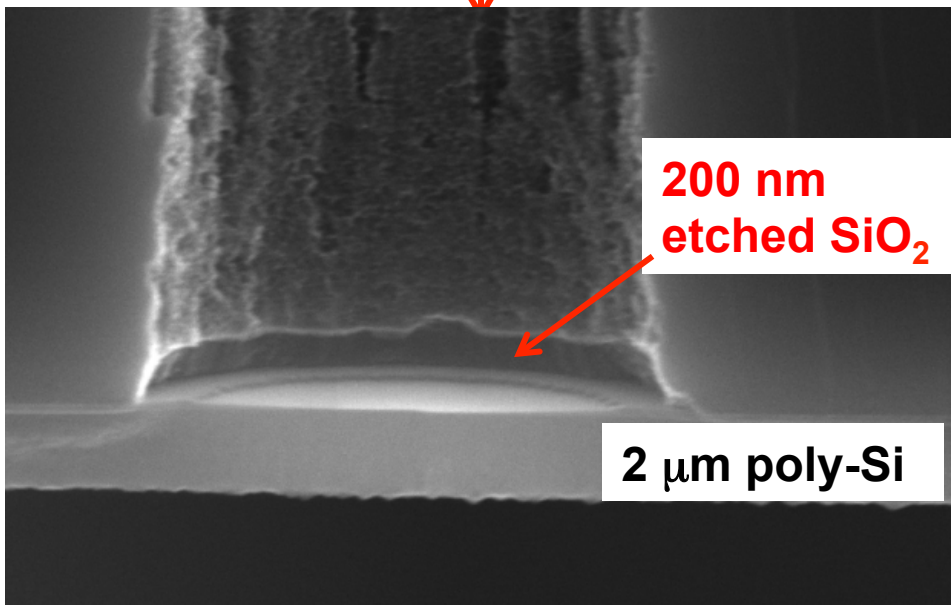
Ohmic columns optimized for depth



Junction columns optimized for uniformity

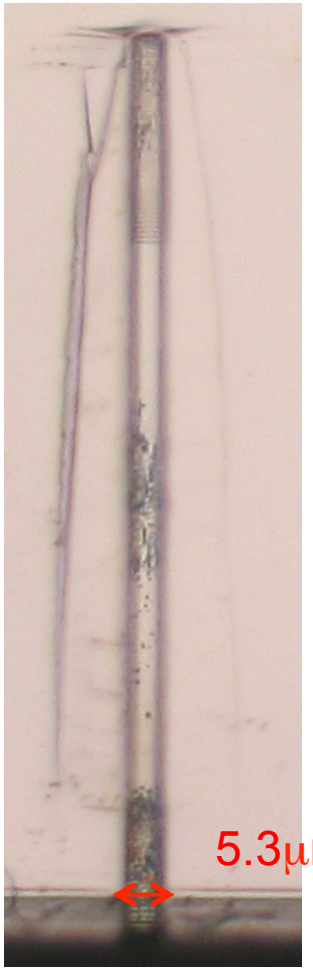
Testing different etching depth and etching through oxide layer for SOI approach



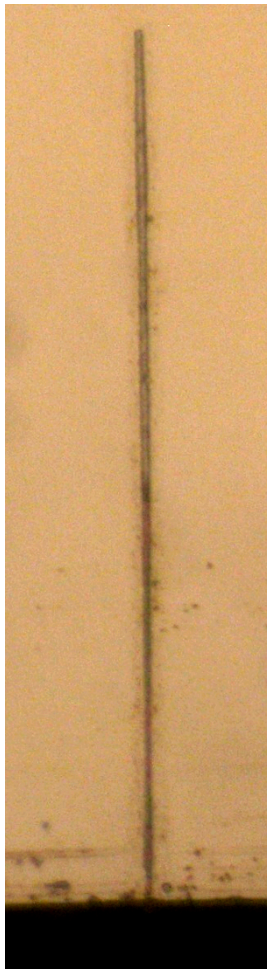


Poly-Si filling and 2nd DRIE

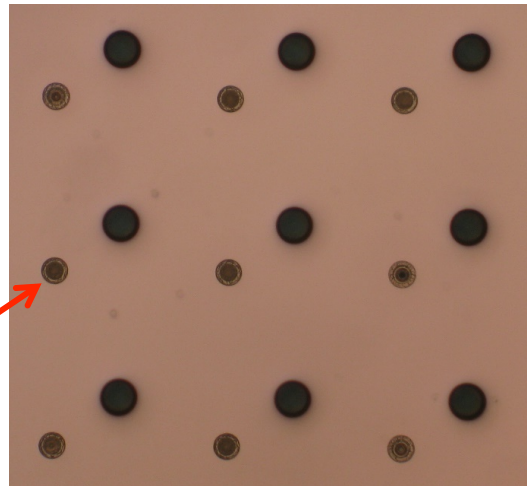
Reducing the hole diameter with poly-Si deposition to ease the 2nd DRIE on the same wafer side

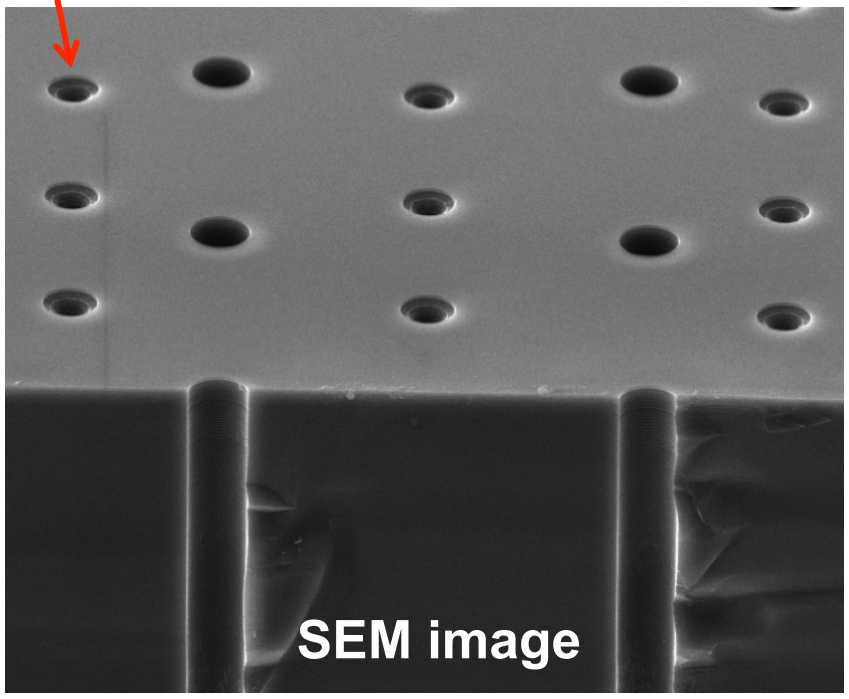


4μm poly-Si

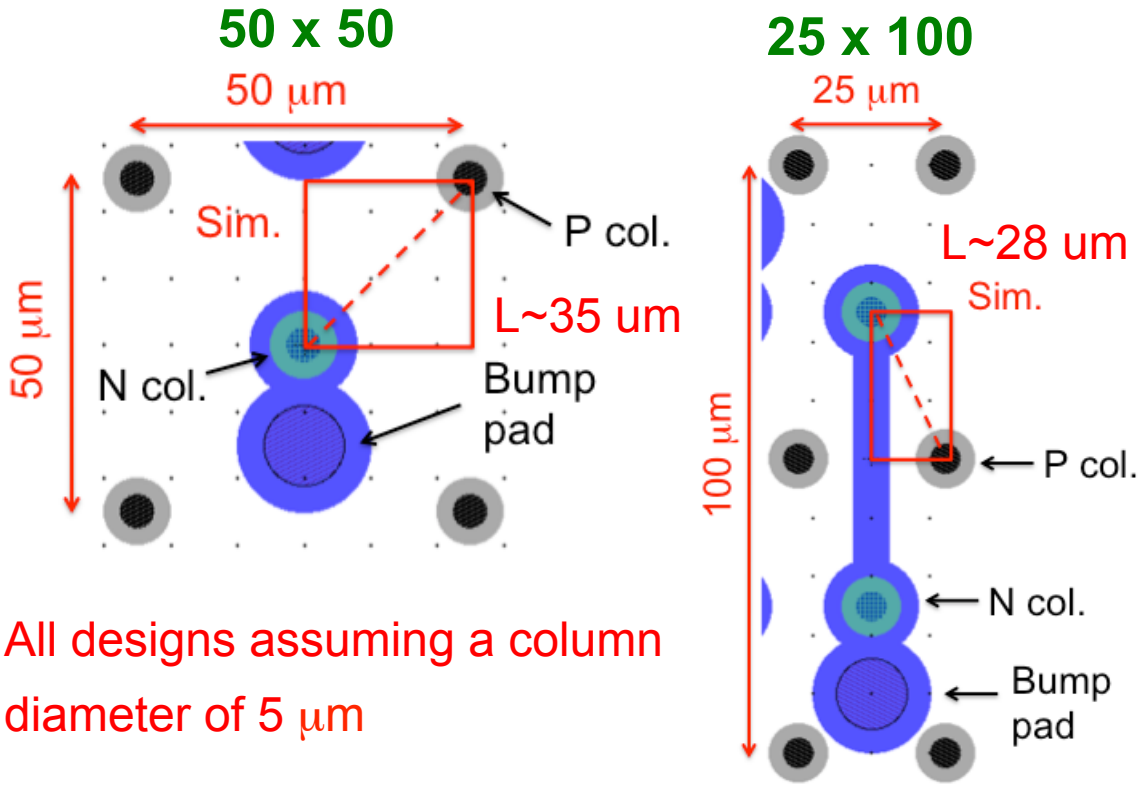


First holes partially filled with poly-Si

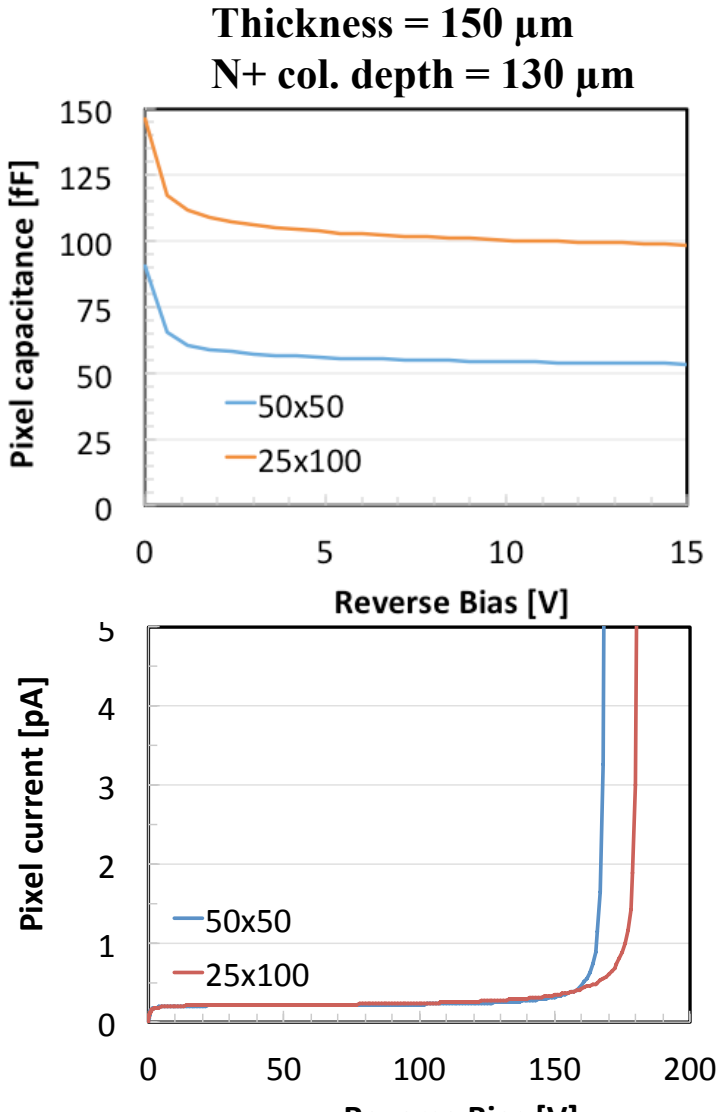




New 3D pixels: design and simulations



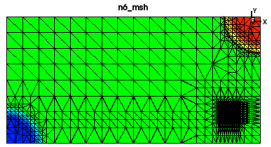
All designs assuming a column diameter of 5 µm

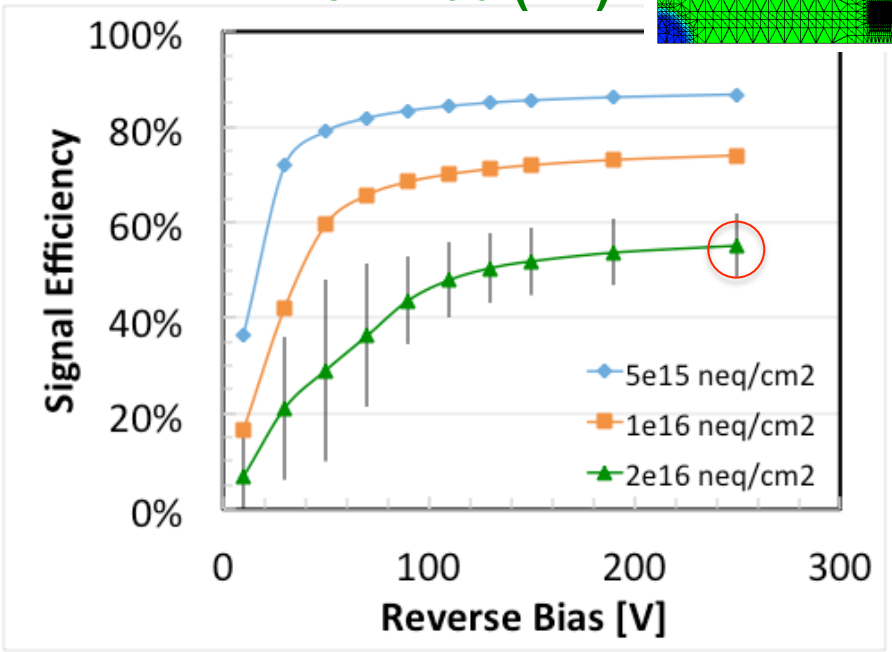


- 50x50 design safe, 25x100 is difficult … too little clearances (new ideas for bump pad to be tested)
- Capacitance compatible with RD53 specs
- Initial breakdown voltage high enough

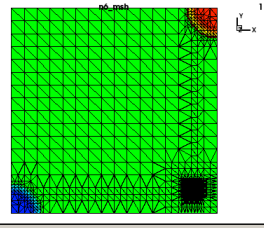
Simulated signal efficiency (preliminary)

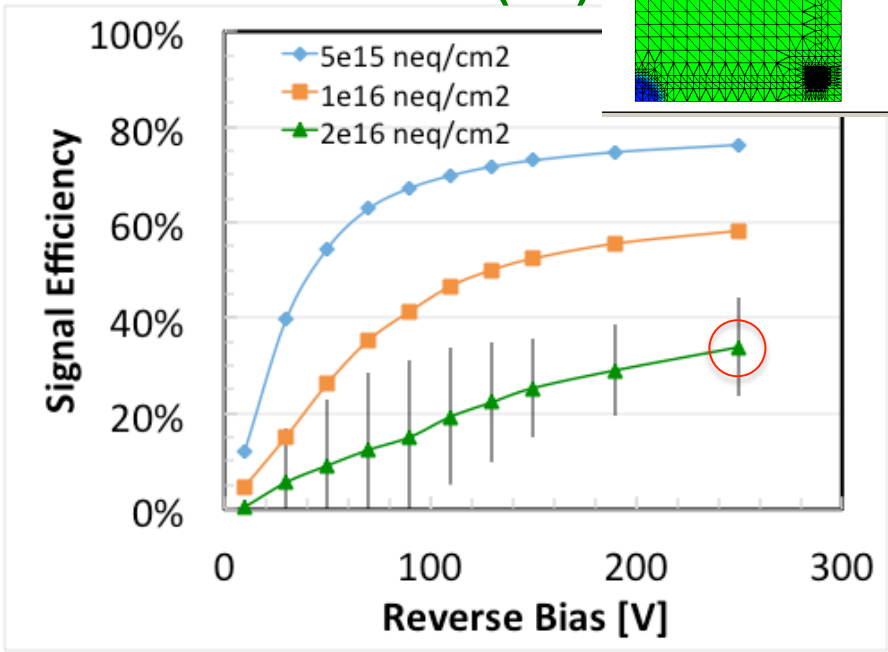
25 x 100 (2E)





50 x 50 (1E)





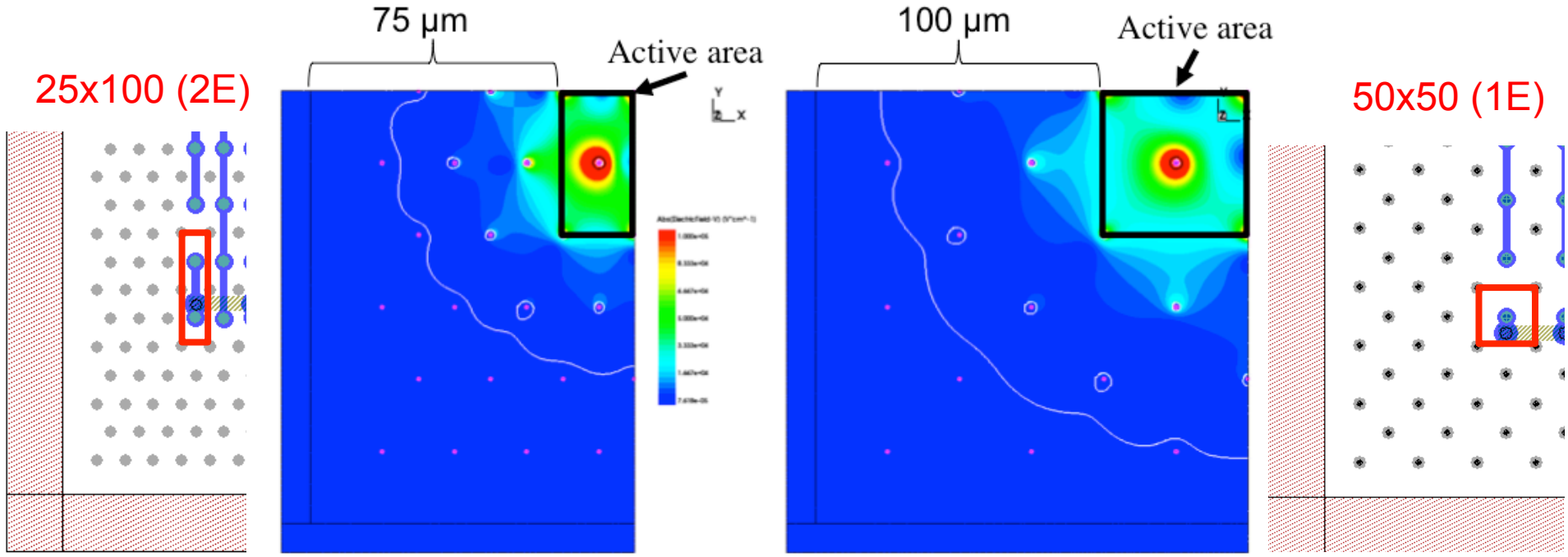
- 3-trap level "Perugia" model, parameters from D. Pennicard, NIMA 592 (2008) 16

[Underestimates SE at large fuence, improved model being developed]

- 1 μm thick (~2d) slice, with MIP vertical hits at several different points
- 20-ns integration of current signals, average, and normalization to injected charge
- Higher Signal Efficiency at lower V_{bias} in 25x100 (2E), as expected due to smaller L

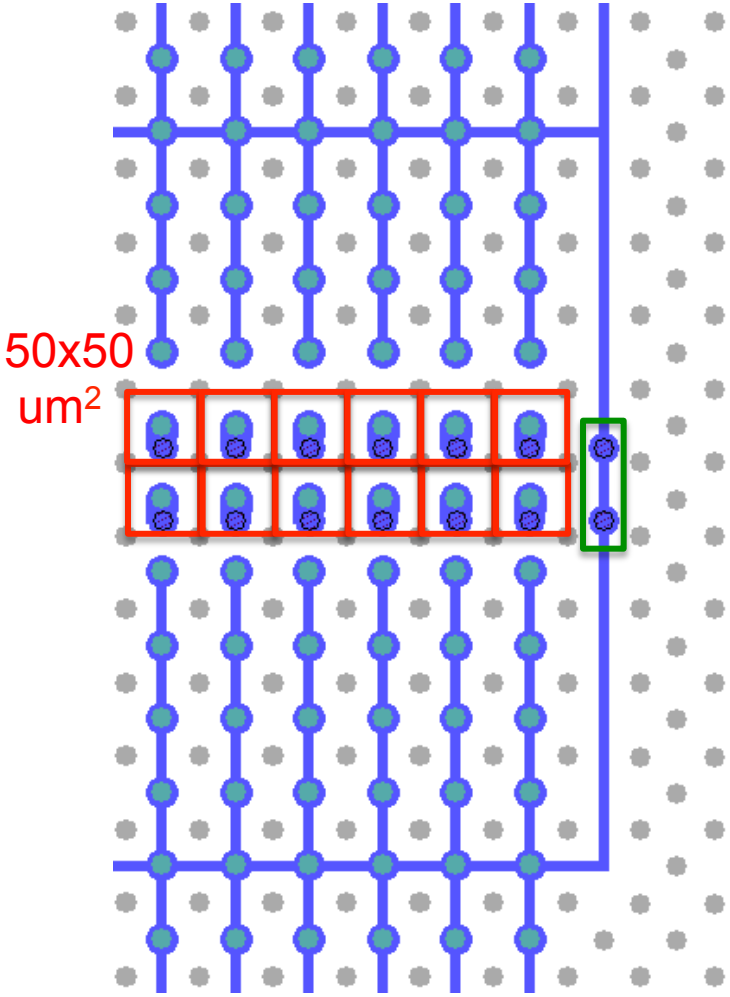
Slim edges

- Slim edge concept based on multiple ohmic columns termination developed for IBL (~200 μm) M. Povoli et al., JINST 7 (2012) C01015
- It can be made slimmer by reduced inter-electrode spacing (safely 75 - 100 μm, more aggressively down to ~50 μm)
- 3D guard rings also possible with similar dead area

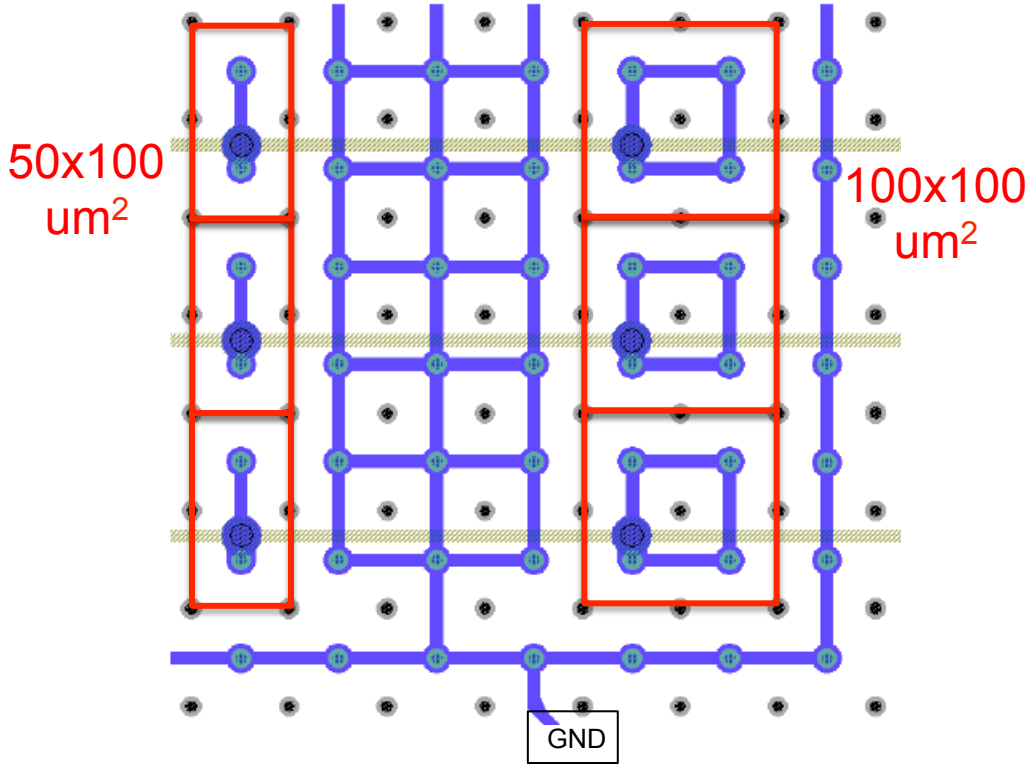


New pixels with existing ROCs ?

ATLAS FE-I4 50x50 (1E) + grid

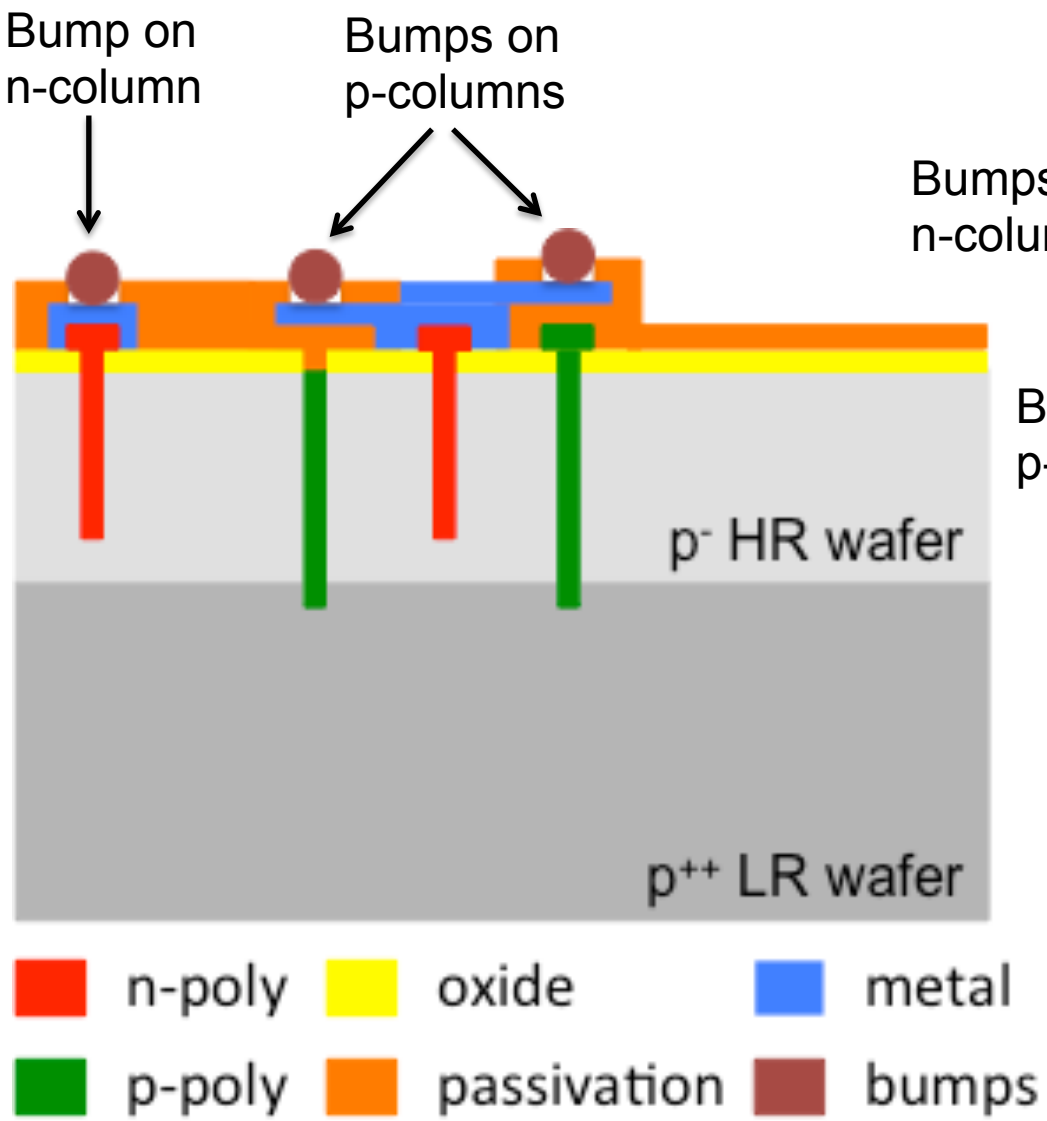


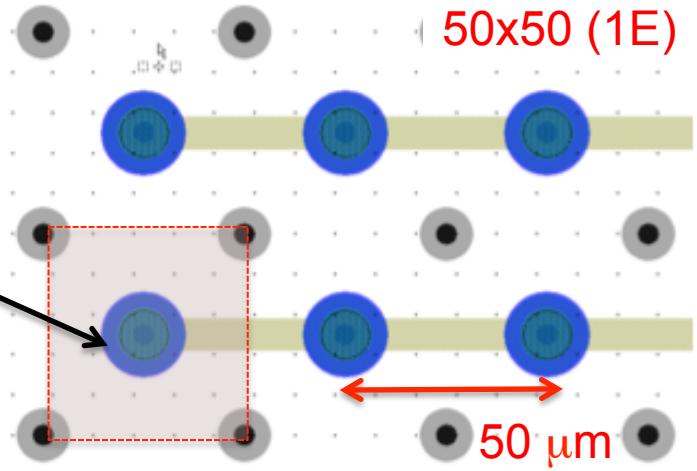
CMS PSI46: 50x50 (2E+4E) + grid

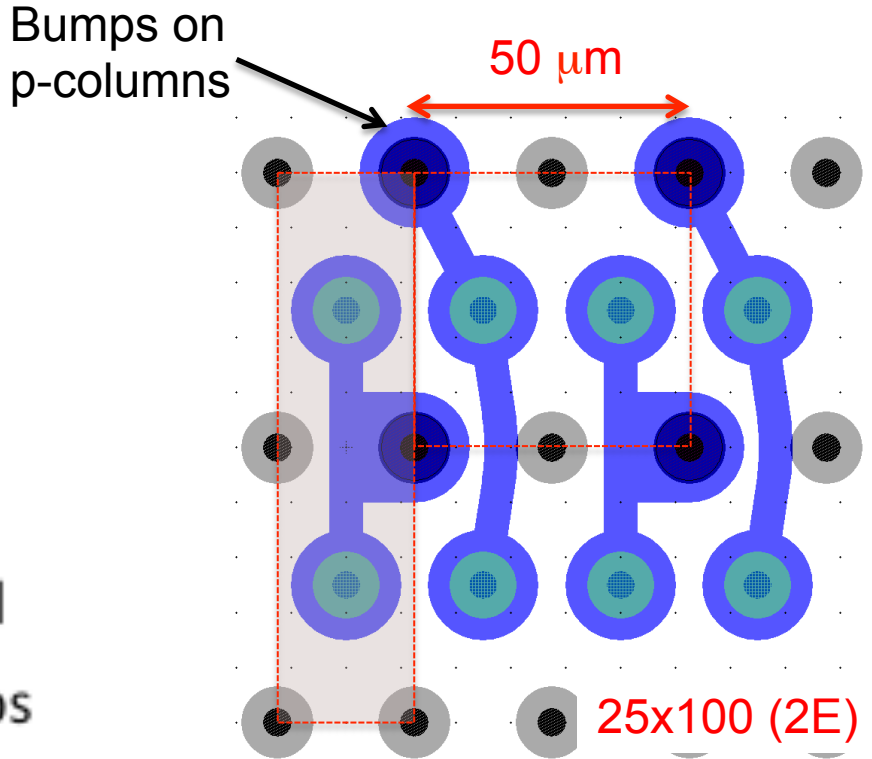


Small pixels take all bonding pads
+ rest of pixels at GND using a metal grid and extra-pads at the periphery

Bumps on columns

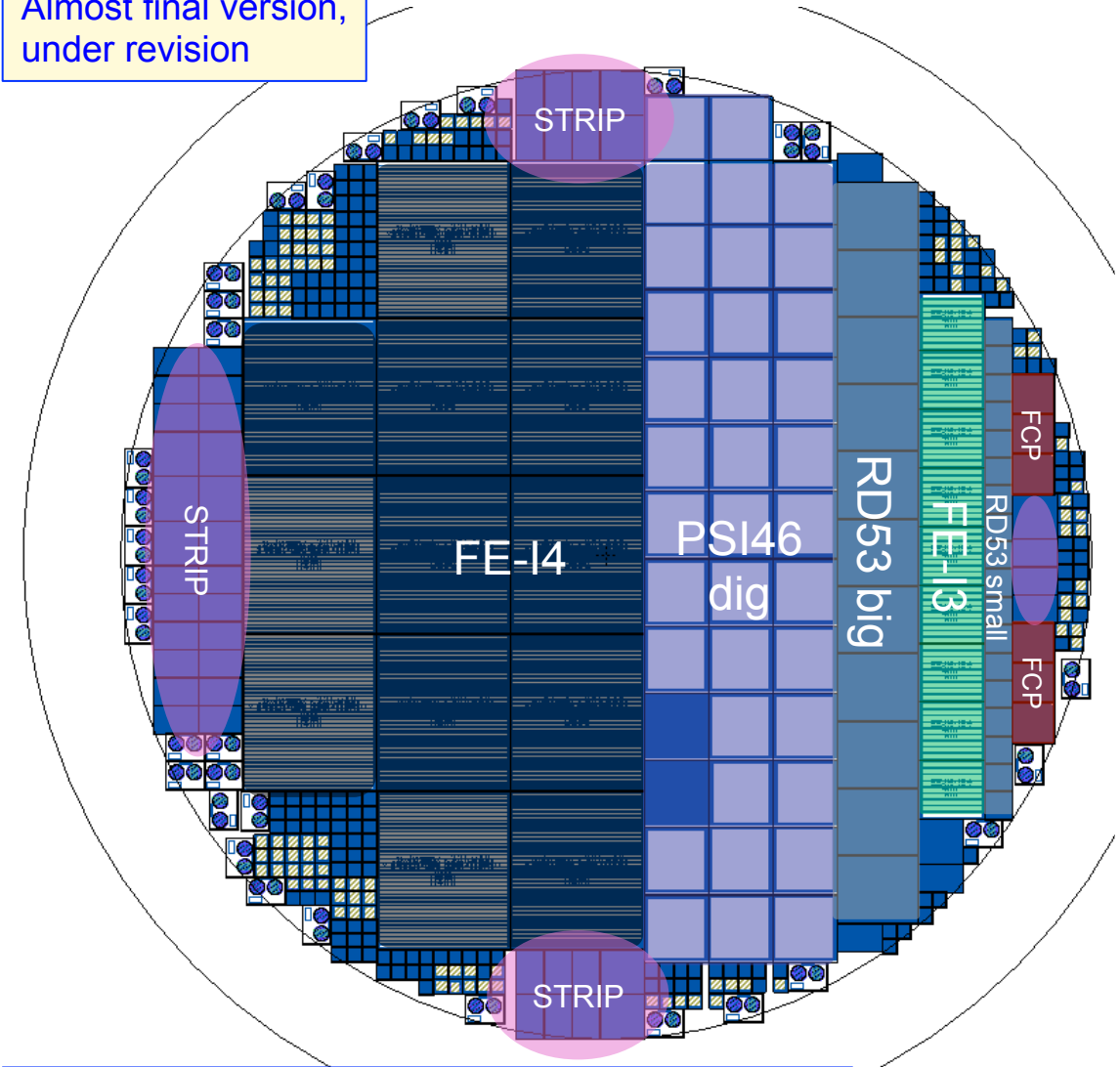






3D Pixel Wafer Layout

Almost final version, under revision



Many different pixel geometries and pitch variations:

- FE-I4
  - 50 x 250 (2E) std
  - 50 x 50 (1E)
  - 25 x 100 (1E and 2E)
  - 25 x 500 (1E)
- FE-I3
  - 50 x 50 (1E)
  - 25 x 100 (1E and 2E)
- PSI46dig
  - 100 x 150 (2E and 3E) std
  - 50 x 50 (1E and 2E)
  - 50 x 100, 100 x 100 (2E + 4E)
  - 50 x 100, 100 X 150 (2E + 6E)
  - 25 x 100 (1E and 2E)
- FCP
  - 30 x 100 (1E)
- RD53
  - 50 x 50 (1E)
  - 25 x 100 (1E)
  - 25 x 100 (2E)

+ Test structures (strip, diodes, etc)

Fabrication plans at FBK

- Ready to go with first 3D batch (~15 SiSi DWB wafers)
  - 5/6 wafer 130μm thick, p-columns with poly "cap"
  - 4/5 wafer 130μm thick, p-columns without poly "cap"
  - 3/4 wafer 100μm thick, p-columns with poly "cap"
- Delivery expected in ~4-5 months

- Mean time we ordered also SOI wafers from ICEMOS:
  - Due by July
  - Planned for use in PAE batch, now being designed
  - Further tests of deep SiO_2 etching planned for 3D in view of possible future use