

Genova Pixel-Lab Setups and Activities



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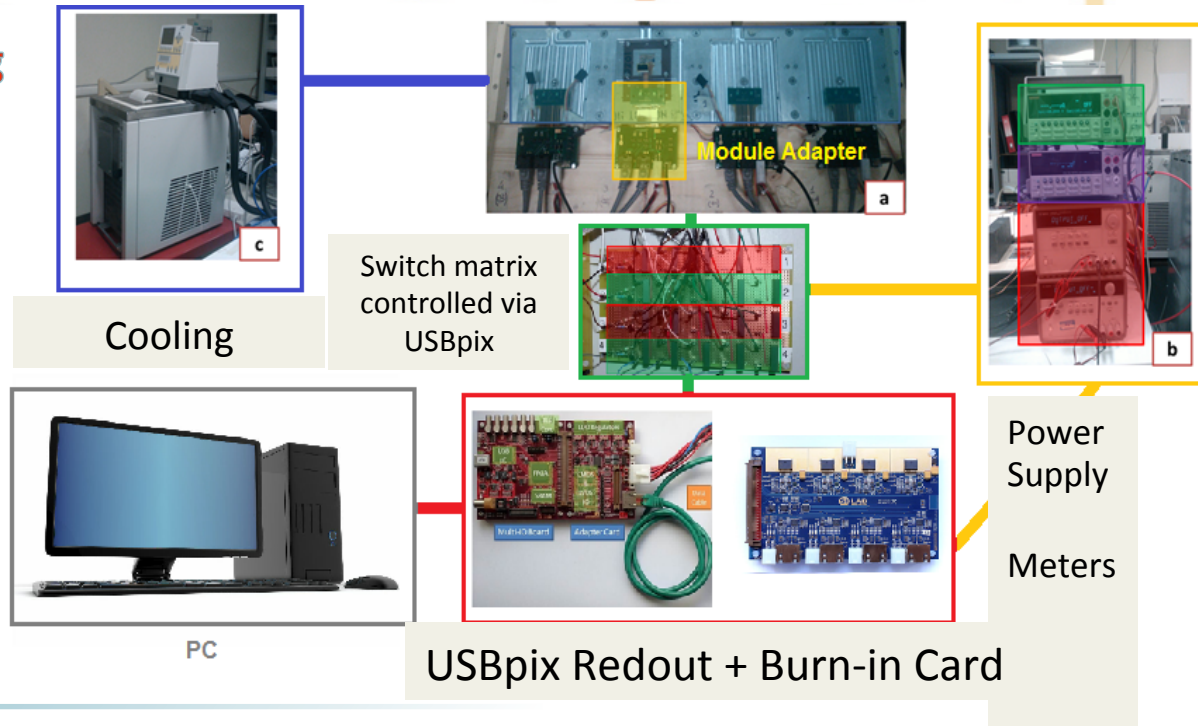
AVAILABLE SETUPS

BASIC SETUPS: USBPIX + STCONTROL

Setup for Planars and 3Ds Testing

4 Single or double FE-I4 modules can be tested sequentially using 2 USBPix (1 Master and 1 slave) + 2 BURN-IN Card Adapters which replace the standard USBpix FE-I4 adapter card

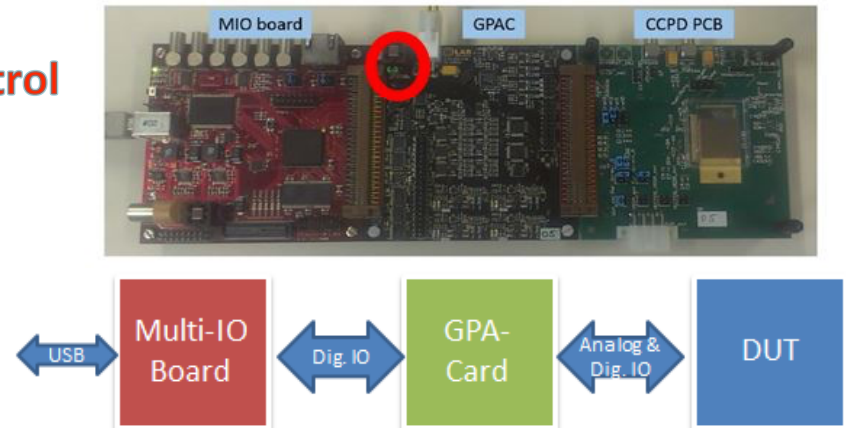
The software used for data taking is STControl



Setup for HV-CMOS: Usbpix+GPAC+DUT

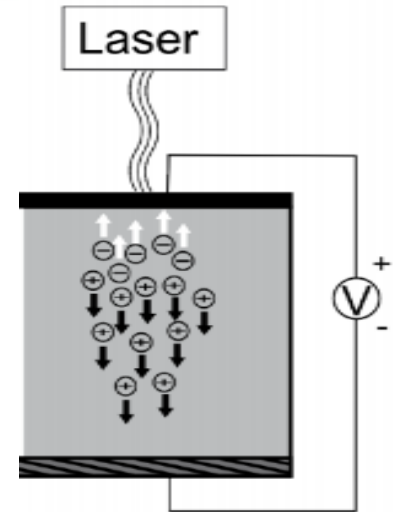
The software used is a modified version of STControl

The General-Purpose-Analog-Card (GPAC) is an adapter card for the Multi-IO FPGA board. It extends the digital IO capabilities of the Multi-IO card by analog blocks (power supplies, voltage and current sources, fast ADC etc.) , programmable level LV-CMOS, and LVDS digital IOs.



LASER SETUP

Most of the particles that are detected by the ATLAS pixel detector are MIPs.

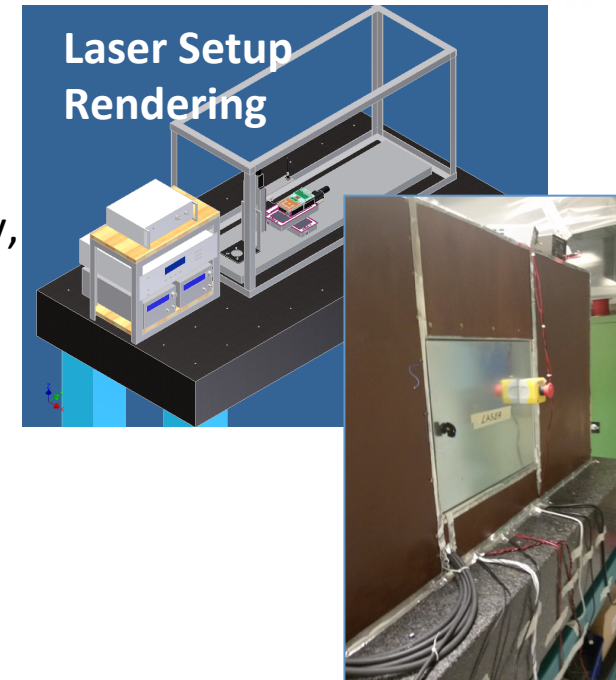


- ✓ By traversing the sensor they produce approximately 80 electrons/ μm
- ✓ Wavelengths used for our setup is 1060 nm ($E_\gamma = 1.17$ eV)
- ✓ Deposition like MIPs
- ✓ Useful to find efficiency map of one pixel

- ✓ **Remote controlled X, Y, Z and Phi stages**
- ✓ **50 ps laser synchronized with 40 MHz clock** of USBpix
Prototype board for dividing the USBPix clock (1/2000) and trigger the laser
In testing a new board with adjustable 250 ps step fine delay, with microcontroller and USB interface.

- ✓ **Stages controlled by ST control software**

- ✓ **System tested** to work with 3D module, but it works also on other types of sensors

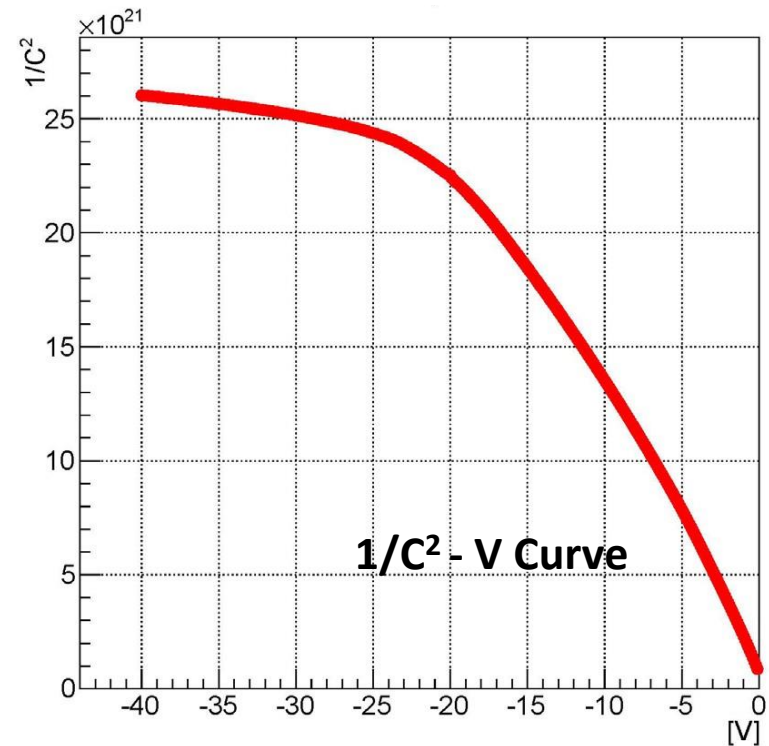
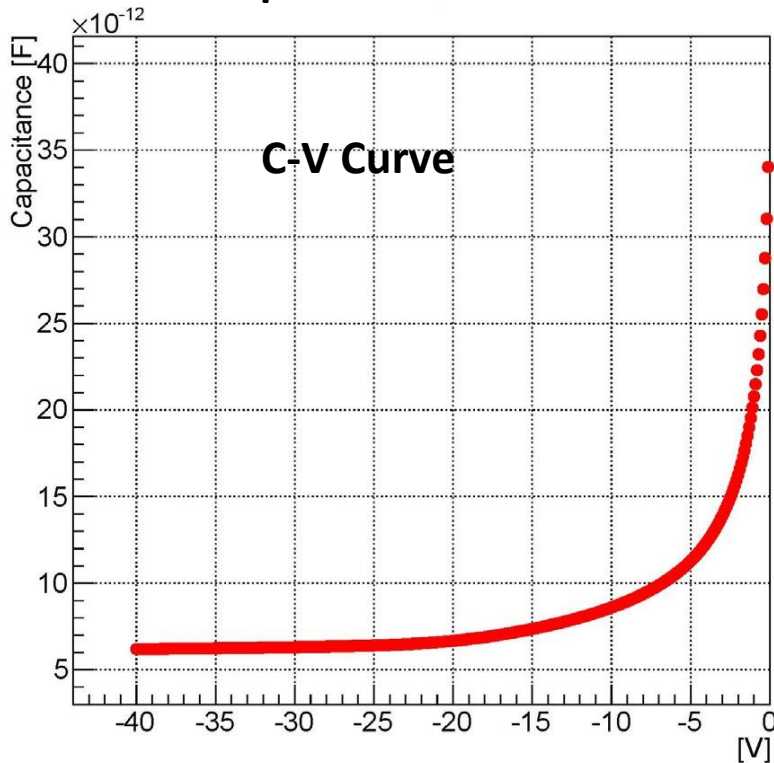


C-METER SETUP

- ✓ Frequency: $1 \text{ MHz} \pm 0.01\%$
- ✓ Possible to use: External or Internal Bias
(Range 0 – 100 V Resolution 1 mV)
- ✓ Possible to do C(G)-V , C(G)-t curve with floating or grounded DUT
 - ✓ C Measurement Range: $1 \text{ fF} \sim 1.9 \text{ nF}$
 - ✓ G Measurement Range: $1 \text{ nS} \sim 12 \text{ mS}$



We have developed a PC interface controlled via GPIB with ROOT graphic libraries integrated





MEASUREMENTS IN PROGRAM

FBK PLANARS AND STRUCTURES

FBK Planars:

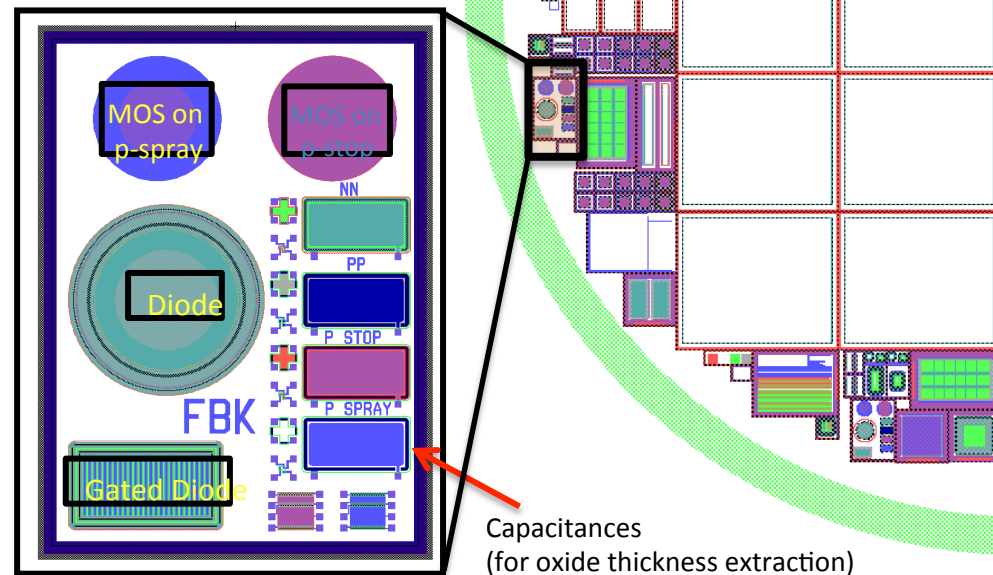
- ✓ p-type SiSi DWB wafers from IceMOS
- ✓ $100 \div 130 \text{ }\mu\text{m}$ high-R active sensor thickness
- ✓ Bump-bonding: 5 wafers at IZM, 1 at Selex (W69)
- ✓ **Bare Sensors:** I-V, C-V, charge collection with laser and Cremat Amplifier/Shapers → (Available)
- ✓ **Bump-Bonded Sensors:** Assembled with flex / PCB
 - ✓ Complete Lab for Sensor and FE Characterization (IV, Digital, Threshold scans...) including Laser and Source Tests with ^{241}Am and ^{90}Sr . → (Available from end of June)

FBK Test structures:

Received a diced wafer with test structure and 10 FE-I4 tiles

- ✓ I-V, C-V measurements, charge collection with laser and Cremat Amplifier/Shapers
↘ (Available)

Sensors: FE-I4 size

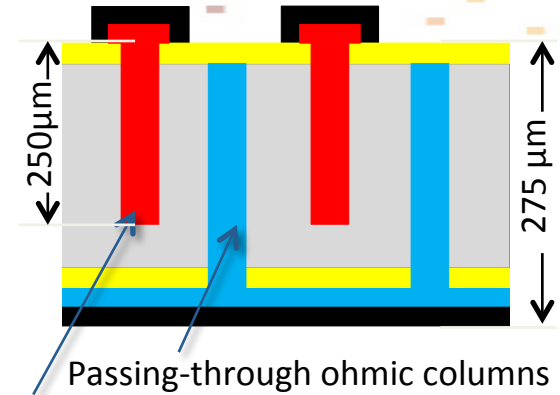


FBK IBL LIKE 3Ds ON 6" WAFERS AND HV-CMOS

FBK 3Ds:

Defect rate higher than IBL: no totally good FE-I4!

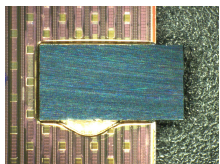
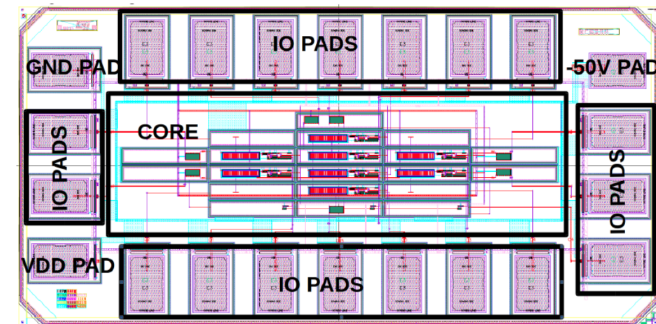
- ✓ One wafer currently for bump-bonding at Selex with special bump-mask: **leave unconnected pixel column with low V_{BD}**
- ✓ We will receive the two worst sensor assembled to FE-I4 to check that the bad columns are really unconnected (bumps are missing only on sensors side and FE-I4 side bumps can connect to open bump-pads)
- ✓ If the assemblies have not low breakdown assemble into dressed modules: flex or PCB and complete Lab Characterization including Laser and Source Tests with ^{241}Am and ^{90}Sr → **(Available from end of June)**



Partially etched junction columns
Column (10÷13 μm) partially filled with doped poly-silicon

Italian HVR CCPD

- ✓ Test the prototype submitted in December to ST Microelectronics **should arrive this July**
- ✓ Active and passive diodes
- ✓ We think to do I-V, C-V curve, test charge collection with laser and Cremat Amplifier/Shapers, CSA (Charge Sensitive Amplifier) measurements and checking it with simulation



We have also 2 HV2FEI4v2 chips to make to new assemblies and they will be tested with USBpix+GPAC (+ other 2 already assembled actually in debug)

↘ **(Available)**

CONCLUSIONS

- ✓ Starting from the end of this month we have in planning many measures on Planars, 3Ds and HV-CMOS.
- ✓ Many efforts should be also done on test scans improvement and development.
- ✓ It could be a good occasion to share competence in our community.
 - ✓ Anyone is interested to participate is surely welcome in our Lab!

