SLP1 testing progress report

for the Executive Board meeting

Christos Gentsos

Aristotle University of Thessaloniki

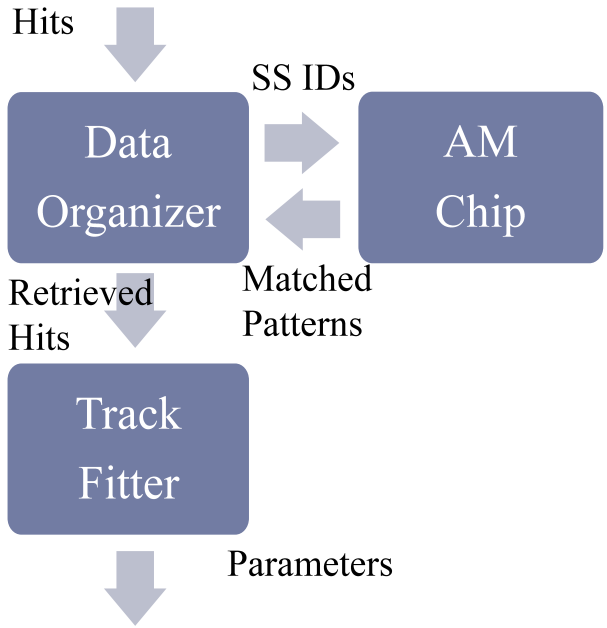
May 29, 2015

Outline

Outline

Testing goals

- Need to test the DO & TF architecture on the hardware
- Able to run many events (some thousands ideally)
- Also need to take runtime performance figures
- Keep testbench portable between simulation and hardware
- That way we can quickly debug any problems that may appear



Testing method

- Use IPBus for ethernet communication
  - fast transfers
  - already tested
- Use the on-board DDR3 memory instead of the proposed one
  - can correct for performance later, or
  - can remove the impact by using large FIFOs
- First test the firmware without the AMChips
  - One thing at a time, one less problem to worry about
- Use the systemverilog testbench for hardware verification
  - Use the IPBus runtime library via SystemVerilog DPI

Outline

Implementation

- Implemented a dual-port memory controller structure
  - can access the memory directly from IPBus
  - has a fast hardware port for firmware access to RAM
  - successfully tested on the FPGA board
- Implemented a firmware feeding the DO+TF
  - communication protocol with IPBus
  - buffering to remove transfer impact on performance
  - Complex firmware with many clock domains

Implementation

- Simulation times were long, ~1.5 hour for the first event
- Developed an external memory model and an IPBus bus functional model
- Simulation times still long but acceptable at ~20mins for the first event
- Later events come quicker, huge penalty for IPBus to initialize the memories

Progress

- Many problems encountered and solved in the process
  - Logic bugs in the test firmware
  - Logic bugs in the memory controller
  - Timing issues when putting it all together
- Some remain to be solved
  - IPBus race conditions on the testbench
  - Whatever presents itself next???

Summary

- A lot of work was needed, more than expected
- Seems to finally be coming to an end
- Strong test setup when finished