# LAR CALORIMETER PHASE II UPGRADE

F. Tartarelli Atlas Italia, Bologna

# LAr Phase II upgrades

- Electronics
  - Upgrade of LAr FE electronics ✓
  - Upgrade of Lar BE electronics ✓
- Hadronic End-cap cold electronics
  - No need to replace the cold electronics inside the EC cryostats ✗
  - Will replace the HEC Low-Voltage PS ✓
- Detector upgrades
  - Forward calorimetry: various options still open ?

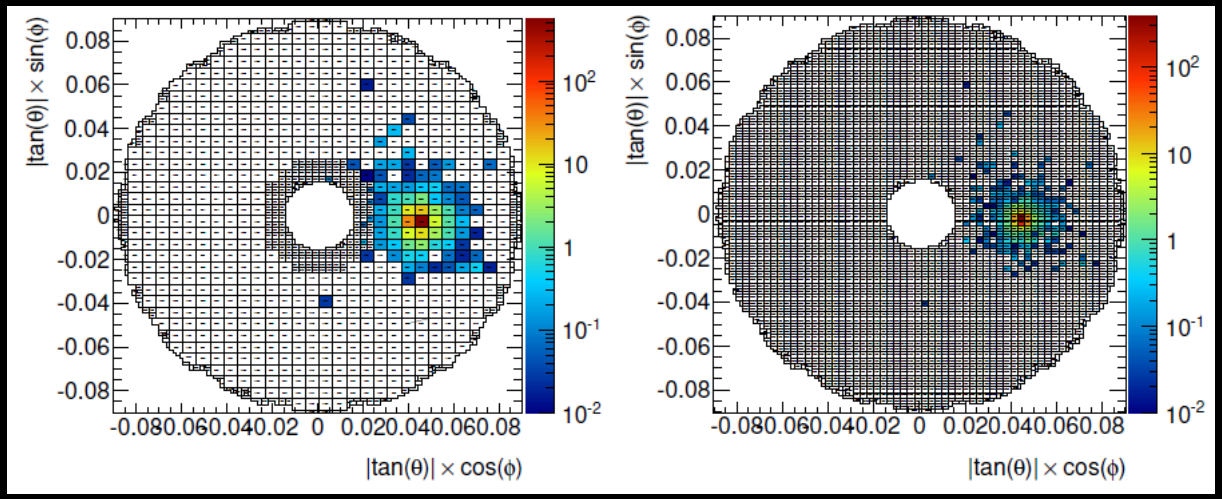
# Detector upgrades

- Problems with FCAL at high luminosity:
  - LAr may boil and produce bubbles (still under investigation)
  - Ion build up in LAr gap distorts the signal pulses
  - HV drop in protection resistors (1-2 MΩ) due to current increase
- Various option:
  - No change.
    - If boiling can be excluded.
    - FCAL heating simulation on-going; Mockup measurements available;
    - Situation not yet clear;
    - need also to assess with simulations the loss of performance
  - Mini FCAL
  - sFCAL

# sFCAL

- Replace FCAL with a new sFCAL with following characteristics:
  - Smaller gaps: 260 μm → ~100 μm
  - Addition of LN2 cooling loops
  - Replacements of motherboards to change HV resistors and remove all 4 → 1 channel sums (to increase the read-out granularity in first section FCAL1)
- Will cover with up to $|\eta|=4.9$ as today
- Best solution in terms of performance:
  - Good match with tracking at large eta
- Problems:
  - Need to empty, warm-up, open, the EC cryostat: detailed risk analysis in progress (risks for the detectors inside and the cryostat itself)
  - High radiation environment
  - Need to find space for new cabling and services
- Expensive:
  - This option is only in the high costing scenario

Current FCAL

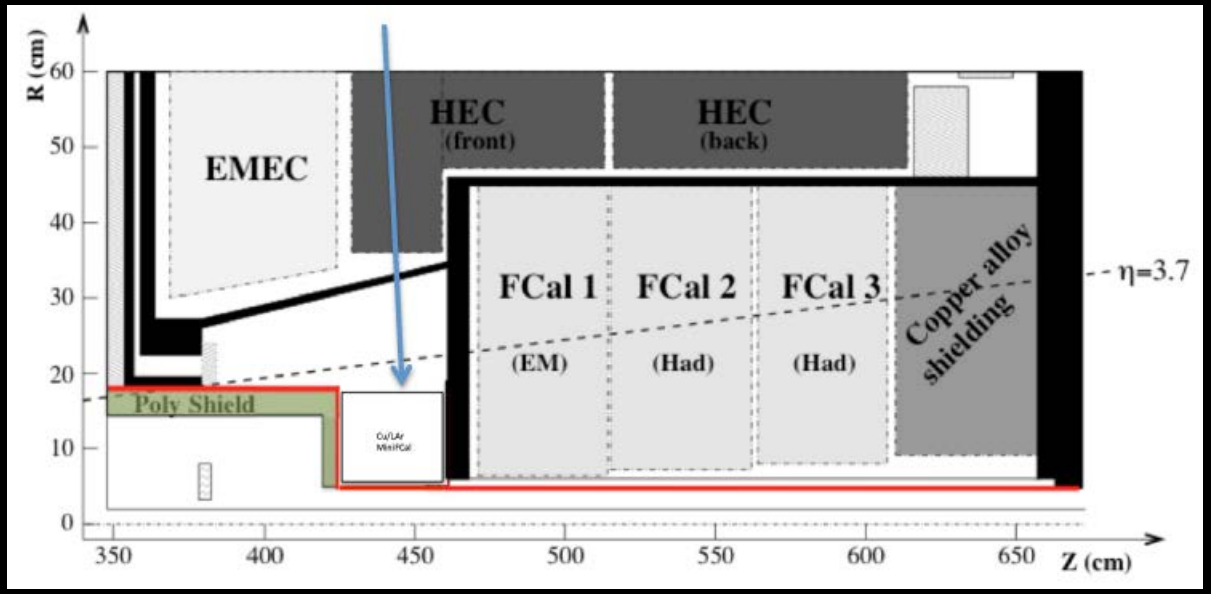


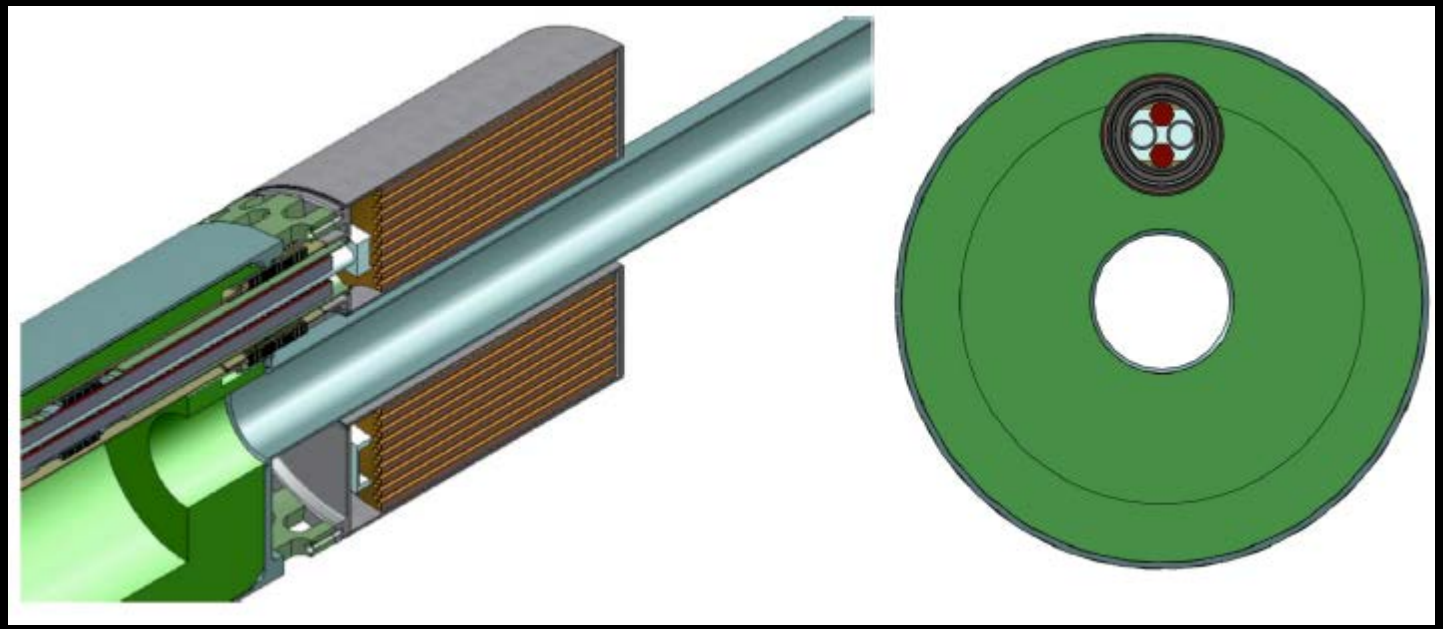

100 GeV electron simulation

# miniFCAL

- miniFCAL is a smaller FCAL located in a vacuum space in front of FCAL1 to reduce the flux on it:
  - preferred option if sFCal is not selected (risks, cost) and if energy density in FCal need to be reduced
- Baseline technology: Cu/LAr with 100 μm gaps
  - Alternative: (Diamond/Cu) or W/Si (*)
- No need to fully open the cryostat, only the warm cover:
  - Will have its own cryostat and supplies
- Main challenge is services (LAr, LN2 cooling loops, cabling). In current proposal these are delivered via an 80mm diameter conduit; this introduces a material asymmetry (in ϕ) in front of the device.
- Cu/Lar option for miniFCAL is relatively inexpensive
  - In low/normal cost scenario

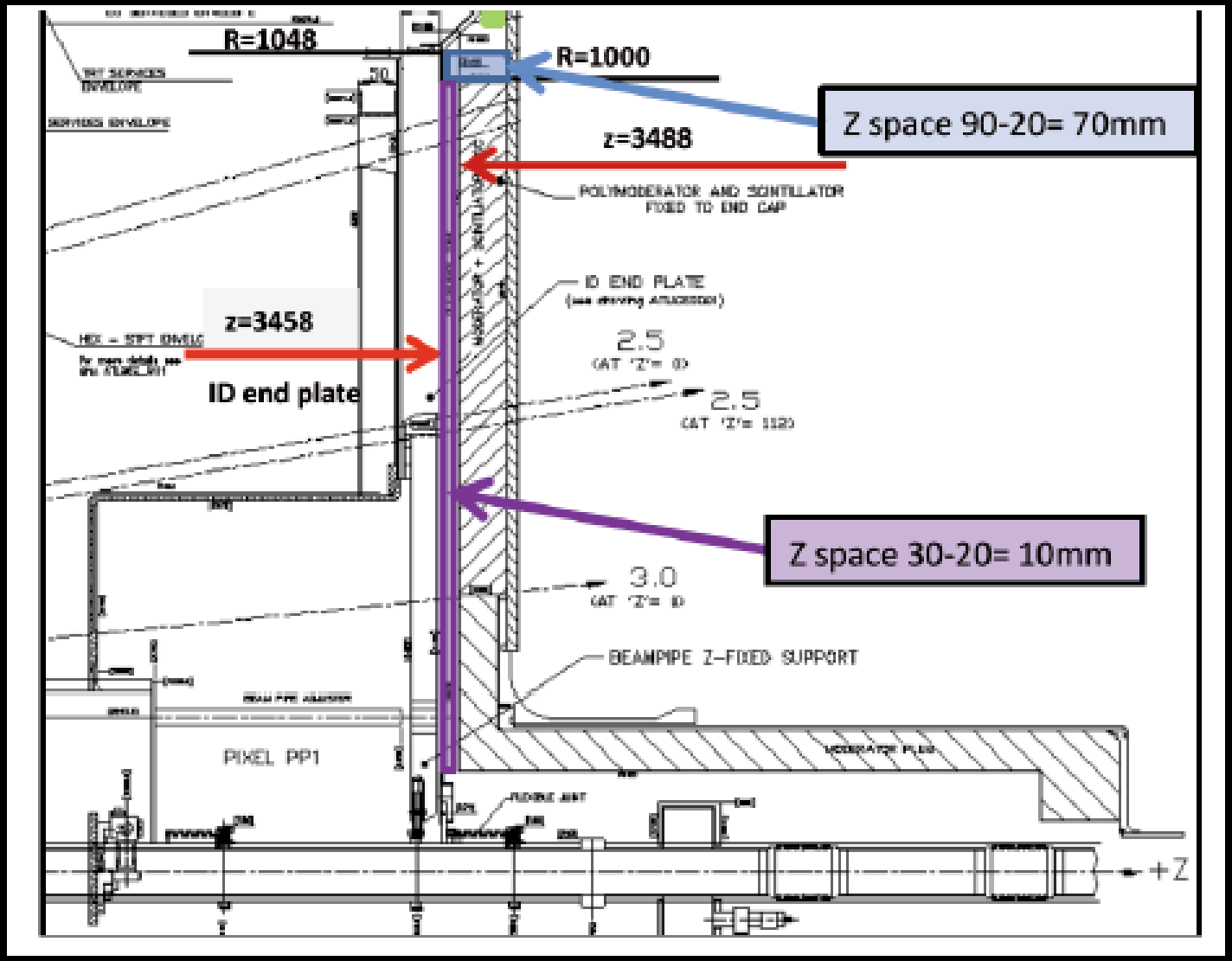
(*) see later


R (cm)
60
50
40
30
20
10
0
EMEC
HEC
(front)
HEC
(back)
FCal 1
(EM)
FCal 2
(Had)
FCal 3
(Had)
Copper alloy
shielding
η=3.7
Poly Shield
350
400
450
500
550
600
650
Z (cm)



# Si/W 4D Precision Timing Detector

- Besides the upgrade options already in the Phase II LOI (sFCAL, miniFCAL), more recently there has been a new proposal
- Precision Si/W timing detector in front of LAr endcap cryostat covering region $2.4 < \eta < 4$
  - in the region currently occupied by the MBTS
- High granularity + measurement of arrival time of charged particle tracks to assign them to different vertices
  - need ~10 ps timing resolution
- Might include an additional Si/W miniFCAL layer that would be located close to the front of the endcap cryostat, rather than directly in front of the FCal1
  - Same technology
  - Coverage extends to $|\eta|=4.9$
  - Possible disadvantage is the lever-arm between miniFCAL and the FCAL

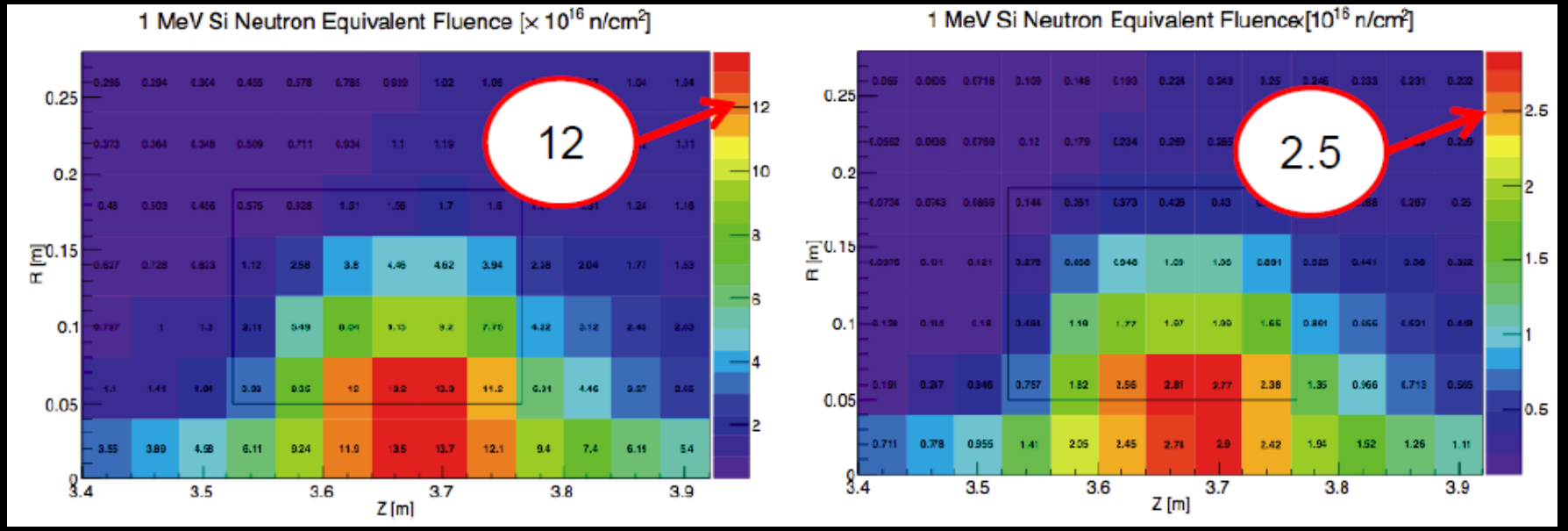

R=1048
R=1000
Z space 90-20= 70mm
z=3488
POLYMODERATOR AND SCINTILLATOR FIXED TO END CAP
ID END PLATE
z=3458
ID end plate
2.5
2.5
Z space 30-20= 10mm
3.0
BEAMPIPE Z-FIXED SUPPORT
PIXEL PP1
+Z

# Sensor technology

- Sensor technology still to be defined:
  - Estimation of neutron background is crucial
  - Candidates: LGAD (Low-Gain Avalanche Detector), HV-CMOS,…
- Only in the high cost category

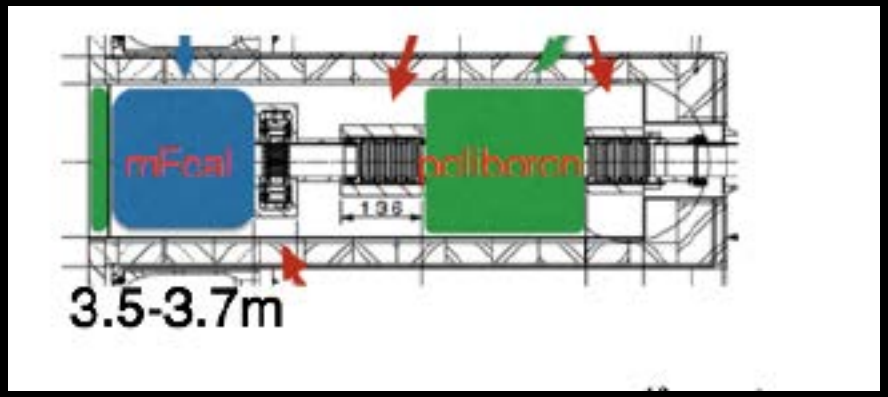
Table 3: Possible detector technologies to be deployed for a timing detector *(to be checked)*

| | Area | Resolution | | Noise | Efficiency | Max. Dose |
|---|---|---|---|---|---|---|
| | [mm$^2$] | Time [ps] | Space [$\mu$m] | [e$^-$ rms] | | [Mrad] |
| Hybrid pixel | 20×20 | 100 | 10 | 100 | 1 | 100 |
| Monolithic pixel (HVCMOS) | 0.05×0.05 | 100 | 10 | (?) | 1 | 1000 |
| LGAD | 1×1 | 10 | 10-50 | - | 1 | 100 |
| Poly-diamond strips | 5×5 | 100 | 10 | 2500 | 1 | 100 |
| Ion MCP | 200×200 | 30 | 10-100 | 100 | 1 | 100 |
| Fiber bundle | 1000×5 | 50 | | | | 10-100 |
| Photocathode MCP | 50×50 | 10 | 100 | | | 0.3 |




w/o poly-boron shielding

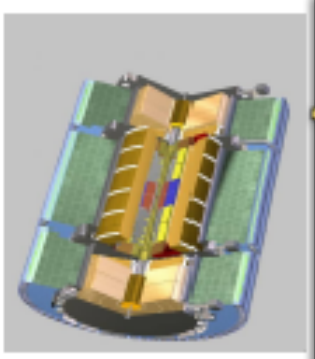
w poly-boron shielding



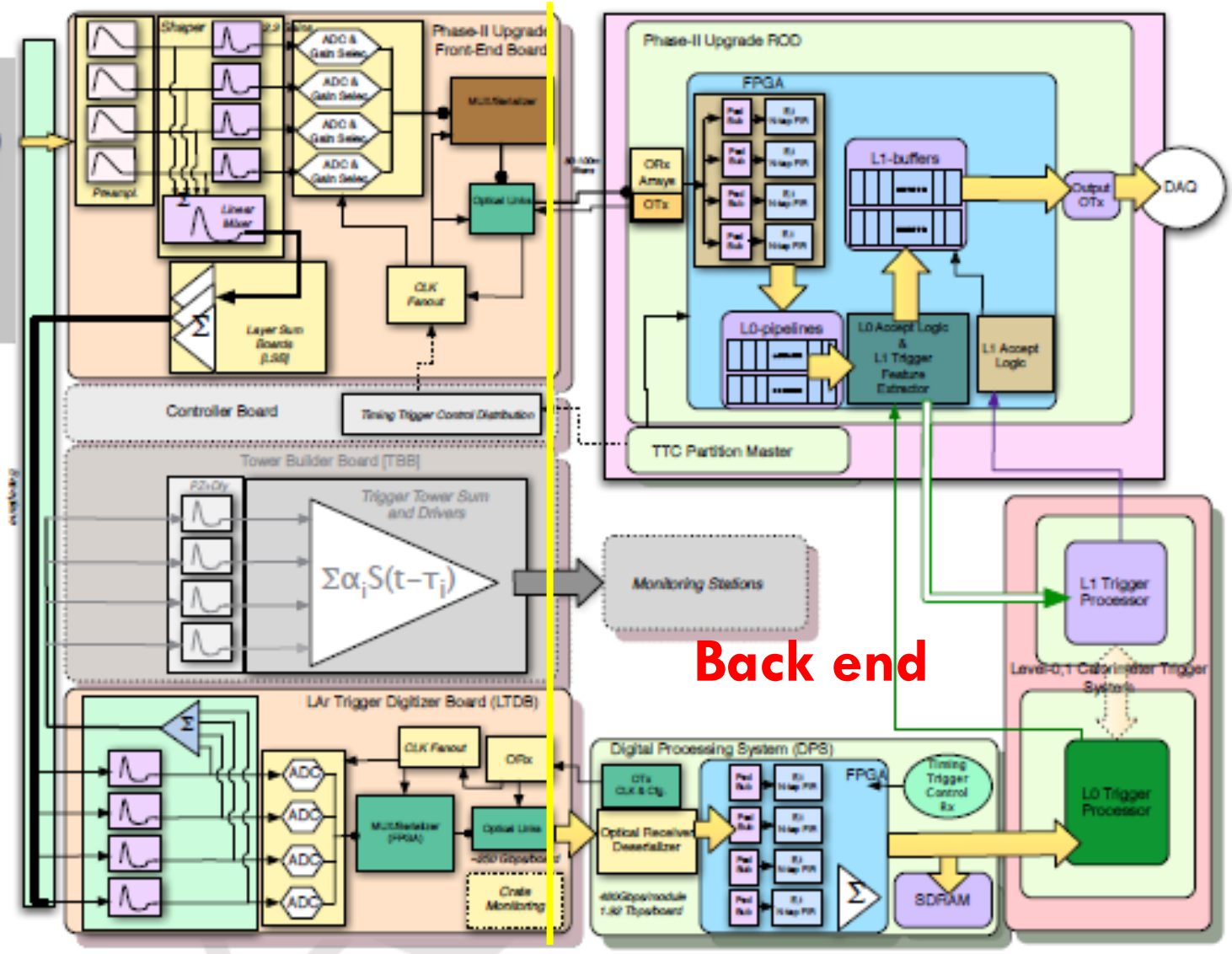
# Electronics upgrade

- LAr Front-End and Back-End electronics will need to be replaced:
  - New ATLAS trigger scheme in Phase II
  - Radiation tolerance
  - Ageing of components
- Goals for Phase-II readout upgrade:
  - fully digital 40 MHz readout → finest granularity trigger input at Level-1
  - low-power, radiation tolerant front-end electronics → simplify cooling and powering
  - re-optimize pulse-shapes, front-end gains and digitization for improved linearity and resolution

# LAr electronic upgrade



**Front end**



# Electronics Upgrade

- New Front-End Boards
- ASIC development of pre-amplifier, shaping, digitisation and serializer
  - Devices may be integrated into a single chip if same technology is chosen → reduced power consumption, simplified cooling system (air sufficient?)
- Optical link development in collaboration with CERN-wide lpGBT and VL+ projects
  - projected usable bandwidth of 8.96 Gb/s per fiber
  - Work on serializer and VCSEL driver in 65 nm technology and on coupling of VCSEL arrays to fiber ribbons
- Improved calibration system with single ASIC for pulser, DAC and digital logic

# Power distribution

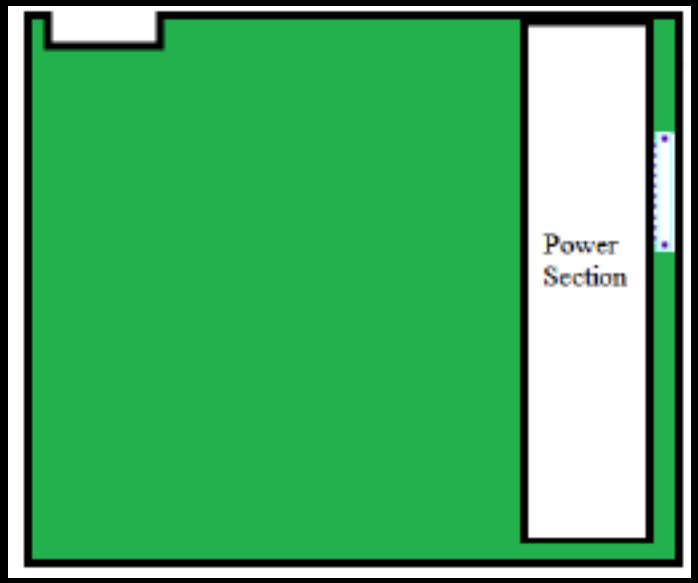
- We would like to design the power distribution scheme for the 1534 new Front-End Boards (FEB2) that will replace the existing FEBs
- This work includes:
  1. Design of the new Low-Voltage Power Supply mainframes
  2. Design of the power distribution part of the new FEBs
- Continuation/Extension of the work we are doing for the new Trigger Boards of Phase I:
  - For Phase I we are doing only 2., as the LVPS will remain the same ones we are using in RUN2

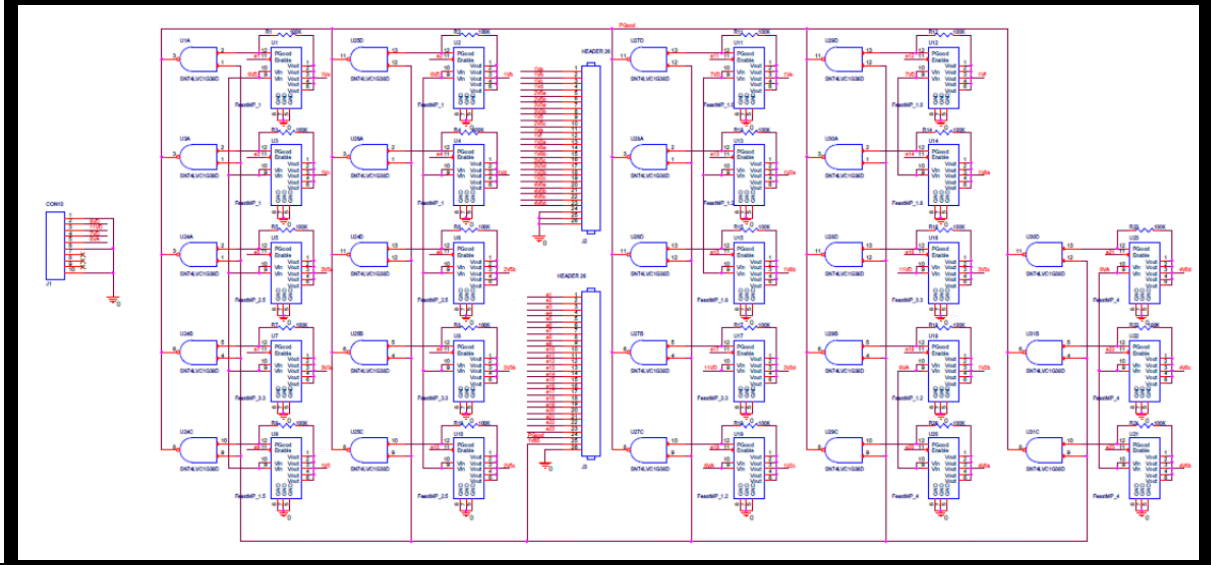
# New LVPS

- New LVPS:
  - Generate and distribute to the FEB2s one single voltage 12V or 24V (starting from 280V as of today)
  - Maybe an additional negative voltage will be needed
  - This compares to the 7 low voltages as of today
  - and produce on board the needed low voltages using POLs.
- Two options will be investigated
- Custom development:
  - eg, improve the design of the units produced by CAEN under old CSN5 APOLLO project (Si MOSFETs → GaN MOSFETs)
  - Still waiting for a prototype we ordered from CAEN
- Commercial solution:
  - Evaluate solutions already available on the market
  - "bare" units that will anyway need to be integrated with cooling, control,…
  - Some candidates identified

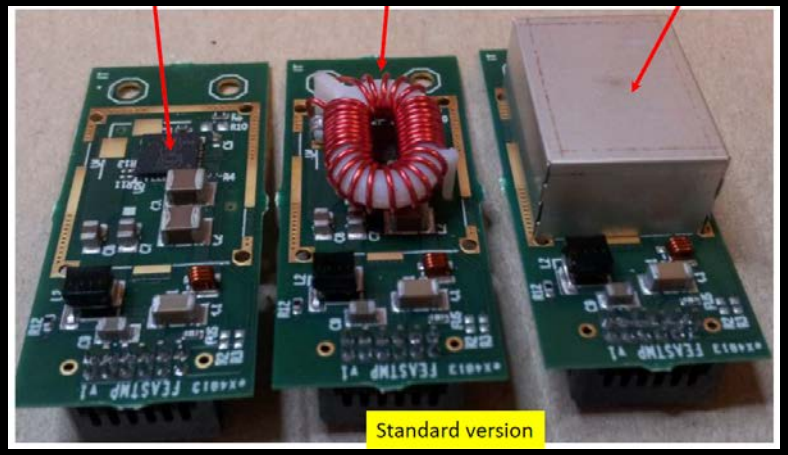
# Power distribution on board

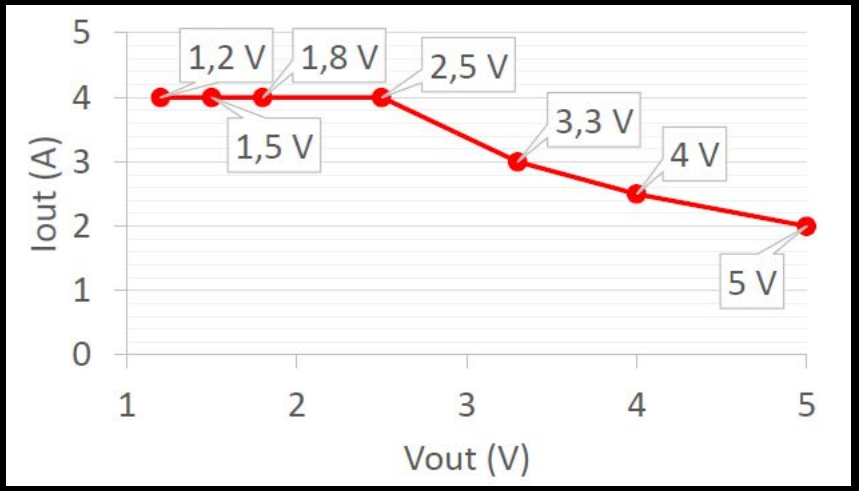
- As for Phase I, there are various aspects
  - Design of the section of the board devoted to powering
  - Choice and characterization of the components: POLs and LDO
- radiation tolerant point-of-load DC-DC converters with small form factor, high power and possibility to operate in magnetic field are needed

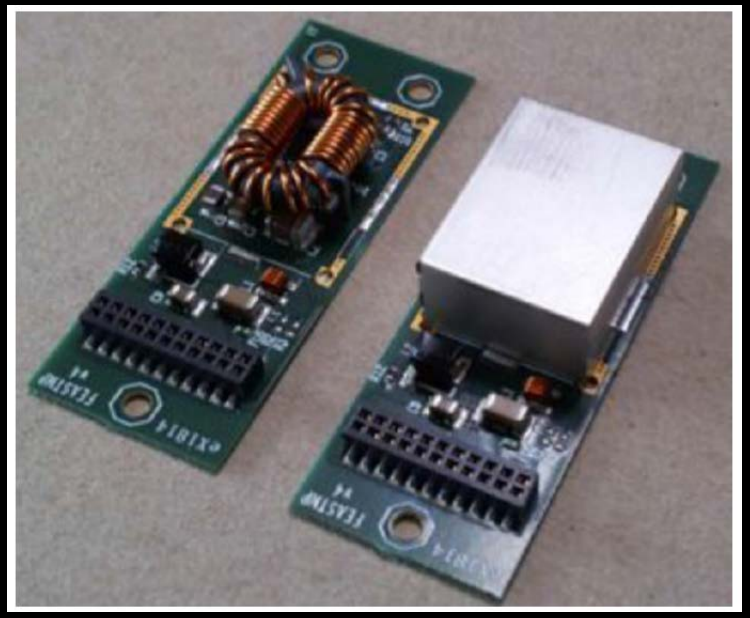


(LTDB Phase I)



Continuous 4A load capability (dependent on output power level, limited to 10W)

# LAr trigger

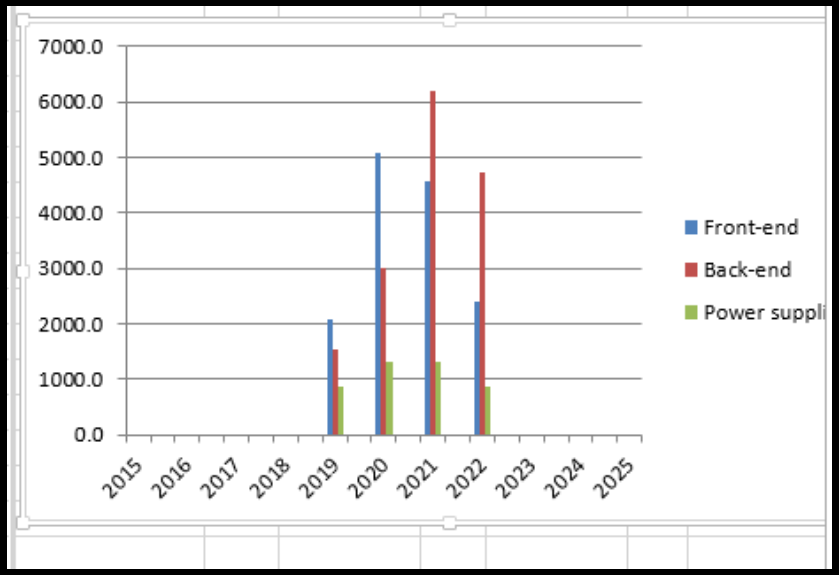
- The upgrade of the front-end electronics opens the door to the possibility of implementing more complex selection algorithms, similar to those now implemented in the offline or high-level trigger, already at lower trigger levels, possibly Level 1.
- We would like to pursue these goals:
  - studying new trigger algorithms
  - contributing to the design of the new trigger architecture
- Already performed some LAr trigger studies using a FPGA demonstrator board but to do more accurate studies we would like to assemble a more complex set-up
  - buy an ATCA crate and build a dedicated board to host sample FPGA (on a AMC mezzanine for more flexibility.)
  - We plan to acquire few FPGA and select the one more suitable for our implementation (based on number of gates, I/O and clock speed).
  - Need to build a board (ROD injector) that will simulate the input data flow.
- We want to:
  - study how to handle the expected data flow from the calorimeter
  - how to arrange and partition the data
  - Write algorithms to select EM clusters (or other objects) , using information from shower shapes, …
  - Perform detailed simulations to study the impact on selected physics channels

# Schedule

- Phase-II IDR and TDR can be aligned for LAr electronics and detector upgrade:
  - LAr Phase-II IDR 2016
  - LAr Phase-II TDR 2017
- Detector and electronics constructions planned to start in 2018/2019
- IDR/TDR for MiniFCal options and Si/W 4D detector can be further delayed, if needed, since construction time is expected to be shorter than for sFCal

# Cost

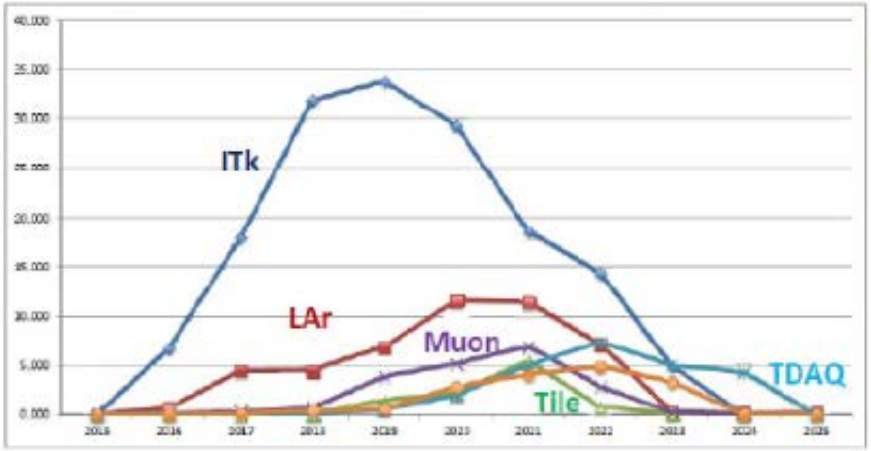
- In all cost scenarios:
  - New electronics: 34 MCHF
- High cost scenario: in addition
  - Hi-granularity FCAL: 11 MCHF
  - Si/W timing detector: 4 MCHF
  - (+miniFCAL Si/W: 3MCHF)
- Medium/Low cost scenario:
  - miniFCAL Cu/Lar: 700 kCHF

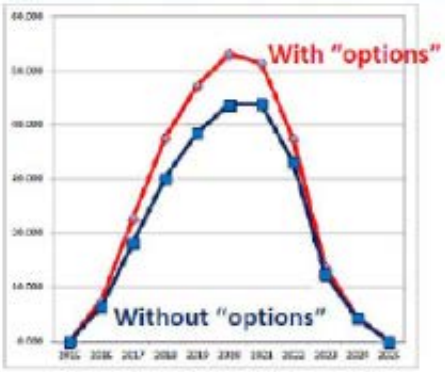



- (Approx numbers, no tooling,...)

# Backup

# Reminder – Phase II Cost Estimates LOI




Phase-II Scoping

Aim to have first discussion with numbers at USC on 11/12/14

| | LoI Numbers Repeated for Information | | | | New Numbers, Will need to Expand Table for Multiple Options per Project | | | |
|---|---|---|---|---|---|---|---|---|
| LoI Project Title | LoI Cost Without Options | LoI Options | LoI Cost Plus Options | (old sum) | Revised Base Cost | Comments | Current Options | Current Options Estima |
| ITk | 131.500 | 5th layer strip-> pixel | 26.000 | 157.500 | | | | |
| LAr | 32.124 | sFCAL + HEC | 15.096 | 47.220 | | | | |
| Tile | 7.483 | FE boards + HVPS | 2.517 | 10.000 | | | | |
| Muon | 19.632 | BW TGCs | 0.500 | 20.132 | | | | |
| TDAQ | 23.315 | MDT Trigger | 0.900 | 24.215 | | | | |
| Infrastructure | 16.280 | | 0.000 | 16.280 | | | | |
| | 0.000 | | 0.000 | 0.000 | | | | |
| | 0.000 | | 0.000 | 0.000 | | | AFP Phase-II | |
| | | | | | | | Other | |
| SUM | 230.334 | | 45.013 | 275.347 | | | | |

Slide from P. Allport

## LAr PHASE II upgrade (LS3)

12/12/2015

| | | it will happen [MCHF] | it might happen [MCHF] | 2015 [MCHF] | 2016 [MCHF] | 2017 [MCHF] | 2018 [MCHF] | 2019 [MCHF] | 2020 [MCHF] | 2021 [MCHF] | 2022 [MCHF] | total [MCHF] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | ***LAr electronics*** | | | | | | | | | | | |
| 1 | ***HV supplies for FCAL*** | 0.080 | | | | 0.004 | | 0.004 | 0.048 | 0.024 | | 0.080 |
| | ***Low Voltage power supplies*** | | | | | | | | | | | |
| 2 | LVPS | 3.184 | | | | 0.159 | | 0.159 | 1.910 | 0.955 | | 3.184 |
| 3 | DC-DC Point of Load Regulators | 2.122 | | | | 0.106 | | 0.106 | 1.273 | 0.637 | | 2.122 |
| 4 | LVPS for HEC front-end | 0.478 | | | | 0.024 | | 0.024 | 0.287 | 0.143 | | 0.478 |
| 5 | Cabling, monitoring, testing | 0.424 | | | | 0.021 | | 0.021 | 0.254 | 0.127 | | 0.424 |
| | ***Calibration system*** | | | | | | | | | | | |
| 6 | EM and FCAL | 1.698 | | | | 0.085 | | 0.085 | 1.019 | 0.509 | | 1.698 |
| 7 | HEC | 0.212 | | | | 0.011 | | 0.011 | 0.127 | 0.064 | | 0.212 |
| | ***FE ASIC and components*** | | | | | | | | | | | |
| 8 | R&D and prototypes | 0.467 | | 0.047 | 0.420 | | | | | | | 0.467 |
| 9 | ASIC Production | 4.130 | | | | | 0.083 | 2.808 | 1.239 | | | 4.130 |
| 10 | Other components | 0.424 | | | | | 0.008 | 0.288 | 0.127 | | | 0.424 |
| 11 | Tests | 0.085 | | | | | 0.002 | 0.058 | 0.026 | | | 0.085 |
| | ***FE boards*** | | | | | | | | | | | |
| 12 | Prototypes and tests | 0.438 | | 0.219 | 0.219 | | | | | | | 0.438 |
| 13 | Materials | 3.608 | | | | 0.180 | | 0.180 | 2.165 | 1.082 | | 3.608 |
| 14 | Assembly | 1.910 | | | | 0.096 | | 0.096 | 1.146 | 0.573 | | 1.910 |
| | ***Back end electronics*** | | | | | | | | | | | |
| 15 | Links from FEB-2 to ROD-2 | 2.335 | | | | 0.117 | | 0.117 | 1.401 | 0.701 | | 2.335 |
| 16 | Prototypes | 2.122 | | | | 0.212 | 1.910 | | | | | 2.122 |
| 17 | Crates, PS and CPU | 0.409 | | | | | | 0.041 | 0.245 | 0.123 | | 0.409 |
| 18 | TTC/Controllers | 0.123 | | | | | | 0.012 | 0.074 | 0.037 | | 0.123 |
| 19 | Transition Modules | 0.344 | | | | | | 0.034 | 0.206 | 0.103 | | 0.344 |
| 20 | Pre-Processor boards (ROD-2) production and testing | 4.401 | | | | | | 0.440 | 2.641 | 1.320 | | 4.401 |
| 21 | ***DCS and Monitoring*** | 0.212 | | | | | | 0.021 | 0.127 | 0.064 | | 0.212 |
| 22 | ***Irradiations*** | 0.265 | | 0.027 | 0.239 | | | | | | | 0.265 |
| 23 | ***System Tests and testbeams*** | 2.547 | | 0.255 | 2.292 | | | | | | | 2.547 |
| 24 | ***Logistic (Infrastructure, shipment)*** | 0.106 | | | | | | 0.011 | 0.064 | 0.032 | | 0.106 |
| | ***HEC PAS*** | | 2.3 | | | | | | | | | |
| | ***sFCAL*** | | 8.5 | | | | | | | | | |
| | ***Cryostat opening/closing*** | | 3.8 | | | | | | | | | |
| | TOTAL | **32.124** | **14.600** | 0.547 | 3.170 | 1.015 | 2.003 | 4.517 | 14.379 | 6.494 | 0.000 | **32.124** |