SVT organization for TDR

1. Major decisions needed and R&D required to make them.
   - **Layer 0 technology:**
     - **Hybrid Pixel:** Want to demonstrate that reduction in the front-end pitch to 50x50 μm² and in the total material budget is possible to meet Layer0 requirements. Working on a plan to test this option with beam Sep. 2010.
     - **CMOS MAPS:** Plan to build a multichip CMOS MAPS prototype module with specs close to the SuperB Layer0 requirements → Testbeam in 2010.
     - All the module components could be the same for a Layer0 module based on MAPS/Hybrid Pixels
     - **Striplets:** evaluate real limit of FSSR2 speed with high background.

2. Manpower in place and still required
   - Still Working on a better estimate of manpower for TDR
   - Old estimate: Phy~6 FTE (~4 avail.), Mech Eng.~ 4 FTE (< 2 avail.), Electr. Eng. ~ 6 FTE (<4 avail.)
   - Layer0 activities somehow covered
   - External layer design: interest from some groups but lack of manpower and activities not yet started (no real commitments yet).
   - Mechanics: long list of activities but < 2 FTE involved
3. Milestones (very preliminary)

- **May '09**: finalize readout architecture for MAPS & Hybrid pixel front-end chips
- **Sept-Nov '09** chips submission
- **Sept '09** high resistivity pixel sensor production
- **Jan - July 2010**: lab test (sensor/front-end chip/MAPS) → bump bonding hybrid pixel / MAPS module assembly → lab test
- **Sep 2010**: testbeam

### Status of WBS planning

- Major activities defined
- Need to fill in manpower
- Iteration with Institutions
SVT Activities for TDR (I)

Activities now more focused on TDR preparation (end of 2010)
Some R&D still needed for Layer 0:

- Plan to build a multichip CMOS MAPS prototype module with specs close to the SuperB Layer0 requirements → Testbeam in 2010.
  - All the module components could be the same for a Layer0 module based on Hybrid Pixels.

• Activity funded by INFN. Institutions: Bologna, Milano, Pavia/Bergamo, Pisa, Roma III, Torino, Trieste.

• Hybrid Pixel: more emphasis now on this option; it could become the baseline Layer0 option for the TDR in case MAPS are not considered mature enough by that time.
  - Need to demonstrate by 2010 that reduction in the front-end pitch to 50x50 μm² and in the total material budget is possible to meet Layer0 requirements.

• Striplets: continue to evaluate the use of FSSR2 readout chip and light interconnections from sensor to front-end
SVT Activities for TDR (II)

Background Simulation:
- This set the scale for requirements on Layer0 and the inner SVT Layers.

External Layers Design
- Technology is not an issue
- Need to optimize the geometry with Fast Simulation (D. Brown’s talk)
- Need to evaluate the best front-end chip for strip modules among the ones “on the market” (FSSR2...)

Off Detector electronics and DAQ Development
- (M. Citterio, M. Villa’s talk)

Mechanics:
- Beam-pipe design
- Light support and cooling for Layer0 modules (F.Bosi’s talk)
- Module design for the external Layers
- Design the full SVT support structure (want to have the Layer0 easily accessible for replacement). Important interplay with IR design.

- A significant amount of work is needed for the TDR and not all listed activities are well covered.