Super Nemo Absolute Time Stamper

A high resolution and large dynamic range time stamper chip

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Time measurements

**Time stamper vs TDC**

- TDC: time measured between a Start & a Stop
- Time Stamper: absolute time measurement

**SuperNemo experiment:** 2 events will be stamped \( \Rightarrow \Delta t = t_2 - t_1 \)

\[ \sigma_t = \sigma \sqrt{2} \]

\( \Delta t = t_2 - t_1 \)
Requirements for SuperNemo Calorimeter Time Measurements:

- time resolution < 100ps RMS

Requirements for SNATS:

- SNATS résolution ≅ time résolution / \sqrt{2} ≅ 70ps RMS

- LSB ≅ 250ps
Contraints of Super Nemo Absolute Time Stamper Chip

SNATS: parameters definition

LSB $< 250$ps

- AMS CMOS 0.35$\mu$m: typ cell delay around 200ps
- For a minimum INL: Max number of cell in a DLL = 32

☞ Clock frequency needed: 160 MHz

Provided by the board through commercial PLLs
SNATS Chip specifications:

- Technology Process: AMS CMOS 0.35µm
- Clock Frequency: 160MHz
- Number of cells: 32
- Dynamic Range: 53 bits
  - 48 clock counter bits
  - 5 interpolator bits
  - Time coverage: 20 days
- LSB = 250ps
- DNL < 10%
- Channels per chip = 16
Association of a counter and an interpolator:

**Fine Time Measurement** → high resolution

**Coarse Time Measurement** → dynamic range
Architecture of Super Nemo Absolute Time Stamper

SNATS Chip principle:

SNATS Chip (Super Nemo Absolute Time Stamper)

Delay Locked Loop

Master Clock @\( F_\text{in} \)

Hit

\( C_0 \) \( C \)

\( \text{CLK} \) \( \text{RESET} \)

Coarse Time Counter: \( N \) bits

Coarse Time Memory

Fine Time Decoder: \( N \) bits

Time measurement: \( N+Q \) bits

Phase Detector

Voltage controlled delay line: \( M \) cells

Q0-Q15

Q16-Q31

Q32-Q47

\( \text{Chain4} \)

\( \text{Chain8} \)

Tronçon 4 bits

Tronçon 4 bits

Tronçon 4 bits

16

16

16
SNATS Chip challenges:

- To ensure a delay in each DLL cell lower than 200ps

  Dealing with temperature variations
  Process & mismatch variations

- To make an easy and reliable matching between fine and coarse time

  Improvement of architecture
**Super Nemo Absolute Time Stamper Challenges**

Phase error < 20ps

- Delay Locked Loop
- Master Clock
- V. delay1
- V. delay2
- Phase Tuning
- delay line: 32 cells
- Phase Detector
- Charge Pump & Buffer
- V_pump
D.L.L delay cell:

- structure optimized:
  1 starved inverter + 1 inverter followed by 1 buffer + 3 buffers
Minimum delay cell:

- $\approx 150$ ps at $27^\circ C$
- $\approx 166$ ps at $60^\circ C$

Montecarlo « Process & Mismatch »

![Histogram at 27°C](image.png)
SNATS : Matching of fine time and coarse time

DLL and counter are synchronous but not in phase

<table>
<thead>
<tr>
<th>Counter</th>
<th>N-1</th>
<th>N</th>
<th>N+1</th>
</tr>
</thead>
<tbody>
<tr>
<td>DLL</td>
<td>0</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>1</td>
<td>0</td>
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<tr>
<td></td>
<td>1</td>
<td>2</td>
<td></td>
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<tr>
<td></td>
<td></td>
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<td>3</td>
</tr>
</tbody>
</table>

DLL code : 0
Counter code : N instead of N+1

1 clock period error
SNATS: Matching of fine time and coarse time

Generally: 2 shift phase counters

Drawbacks:
- → silicon area (2 compteurs + multiplexeur)
- → power consumption
**Principle:** production of a hit which latches the coarse time register depending on the state of latch fine time register
SNATS : Matching of fine time and coarse time

Synchronizer correction:

CLK

Counter

N-1 N N+1

DLL

0 1 2 3 0 1 2 3 1 0 1 2 3

Status_dll

Hit

Hit_dll

Hit_counter

DLL Code : 0
Counter code : N+1

Code corrected!
SNATS Topology

- 48 registers
- 5 bit encoder
- 32 registers + 1
- DLL
- 48bit Gray counter
- Syncrho
- Inhibit
- Data/Hit

9 D.L.L's : 8 for 16 TDC channels and 1 for test
SNATS Topology

- **Master Clock: LVDS**
- **Inputs:** unipolar signals from analog front end circuit with adjustable amplitude
  - One comparator on each input sharing a common external reference.
- **Outputs:** CMOS 3.3V level compatible with FPGAs
SNATS: layout & package

Size: 4467 µm X 2853 µm

Package: CQFP100
SNATS : test boards

test-board for fine tests

test-board for yield tests
SNATS : Measurements

Differential Non Linearity : ± 0.2LSB
Integral Non Linearity : ± 1.3LSB

Resolution : $\sigma = 71$ ps ... Requirement=70ps!
SNATS : Measurements

DNL for a differential time measurement : ± 0.024 LSB

INL for a differential time measurement : ± 1.98 LSB

Resolution for a differential time measurement : \( \sigma = 109 \) ps

Resolution for a differential time measurement : \( \sigma = 109 \) ps
SNATS : Measurements

Summary

• Power:
  – 10mA / DLL + 35mA (LVDS receivers + counter + registers..)
  ⇒ P= 380 mW for 16 channels

• DNL: ± 0.2LSB

• Differential DNL: ± 0.024LSB

• INL: ± 1.3LSB

• Differential INL: ± 1.98LSB
THE END