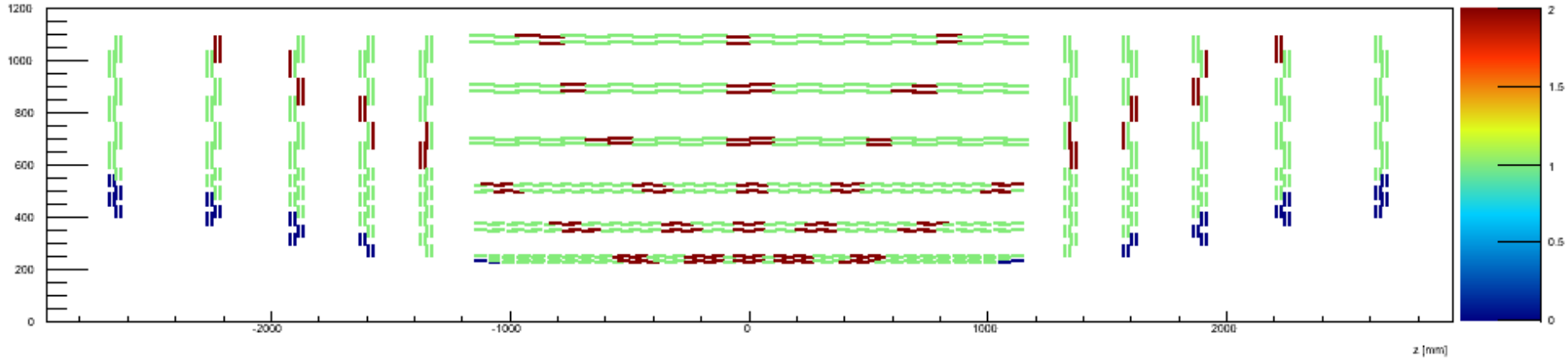
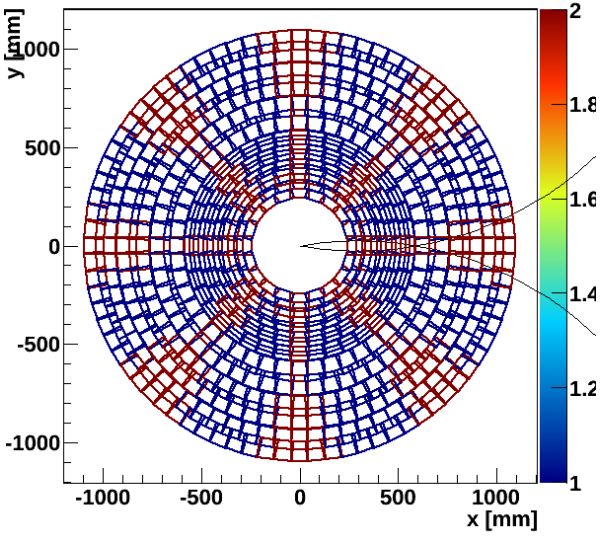
Data formatting for DO tests

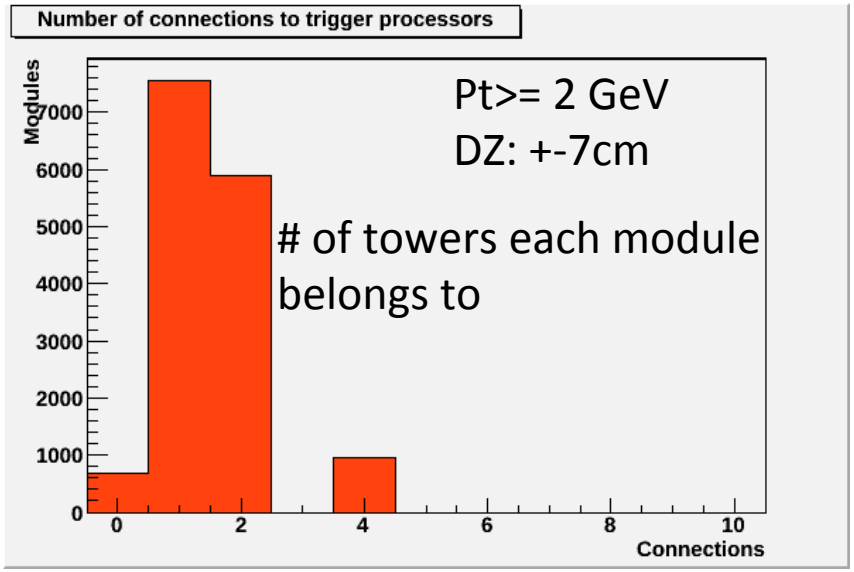
Giacomo Fedi

Baseline Trigger Tower: 6 in eta x 8 in phi

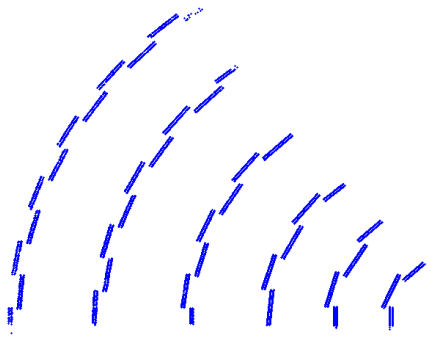
~ 15K modules/fibers over 48 trigger towerrs, → ~ 320 modules(modules) per trigger tower



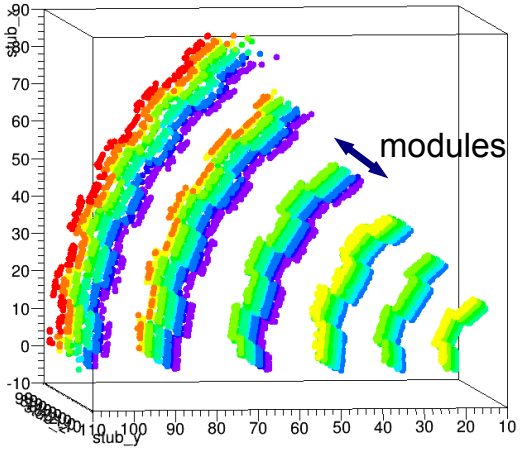


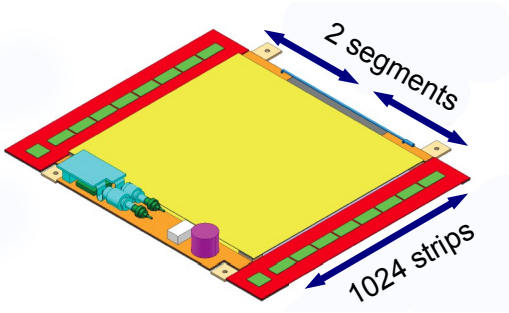


→ Encoding of a pattern

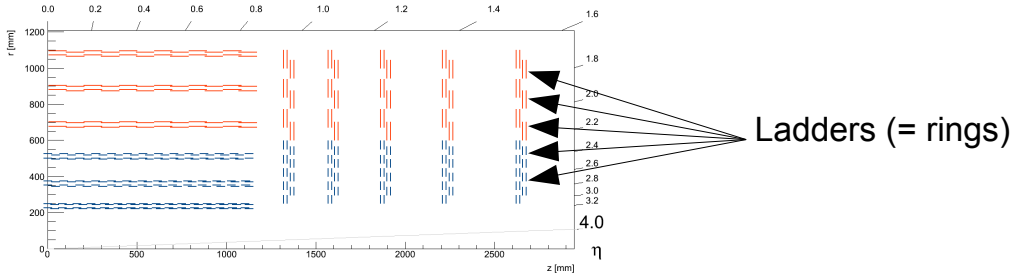


Superstrips in barrel sectors





Superstrips in endcap sectors



Formatting CBC stub data

- PRBF0 - 32 bits

SOF	SOF	SOF	SOF	BX	BX	BX	BX	BX	BX	BX	BX	BX	BX	BX	BX
T	T	T	T	FE	FE	FE	FE	FE	FE	FE	CLR	CHIP	CHIP	CHIP	S
S	S	S	S	S	S	S	B	B	B	B	B	rsvd	rsvd	rsvd	rsvd
T	T	T	T	FE	FE	FE	FE	FE	FE	FE	CLR	CHIP	CHIP	CHIP	S
S	S	S	S	S	S	S	B	B	B	B	B	rsvd	rsvd	rsvd	rsvd
T	T	T	T	FE	FE	FE	FE	FE	FE	FE	CLR	CHIP	CHIP	CHIP	S
S	S	S	S	S	S	S	B	B	B	B	B	rsvd	rsvd	rsvd	rsvd
EOF	EOF	EOF	EOF	nSt	nSt	nSt	nSt	nSt	nSt	nSt	nSt	nSt	nSt	nSt	nSt

- PRBF1 - 32 bits

SOF	SOF	SOF	SOF	BX	BX	BX	BX	BX	BX	BX	BX	BX	BX	BX	BX
T	T	T	T	DTC	DTC	DTC	DTC	FE	FE	FE	FE	FE	FE	FE	CLR
CHIP	CHIP	CHIP	S	S	S	S	S	S	S	S	B	B	B	B	B
T	T	T	T	DTC	DTC	DTC	DTC	FE	FE	FE	FE	FE	FE	FE	CLR
CHIP	CHIP	CHIP	S	S	S	S	S	S	S	S	B	B	B	B	B
T	T	T	T	DTC	DTC	DTC	DTC	FE	FE	FE	FE	FE	FE	FE	CLR
CHIP	CHIP	CHIP	S	S	S	S	S	S	S	S	B	B	B	B	B
EOF	EOF	EOF	EOF	nSt	nSt	nSt	nSt	nSt	nSt	nSt	nSt	nSt	nSt	nSt	nSt

- PRBF2 - 40 bits

SOF	SOF	SOF	SOF	BX	BX	BX	BX	BX	BX	BX	BX	BX	BX	BX	BX
T	T	T	T	PRB	PRB	PRB	PRB	DTC	DTC	DTC	DTC	FE	FE	FE	FE
FE	FE	FE	CLR	CHIP	CHIP	CHIP	S	S	S	S	S	S	S	S	B
B	B	B	B	rsvd	rsvd	rsvd	rsvd								
T	T	T	T	PRB	PRB	PRB	PRB	DTC	DTC	DTC	DTC	FE	FE	FE	FE
FE	FE	FE	CLR	CHIP	CHIP	CHIP	S	S	S	S	S	S	S	S	B
B	B	B	B	rsvd	rsvd	rsvd	rsvd								
EOF	EOF	EOF	EOF	nSt	nSt	nSt	nSt	nSt	nSt	nSt	nSt	nSt	nSt	nSt	nSt

Info from the CIC

- Stub Address
- Stub Bend
- Chip ID
- CLR: left or right

Info to add

- T: type of chip
- FE: Module ID
- DTC: Front end ID
- PRB: Pulsar ID

Current (hit) superstrip and bank format

- Developed for study purposes, but for the moment is ok

SS (hit) 16 bit:

Bank hit 18 bit:

M: module

L: ladder

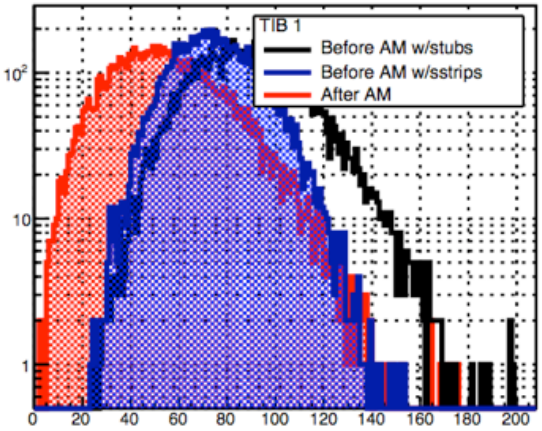
Z: Z position

S: strip

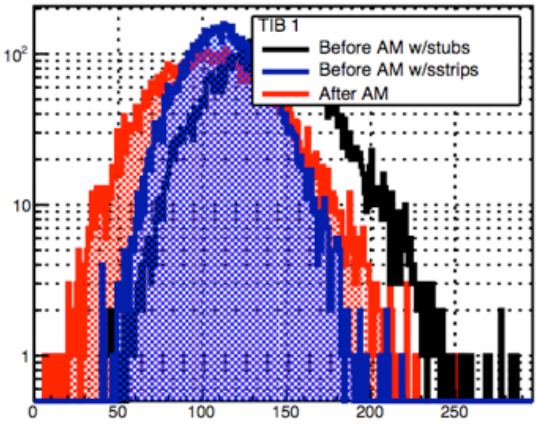
Don't care logic:

S	DC1	DC0
Don't care	0	0
0	0	1
1	1	0
Never active	1	1

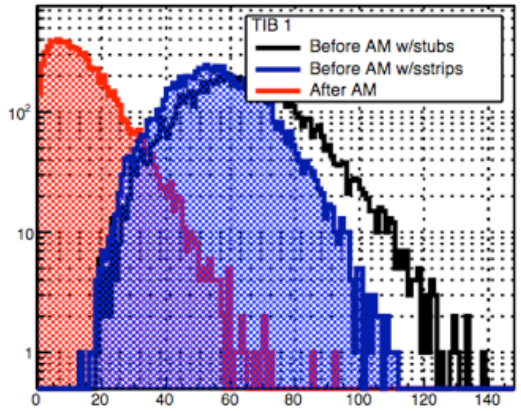
Requirements for the AM2020 chip



PU140 - 2 GeV



PU200 - 2 GeV



PU140 - 3 GeV

Option to increase the thresholds save ~30%