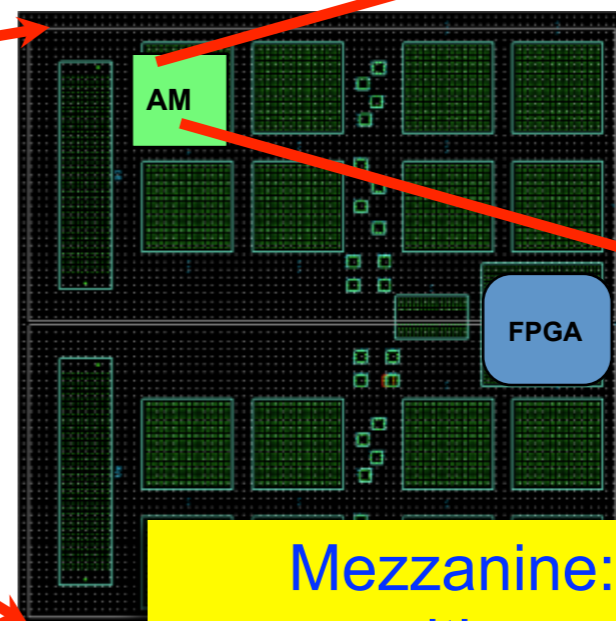
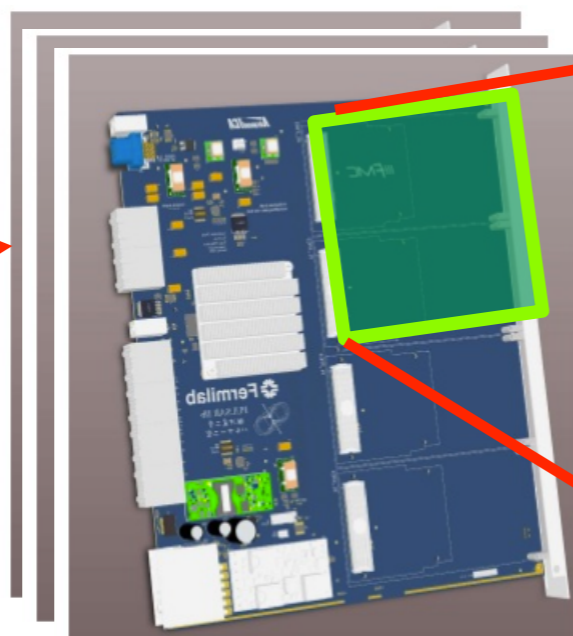


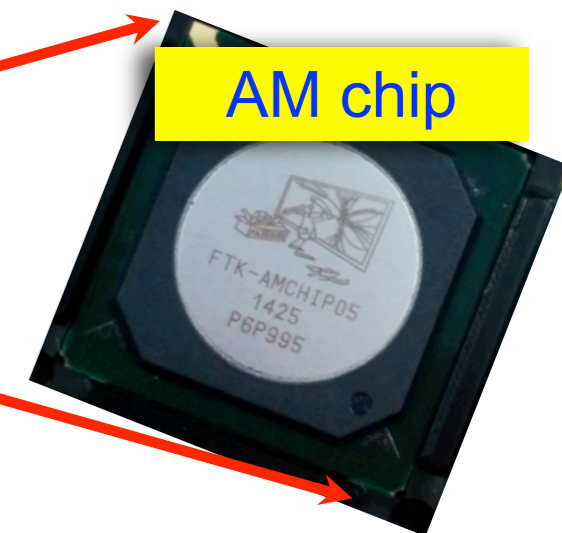
few hundred stubs/sector
up to 600 Gb/s



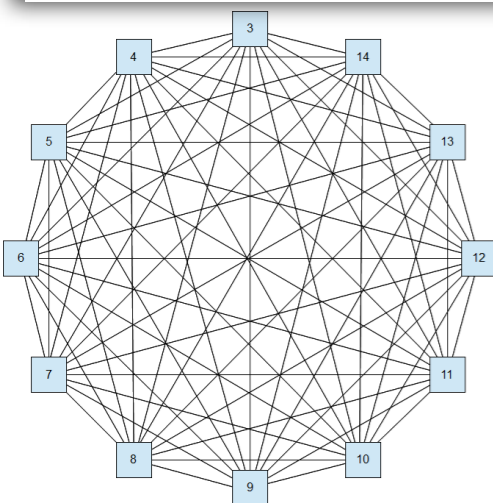
40-100 G full mesh ATCA shelf



Mezzanine: pattern recognition and track fit

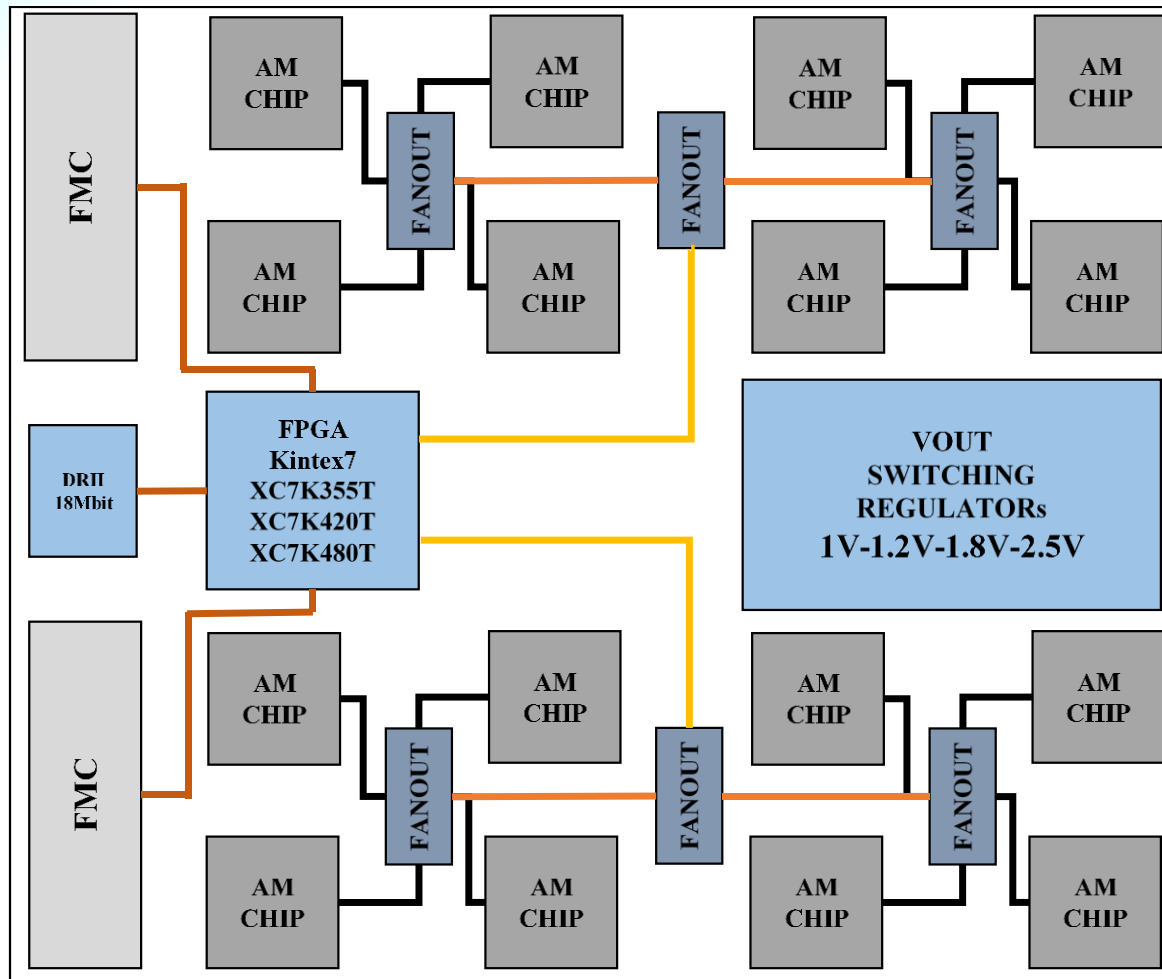


AM chip



- Send data to PRM in each ATCA shelf
 - Data distributed to Pulsar boards in time multiplexed mode
 - Perform pattern recognition using AM chips
 - Track fit with FPGA (PCA, Hough transform, Retina etc)

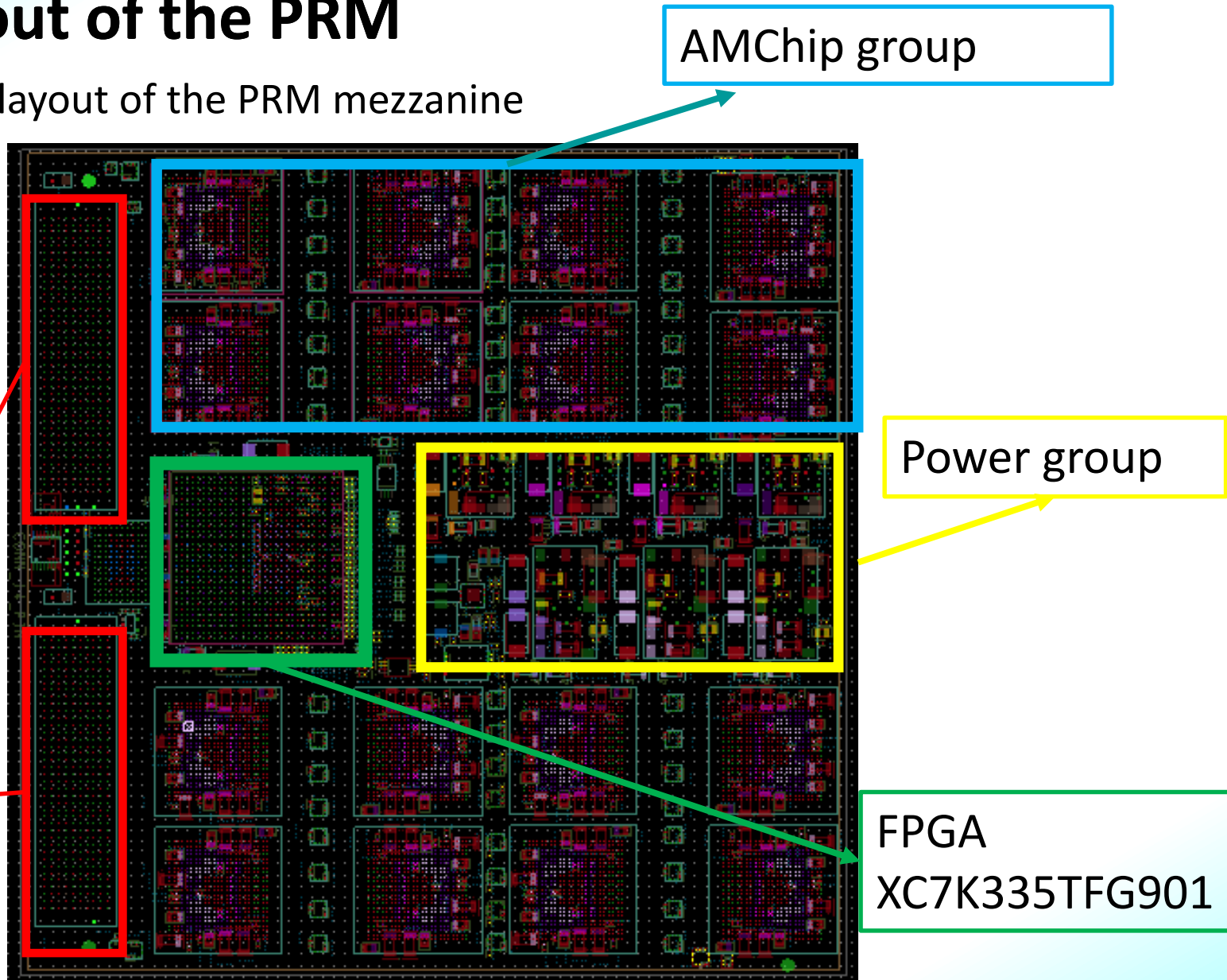
The architecture of PRM

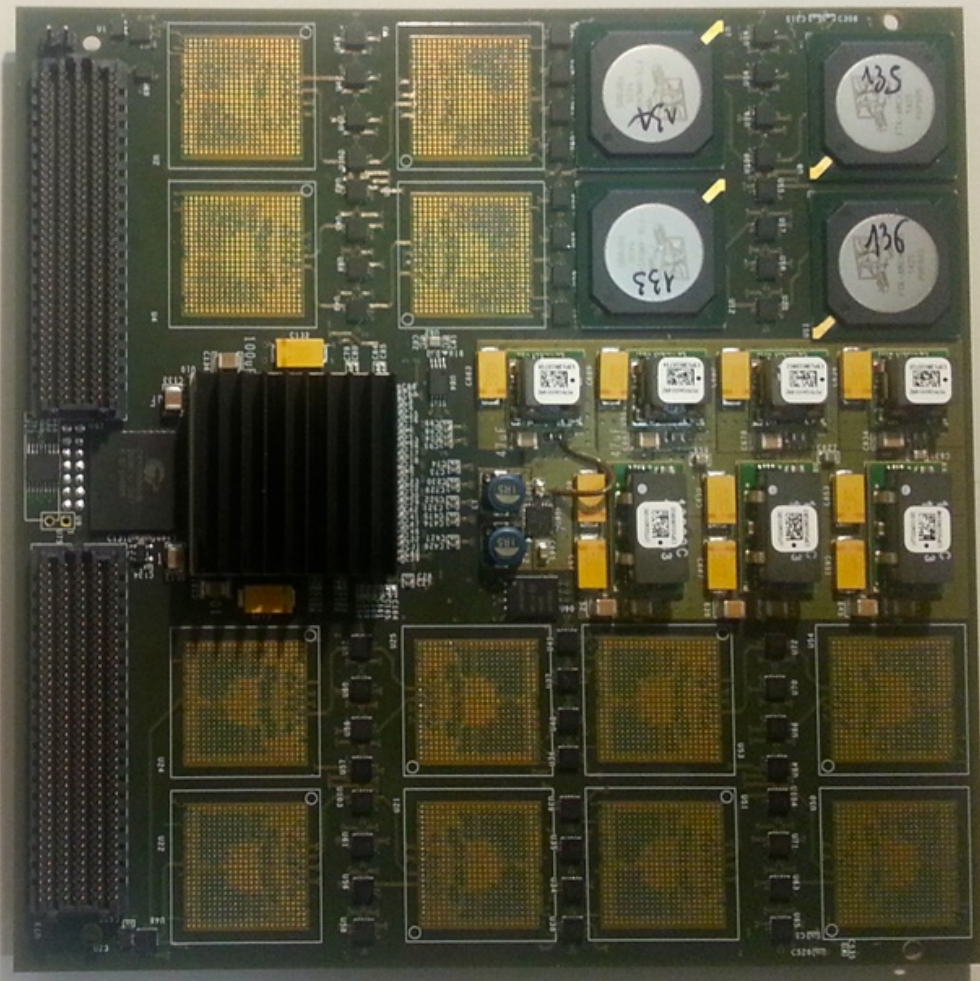


- Double FMC mezzanine 14.9x14.9 cm²
- Kintex-7 FPGA
- FMC compatible with Pulsar IIB & satisfy the Vita 57.1 standard
- I/O bandwidth for each FMC connector
 - 64Gbps (GTX transceiver)
 - High speed LVDS signal
- DDRII external memory
- Support AMchip05/AMchip06

Layout of the PRM

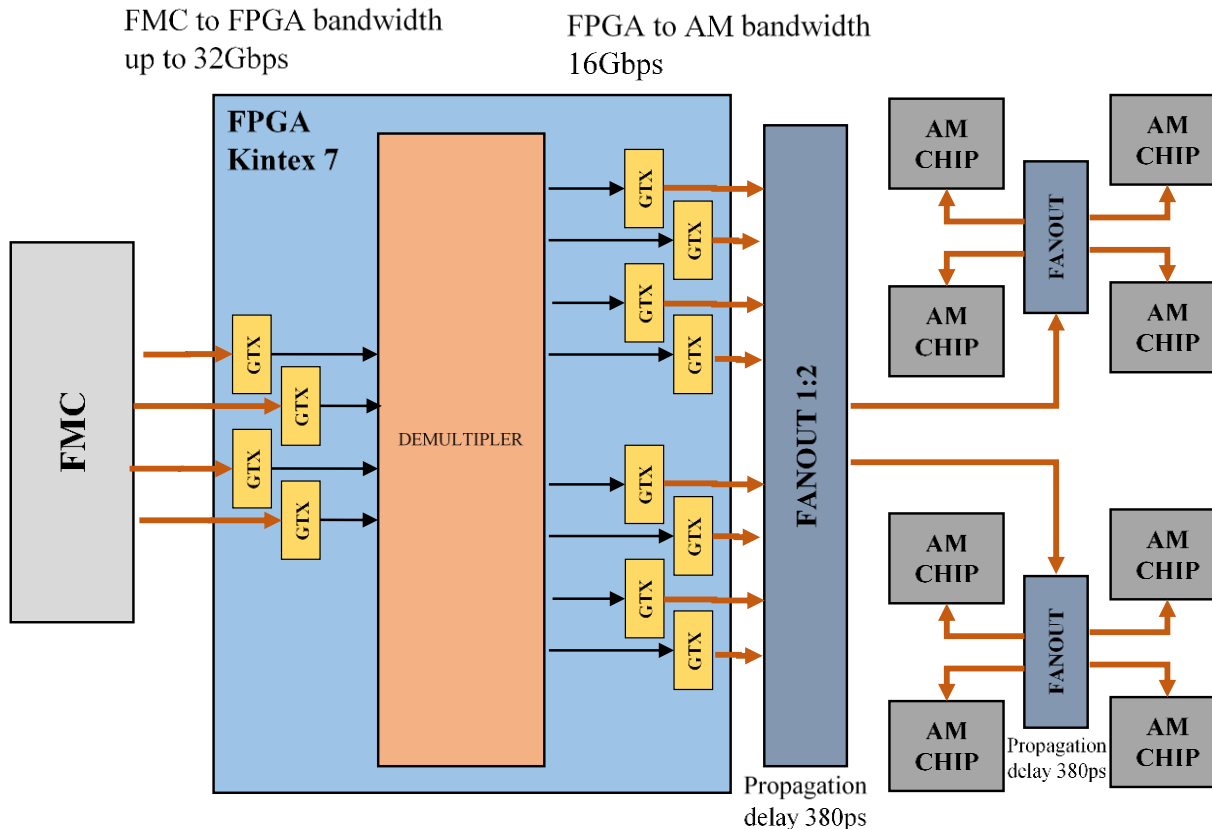
- The layout of the PRM mezzanine





Input data distribution

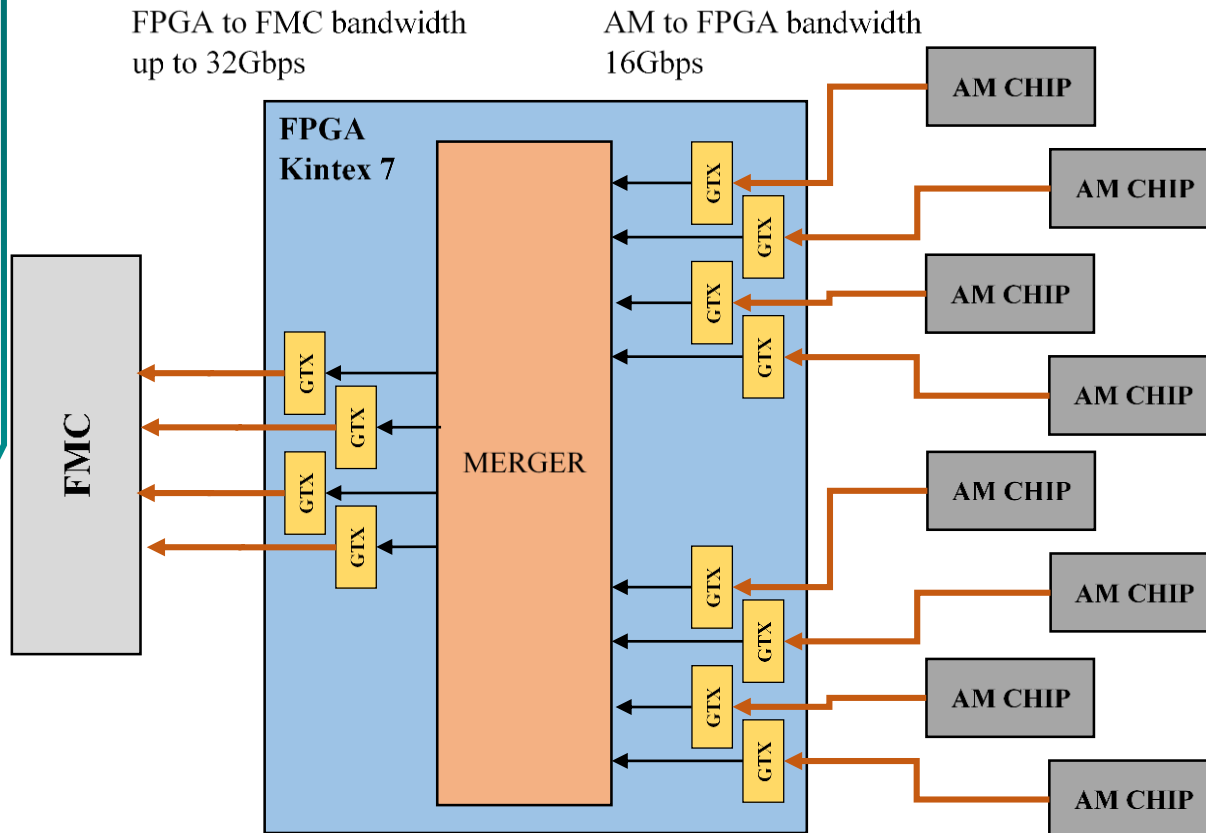
- Half part of the PRM mezzanine



- Each bus to the AM chip has a dedicate transceiver
 - 8 links@2Gbps for serve all the 8 input buses of the AM
- Minimized the latency of connection
 - The Fanout buffer introduces a delay of 380ps
- The total bandwidth to the AMchip after the spitting is 8Amchip with 8links @2Gbps
 - 128Gbps to AM

The output data flow

- The output connection of half mezzanine



- Each output of AM chip is connected to FPGA (**star connection**)
 - 16 links@2Gbps in parallel are connected directly to FPGA
- Minimized the latency of connection
- The latency is due to the deserialization/serialization of output road stream in the FPGA transceiver
- The output bandwidth from FPGA to FMC > to the AM to FPGA input bandwidth
 - No latency introduced by the merger



Pattern Recognition Engine flow



$\Delta t_{\text{pattern_reco}}$

$\Delta t_{\text{track_fit\&cleaning}}$

