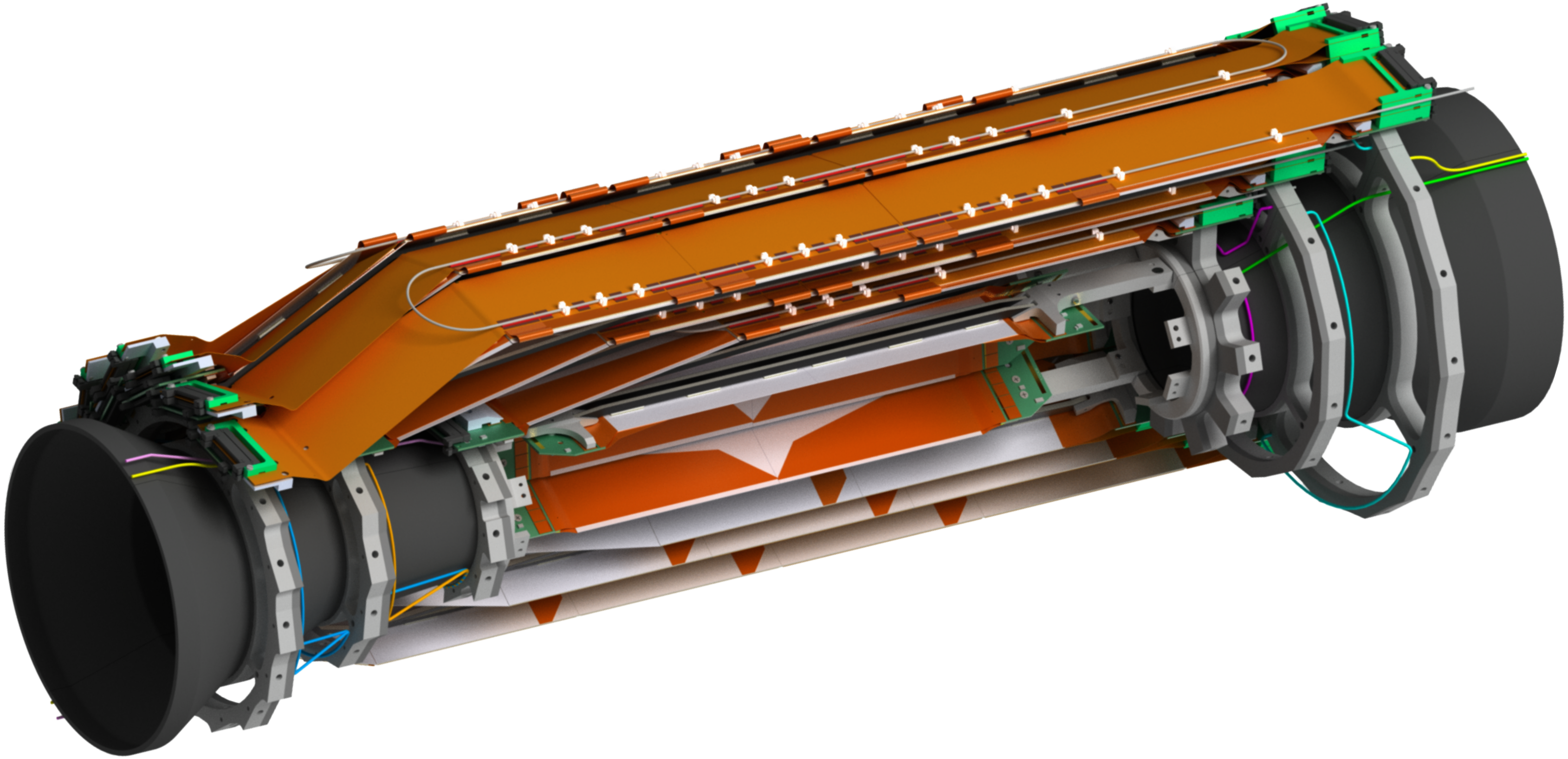
SVD
Stato, prospettive e richieste



Meeting con i Referees
30 Marzo 2015

S.Bettarini per Belle2-SVD

OUTLINE

SVD general:

- SVD new organization
- Schedule
- Pitch Adapter Issues

Pisa:

- Produzione FW/BW assemblies
- Montaggio moduli
- Nuove Richieste

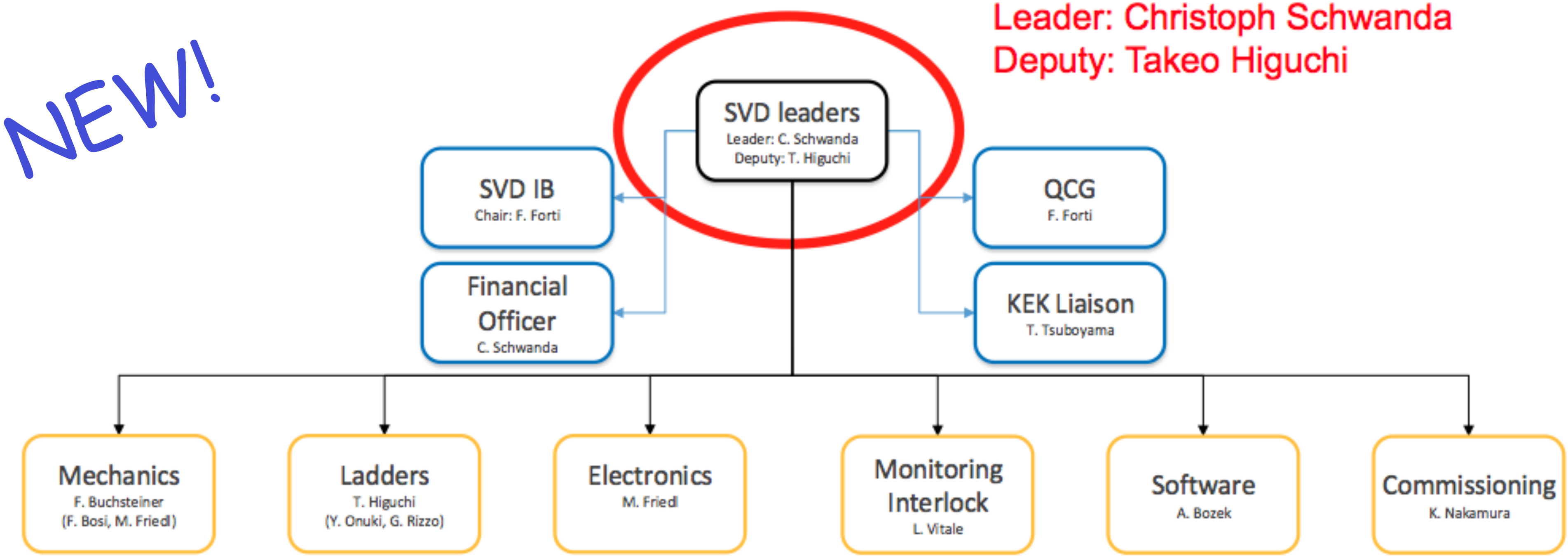
Trieste:

- Test sensori
- Radiation monitoring (BEAST)
- Monitoring/ILK temperatura/umidita'

SVD Group Organization

NEW!

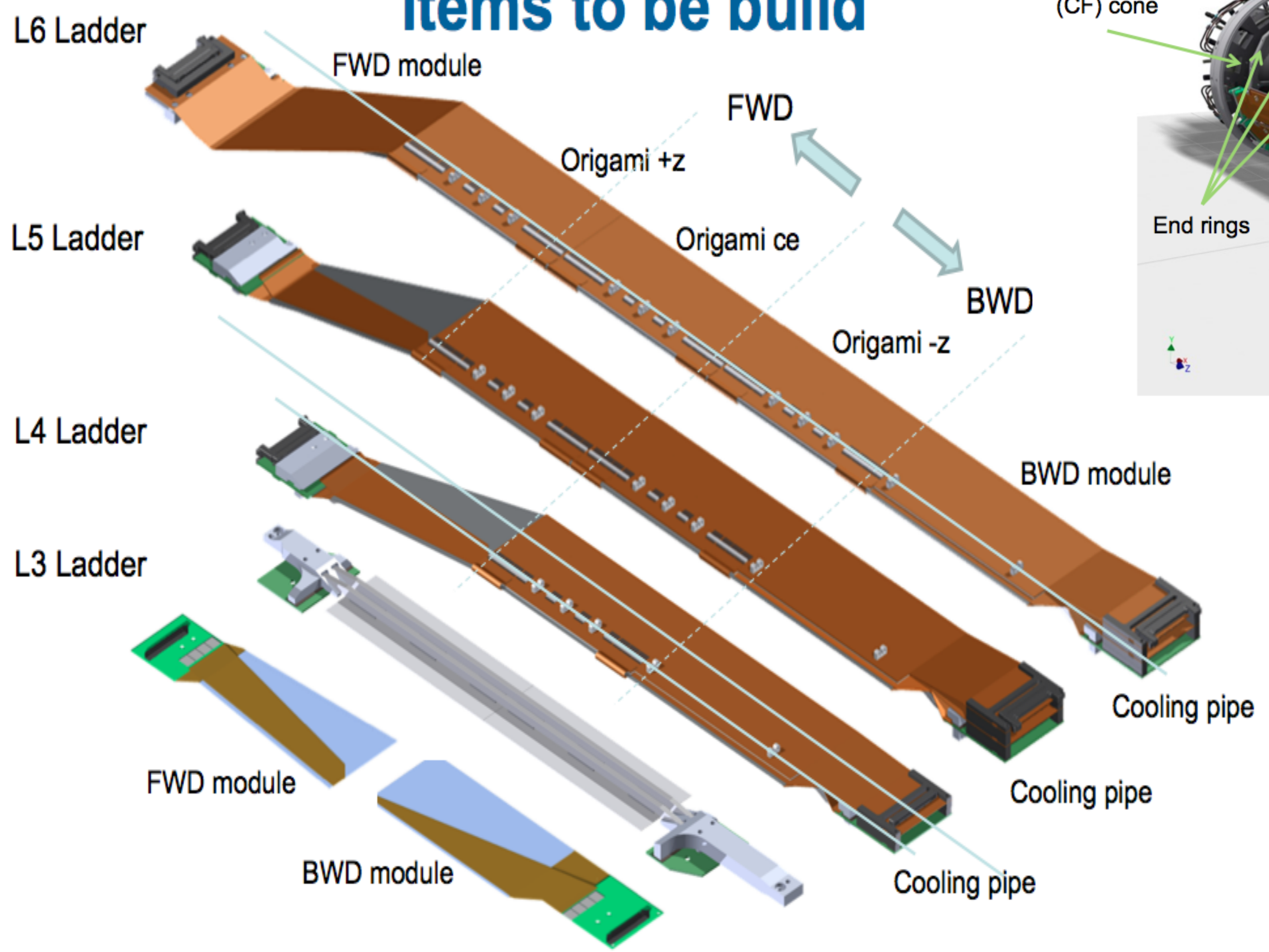
New leaders appointed Feb. 7th
Leader: Christoph Schwanda
Deputy: Takeo Higuchi

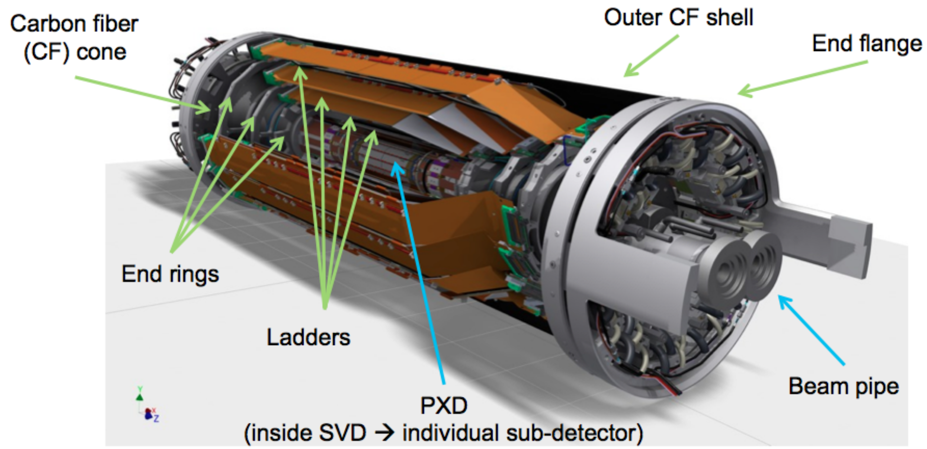


SVD Sub-Group Coordinators

Sub-group	Coordinator	Deputy	Advisor
Mechanics	Florian Buchsteiner	Markus Friedl	Filippo Bosi
Ladders	Takeo Higuchi	Yoshiyuki Onuki	Giuliana Rizzo
Electronics	Markus Friedl		
Monitoring & Interlocks	Lorenzo Vitale		
Software	Andrzej Bozek		
Commissioning	Katsuro Nakamura		

Items to be build



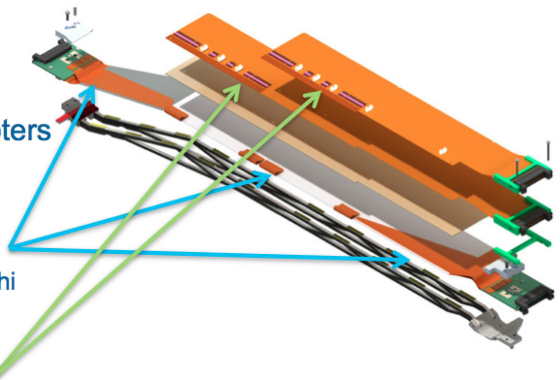


SVD Ladder Assembly Sites

- L3 ladders: Univ. of Melbourne
- L4 ladders: TIFR (@ IPMU)
- L5 ladders: HEPHY Vienna
- L6 ladders: Kavli IPMU
- FWD/BWD sub-assemblies: INFN Pisa

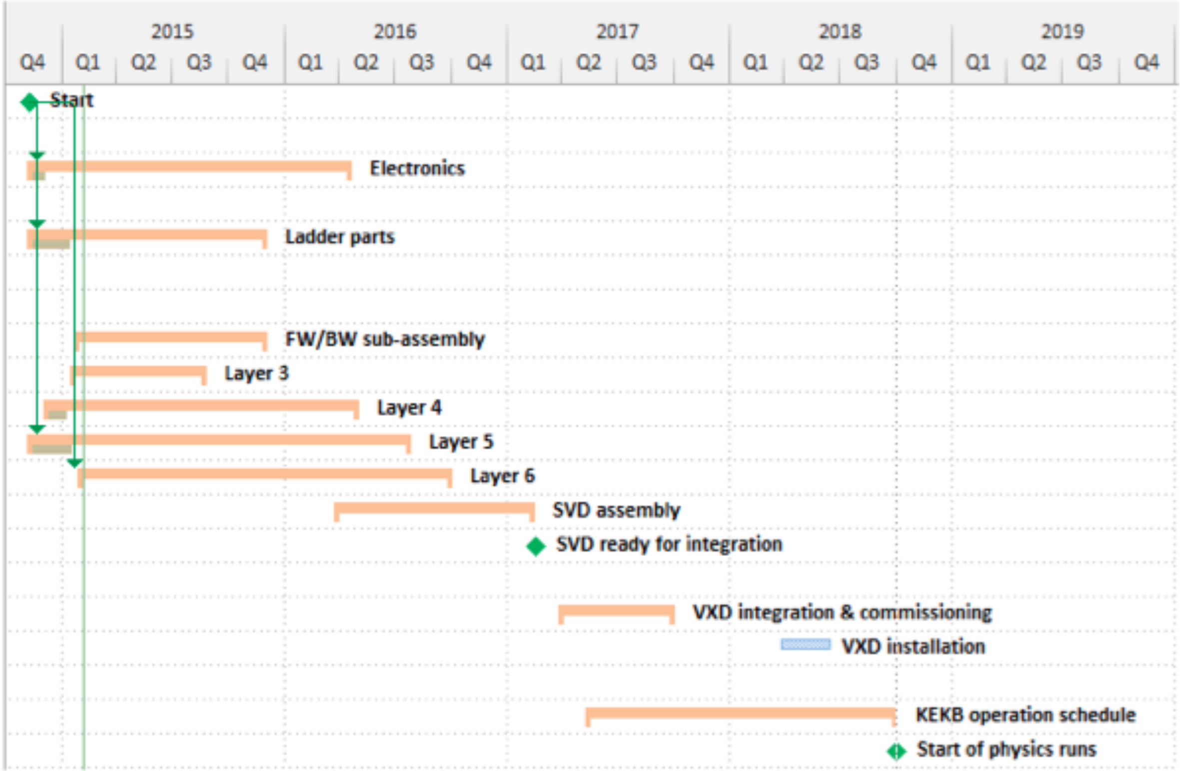
Pitch Adapters

- Flex circuit to connect sensor strips to APV25 chips
- Two types of pitch adapters
- **FlexPA**
  - Flexible, single-layer
  - PF,PB,P3F,P3B,PA
  - Produced by Tokai Denshi
- **PA0**
  - Flat, dual-layer
  - Glued onto Origami hybrids
  - Produced by Taiyo



SVD Schedule Overview
(to match global Belle2 schedule)

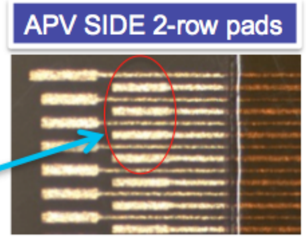
	Name	Start	Finish	Durati
1	Start	Sun 09.11.14	Sun 09.11.14	1 d?
2				
3	Electronics	Mon 10.11.14	Fri 15.04.16	375 d
15				
16	Ladder parts	Mon 10.11.14	Mon 30.11.15	276 d
67				
105				
106	FW/BW sub-assembly	Mon 26.01.15	Mon 30.11.15	221 d
118	Layer 3	Mon 19.01.15	Fri 21.08.15	155 d
131	Layer 4	Mon 08.12.14	Fri 29.04.16	365 d
149	Layer 5	Mon 10.11.14	Fri 22.07.16	445 d
171	Layer 6	Mon 02.02.15	Tue 27.09.16	432 d
185	SVD assembly	Mon 28.03.16	Fri 10.02.17	230 d
189	SVD ready for integration	Fri 17.02.17	Fri 17.02.17	0 d
190				
191	VXD integration & commissioning	Thu 30.03.17	Fri 29.09.17	132 d
196	VXD installation	Mon 26.03.18	Fri 15.06.18	3 mo
197				
198	KEKB operation schedule	Mon 15.05.17	Fri 28.09.18	360 d
203	Start of physics runs	Tue 02.10.18	Tue 02.10.18	0 d

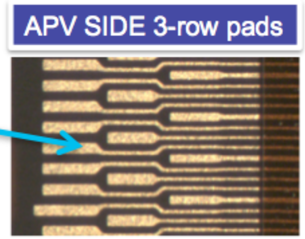


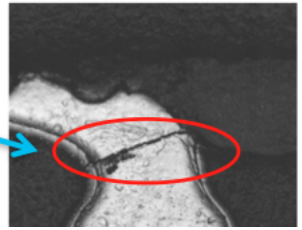
For BW-FW subassembly, the production could start after the final Flex Circuits are received and it will take ~6 months.

Pitch Adapters Issues

- **Problem #1**
  - Related to **FlexPA**
  - Arose end of 2013
  - Size of pads on APV side were too small for wire bonding
  - Could be solved by design change
- **Problem #2**
  - Related to **PA0** only
  - Disconnected lines due to cracks close to bond pads of PA0
- **PA task force formed to solve issues**

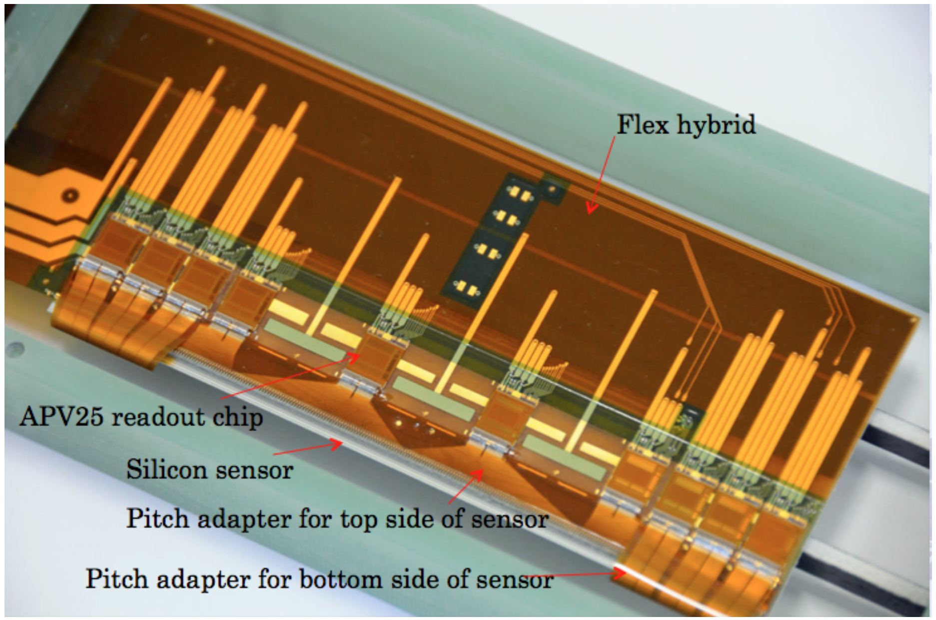






#1:

- Tested samples of the flex new production have been delivered in mid-March
- Now under survey@IPMU



PA0

#2:

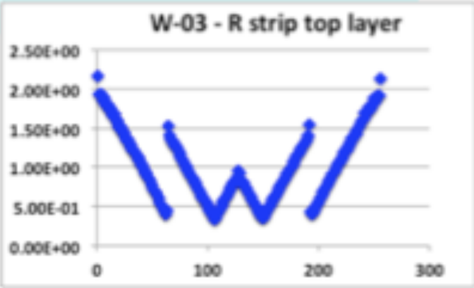
- Requires re-production of all Origami hybrids with thinned APV chips
- More robust design against cracks implemented
- Alternative single-layer option (2nd vendor) to be pursued

Plan for PA0/ORIGAMI reproduction

- Sept. 2014: discovered ORIGAMI circuits cannot be used since PA0, pitch adapters, glued on them, have cracks/opens→ reproduction
- Several months of investigations/test productions to find a solution for PA0 → Feb 2015 new PA0 design ready for a test production.
- **Original Plan PA0/ORIGAMI reproduction** (Feb 2015 B2GM):
  1. Produce 24 PA0 (2 variants) with new design, more robust against crack, + other design changes needed.
  2. Evaluate PA0 quality (bare samples) with electrical test/visual inspection
     - ~ Mid March ⟵ We are here
  3. Assemble 12 PA0/ORIGAMI = batch0 to verify:
     - no cracks develop on PA0 during full assembly procedure: various electrical tests in different phases of the process foreseen.
     - verify all ORIGAMI assembly steps before mass production.
     - ~ end April
  4. Start mass production for PA0/ORIGAMI assembly (if point 3 OK).

     ~ starting mid May → Nov. 2015 + 1 month contingency

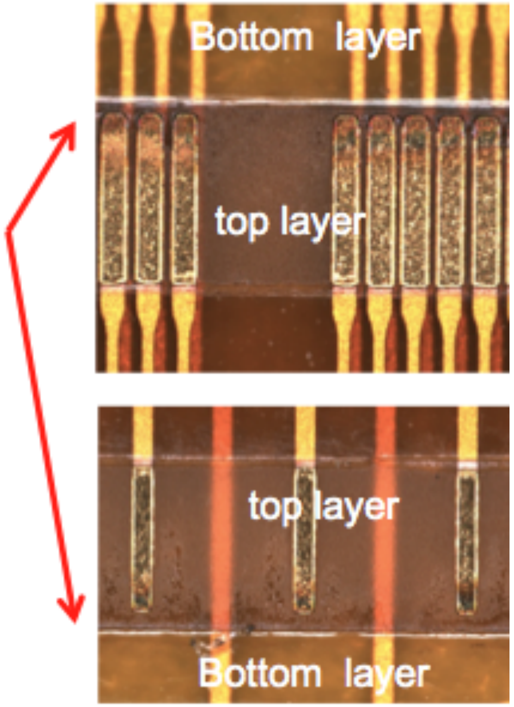
Evaluation of new PA0 produced



- **24 PA0 with new design**
  - No cracks found: no opens, from electrical test, no small cracks seen by visual inspection.
  - A few shorts found on 6/24 pieces
  - Yield 75%, acceptable

- **Unexpected new issues on PA0: "glue spread"**
  - PA0 are made of 2 layers: interlayer glue spreads onto edge of the top layer, covering part of the APV pads and with a lot of residuals on sensor side pads. Details in next slides.

  - Problem under investigation with the company; maybe due to changes in design needed to cure other problems.
  - Some bonding tests done, not conclusive, but glue spread could be very nasty since the effect it's not under control.
  - It may require additional changes in the PA0 design or only changes in the gluing procedure among the 2 layers.
  - Depending on findings in next 1-2 weeks, we can evaluate how much time is needed to solve issue or reproduce new PA0 if needed.



Proposal for a new plan

Variations to the Original Plan

1. Produce 24 PA0 with new design
2. Evaluate PA0 quality (bare samples) with electrical test and visual inspection ~ Mid March

- **While investigate/solve new PA0 issue we want to**

3. Continue with the assembly of 12 PA0/ORIGAMI (batch0), with present PA0, to verify:
   - 3.1 no cracks until the end of stressfull assembly steps
   - 3.2 verify all the ORIGAMI assembly procedure up to SMD and reflow (all the stressfull steps for PA0) but NO APV chips will be lost. ~ → Mid April (or ~end of April if we continue up to the APV assembly/wirebonding)

- Time to solve new PA0 glue spread issue depends on what we find in next 1-2 weeks

3 bis Insert an additional batch0.1 PA0+ORIGAMI assembly, with final PA0 reproduced, before mass production.

4. Start mass production PA0/ORIGAMI assembly

- in original plan: starting mid May → Nov. 2015 + 1 month contingency
- → new schedule for mass production depends on time to solve PA0 glue spread or time to switch to the plan B (single layer PA0 on ORIGAMI)

Ladder Production

- Despite the issues causing a delay in the ladder production, each site is developing the assembly procedures.

Site Qualification Reviews

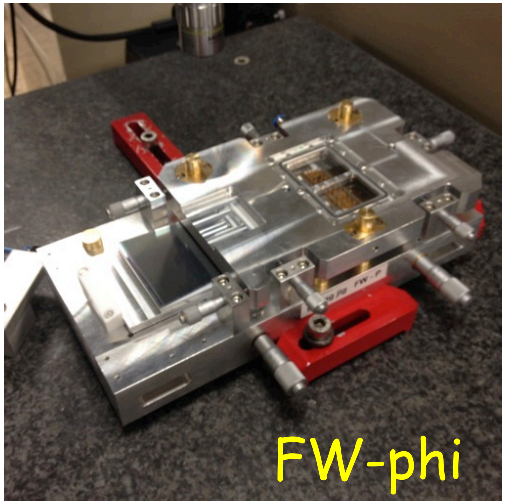
- The reviews help the groups to
  - Design stable and reliable **procedures**
  - **Document** the procedures and the QC/QA
  - **Communicate** with other sites
  - **Organize** the manpower and schedule
- **It should not be a one-time event, but rather a work method**
- A qualification site visit of the committee is required.
- Class C qualification already completed for
  - Pisa
  - IPMU
  - HEPHY
  - TIFR

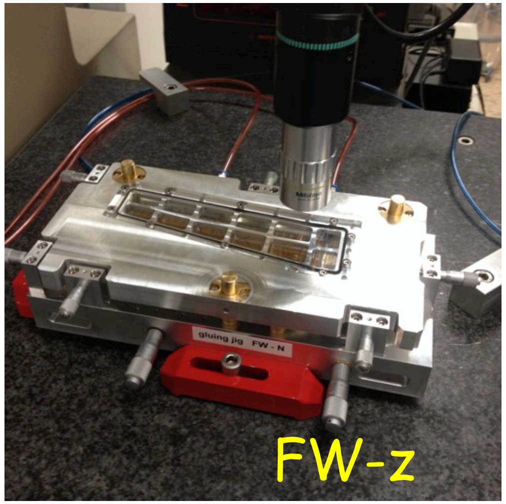
Qualification review matrix

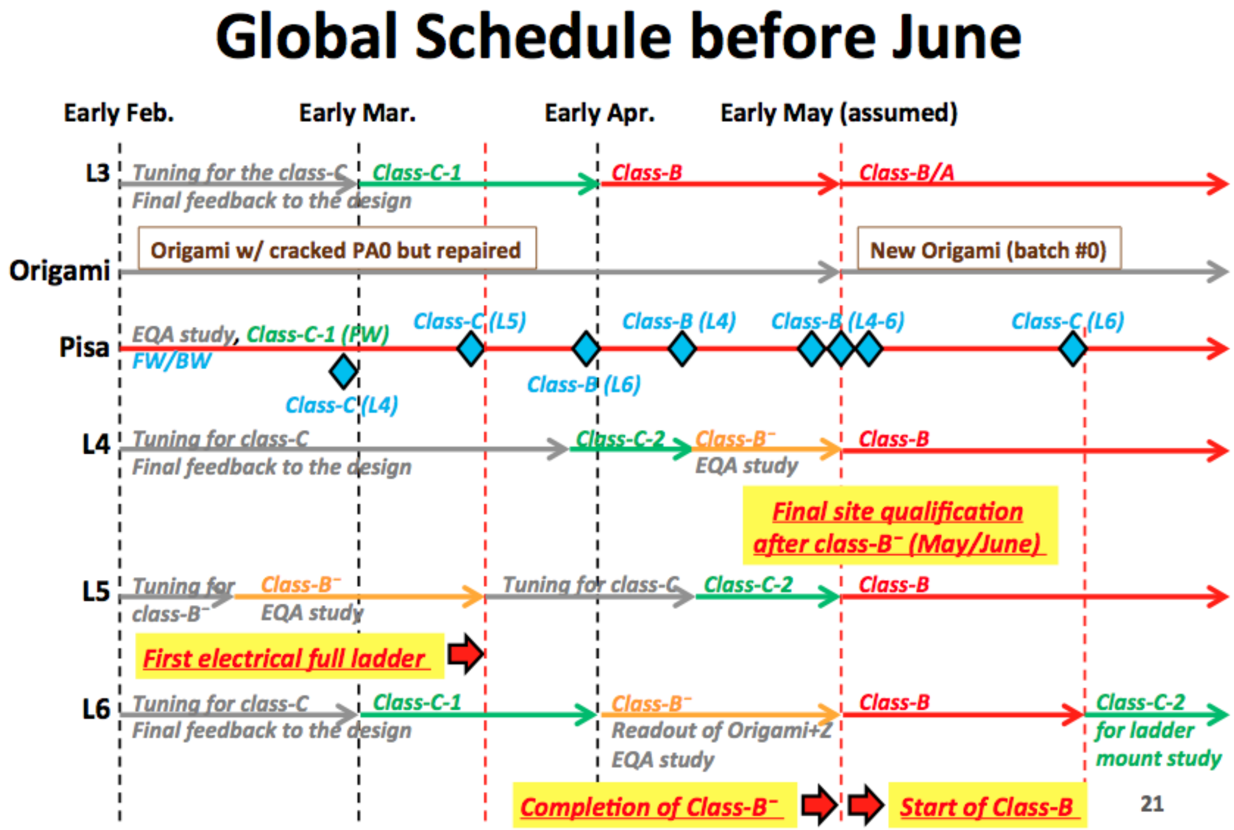
Site	Type	Date
Melbourne	Full	April 2015
Pisa	Class C	3-4/10/2014
Pisa	Full	TBD
TIFR	Class C	5/2/2015
TIFR	Full	TBD
HEPHY	Class C	19/1/2015
HEPHY	Full	TBD
IPMU	Class C	31/10/2014
IPMU	Full	TBD

FW-BW subassembly production

The final gluing jigs and the procedures have been tuned to produce the Class C (mechanical) and Class B (electrically working, built with low quality parts) needed by the ladder assembly sites.

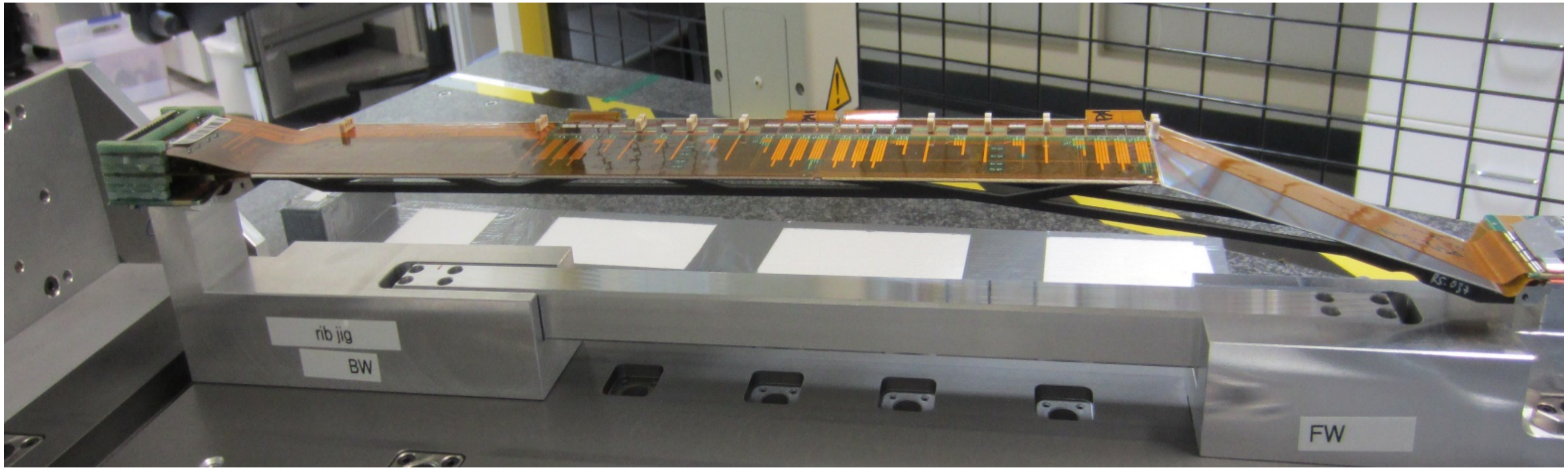






Costruito il primo ladder elettricamente funzionanate (L5)

- Vienna ha finito (24/3) di costruire il primo ladder class B:

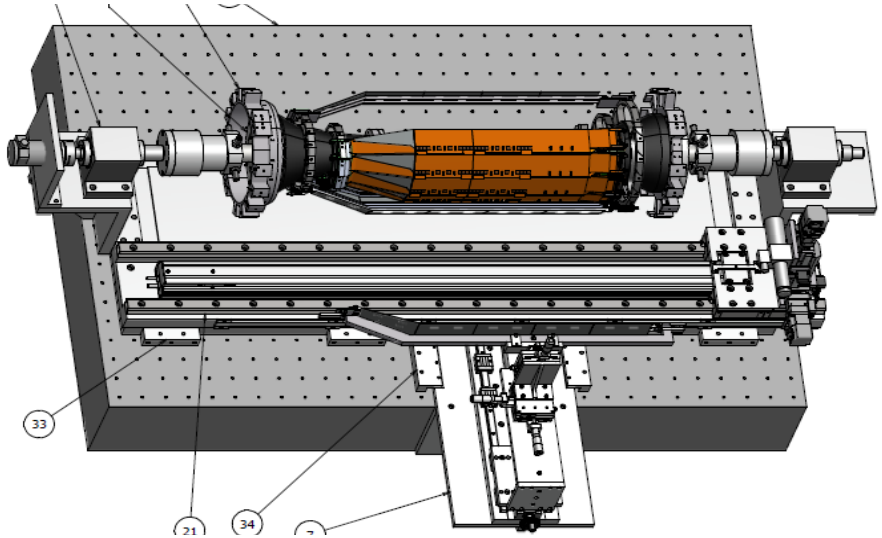


- Usati i tools meccanici e procedure finali
- Caratterizzazione elettrica → completamente funzionante
- Una milestone importante!

Ladder mount

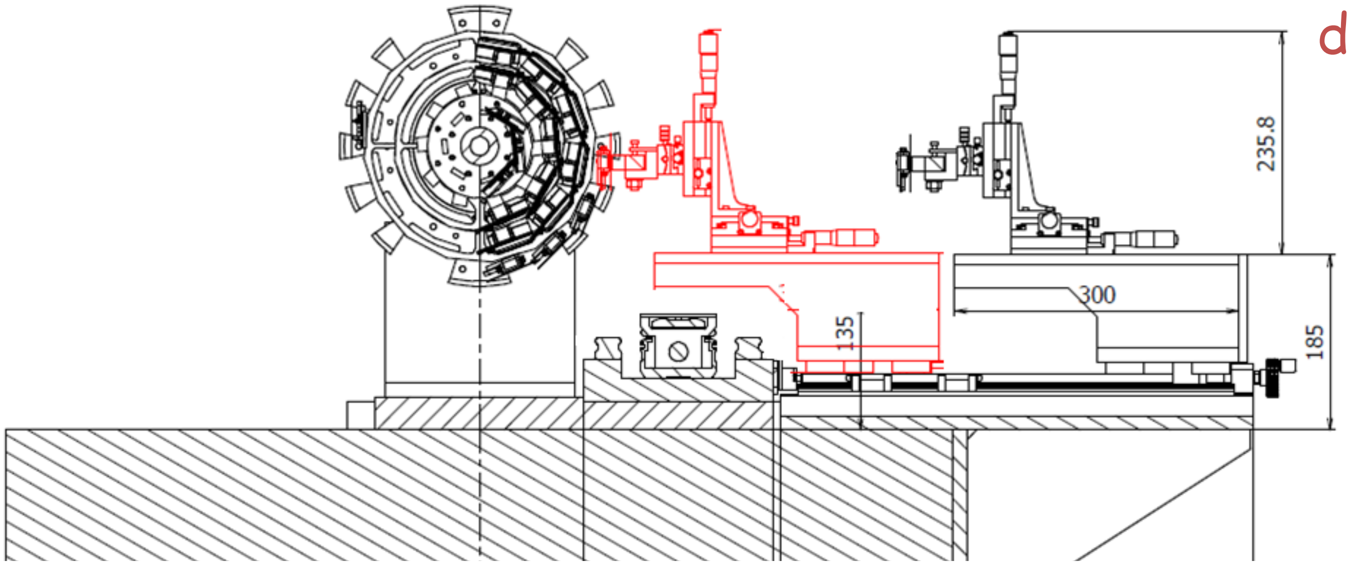
- Clearance between modules:

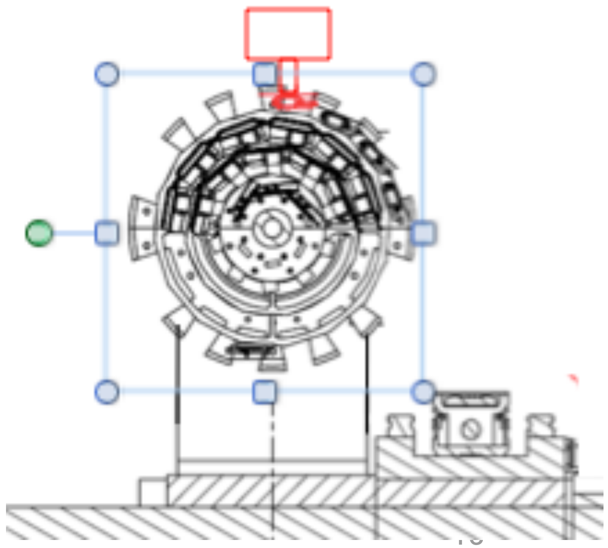
Less than 1 mm!



Option 1: hold ladders with arm and approach to the end rings by side, insert pins of ladders to the positioning holes.

Option 2: support ladders from top using a sliding guide in vertical direction.

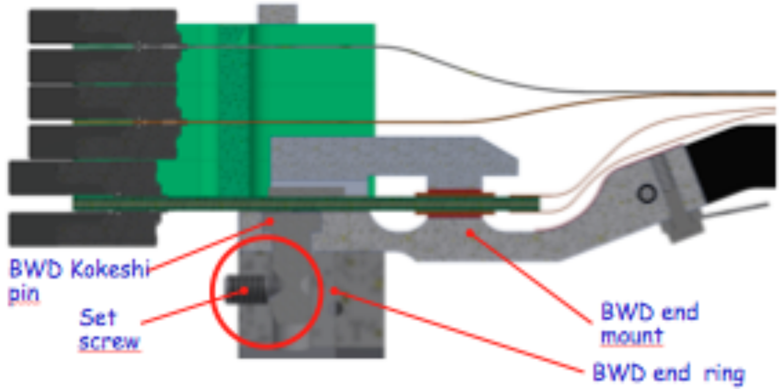




Conceptual Top mounting procedure

- According to our (BaBar-SVT) experience, the whole operation can be split into 3 main phases:

1. Ladder loading from the shipping box to the "Two Arm Support", fixed to a sliding cart and equipped at each end with a thin flat pincer, hosting the K-pin.



2. Horizontal movement of the ladder on top of the end-rings
3. Guided lowering and locking of the ladder in its final position

- The system will be mechanically designed/realized/tested at home, reproducing the essential features on a mock-up and then shipped to KEK
- Now working on the design of the prototype two arm support, in order to be tested in June @KEK.

Nuove Richieste

1. Board addizionali per Power Supply (V separation n-side):
   - Motivazione/ Quantita'
   - Analisi nuovi tests (vedi presentazione G.R.)
2. Acquisto di ulteriori rivelatori o(25) (large HPK: L4→6):
   - Il numero attuale non congruo per garantire la produzione dei ladders con un sufficiente # spares (prescrizione BPAC)

Richiesta Power Supply: 19kE

- Il Vsep e' la differenza di tensione che si stabilisce tra la faccia del rivelatore (N o P) e l'ingresso dell'amplificatore
- Sul P-side e' obbligatoria perche' in caso di qualche pinholes (C rotto) l'alta corrente in ingresso puo' non far funzionare l'intero chip
- Dai tests recenti sui moduli veri abbiamo capito che sull'N-side la Vsep puo' recuperare (far tornare a funzionare efficientemente):
  - i canali dovuti ai pinholes
  - i canali rumorosi (field-plate effect)

Prodotto	Q.ta	Prezzo unitario	Sconto %	Totale aggiudicato	Spare	CostoSpare	CostoTotale	G
SY4527	2	5700	10	10260.00	1	5130		A
A4533	2	1450	10	2610.00	1	1305		R
A2519A	12	1950	15	19890.00	3	4972.5		A
A1510	2	4800	18	7872.00	0	0		+
A1519B	4	4800	10	17280.00	1	4320		~30%
TOTALE				57912.00		15727.50	**73639.50**	spare
30% aggiudicato				17373.60				

Richiesta:

A1510	2	4800.00	18	7872.00	1	3936	11808.00
Tasse	8%	consumable tax sul totale					6835.8
TOTALE							**18643.80**

Richiesta rivelatori HPK (Large DSSD):150 kE

- Le indicazioni del BPAC:
  - Ladder complessi da costruire (necessario aumentare le parti spares durante la costruzione)
  - Finire la produzione con un congruo numero finale di ladder spares
  - Si tratta di aumentare di un 10% le parti per arrivare ad un 20% di spares
- Istituzioni di SVD si stanno impegnando sul procurement degli small DSSD, chips, PAs, hybrids, ribs, parti meccaniche.
- Il fattore limitante e' costituito dai rivelatori large DSSD:

(Financial shortfall for SVD)

Type	Number	Unit cost kYen	TOTAL (kYen)	With tax	TOTAL (Euro)
Large DSSD	25	702	17550	18954	146.25
Small DSSD	10	988	9880	10670.4	77.1875

Considerazioni

- Sono necessari 8 mesi per produrre i nuovi rivelatori: l'ordine deve essere necessariamente fatto nella II meta' del 2015, affinche' si possa costruire gli spares verso la fine della produzione dei ladders gia' previsti (entro meta' 2016).

- Il contributo finanziario italiano all'SVD si e' concretizzato nei PS ed nei jigs di costruzione dei FW/ BW subassemblies, forse minore di quanto sarebbe stato dovuto se fossimo stati fin dall'inizio nel progetto.

Belle II – Trieste in sintesi (2015)

- Partecipanti
  - L. Bosisio 60%
  - L.Lanceri 90%
  - L.Vitale (*) 90%
  - G.Cautero (Elettra) 10%
  - D.Giuressi (Elettra) 10%
  - H.Menk (Elettra) 10%
  - + Assegno ricerca biennale!

  (*) coord. Monitor SVD
- Servizi di Sezione
  - P. Cristaudo (NTC)
  - M. Bari (FOS)
  - A. Zanetti (umidità, PLC)
  - G. Venier (commissioning…)
- Responsabilità hardware
  - Test sensori microstrip DSSD, da Micron e HPK
  - Per VXD = PXD + SVD monitor radiazione e trigger per beam abort
  - Monitor temperatura (NTC, FOS) e umidità (con "sniffing pipes"), interlock (PLC)
- Prev. – Assegn. - Impegni 2015
  - Missioni 49 - 37 - 4.7 kEuro
  - Consumi 17 - 12 - 2.5 kEuro
  - Apparati 107 - 107 - 0 kEuro
  - Trasporti 2 - 2 - 0.2 kEuro

Profilo di spesa previsto (Trieste)

Item	2013	2014	2015	2016	TOT
Initial CORE	5	75	70	0	**150**
DSSD tests	2.5	0	0	0	2.5
Rad.Mon.+Abort (diamonds, cables, etc)	2	7	**96**	10	115
Rad.Mon.+Abort (electronics)	0	4	4	19	27
Temperature Mon. (FOS fibers, offers)	0	**17.5**	**1**	**30**	**48.5**
Temperature Mon. (NTC thermistors)	0	3	2	4	9
Humidity Mon. (very preliminary)	0	0	10	0	10
TOTAL	4,5	31.5	113	63	**212**

Note (*nessun problema particolare in vista, per il momento*):

1) Acquisto "FOS interrogator" (30 kE, 2016) anticipato al 2014, Pisa
2) Acquisto di 24 sensori diamante scCVD nel 2015:
   - siamo pronti (scelta dopo test prototipi: Cividec) !
   - L'ordine sarà spezzato in due parti
3) Dettagli: qualche scambio, spese 2014-2015, per rinvio acquisti finali FOS

Progressi, da Dicembre 2014 - 1

- Preparata una schedula dettagliata delle attività; la documentazione per sign-off è in preparazione
- Test DSSD Micron e HPK (L.Bosisio, I.Rashevskaya)
  - Laboratorio pulito rimesso a nuovo
  - Effettuati test completi su 12 sensori Micron e 3 HPK
  - Disponibilità a ulteriori test su sensori HPK
- Sistema monitor temperatura, NTC (P.Cristaudo)
  - Sistema di lettura: completato disegno finale
  - Montate due schede finali (su 3 +spares), testate e funzionanti
  - Procurate (CERN) e testate 10 schede ELMB (3 + 7 spares)
  - Software LabView OK (next: Epics…)

Progressi, da Dicembre 2014 - 2

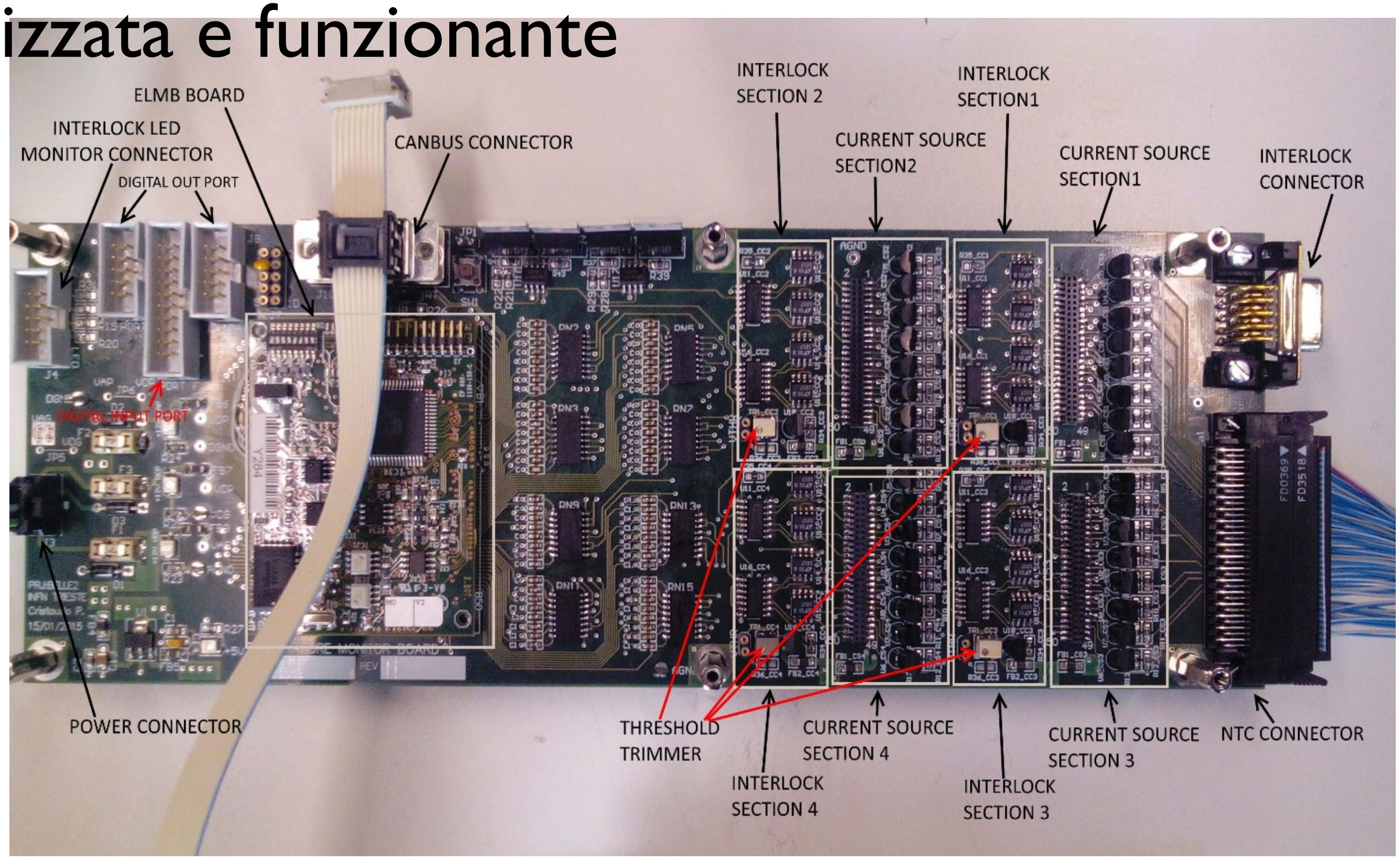
- Sistema monitor temperatura, FOS (L.Vitale, M.Bari)
  - Ricevuto “FOS interrogator” Micron Optics, software installato
  - Prototipi fibre con fino a 8 sensori, da due provider: test OK
  - Varie configurazioni, 4 x 1 couplers etc.: attenuazione OK
  - Da fare adesso: organizzare calibrazioni, ordini finali
- Sistema monitor umidità e interlock (L.Lanceri, A.Zanetti)
  - Ricevuti: sensori dew point Vaisala e “chilled mirror” di riferim.
  - Ricevuta PLC Schneider + starter kit, software installato
  - Ordinato un PC dedicato
  - Iniziato il disegno e l’acquisto di materiale per le interconnessioni con sniffing pipes, flussometri, pompa

Progressi, da Dicembre 2014 - 3

- Monitor di radiazione e beam abort (L.B., L.L., L.V., + studente M. Zuppichin, + Elettra)
  - Messe a punto le procedure di test e i programmi di analisi:
    - Caratteristiche I-V, al buio e con sorgente beta
    - MIP (sorgente beta): fit Landau, fit Charge Collection Efficiency
    - Stabilità delle correnti misurate con sorgente a diverse distanze, fit con modello di “shallow” e “deep traps”
    - TCT (sorgente alfa): misura dei tempi di transito e delle mobilità di elettroni e lacune, controllo dell’ uniformità del campo elettrico
  - *Prototipo scCVD E6/Cividec, montaggio e cablaggio “finale”: OK*
  - Pronti per iniziare gli ordini…
  - (Prosegue il disegno dell’elettronica di lettura e beam abort)

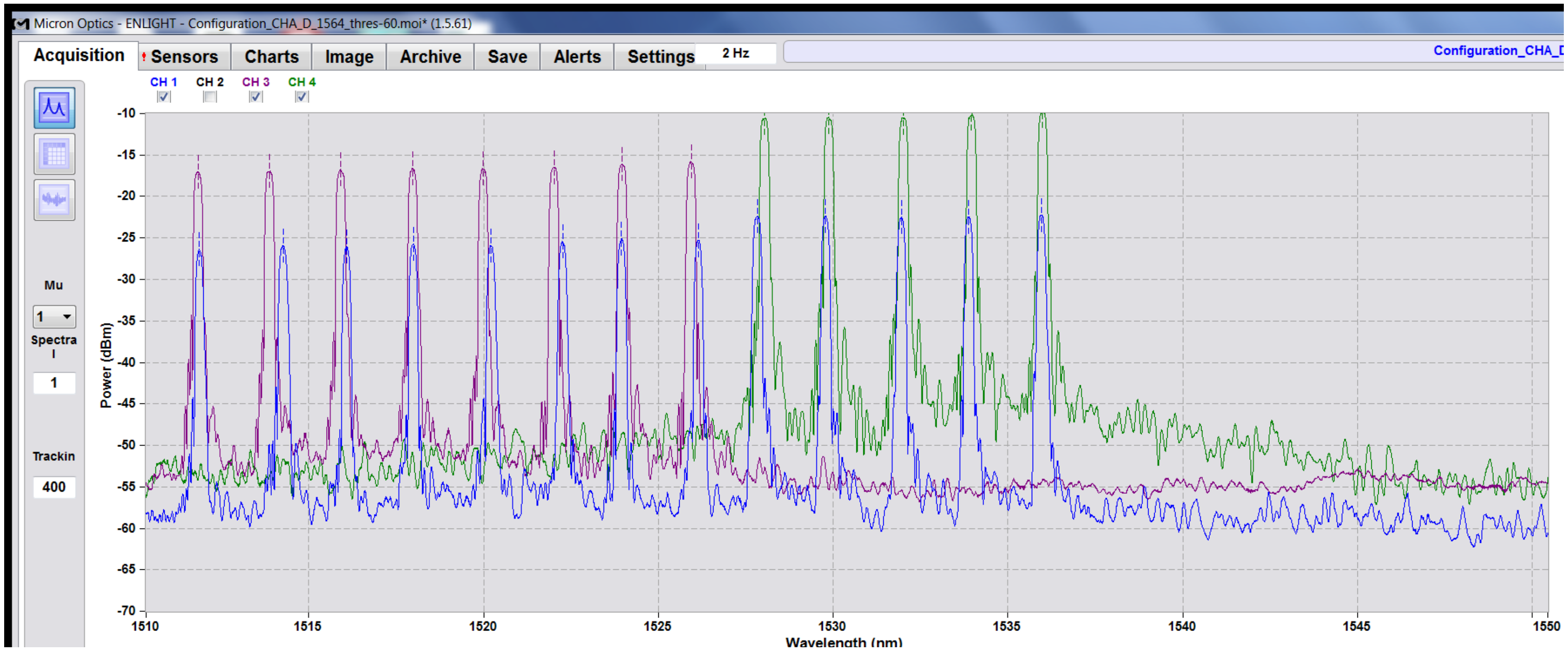
Highlights – I (NTC readout)

- Motherboard finale per lettura termistori NTC con scheda ELMB (processore, ADC, MPX), current sources, segnali interlock, connettore CANBUS: realizzata e funzionante



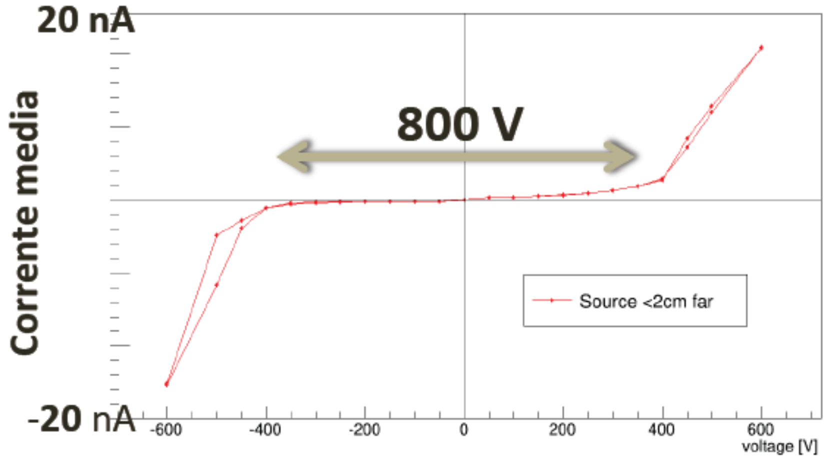
Highlights – 2 (FOS sensors)

- 5 sensors fiber direct to interrogator
- 8 sensors fiber with 1x2 splitter
- 2 fibers (8 sensors +5 sensors), 1x4 splitter, 30m fiber and all PC/APC connectors is ok, the attenuation is ~ as expected

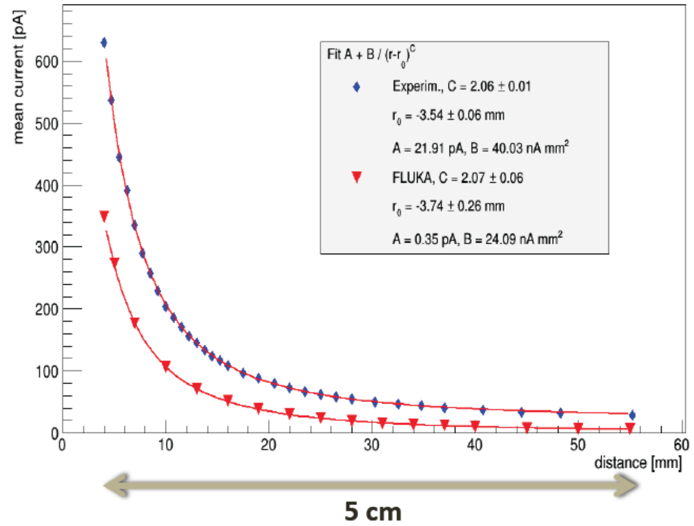


Highlights – 3 (scCVD sensors)

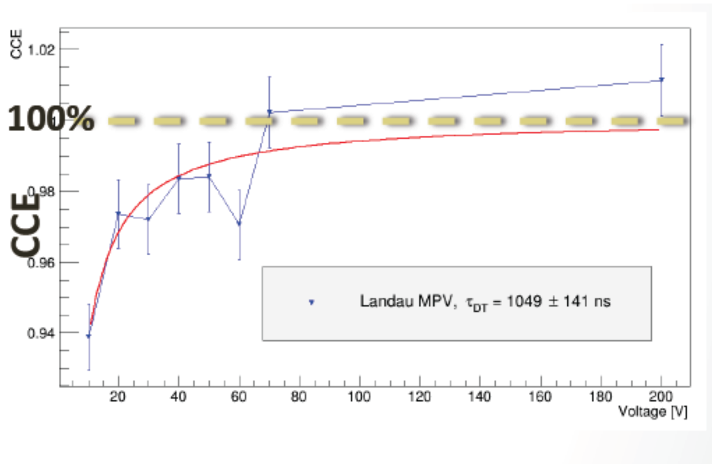
Caratteristica I-V, con sorgente beta



Corrente vs distanza sorgente



Charge Collection Efficiency, dalle MIP



Mobilità di elettroni e lacune, da TCT