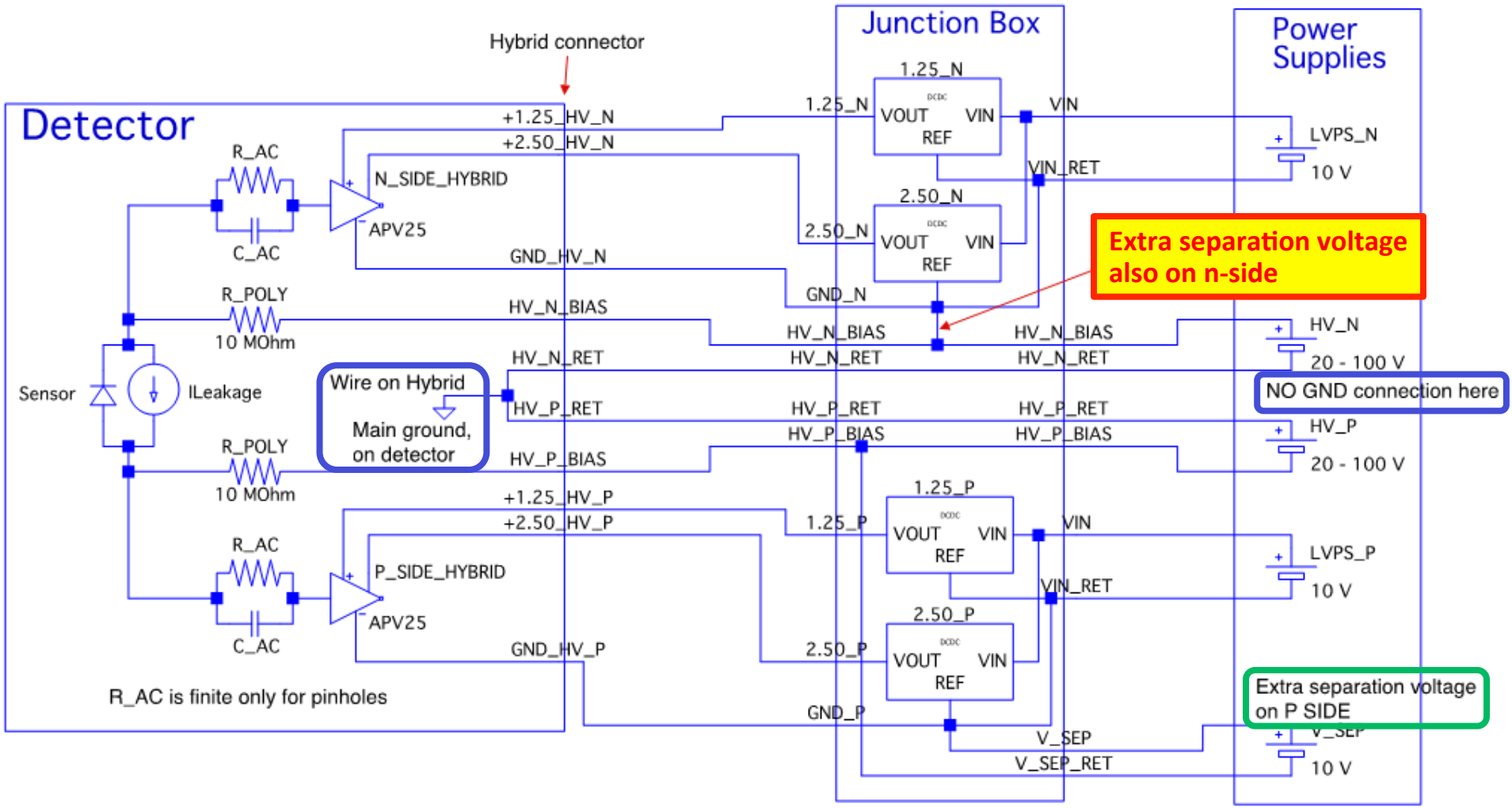
Pinholes and their effects of APV25 chips

- Pinholes
  - sensor strips are capacitively coupled to APV25
  - The capacitors, integrated on the sensor strips, can occasionally have a short circuit→ pinhole.
- Pinhole can give DC current into/out from APV, which can:
  1. permanently disable the whole APV chip on p-side
     - due to APV INVERTER, used to change signal polarity and increase the dynamic range only on p-side (APV dynamic range +7MIPs /-2.5MIPs)
     - problem only arises on p-side (INVERTER) if current flow INTO APV:
       - APV input sits at +0.75V w.r.t APV_GND=HV_Bias
       - p side strips, collect holes, sit at HV_Bias+Ileak*Rbias →cna inject current INTO APV
     - problem only if Ileak is big (rad damaged sensors) or/and several pinholes are connected to the same chip (details in backup slides)
  2. disable the single APV channel where pinhole is connected.
     - same effect on p and n side
- In CMS (single side sensor, p-side strips) all pinholes were then NOT connected to the APV chip to avoid problem 1

What we do in Belle2-SVD for pinholes

- In Belle2-SVD we proposed a new strategy for the pinholes!
- Saturation effect of the whole p-side chip can be avoided applying an extra voltage (Vsep) on APV_GND w.r.t HV_Bias
  - can rise Vsep to positve voltage so the current flows out of the APV chip, to sensor strip, and saturation cannot happpen.
  - Extra voltage used already in BaBar to inhibit issues due to pinholes/p-stop short
- Advantages: disconnecting all the pinholes (as in CMS) can be difficult & new pinholes can develop later (radiation accidents!)
- This scheme (next slide) was proposed originally only to p side, since chip saturation cannot happen on n-side
  - CAEN boards for p side foreseen
- Recent studies on APVDAQ teststand (with real SVD modules) proved Vsep is effective:
  1. to avoid whole chip saturation on p side (expected)
  2. to cure single pinholes on p and n side (new)
  3. to recover single noisy strips: field plate effect of AC metal connected to the Vsep voltage via APV input (new)
- CAEN board for n side are needed

New Powering Scheme

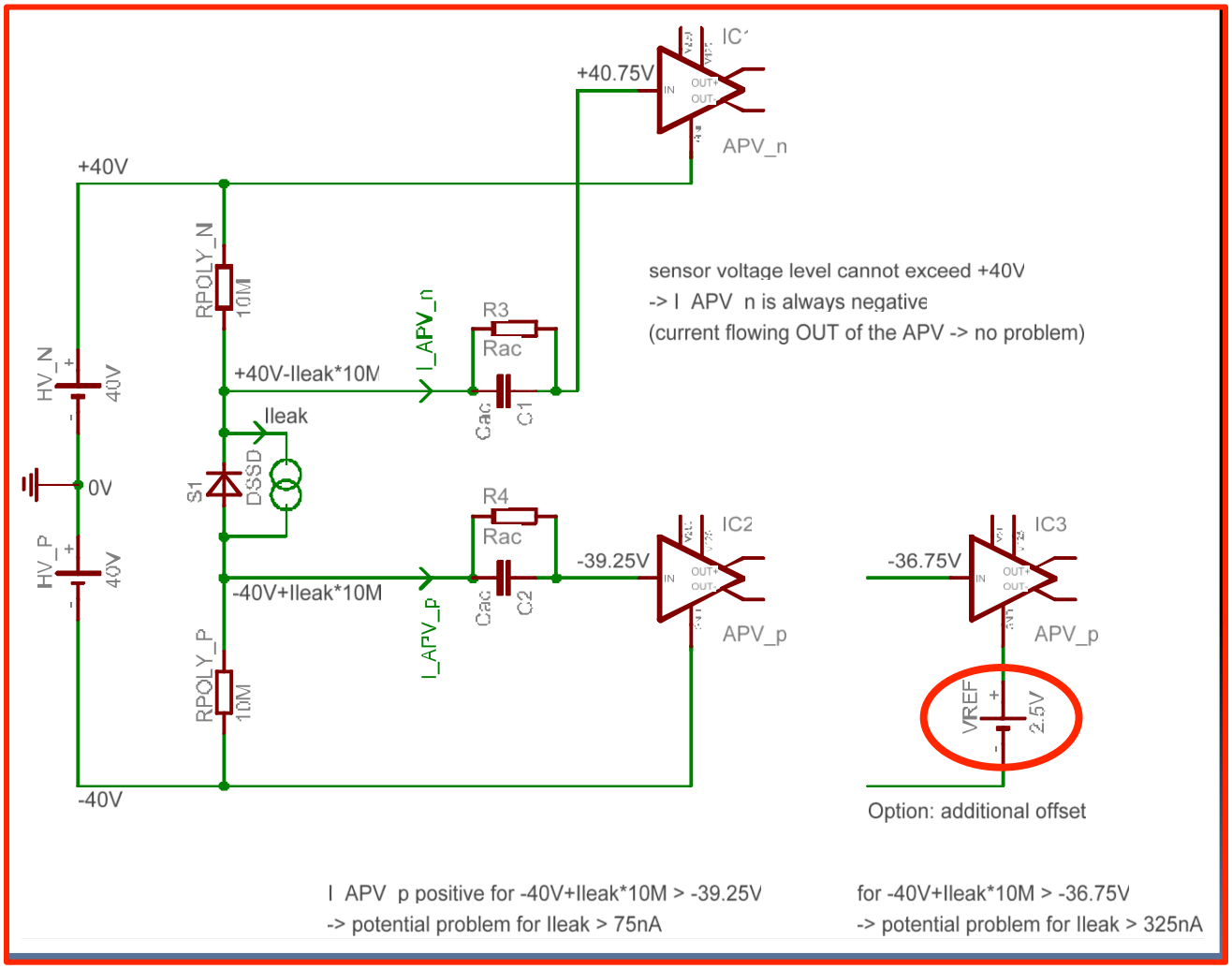


Vsep-extravoltage advantages

Recent studies on teststand with real SVD modules proved Vsep effects and various advantages on p and n side

1. Saturation effect on p side, on chips with several pinholes connected, demonstrated and cured with Vsep
   - Whole chip saturation starts with Vsep<-3V
   - All chans including pinholes, work normally -2.5V<Vsep<-0.5V
   - Pinholes stop working with Vsep>-0.5 V the other chans ok
2. Vsep can cure single connected pinholes on p & n side
   - with Vsep set to equalize the strip voltage and the input of the APV (+0.75V) no significant DC current is flowing in the pinhole and APV channel can work normally: Vsep=-0.75V cure pinhole, for very low Ileak
3. Applying Vsep, via the APV input, on AC metal strips (no pinholes/AC capacitor OK) can be beneficial for noisy strips:
   - AC metal acts as a field plate above the n+ strip implant
   - With the right polarity/value can reduce strip leakage current coming from defects localized at the Si/Si02 surface
   - Noise reduction on defective strips observed/effect still under study

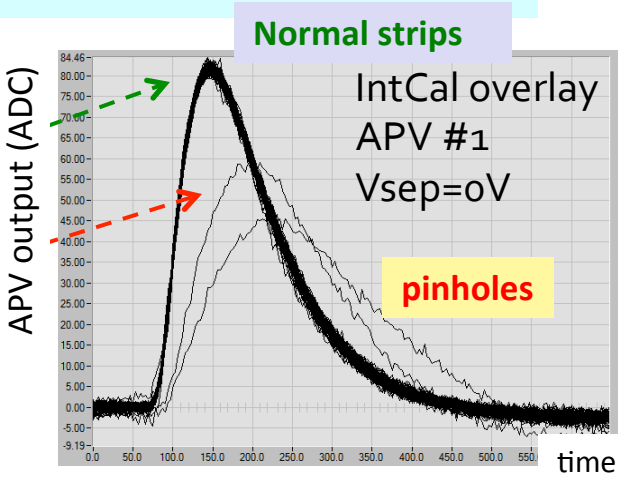
Pinholes studied on APVDAQ teststand

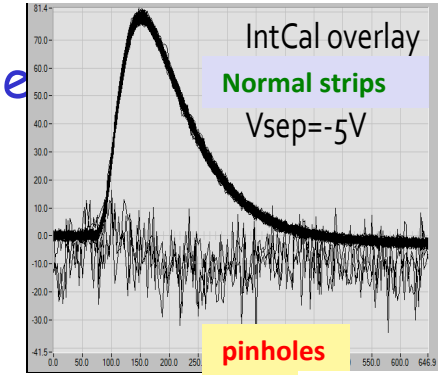


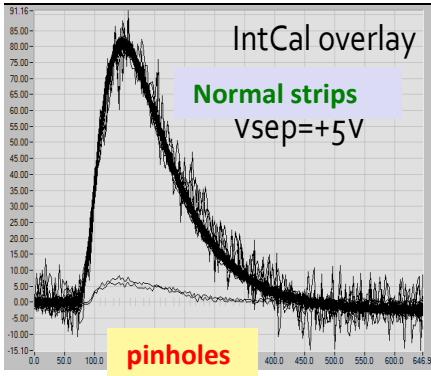
- **p-side only**: large current flow INTO APV, (several pinholes) is a problem for the whole chip
- p & n side: small current (single pinhole) disable a single APV channel
- Remedy: offset voltage between HV bias and APV_GND
- Some noisy channels (not pinholes) can be recovered with Vsep acting on AC metal as field plate

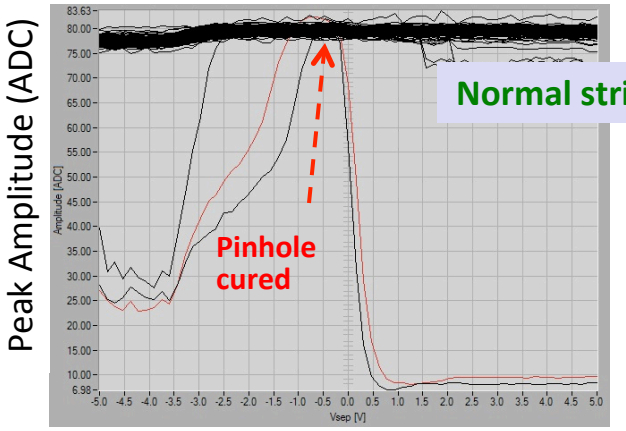
APV response to internal calibration

- Signal (MIP equivalent) injected from internal APV calibration circuit
- Peak amplitude:
  - 85 ADC for normal strips
  - smaller for pinholes connected
- Peak amplitude on pinholes reacts to Vsep extra voltage, as expected
- Vsep negative, -0.75V can cure single pinholes
  - equalize strip voltage and APV input

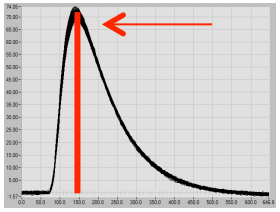








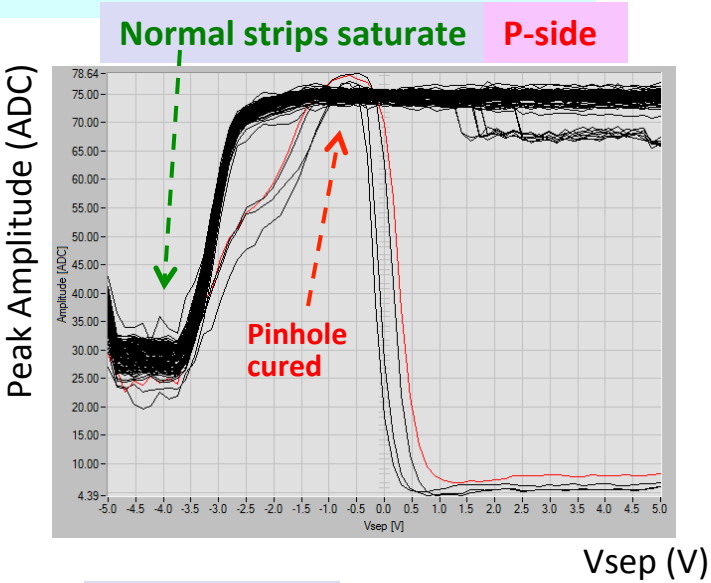
Only peak amplitude sampled & fine Vsep scan implemented on APVDAQ



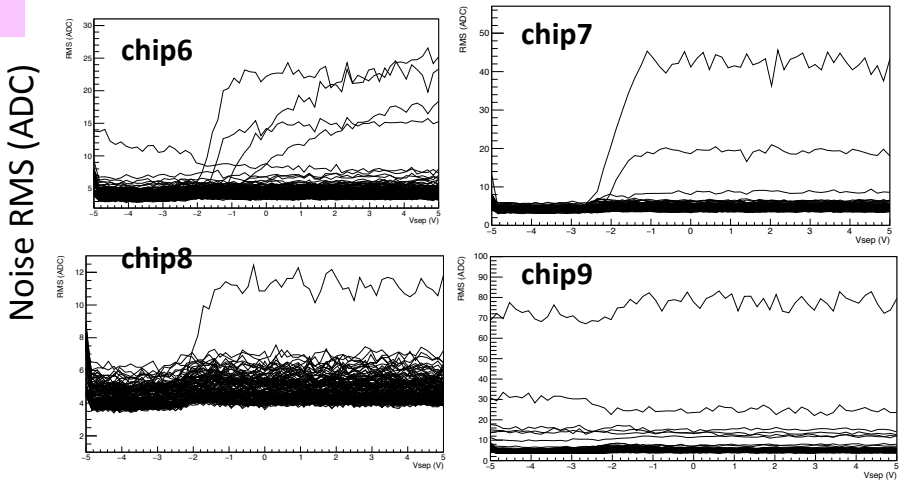
Vsep scan results

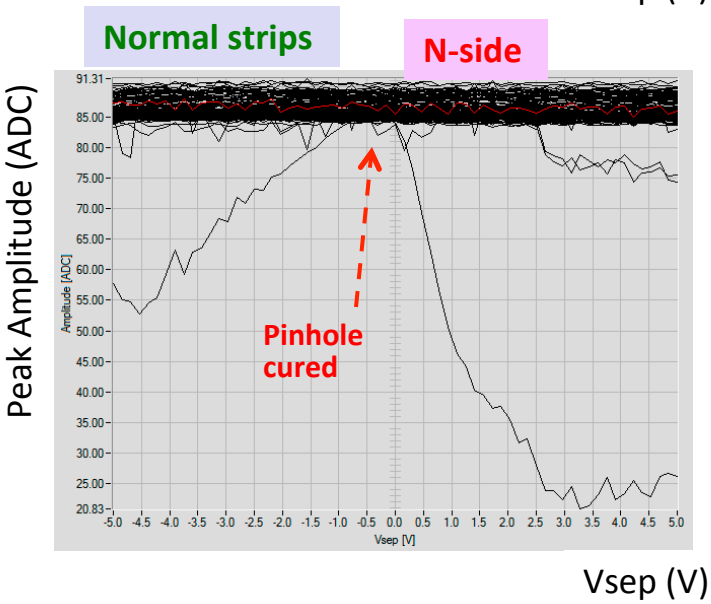
1. Whole chip saturation induced artificially with Vsep<-3V in chips with several pinholes connected
2. Single pinholes on p and n side cured
3. Some single strips noisy (not pinhole) can be cured : field plate effect of AC metal connected to the Vsep voltage via APV input (new effect under study)

- Vsep adds some degree of freedom on p and n side to compensate some defects



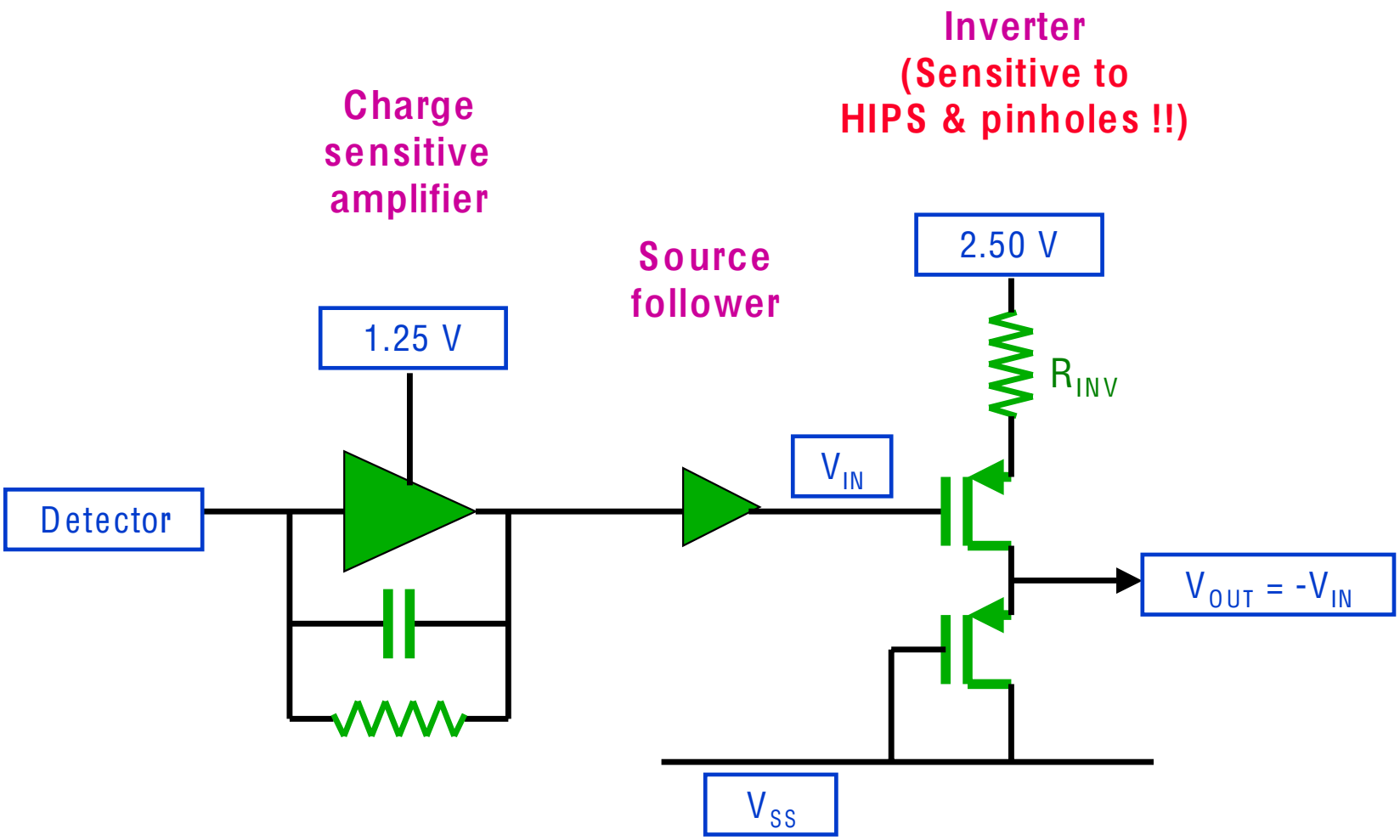
N-side





Backup

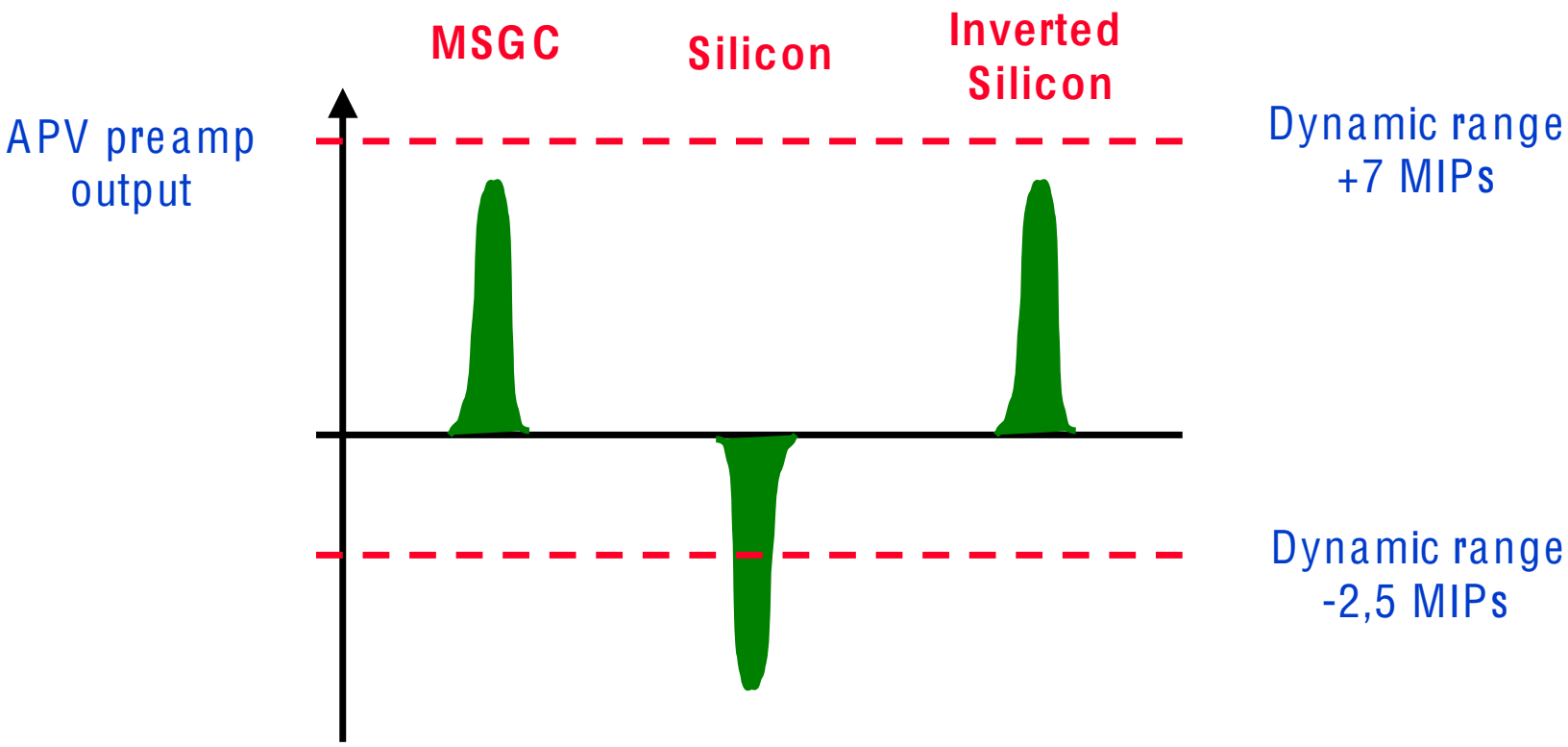
Introduction
Internal Workings of the APV



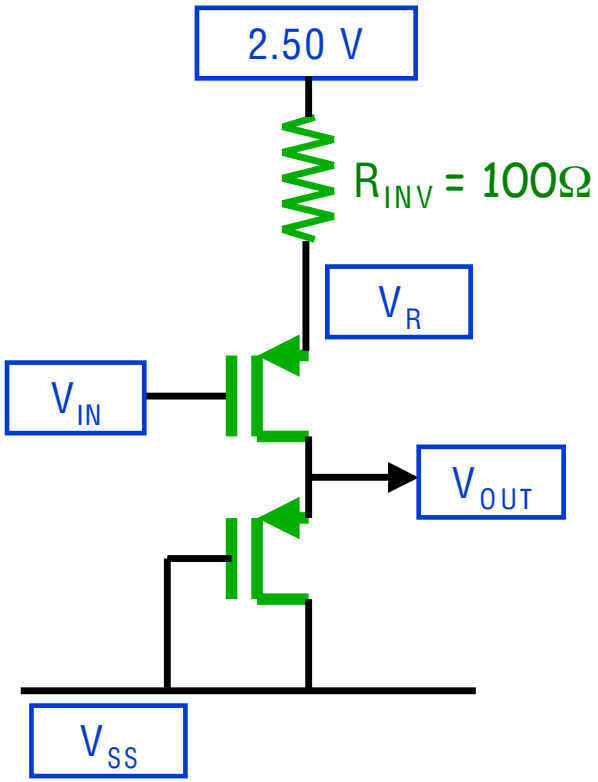
Introduction
Internal Workings of the APV

Why is the inverter there ?

– It increases APV dynamic range for silicon strip detector.



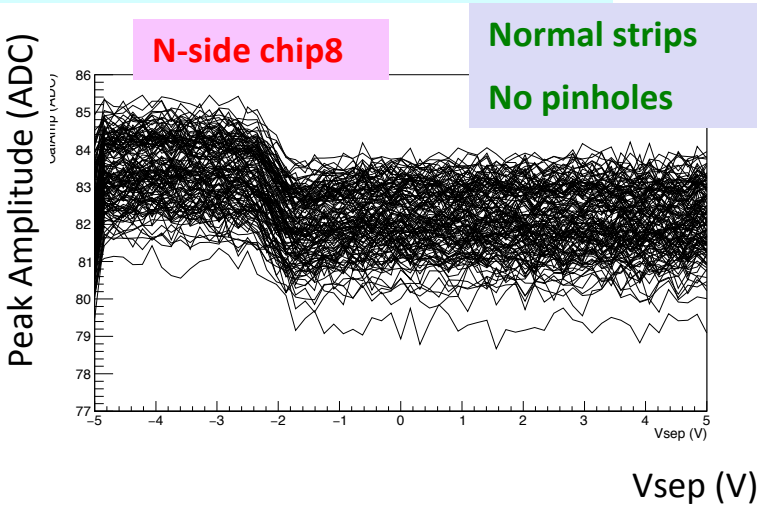
Introduction
How HIPs & Pinholes affect the APV



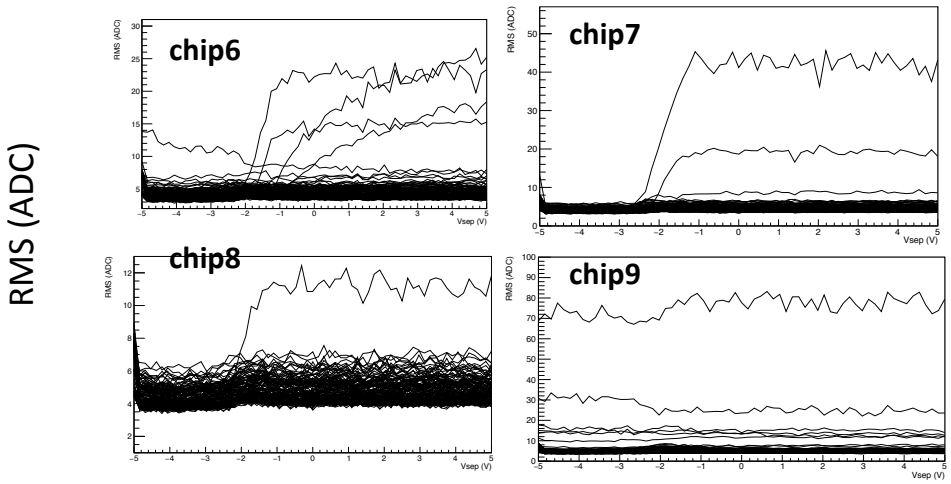
- **Big signal from silicon (holes) gives -ve pulse at V_{IN} :**
  - Inverter FET switches hard on, which steals current from 127 other inverters. (APV disabled until capacitor discharges.)
  - N.B. If R_{INV} were reduced, total current available to inverters would increase.
- **Leakage current via pinhole into APV :**
  - Same again, but permanent.
- **Leakage current via pinhole out of APV :**
  - Inverter FET switches hard off. Takes no current, so other 127 channels still work.

Vsep scan on n side HPK sensor

- Small (a few %) reduction of Calamp (and increase in caltmax) on all n side strip @ Vsep>-2V
- Some single strips become very noisy @ Vsep>-2V → Vsep<-2V can cure them!
- Other noisy strip not sensitive to Vsep



N-side



- Only seen on 1 HPK sensor
- Seen also on other sensor in HEPHY?

- Possible explanation for both effect:
  - field plate effect of AC metal connected to the Vsep voltage via APV input

Vsep scan on n side HPK sensor

1. Small reduction of Calamp (and increase in caltmax) on all n side strip @ Vsep>-2V
2. Some single strips become very noisy @ Vsep>-2V

- Possible explanation for both effects:
  - field plate effect of AC metal connected to the Vsep voltage via APV input
  - Negative voltage (Vsep<-2V) on AC n side metal reduces the extension of the electrons accumulation layer and reduces the effective width of n+ implant
  1. C interstrip, proportional to width /pitch, is reduced for all strips and consequently Calamp (increase) and Caltmax move (sensitive to the Capacitance connected to the APV input)
  2. When the extension of the n strip implant changes the localized defects at surface that can produce leakage current can/cannot contribute to the strip leakage current and noise increase/decrease.
- Field effect on AC metal could be studied on sensors (n and p side) and, to be pragmatic, effects on modules noise vs Vsep should be studied.
- We might find the best optimization for Vsep operation on n and p side to: cure pinholes, reduce the noisy strips

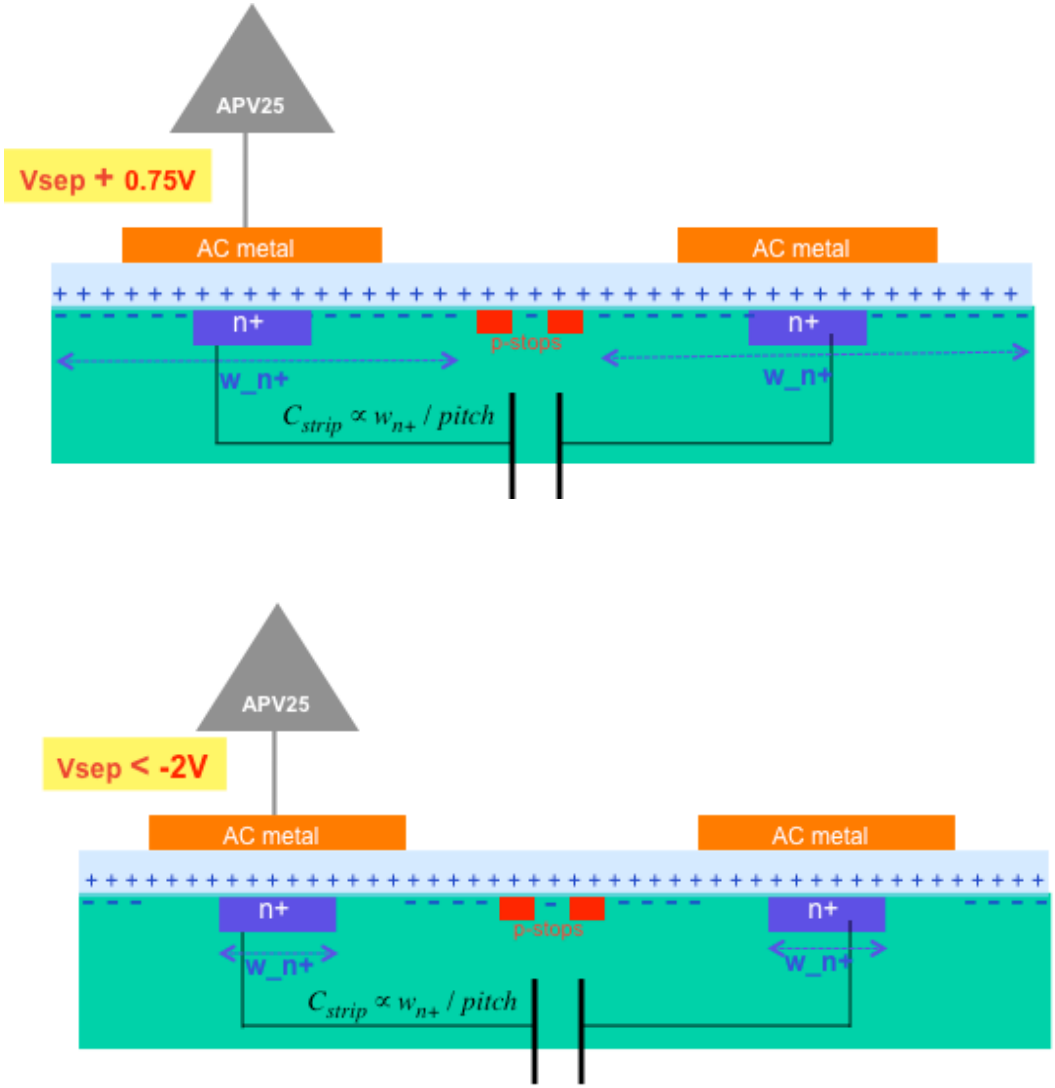
Vsep (V)

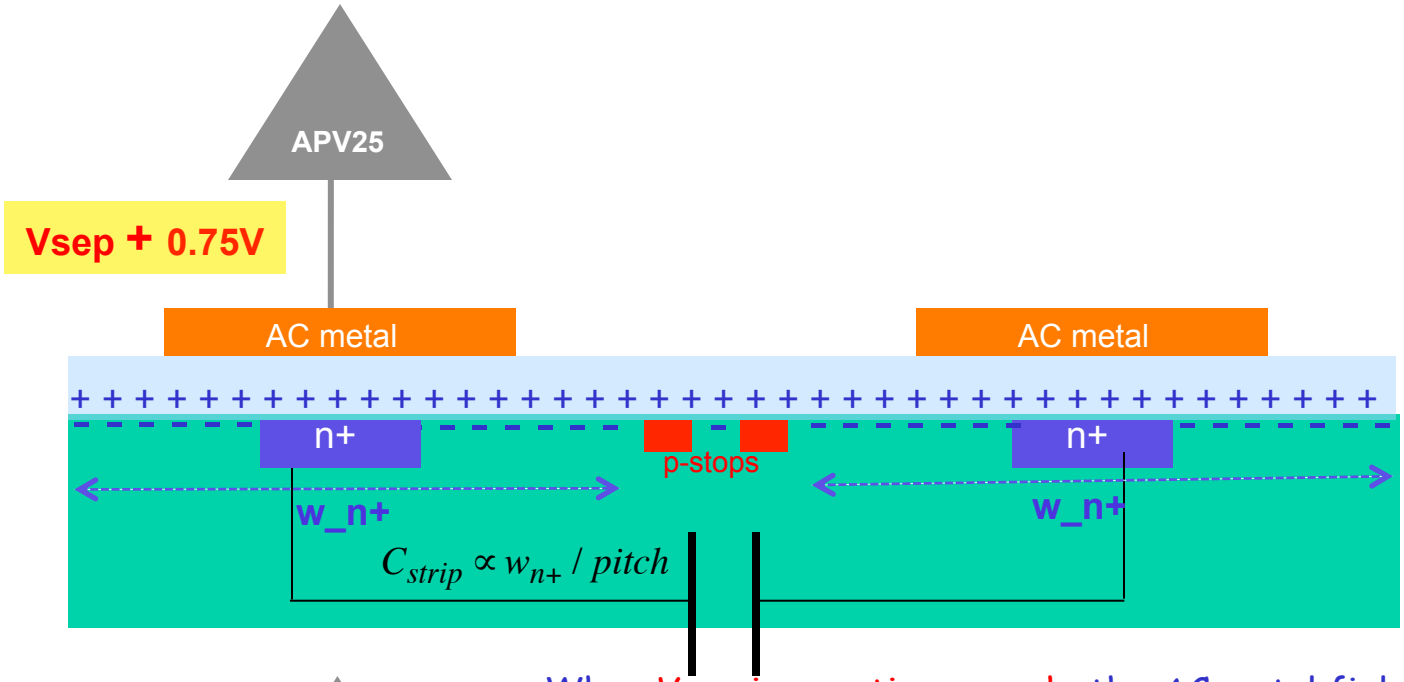
Vsep scan and field effect on AC metal

- With Vsep negative the AC metal acts as a field plate and reduces the accumulation layer estension close to the n+ strip implant → effective implant width w_n+ is reduced

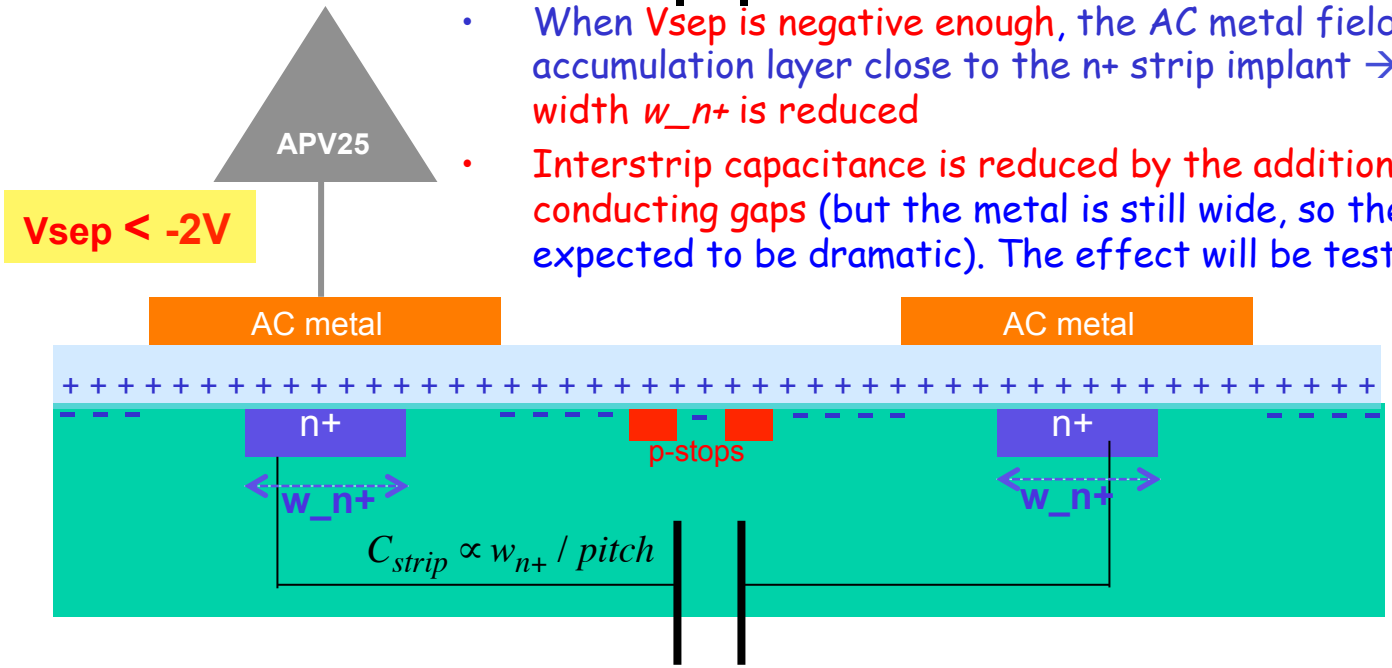
1. Interstrip capacitance, proportional to width/pitch, is reduced → Peak amplitude increases slightly

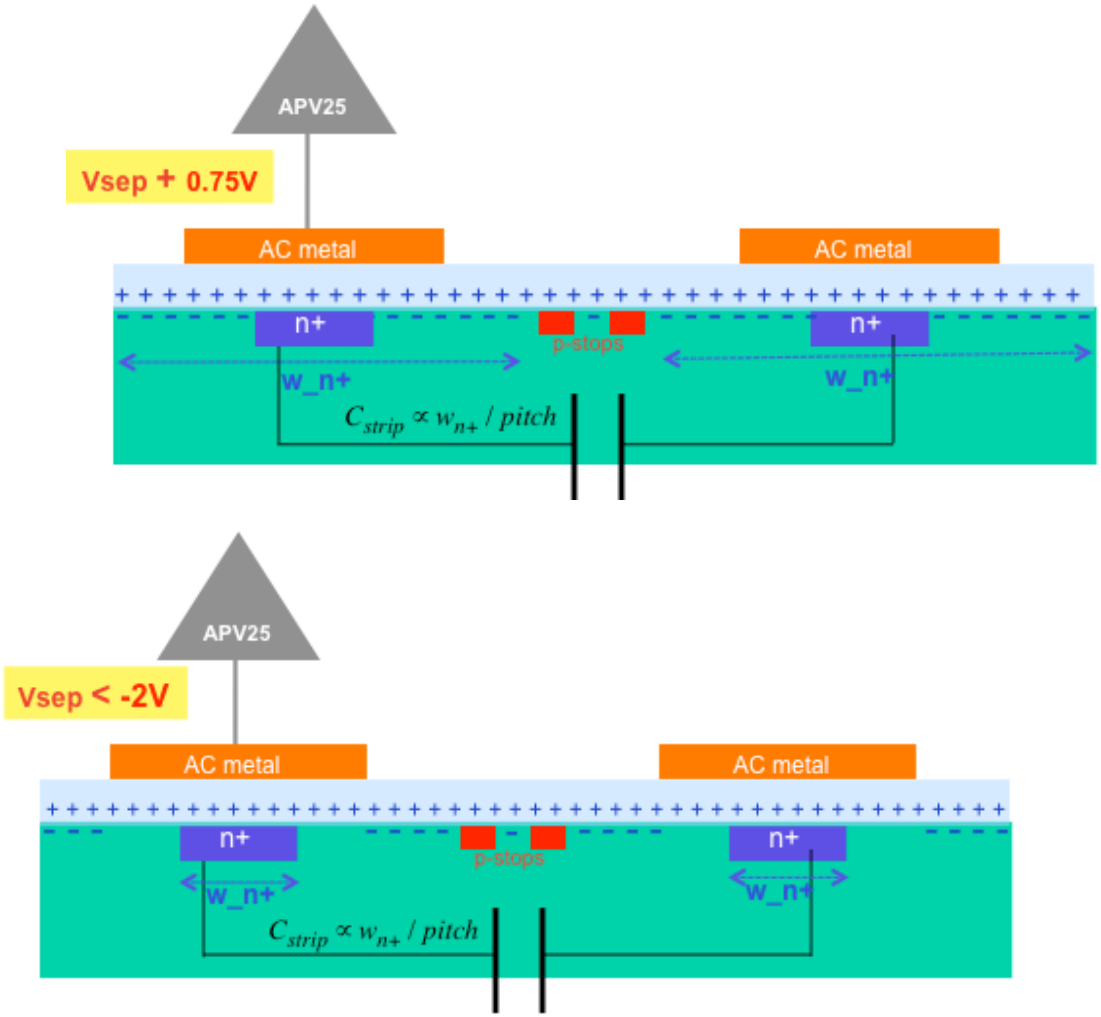
- The Electric field close to the n+ strip is modified by the field plate effect
  - Some defects very close to the surface Si-SiO2 (that can be the origin of high leakage current) can stop to contribute to the strip leakage current??
  - The peak electric field can be lowered, thus reducing the impact ionization in spots where localized defects are responsible for high field values.





- When Vsep is negative enough, the AC metal field plate depletes the accumulation layer close to the n+ strip implant → effective n-strip width *w_n+* is reduced
- Interstrip capacitance is reduced by the addition of two non-conducting gaps (but the metal is still wide, so the reduction is not expected to be dramatic). The effect will be tested on bare sensors.




APV25
Vsep + 0.75V
AC metal
AC metal
n+
n+
p-stops
w_n+
w_n+
$C_{strip} \propto w_{n+} / pitch$
APV25
Vsep < -2V
AC metal
AC metal
n+
n+
p-stops
w_n+
w_n+
$C_{strip} \propto w_{n+} / pitch$