AM06 chip status — Update

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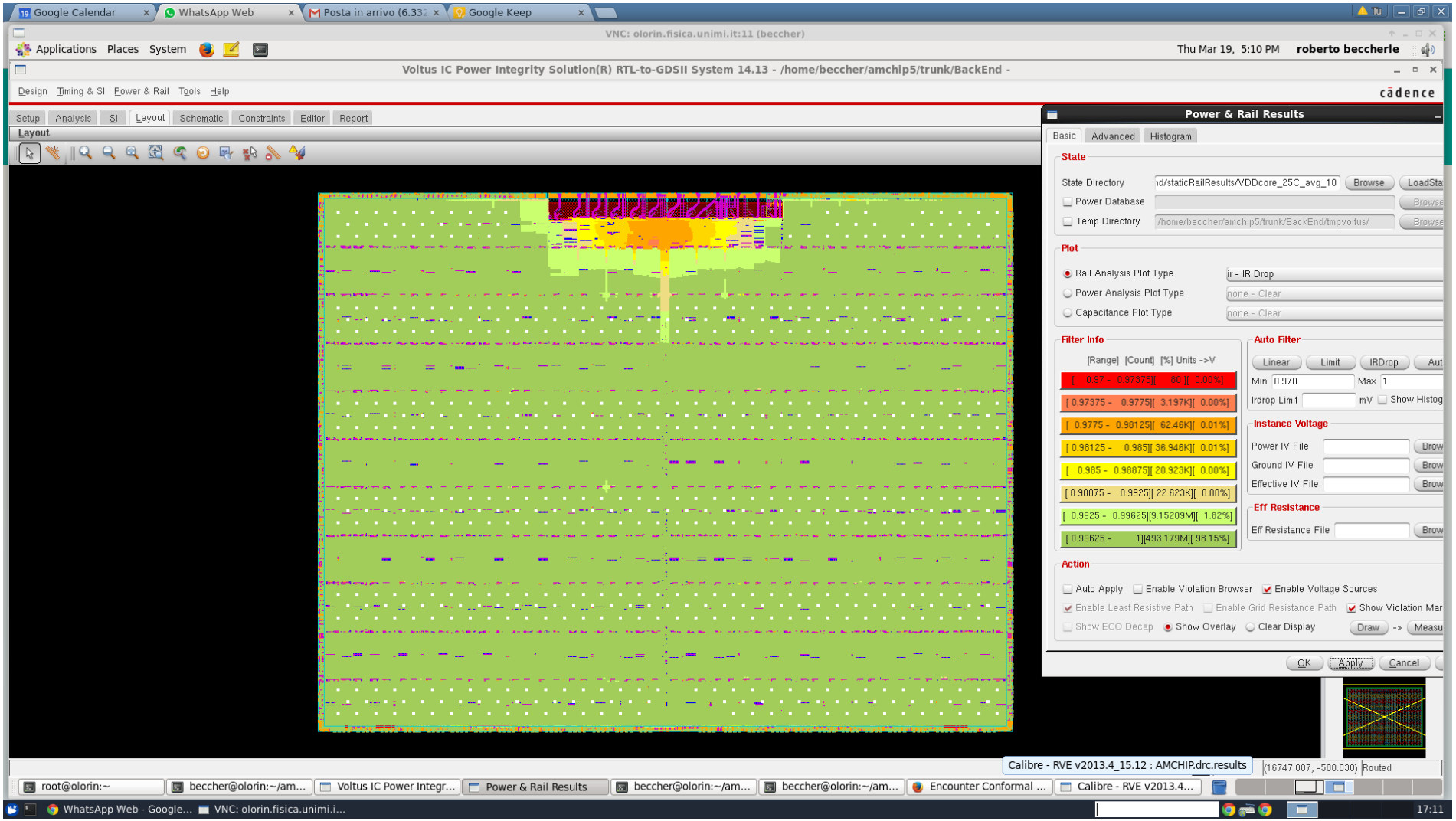
AM06 latest news

- **DRC: no errors**
- **LVS: no errors**
  - BUT: LVS performed in TWO steps, separately on the 2k block and on the top
  - TO TO: manual check at 2k block interface
- **Voltus simulation** (*IR* drop) **on VDD: ok**
  - to be performed also on VSS and on secondary supply nets
- **SELFTEST: ok**
- some **RUNTEST ERRORS**: few missed patterns and few extra patterns in the whole processing chain — a real problem or a simulation artefact?

Voltus simulation results



Max VDD drop: 27 mV