

# **AMBoard Report**

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## Outline

#### •AMBSLP\_V3: Associative Memory Board Serial Link Processor •PCB Design, changes after review

#### •LAMBSLP\_V2: Little Associative Memory Board Serial Link Processor •PCB Design

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•Measures, Tests, Schedule

•Firmware and Software status

# AMBSLP\_V3

- **Design Done**
- PCB will arrive in Pisa tomorrow
- We will perform tests And measure next week
- Ready for the final project in July '15



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- Power distribution
- Configuration through VME
- •Big FLASH 4Gbit for Patterns
- •Fix signal integrity issue



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#### Short Link = 5cm, Exp. BER $\approx 10^{-42}$



Long Link = 50cm, Exp. BER  $\approx 10^{-6}$ 

# LAMBSLP\_V2

**Design Done** 

**4 PCB arrived in January** 

Test HW and FW ok!

Next changes: Pinout for AMchip06 Add Temp Sensor Final design in May '15



#### **Firmware and Software Status**

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- Flowed some fake events without AMchips05 Feed Input data from AUXcard VME and loop on AMboard
- Sending and receiving data to/from the AMchip05
- Loss of Sync Module, checks whether all data streams process the same event (Done)

#### **Firmware and Software Status**

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# **Firmware and Software Status**

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Firmware and Software Status Next steps:

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- Add AMchip05 in the dataflow AUXCard + AMBoard (next weeks)
- •Check the SpyBuffer Freeze Logic Interrupt controller (next week) (see Calliope talk in Friday)
- Implement an automatic PRBS test for production phase (June)
- Remote programming through VME (next year)
- Store Pattern Bank on FLASH Memory (next year)

#### Conclusion

#### •AMBSLP\_V3: Test next week. Final design in July

#### •LAMBSLP\_V2: done, final version in May

# •Firmware and Software: focus on running events with the AMchip05 and AUXcard

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# **Thanks!**

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# Any questions?

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#### New simulation in April with the new boards and chips design

#### In July we will do test with the final boards and AMchip06

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