FTK workshop introduction

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FTK TDR schedule

Legenda																			
Asic submission																			
Stand-alone test		FTK global integration before production																	
Integrated test			- Global integration delayed (missing FW and SW)																
Global Integration & Commissioning											-				/				
Production - Installation		- Starting production before integration																	
Review																			
Installed																			
Months	6	7	8	9	10	11	12	1	2	3	4	5	6	7	8	9	10	11	12
Tasks				2014									20:	15					
Dual Output HOLA																			
Data Formatter +FTK Input Mezzanine		Globa	l Int					pro	duct	tion				com	imis	data	a tak	e	
AUX + SSB + FLIC	Global I		l Int						productio		uctio	on		sioning		1 AMB			
AMchip05		test		test															
AMchip06						t.c	out					test	t. p	rod					
AMBSLP-LAMBSLP				wΑ	M05	AUX						wAN	106		16	5 AM	Bs	com	mis

Installation timeline (from last AUW)

- Final dates depending on the Production Readiness Reviews (PRR)
- Most computing power in AUX+AMB+SSB: staged installation

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	IM	DF	AUX	AMB	AM	SSB	FLIC	Milestones	Expected		
1st	128	32	1	1	05	1	2	Included TDAQ	07/15		
2nd	128	32	16	1	06	8	2	Included TDAQ	09/15		
3rd	128	32	16	16	06	8	2	Full barrel (mu=40)	12/2015 no contingency		
4th	128	32	32	32	06	16	2	Full detector (mu=40)	Mid 2016 + 6 months		
Final	128	32	128	128	06	32	2	TDR Specs	2018 / Lumi driven		

Installation timoling (from last AUW)

Risks for "1st step":

- IPMC SW
- Full DF production (first batch expected by July)
- IM Artix 7 production
- Goal: get a few DFs fully integrated and taking data

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1st	128	32	1	1	05	1	2	Included TDAQ	07/15					
2nd	128	32	16	1	06	8	2	Included TDAQ	09/15					
3rd	128	32	16	16	06	8	2	Full barrel (mu=40)	12/2015 no contingency					
4th	128	32	32	32	06	16	2	Full detector (mu=40)	Mid 2016 + 6 months					
Final	128	32	128	 Risks for "2nd and 3rd steps": AM06+AMboard schedule (very tight) 										
- SSB PCB+FW finalization														

Last FTK schedule for LHCC

End of pp data taking

	Jan-15	Feb-15	Mar-15	Apr-15	May-15	Jun-15	Jul-15	Aug-15	Sep-15	Oct-15	Nov-15	Dec-15
FTK												
ATCA shelv	/es +					4 shelves						
VME crates	s +				1 crate				2 crates			
AM system	1	AM06 subn	nitted		AM06 rece	ived						
					>	> AM06 initial test 200 chips ready						
						>	10 LAMBs	assembled				
first AM bo	bard			FDR		1	>		1 AMB at P	1 and 1 in Pis	a	
						1			>	AMB PRR		
						>		all AM06 t	ested	1		
AM boards	6							>		>		16 at P1
IM Spartan	6					all at P1						
IM Artix7			PRR		10 at CERN		all at P1					
DF	PRR						8 at P1		all at P1			
AUX		PRR					4 at P1		16 at P1			
SSB				PRR			8 at P1					
FLIC							all at P1					
Software							end of 2015 setup ready					

Critical to get a full FTK slice taking data in September. Leaving October for debug/commissioning.