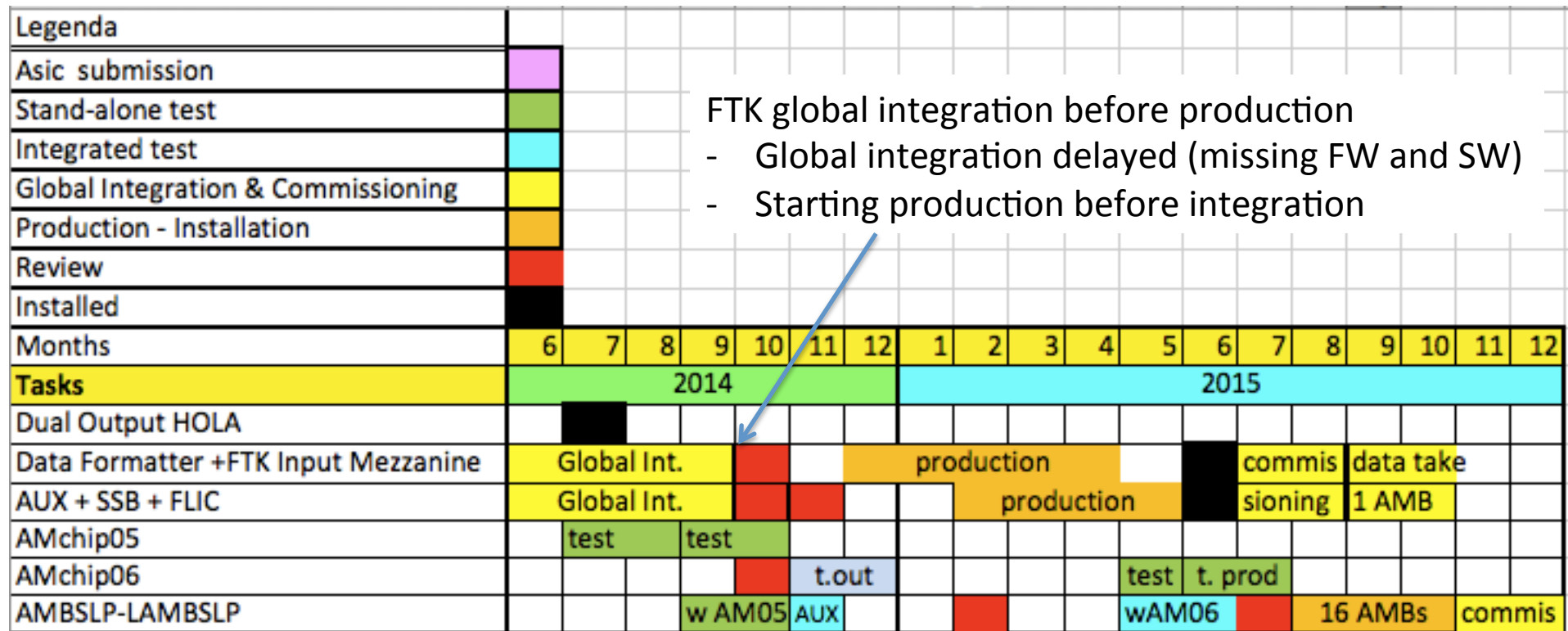


FTK workshop introduction


Alberto Annovi

FTK TDR schedule



Installation timeline (from last AUW)

- Final dates depending on the Production Readiness Reviews (PRR)
- Most computing power in AUX+AMB+SSB: staged installation



	IM	DF	AUX	AMB	AM	SSB	FLIC	Milestones	Expected
1st	128	32	1	1	05	1	2	Included TDAQ	07/15
2nd	128	32	16	1	06	8	2	Included TDAQ	09/15
3rd	128	32	16	16	06	8	2	Full barrel (mu=40)	12/2015 no contingency
4th	128	32	32	32	06	16	2	Full detector (mu=40)	Mid 2016 + 6 months
Final	128	32	128	128	06	32	2	TDR Specs	2018 / Lumi driven

Installation timeline (from last AUW)

Risks for “1st step”:

- IPMC SW
- Full DF production (first batch expected by July)
- IM Artix 7 production
- Goal: get a few DFs fully integrated and taking data

	IM	DF	AUX	AMB	AM	SSB	FLIC	Milestones	Expected
1st	128	32	1	1	05	1	2	Included TDAQ	07/15
2nd	128	32	16	1	06	8	2	Included TDAQ	09/15
3rd	128	32	16	16	06	8	2	Full barrel (mu=40)	12/2015 no contingency
4th	128	32	32	32	06	16	2	Full detector (mu=40)	Mid 2016 + 6 months
Final	128	32	128						Open

Risks for “2nd and 3rd steps”:

- AM06+AMboard schedule (very tight)
- SSB PCB+FW finalization

Last FTK schedule for LHCC

End of pp data taking



	Jan-15	Feb-15	Mar-15	Apr-15	May-15	Jun-15	Jul-15	Aug-15	Sep-15	Oct-15	Nov-15	Dec-15
FTK												
ATCA shelves + ...						4 shelves						
VME crates + ...					1 crate				2 crates			
AM system		AM06 submitted			AM06 received							
					-->	AM06 initial test 200 chips ready for usage						
					-->	10 LAMBs assembled						
first AM board				FDR			-->		1 AMB at P1 and 1 in Pisa			
									-->	AMB PRR		
						-->		all AM06 tested				
AM boards								-->	-->		16 at P1	
IM Spartan6						all at P1						
IM Artix7			PRR		10 at CERN		all at P1					
DF	PRR						8 at P1		all at P1			
AUX		PRR					4 at P1		16 at P1			
SSB				PRR			8 at P1					
FLIC							all at P1					
Software							end of 2015 setup ready					

**Critical to get a full FTK slice taking data in September.
Leaving October for debug/commissioning.**