Phase-1 upgrades

RPC miniworkshop

Roma 26 marzo 2015

Summary

- Barrel Sector Logic to MuCTPi Interface Board for Phase-I

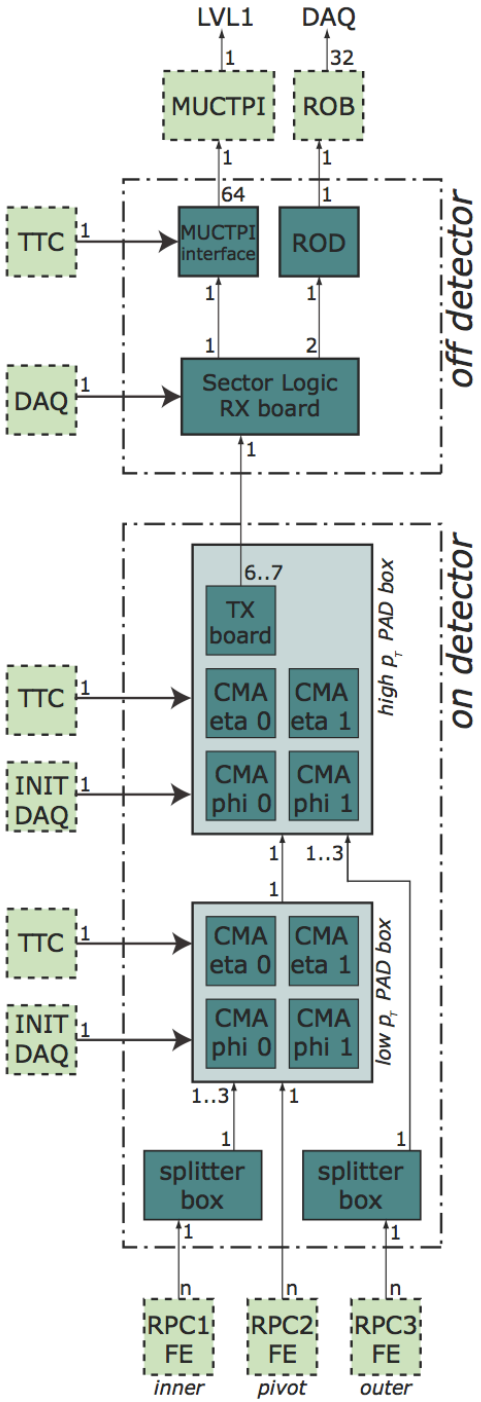
- The PAD Trigger Logic Board

- The BIS78 Project

Barrel Sector Logic to MuCTPi Interface Board for Phase-I

R.Giordano, V.Izzo, S.Perrella, A.Salamon, R.Vari

RPC trigger path to MuCTPI



RPC Data from Front-end to Coincidence Matrix (CM) and PAD

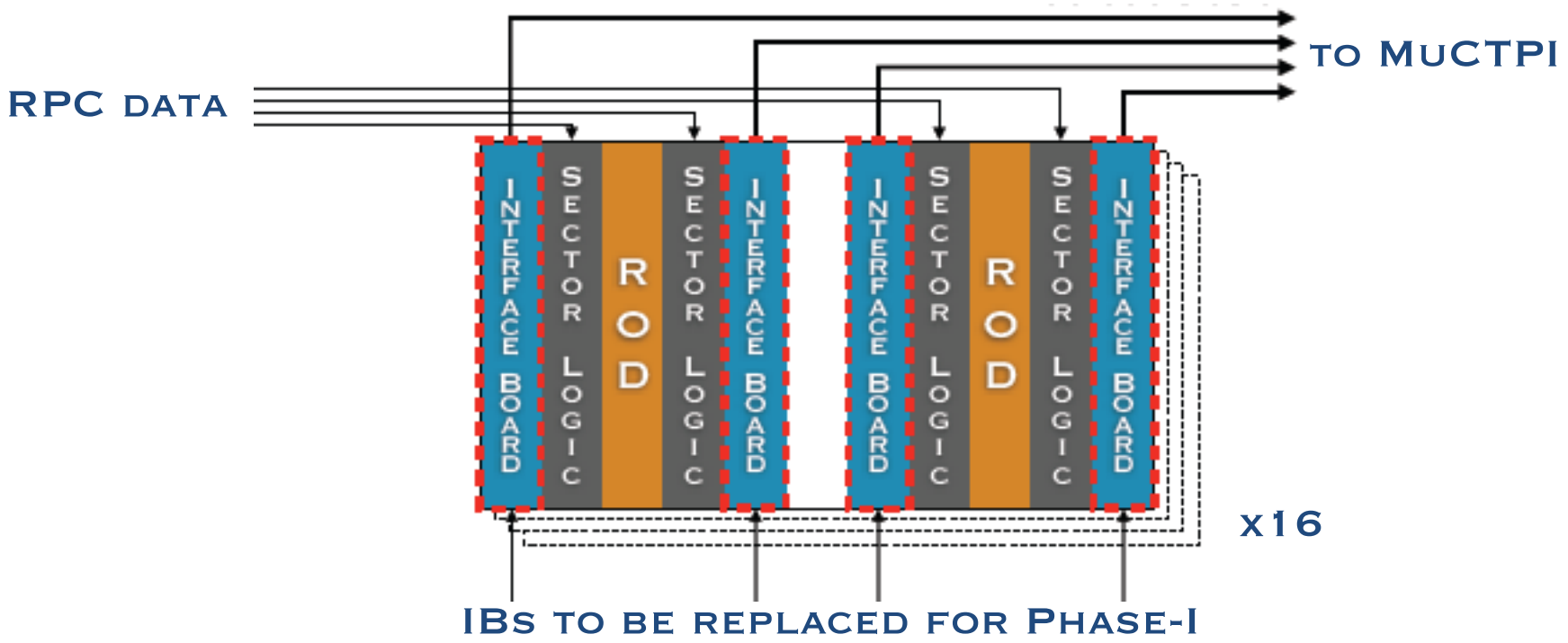
Then transferred via Optical Link (G-Link) to off-detector

RPC Trigger data received in USA15 by Sector Logic

Then transferred to MuCTPI via MuCTPI Interface board on copper cables

Motivation of the optical upgrade

USA15 L1 Barrel DAQ Crates

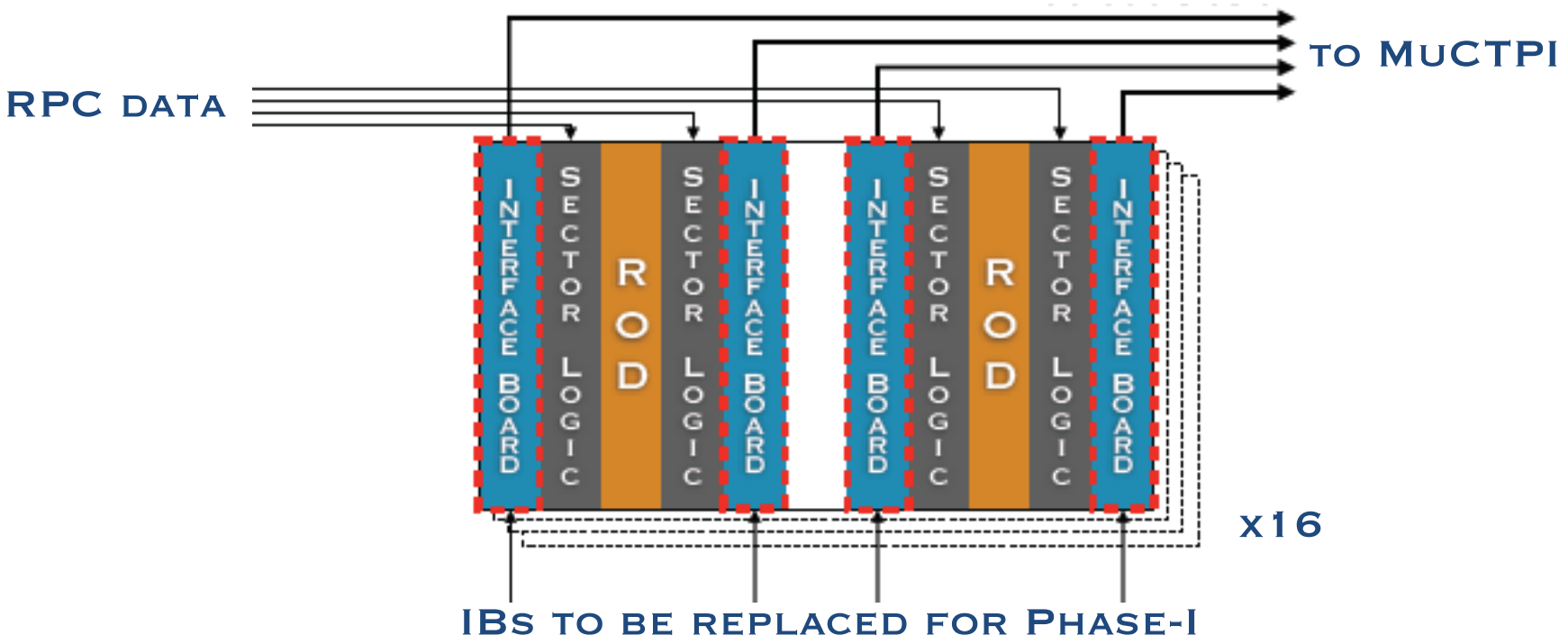


Necessary since the new MuCTPi for Phase-I will accept optical input only

The new end-cap sector logic will go optical as well.

Motivation of the optical upgrade

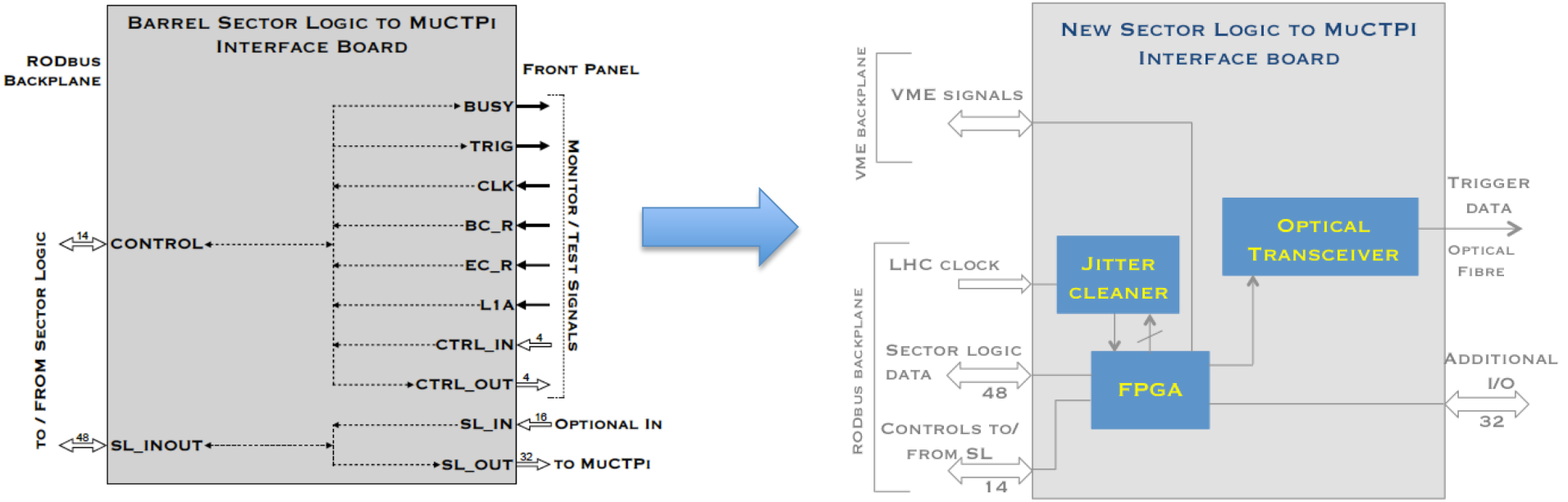
USA15 L1 Barrel DAQ Crates



64 SL-MuCTPi VME interface boards + 64 copper cables will be replaced with:

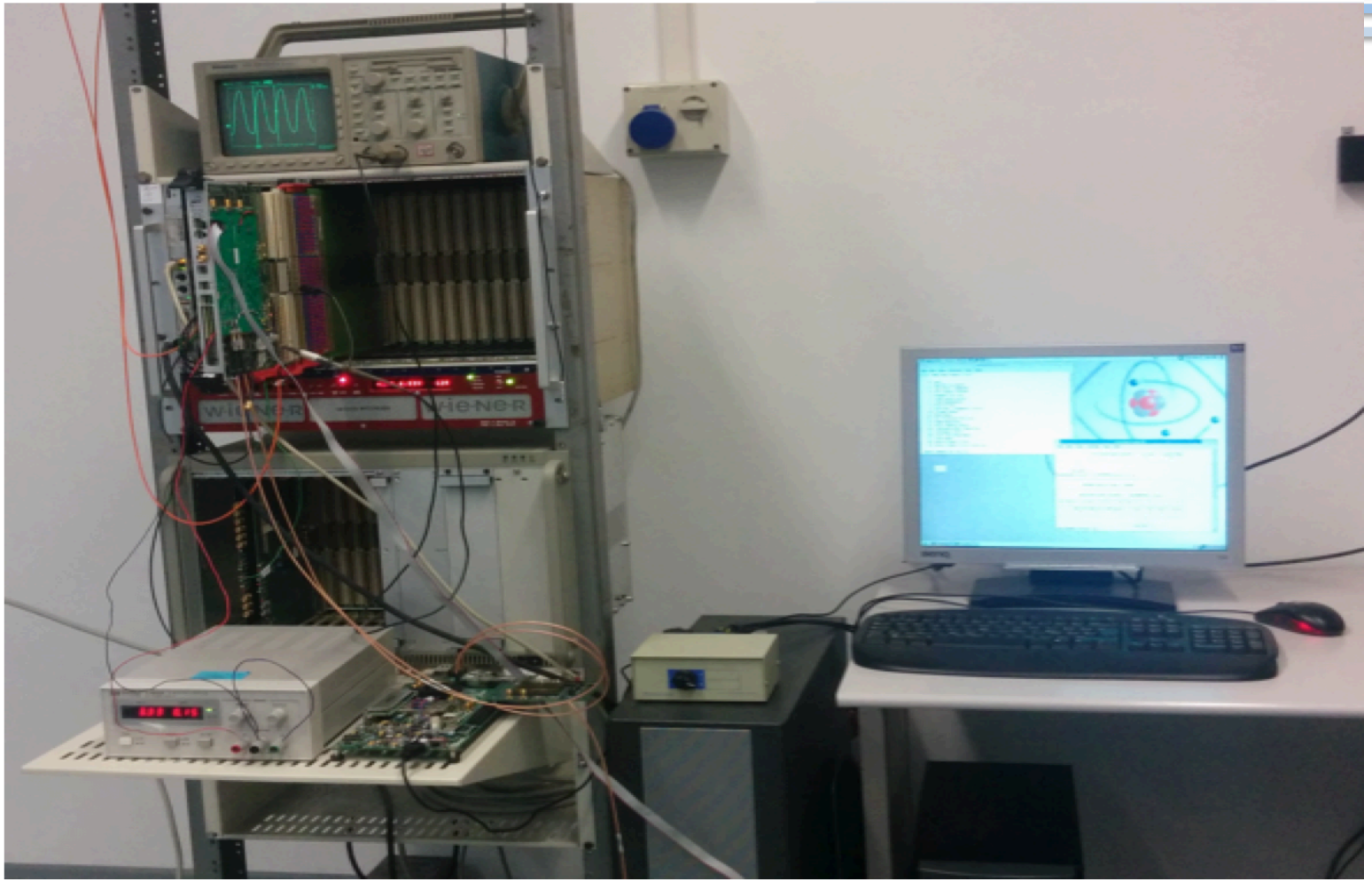
64 new interface boards (same VME crates) + 64 new optical fibers

New Interface Board



- FPGA used to connect to VME and backplane and to serialize data
- Optical SFP+ transceiver, Data Rate: 6.4 Gb/s → 160 bit @ 40 MHz
- Additional 32 bit I/O signals foreseen on the IB front panel
- Serializer logic must be synchronized with the 40 MHz LHC clock
- up to 4 BCs additional L1 latency

Preliminary tests



TTC clock signal correctly propagated on VME backplane and received by a Jitter cleaner

Presently, we are performing jitter measurements on the received signal, in order to evaluate the impact of the physical layer on the signal integrity of the clock itself

Plans

2014.12: Interface Board preliminary implementation on FPGA demo board

2015.02: PDR

2016.Q1: first prototype

2016.Q3: FDR

2017.Q1: PRR

2017.Q2: production

2018.Q1: installation and commissioning

2015-2018: software development (test software and integration into TDAQ framework)

Manpower

Interested Institutes:

INFN group	FTE	Work
INFN Roma	0.2 physicist 0.1 engineer	Main board schematic, test software, test & commissioning
INFN Napoli	0.3 physicist	Board layout, optical link, DAQ software
INFN Tor Vergata	0.1 physicist	Main Board schematic, interface with SL board

Total FTE number (0.7 FTE/Year) fulfills the requirements

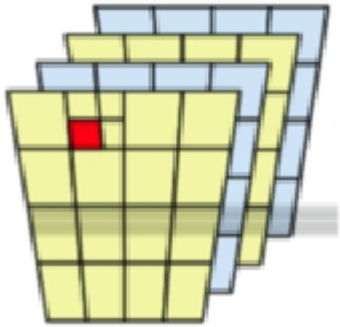
Design done in collaboration with CERN CTP/MuCTPi group to define common parts (same optical interface and transmission protocol)

The NSW PAD Trigger Logic Board

V.Izzo, S.Perrella, R.Vari

sTGC Segmentation

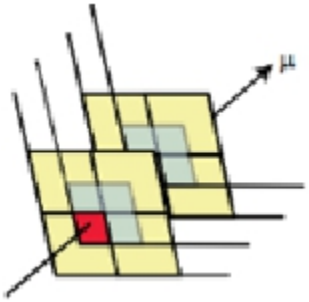
16 sTGC sectors per NSW wheel.



Each sector is divided in inner, middle and outer region.

2 sTGC quadruplets (pivot + confirm) per sector.

4 layers of Pads and 4 layers of strips per quadruplet.



Pads are staggered by half length in eta and phi on the 4 layers.

A logical Pad is defined by the projection of the physical Pads in the different layers (1/4 of the Pad area).

sTGC Trigger Logic

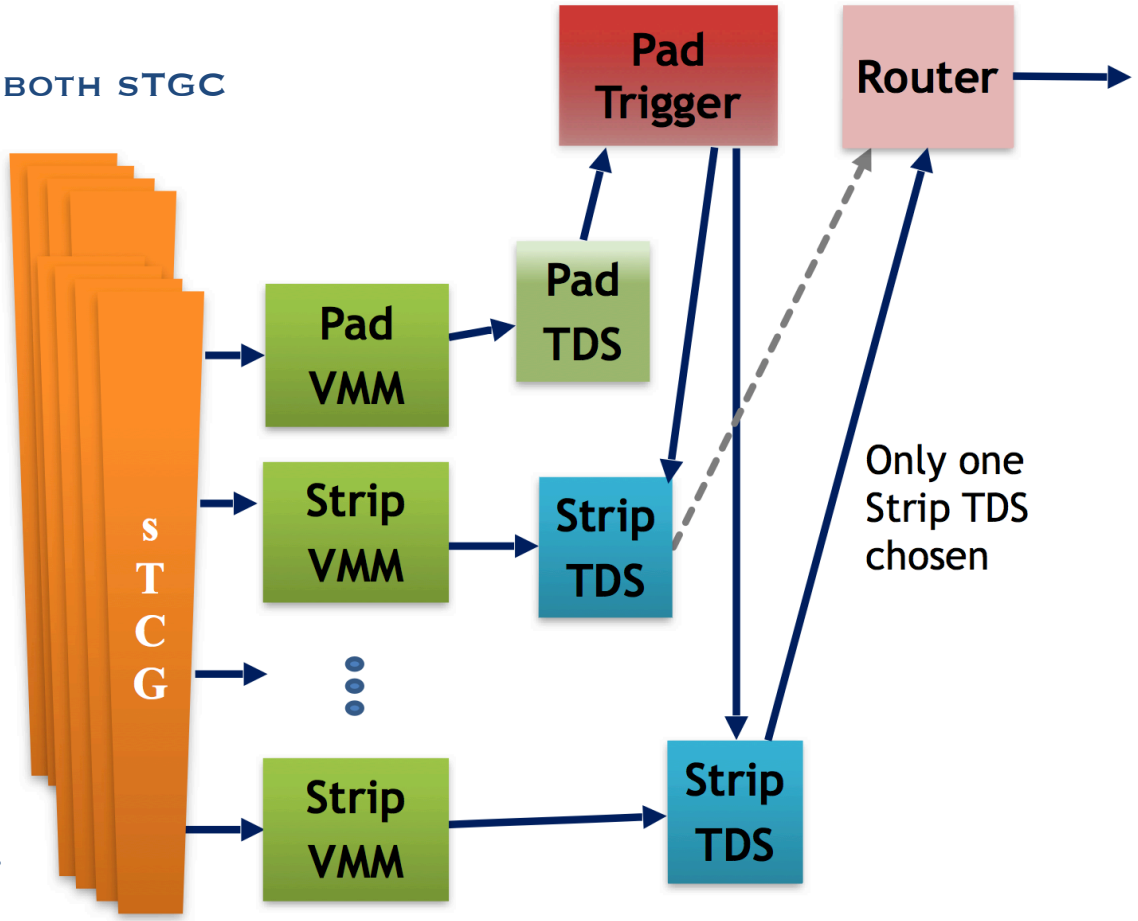
Find a Pad hit coincidence in a tower of logical Pads within one Bunch Crossing.

3/4 Majority logic is required on both sTGC quadruplet.

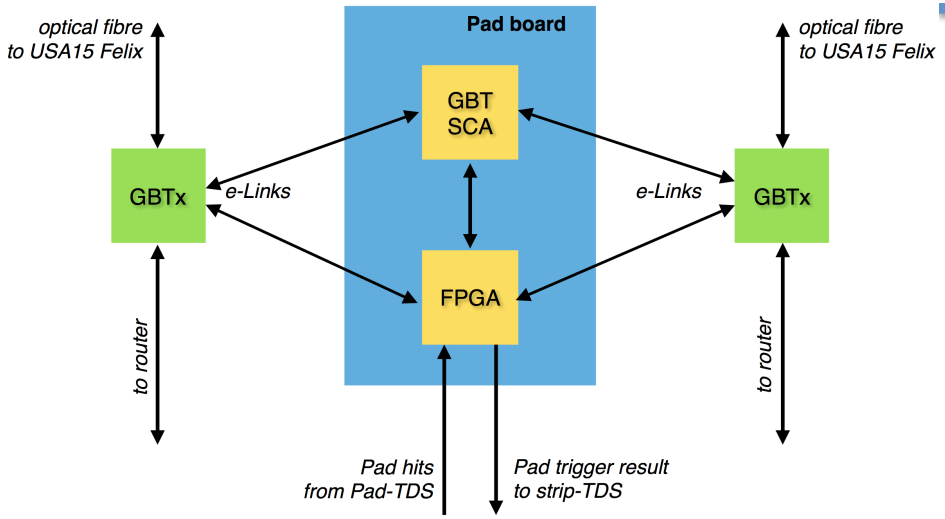
Candidate geometrical coordinates and BCID sent to the front-end strip-TDS chips.

Strip-TDS sends only selected strip data to the routers

16 Pad trigger logic boards on the rim of one wheel (1 per sector), for a total of 32 boards.



PAD Logic Board I/O signals



Bi-directional: GBTx E-links from 2 GBTx (total number of E-links to be defined, most probably 1-2 for the clock(s), 1 for the GBT-SCA, 1-2 for the readout, so up to 5 E-links per GBTx).

Input: sTGC Pad hit signals from front-end Pad-TDS chips (24 serial lines on TwinAX cables)

Output: Pad logic trigger result (up to 3 trigger candidates) to front-end strip-TDS chips (5/6 serial lines on TwinAX cables).

All I/O signals make use of differential LSVS or LVDS standards

FPGA Trigger Logic

Each BC the sTGC Pad hit serial data is sampled, deserialised and BCID tagged:

- 4.8 Gb/s per serial line = 120 bit @ 40 MHz ➜ 20 bit @ 240 MHz from each GTX

trigger logic based on coincidence windows to look for a 3/4 majority on each of the two sTGC quadruplet

The trigger logic is performed independently and simultaneously on three sTGC regions (inner, middle, outer), so that up to three independent trigger words can be produced

The output trigger word is then serialised and sent to the front-end strip-TDS chips:

- Kintex-7 OSERDES serialisers, 640 Mb/s (320 MHz DDR) per line (14-bit word)

A local fan-out on the front-end boards may be needed to transmit the trigger data to all strip-TDS chips

Plans & Manpower

Rome1 and Naples INFN groups are involved so far

2015 Feb.	Preliminary Design Review
2015 Dec.	First Pad board prototype
2016 May	Final Design Review
2016 Sep.	Second Pad board prototype
2017 Apr.	Production Readiness Review
2017 Jun.	production of the 32 Pad boards + 4/5 spares
2017 Sep.	installation and commissioning

The BIS78 project

INFN: bologna, napoli, Roma1, Roma2
MPI (Munich), U Michigan, USTC

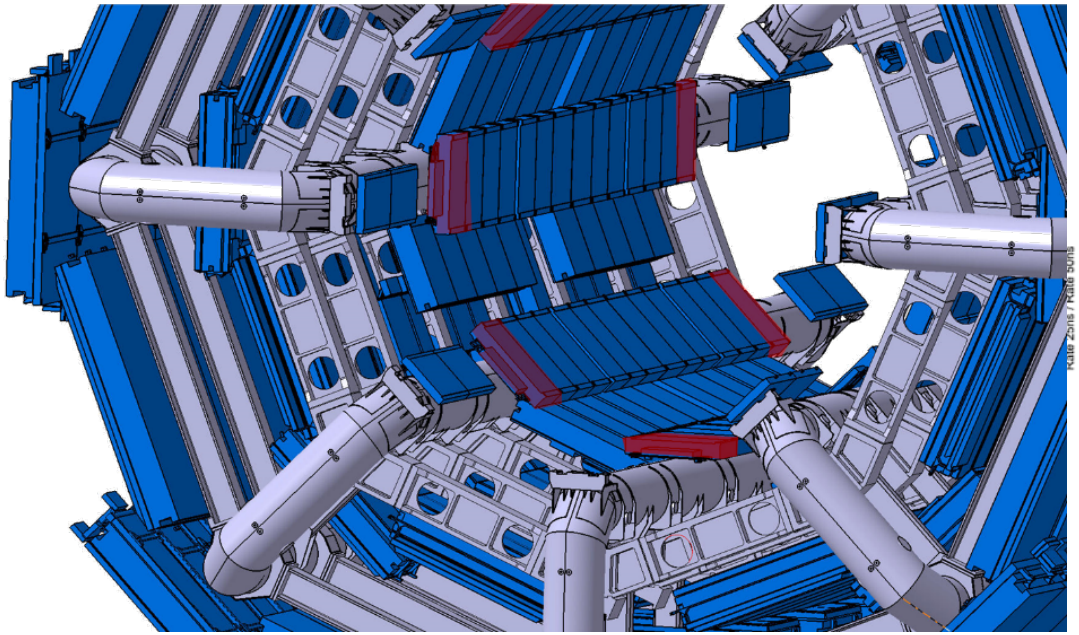
The BIS78 project

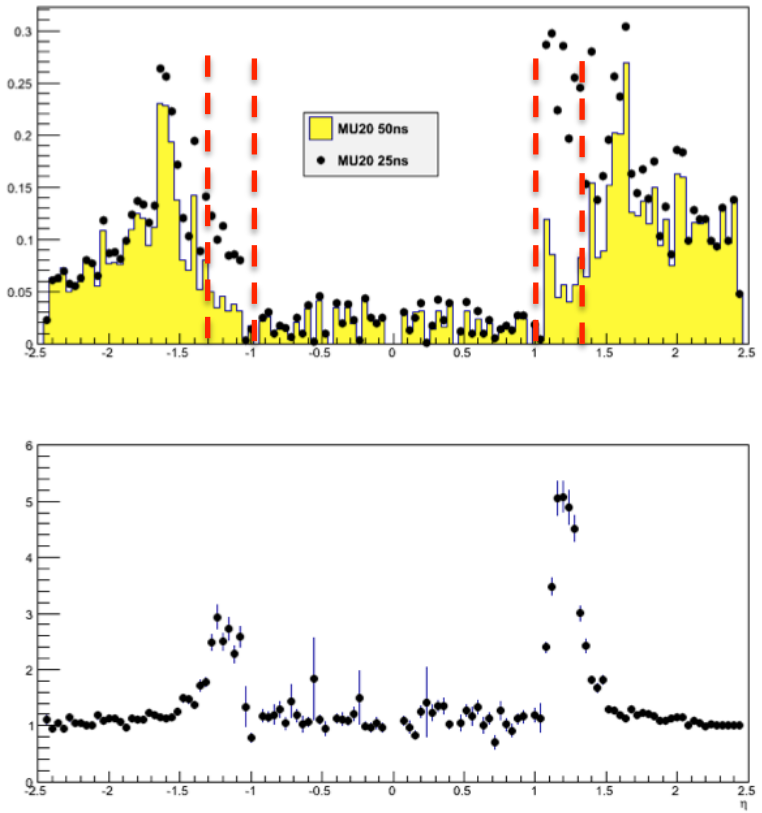
The Barrel/EndCap transition region (1 < eta < 1.3), not covered by the NSW, will suffer from high trigger fake rate with increasing luminosity.

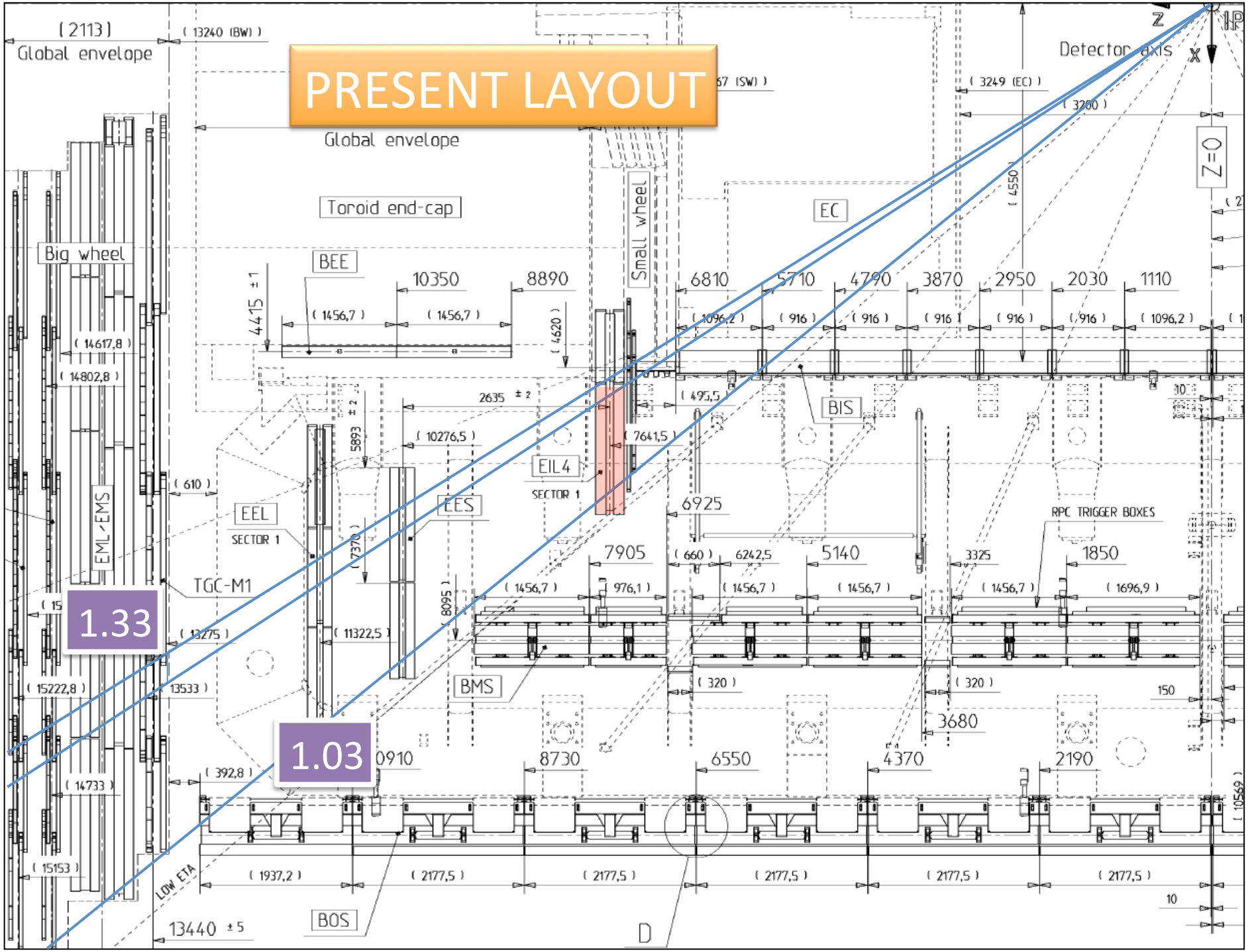
The proposed additional RPC chambers in the Barrel Inner Small region (16 new stations) can significantly reduce the foreseen fake rate.

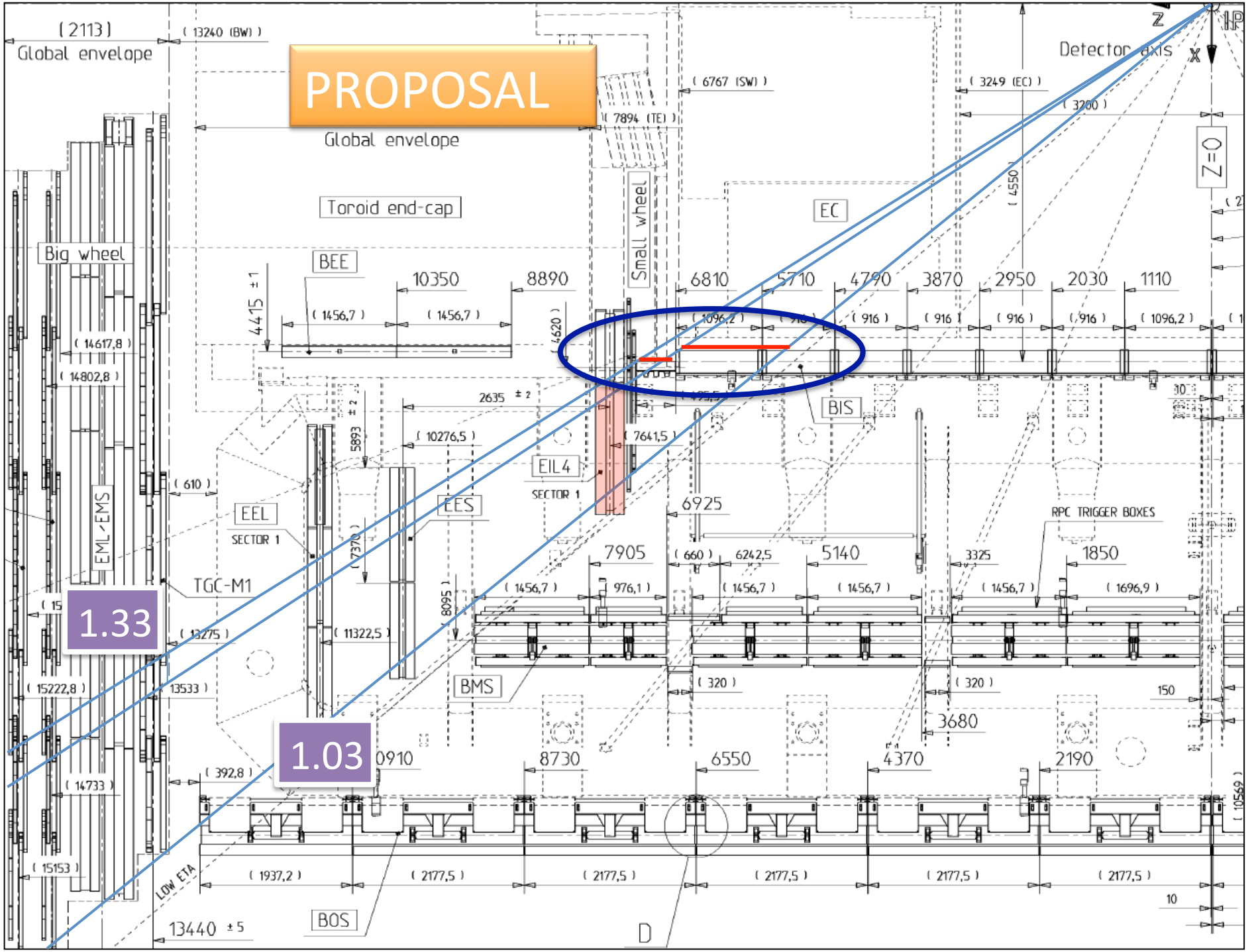
K.Nagano

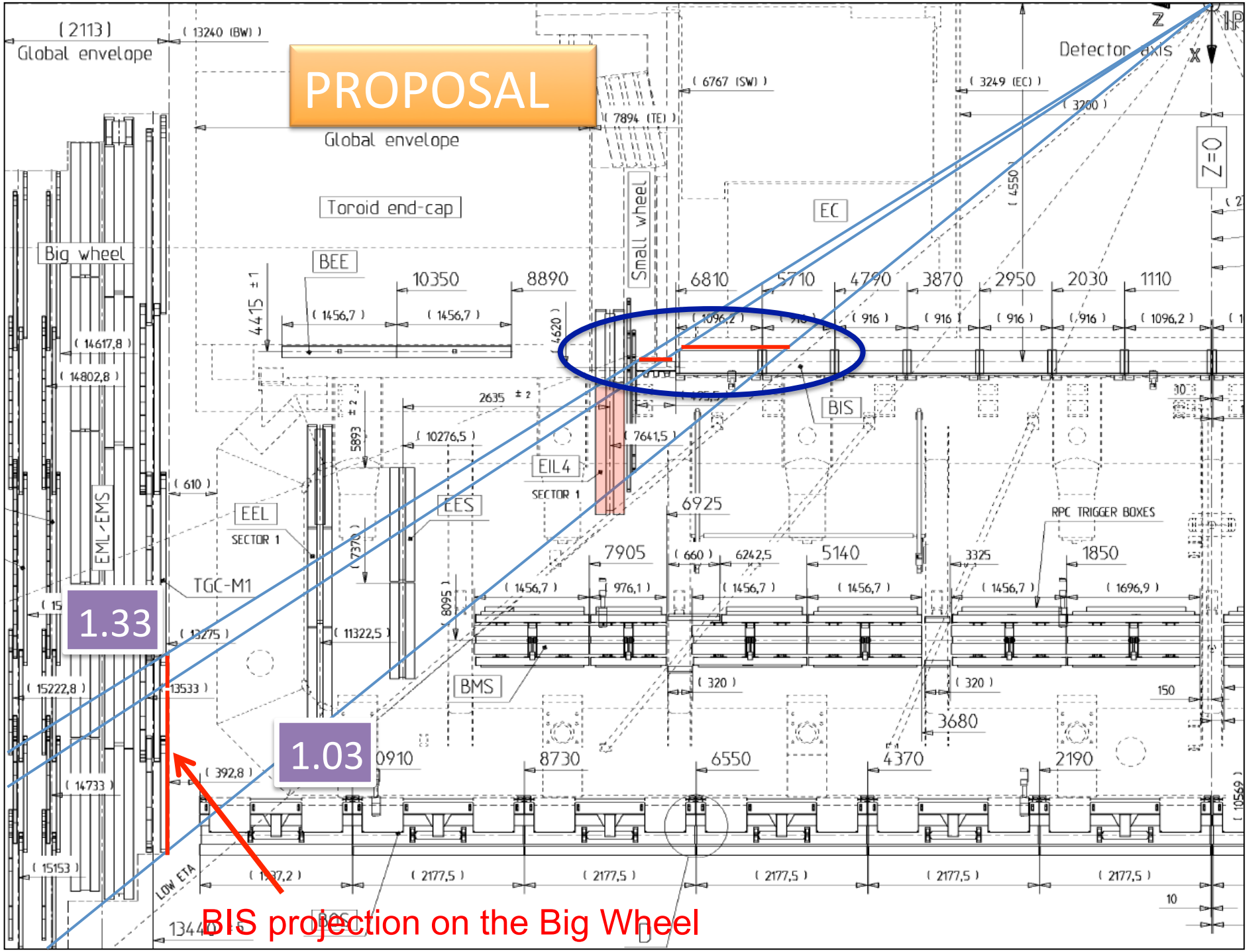
BIS78 on-detector electronics (16 Pads) will receive RPC hits and send the muon trigger candidate data to the End-Cap Sector Logic boards in USA15.






PRESENT LAYOUT
(2113)
Global envelope
(13240 (BW))
Global envelope
Toroid end-cap
Big wheel
Small wheel
EC
BEE
BIS
EIL4
SECTOR 1
EEL
SECTOR 1
EES
EML-EMS
TGC-M1
BMS
BOS
LOW ETA
RPC TRIGGER BOXES
Detector axis
Z
X
IP
Z=0
1.33
1.03
(3249 (EC))
(3200)
(4550)
4415 ±1
(4620)
10350
8890
(1456,7)
(1456,7)
6810
5710
4790
3870
2950
2030
1110
(1096,2)
(916)
(916)
(916)
(916)
(916)
(1096,2)
(14617,8)
(14802,8)
(610)
2635 ±2
5893 ±2
(10276,5)
(7641,5)
(495,5)
(7370)
(11322,5)
(13275)
13533)
(15222,8)
(14733)
(15153)
(392,8)
13440 ±5
6925
7905
(660)
6242,5
5140
3325
1850
(1456,7)
976,1)
(1456,7)
(1456,7)
(1456,7)
(1696,9)
8095)
(320)
(320)
150
3680
0910
8730
6550
4370
2190
(1937,2)
(2177,5)
(2177,5)
(2177,5)
(2177,5)
(2177,5)
(10569)
10
D


PROPOSAL
Global envelope
Toroid end-cap
Big wheel
Small wheel
EC
BEE
BIS
EIL4
SECTOR 1
EEL
SECTOR 1
EES
EML-EMS
TGC-M1
BMS
BOS
LOW ETA
RPC TRIGGER BOXES
Detector axis
Z=0
1.33
1.03


PROPOSAL
Global envelope
Toroid end-cap
Big wheel
Small wheel
EC
BEE
BIS
EIL4
SECTOR 1
EEL
SECTOR 1
EES
EML-EMS
TGC-M1
BMS
RPC TRIGGER BOXES
Detector axis
Z=0
1.33
1.03
LOW ETA
BIS projection on the Big Wheel

BIS78 RPC Trigger path

Each BIS78 RPC chamber will be equipped with about 400 strips (triplet, eta+phi).

One RPC front-end electronics board will read most probably 16 strips and sample each strip hit with 7-bit time information (sampled every 25 ns).

Data coming from 24 FE boards will be serially sent to one Pad board on TwinAx cables.

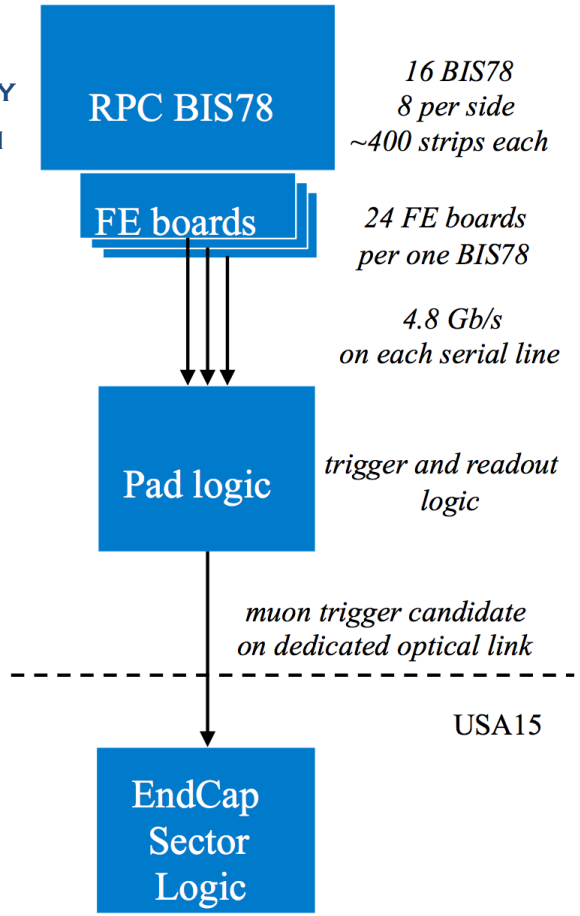
FE_to_Pad serial line bandwidth: 4.8 Gb/s (up to 6.4 Gb/s).

No zero-suppression transmission: 112 Gb/s total raw hit pattern data to be received and processed by one Pad board

Trigger result will be sent to the USA15 EndCap Sector Logics on dedicated optical links.

Optical fan-out needed in USA15 for matching one Pad fibre to 2 or 3 Sector Logic boards.

Under study the possibility to send more than 7-bit time info per each strip (either increasing the number of Pad inputs (up to 32) and/or increasing the FE_to_Pad BW (up to 6.4 Gb/s)



BIS78 RPC Readout path

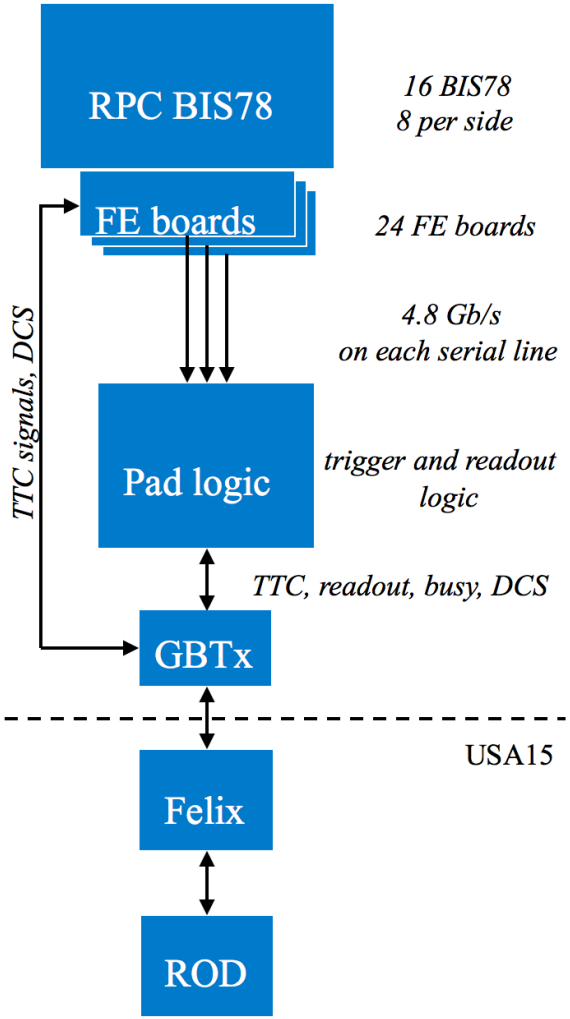
The Pad board will perform the readout logic too.

Readout latency should be compatible with Phase-II.

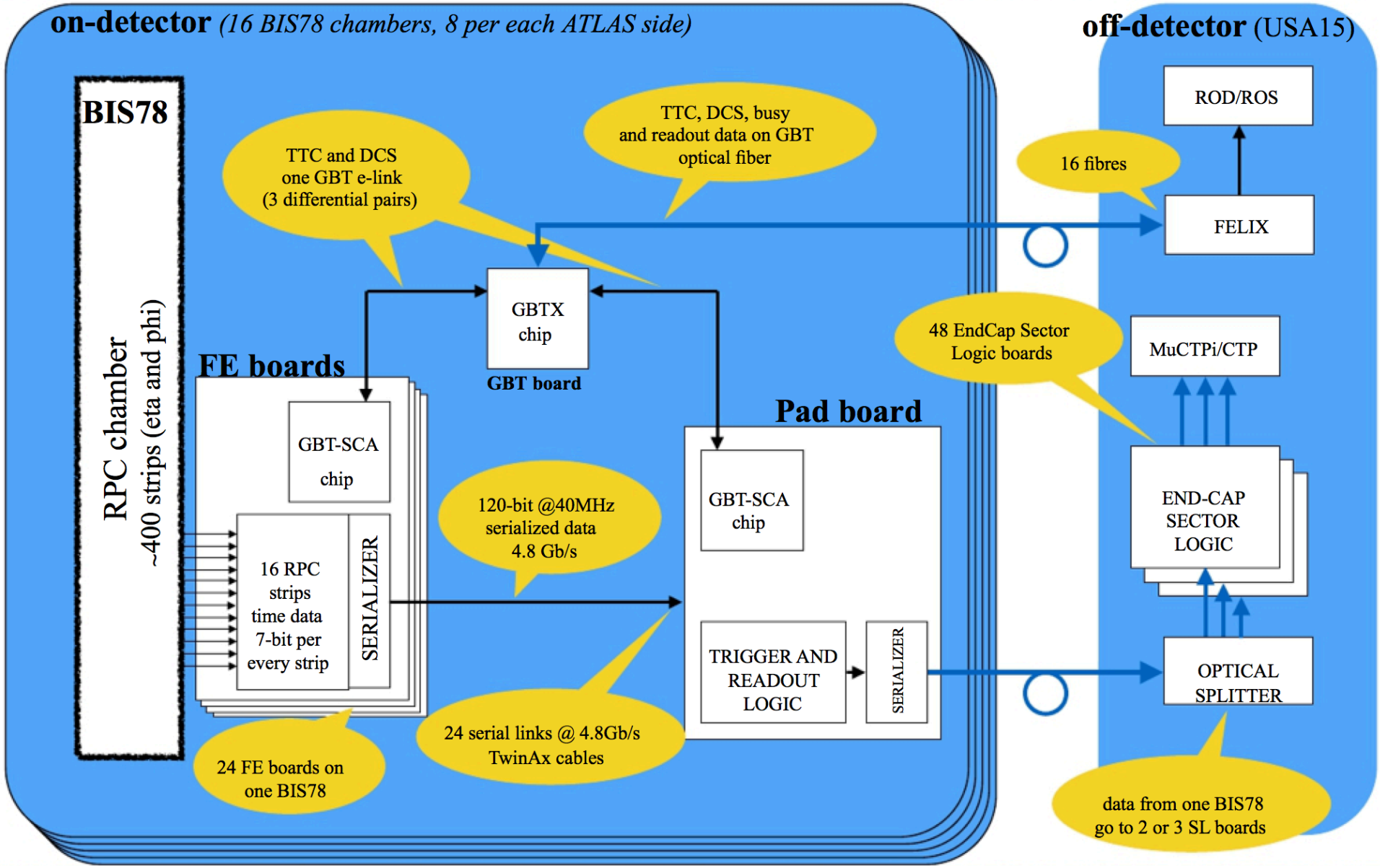
TTC, readout, busy logic and DCS will make use of the GBT system.

The Felix system will be used to send readout data to RODs.

To be chosen which ROD to be used



Preliminary proposal: trigger and readout schema



Conclusions

Still very preliminary trigger/readout schema, I/O interfaces (front-end and USA15 logic) have to be defined before the final schema.

We would like to use the NSW sTGC Pad logic with some modifications:

- 24 serial inputs @ 4.8 Gb/s for the NSW Pad logic;
- Michigan serializer (to be used on the FE boards) is supposed to work @ 4.8 Gb/s (possible bandwidth increase up to 6.4 Gb/s is under study);
- the BIS78 Pad FPGA should have 24 to ~30 high speed serial inputs (4.8 to 6.4 Gb/s);
- one additional serial output for the trigger path.

Optical splitter options for the trigger path have to be studied.

No trigger latency estimate yet (most probably not an issue).

Trigger logic preliminary simulation performed, detailed simulation must follow.

Readout schema to be defined: independent or barrel or endcap (which ROD?).

	NSW sTGC Pad	BIS78 Pad
num. serial inputs	24	24 to 32
input speed	4.8 Gb/s (FPGA up to 8)	(4.8 to 6.4) Gb/s
num. serial output	not defined yet, 3 to 24	1
output speed	320 MHz SDR or DDR	not defined, 4.8 Gb/s

The BIS78 collaboration

INFN Bologna: simulations; performance study; production drawings; DCS

INFN Roma and Napoli: trigger electronics integration (PAD)

INFN Roma2: front-end-electronics and gas volume and chamber design

MPI (Munich): system layout, mechanics, integration, station assembly and test

U Michigan: trigger simulation, serializer, Readout and DAQ

U Science Technology of China: chamber construction, commissioning and R&D