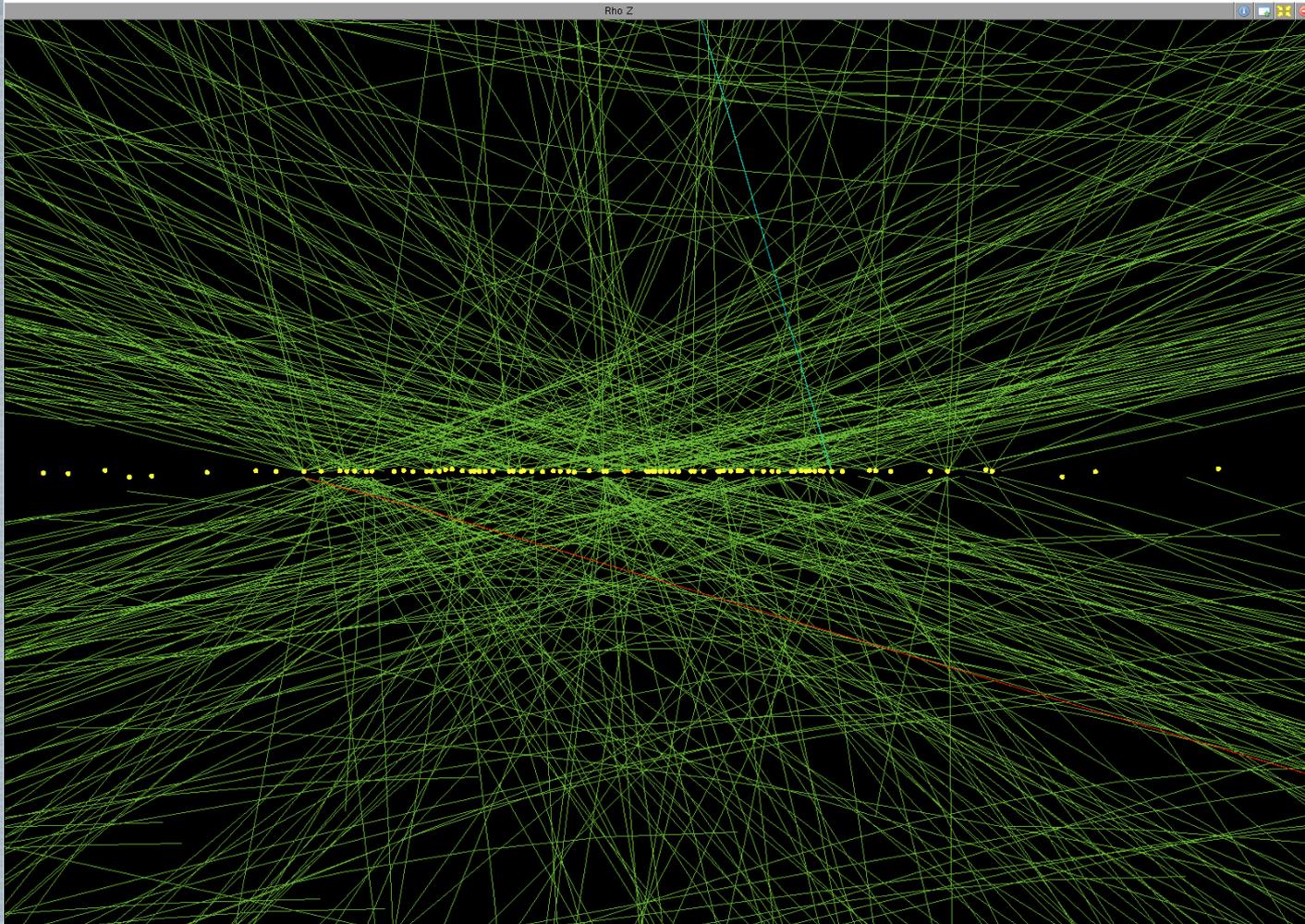
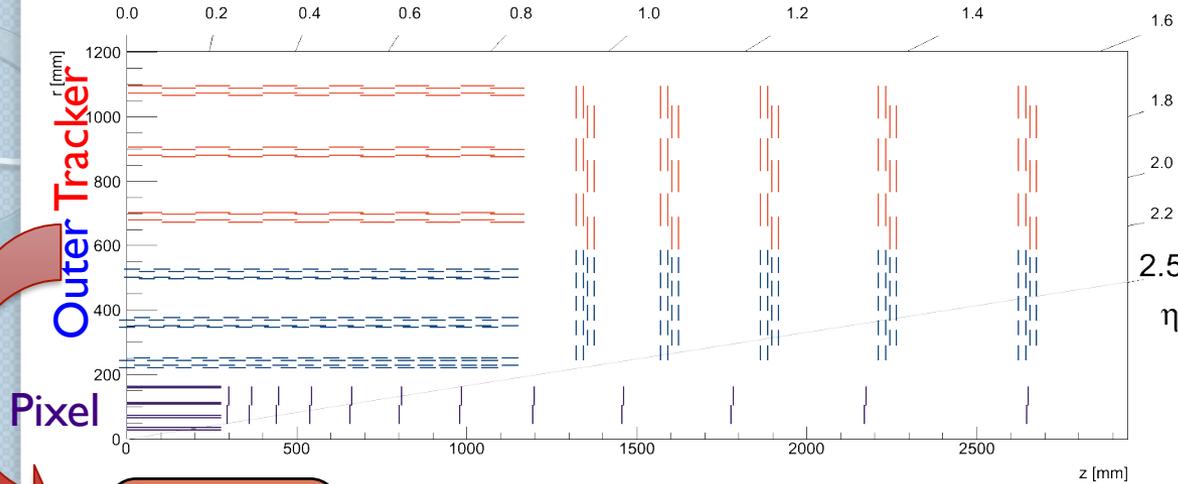


Track Trigger at LI for HL-LHC at CMS

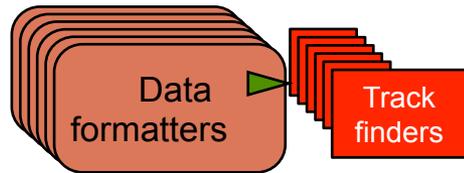


The outer tracker LI trigger

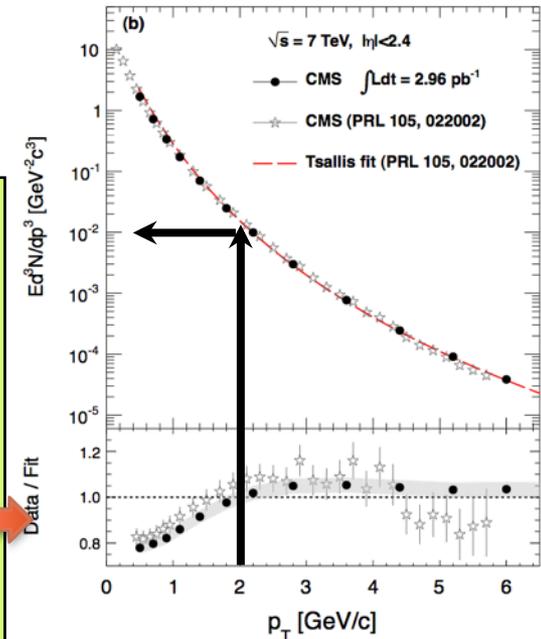


2S (Strip-Strip) Pt modules

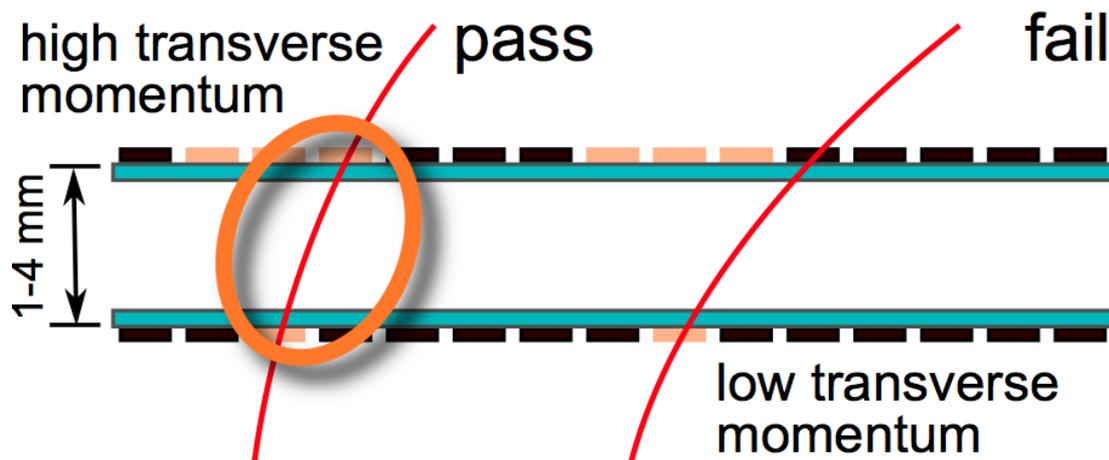
PS (Pixel-Strip) Pt modules



- On detector data reduction ~ 20 , mainly limited by nuclear interactions, conversions and loopers
- Baseline LI latency $12.5 \mu\text{s}$ (possible extension to $25 \mu\text{s}$ if inner pixel included as seeded by outer tracker tracks)
- Track Trigger latency $< 5 \mu\text{s}$
- Trigger providing tracks with $p_T > 2 \text{ GeV}$ at 40 MHz
 - Need time-multiplexing to be able to process $\sim 50 \text{ Tb/s}$ incoming data
 - Expect up to 300 candidate LI tracks to Global Trigger
 - Reduce rate from 40 MHz to 1 MHz

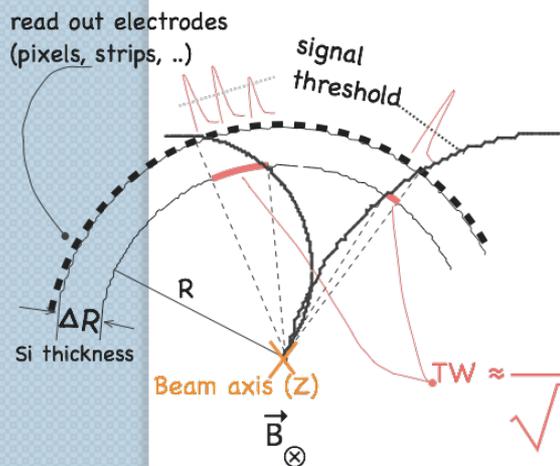


Select only hits from “high-pt” tracks



“stub”

Select “high- p_T ” tracks (>2 GeV) by correlating hits in 2 nearby sensors (stub)

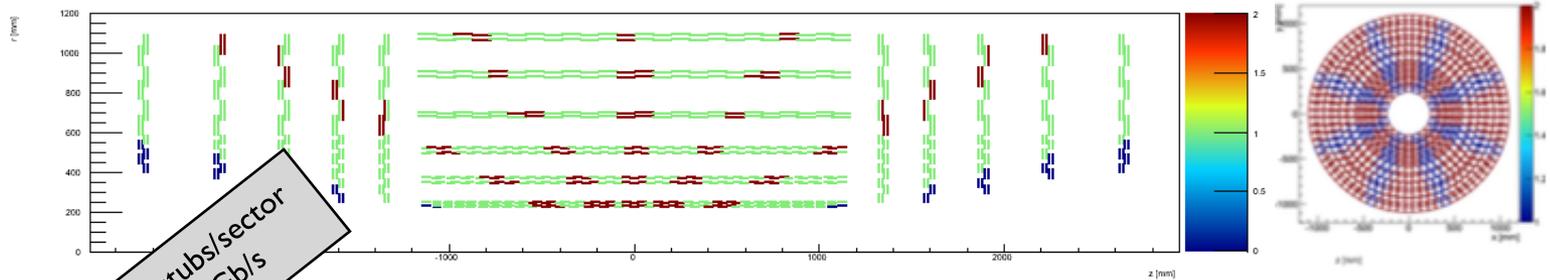


$$TW \approx \frac{\Delta R}{\sqrt{\left(\frac{p_T}{p_{Tmin}}\right)^2 - 1}} \approx \Delta R \frac{p_{Tmin}}{p_T} = 0.15 B \Delta R \frac{R}{p_T}$$

R- Φ plane , “ideal” barrel layer

Large B field of CMS beneficial

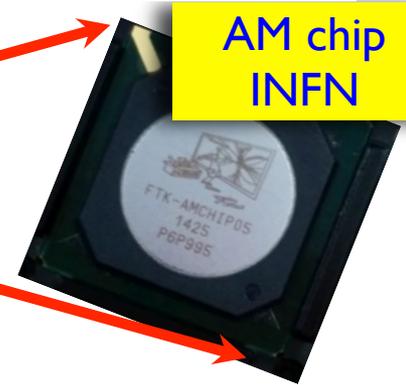
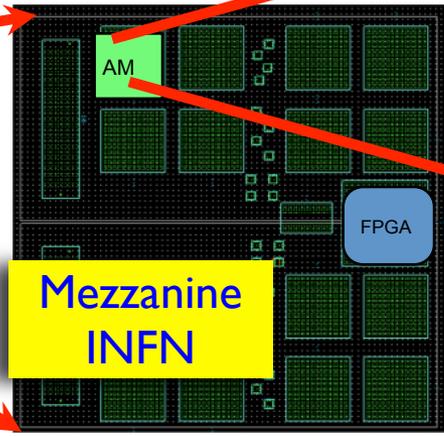
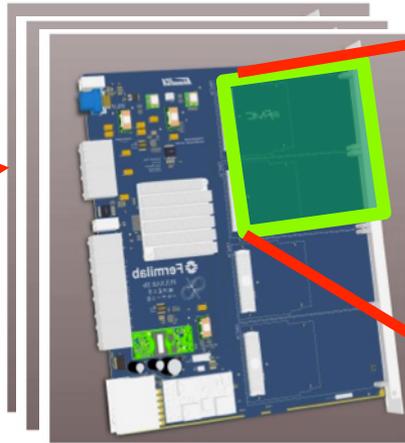
LI Track finding concept



200 to 500 stubs/sector
up to 600 Gb/s

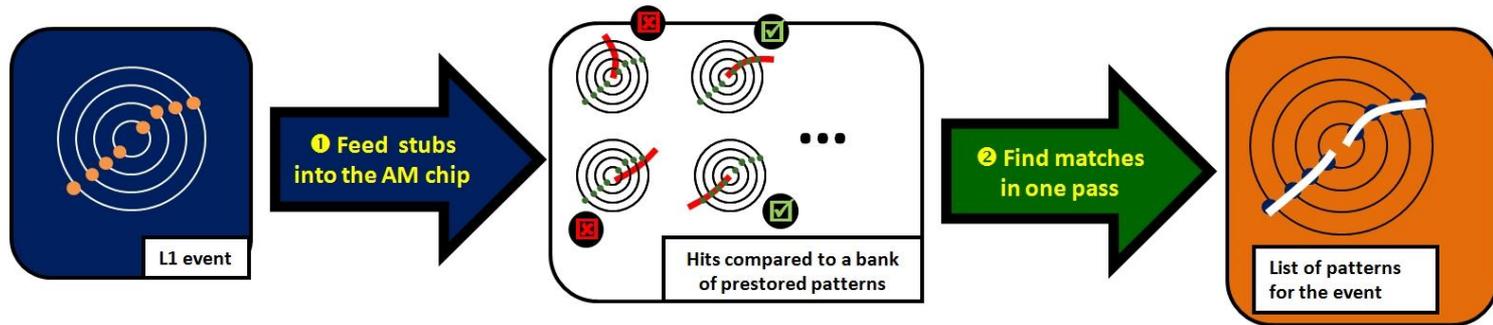


40-100 G full mesh
ATCA shelf



- Send data to Track-finding processors in each ATCA shelf
 - Data distributed to Pulsar boards in time multiplexed mode
 - Perform pattern recognition using AM chips
 - up to 100 roads/tower and 3 M patterns
 - Track fit with FPGA (PCA, Hough transform, Retina, etc.)
 - up to ~20 outputted tracks/tower

Associative Memories



→ Pattern recognition in busy environment is an intensive procedure, but it's a fundamental step:

The better pattern recognition is, the easier trackfit becomes.

→ AM-based pattern recognition is **fast** (*linear wrt the stub multiplicity*) and by construction **pile-up independent**.

→ The goal: **find the best set of pattern banks for the Phase II tracker**



AM Chip	Year	Density (No. Mbits)	Working Frequency (MHz)	Power (W)	Voltage (V)	Technology	Area (cm ²)
AM03	2004	0.5	40	1.26	1.8	180 nm	1
AM04	2012	1.18	100	3.70	1.2	65 nm	0.12
AM06	2014	18.9	100	2-3	1.0/0.8	65 nm	1.6
AM2020	2020?	76?	Up to 200	~2 @100 MHz	0.8	28 nm?	?

Millions of patterns are needed per sector

In summary

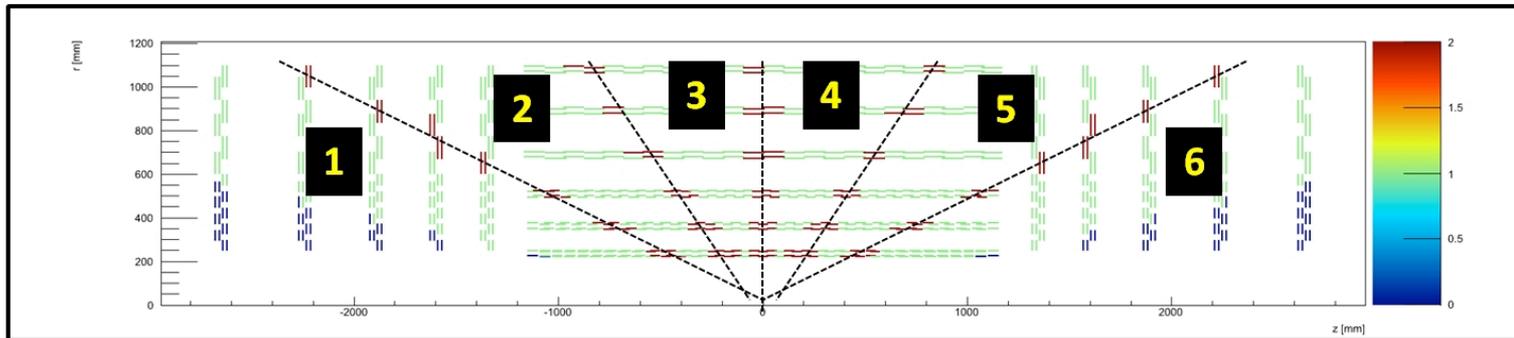
- Select only stubs with $p_t > 2-3 \text{ GeV}$
- The outer tracker is divided into independent and slightly overlapping trigger sectors (6x8), that work in parallel
- Collected stubs in a sector go to the corresponding FPGA, which reduce the resolution, merging strips into “SuperStrips”
- These low resolution hits go to the AM chips, which find the corresponding patterns and send back the roads to the FPGA
- Only hits within the roads go to the fitter, that finally finds tracks and track parameters
 - Can send one road sequentially or all roads together

Status of AM

Geometry and trigger towers

→ What was the trigger configuration tested?

→ We start for the baseline 48 towers configuration



Eta range	1	2	3	4	5	6
<i>Sector numbers</i>	0→7	8→15	16→23	24→31	32→39	40→47
<i>Active layers</i>	5 6 18 19 20 21 22	5 6 7 8 9 10 18 19	5 6 7 8 9 10	5 6 7 8 9 10	5 6 7 8 9 10 11 12	5 6 11 12 13 14 15

→ Three tower types: hybrid, endcap, and barrel

Size of banks

→ Which bank types were tested?

→ The goal is to test the impact of bank parameters on all the tower types, therefore we produced a set of five test banks for each type:

- **BASE:** baseline bank, ie 32 strips, 3 DC bits, and 2GeV/c threshold
- **64/2DC:** bank with larger roads (*64 strips instead of 32*), 2DC bits to reach the same size at the end
- **2DC:** bank with finer roads (*2DC instead of 3*), maximum superstrip size will be 128.
- **3GeV:** only particles with a p_T larger than 3 GeV/c are used to build the bank.
- **Combo:** 32 strips, 2 DC bits, and 3GeV/c threshold

→ Bank sizes are significantly depending on the modified parameters:

<i>Bank size</i>	<i>Endcap</i>	<i>Hybrid</i>	<i>Barrel</i>	<i>Full tracker</i>
<i>Base</i>	1404337	2426024	1865228	91M
<i>64/2DC</i>	1032137	1894642	1465725	70M
<i>2DC</i>	3859272	6382106	5511619	252M
<i>3GeV</i>	1025308	1657378	1310449	64M
<i>Combo</i>	2759465	4395871	3844614	176M

→ If needed, there is still room for improvement (*by adding the stub's PT info to the combo banks*)

Results

→ Single tower results (4/5): baseline vs optimized

		Bank type		Δ (in %)
		Baseline	Optimized	
Endcap	Muon gun efficiency ($N_{hits} \geq 5$)	98,6	98,4	-0,2
	Electron gun efficiency ($N_{hits} \geq 5$)	96,0	93,6	-2,5
	PU140 road rate	119,0	24,0	-79,8
	PU140 fake road proportion	52,8	31,7	-40,0
	PU200 road rate	216,0	38,0	-82,4
	PU200 fake road proportion	62,0	41,7	-32,7
Hybrid	Muon gun efficiency ($N_{hits} \geq 5$)	98,5	97,5	-1,0
	Electron gun efficiency ($N_{hits} \geq 5$)	97,6	95,6	-2,0
	PU140 road rate	248,0	35,0	-85,9
	PU140 fake road proportion	73,7	48,4	-34,3
	PU200 road rate	534,0	61,0	-88,6
	PU200 fake road proportion	83,7	65,6	-21,6
Barrel	Muon gun efficiency ($N_{hits} \geq 5$)	99,0	98,6	-0,4
	Electron gun efficiency ($N_{hits} \geq 5$)	98,5	97,3	-1,2
	PU140 road rate	201,0	36,0	-82,1
	PU140 fake road proportion	62,4	24,9	-60,1
	PU200 road rate	416,0	51,0	-87,7
	PU200 fake road proportion	75,0	41,8	-44,3

→ Putting everything together (except the 64 strips tune), one basically adds all the effects.

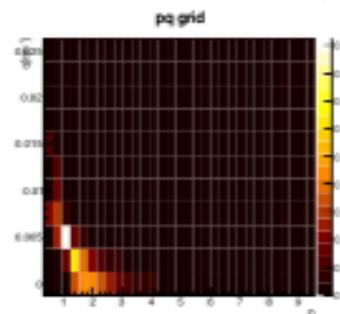
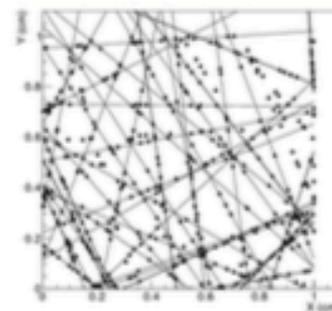
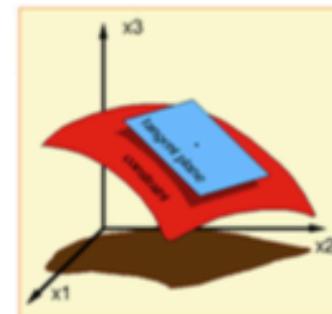
→ Output road rate is well below our requirement (100) in all cases and fake road proportion is also within constraint (50%), except for hybrid towers at PU200.

→ This config only requires 2 times more patterns than the baseline. This is important, but not unrealistic.

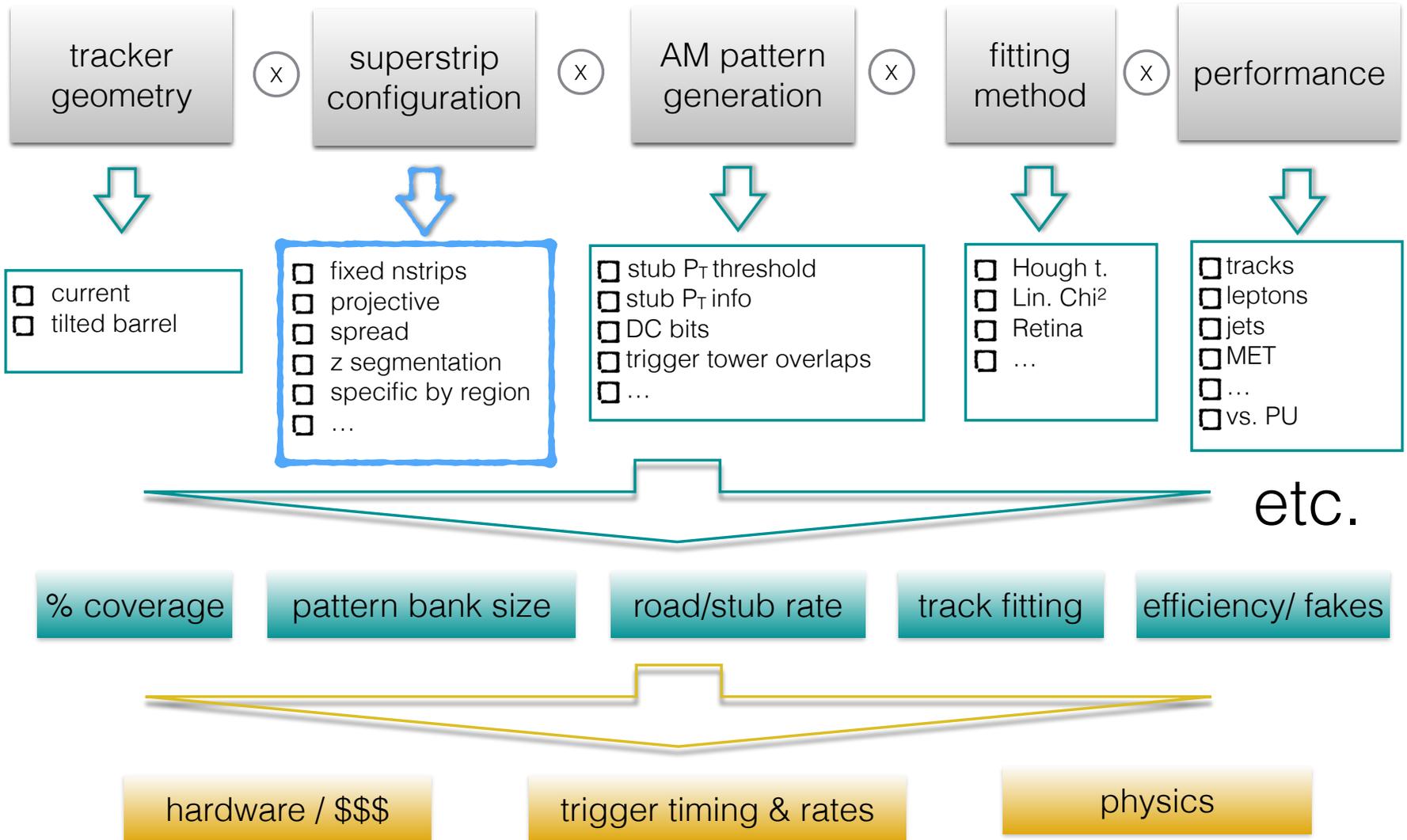
→ Efficiency is close to the baseline result, losses are concentrated in the very low p_T region ($< 5 \text{ GeV}/c$)

And then, track parameter fitting

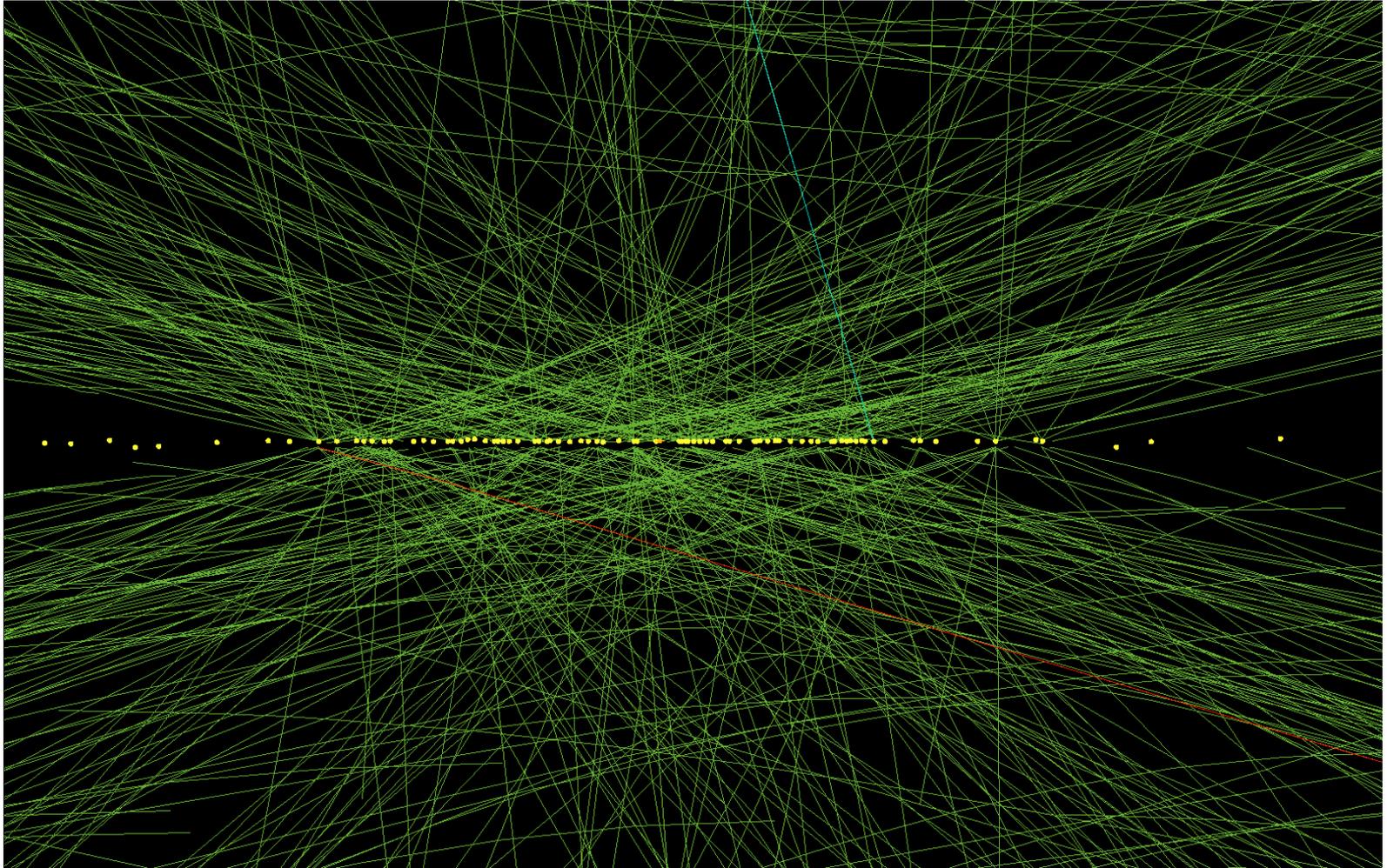
- After pattern recognition
 - Find track candidates
 - Measure track parameters (p_T , ϕ , d_z)
 - Different methods under study:
 - ① Principal component analysis
 - ≈ 3000 iterations per sector for MinBias events
 - ② Hough transformation
 - ③ Retina
 - look for speed, resolution, efficiency, fake rate
- ① Nucl.Instrum.Meth.A623:540-542,2010 doi:10.1016/j.nima.2010.03.063
- ② Hough, P. V. C., 1959, in Proceedings of the International Conference on High Energy Accelerators and Instrumentation (CERN)
- ③ Ristori, Nucl.Instrum.Meth.A453:425-429,2000



Large phase space for AM simulation studies

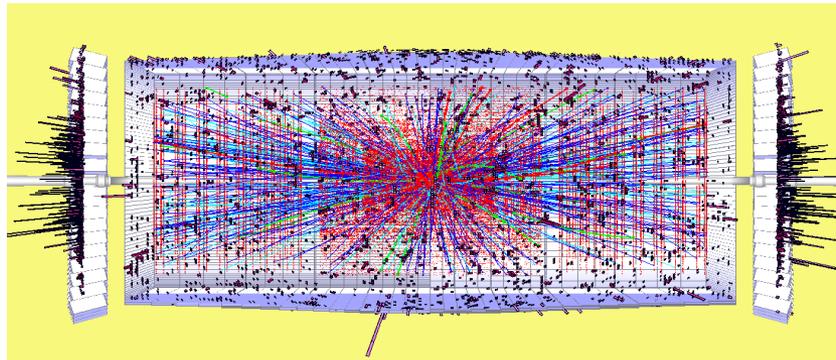


backup

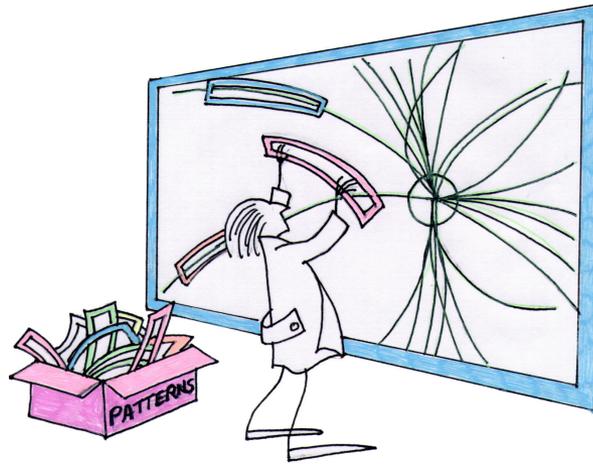


In need of a trigger

- At $5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ up to ~ 140 interactions per bunch crossing
 - About 6k primary tracks per bunch crossing in the Tracker volume $|\eta| < 2.5$...
 - ...plus any other coming from γ conversions and nuclear interactions
 - \sim one order of magnitude larger wrt LHC
 - Severe Triggering conditions
 - Too many primary vertices, need to have smarter triggers combining information from several subdetectors
 - Need to maintain low thresholds for basic objects, even with an increase in the L1-Accept bandwidth (currently at 100 kHz)
 - Both ATLAS and CMS will replace their “inner trackers” to cope with the nasty environmental conditions
 - The usage of the Tracker would help to disentangle among those 140 pileup events

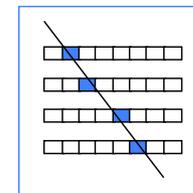
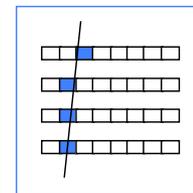
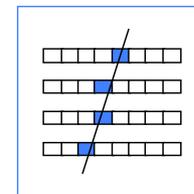
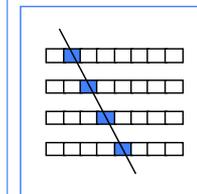
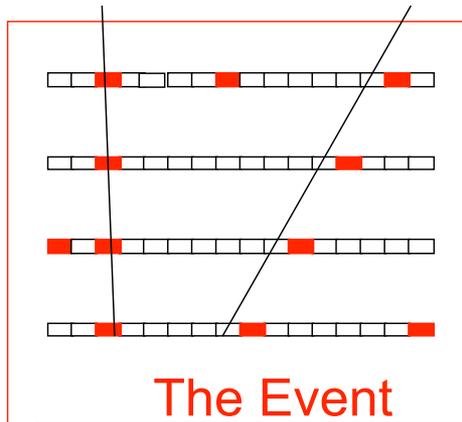


Pattern matching with Associative Memories



The **pattern bank** is flexible set of pre-calculated patterns:

- can account for misalignment
- changing detector conditions
- beam movement
- ...



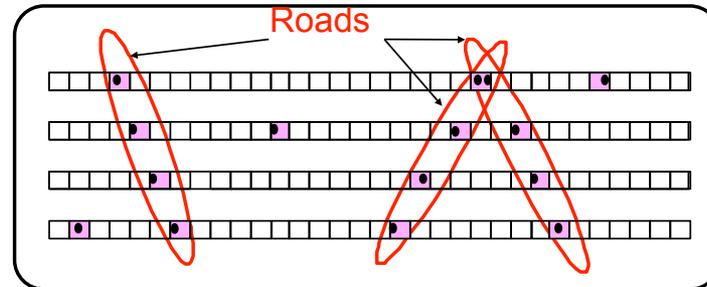
The Pattern Bank

• • •

A two-steps track trigger

1. Find low resolution track candidates called "roads". Solve most of the pattern recognition

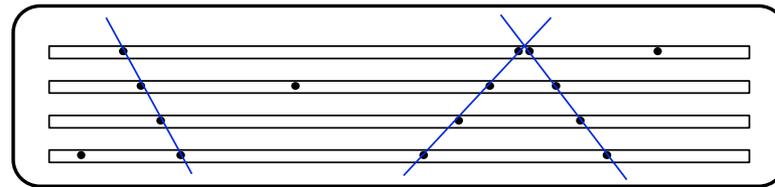
Rimozione dell'80% del combinatorio



AM chip

2. Then fit tracks inside roads.
Thanks to 1st step it is much easier

One fit per second



FPGA

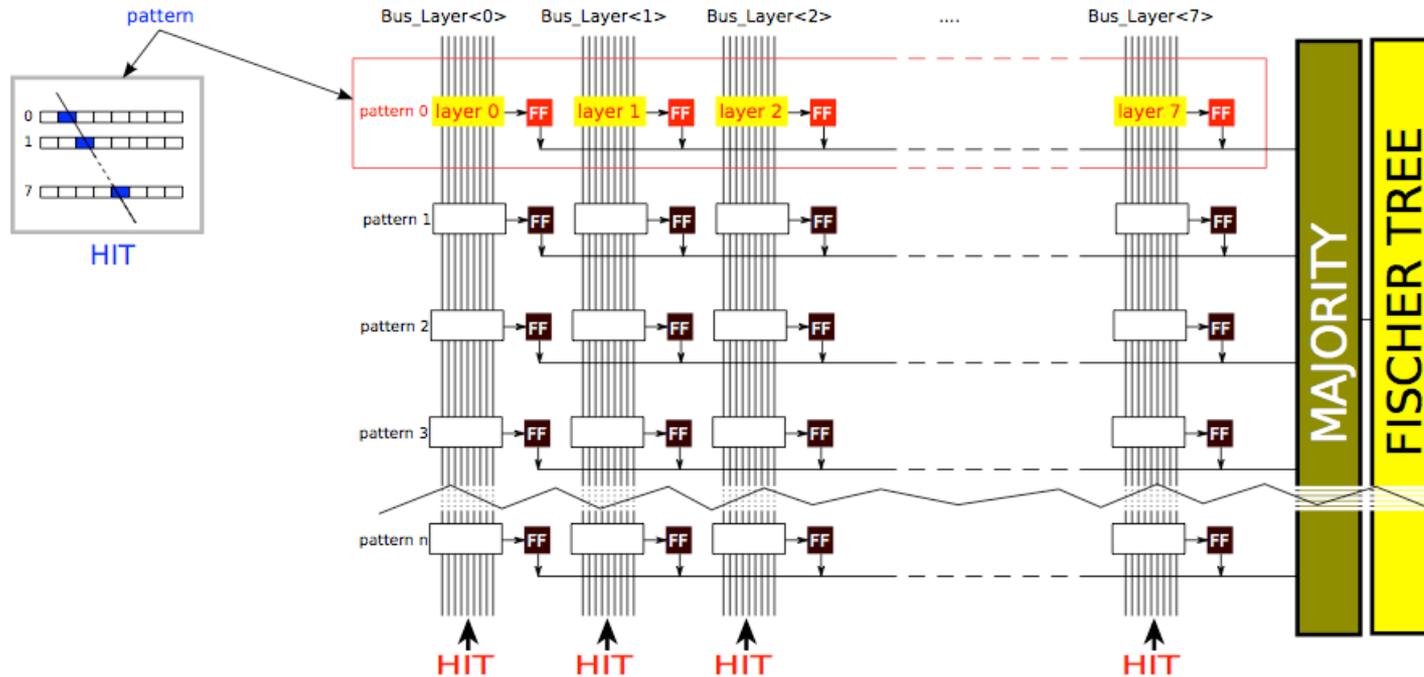


AM chip + FPGA



Find a compromise between bank size, number of fits, RAM and latency

AM chip logic

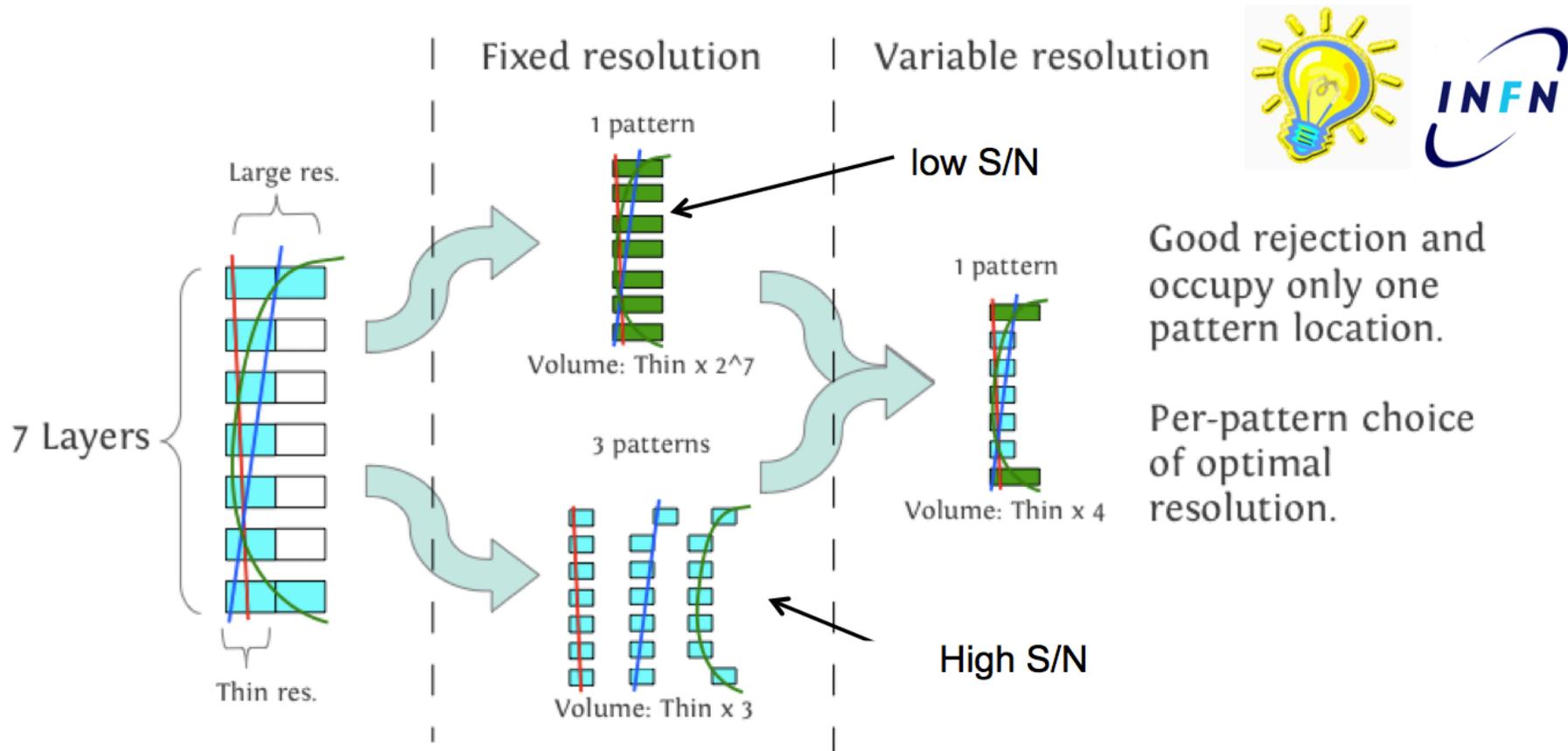


The event hit positions are received over 8 input buses of 15 bits each.

All the hits are then compared with the data stored inside each layer block, as soon as they are loaded into the chip, each one in the corresponding bus. If a layer block is matched, the corresponding Flip-Flop (FF) is set. It should be noted that each hit is fed into the memory only once. In fact the bus line transmits the information to all the layer blocks, and, if matched, all the corresponding FF are set simultaneously. Finally, a given pattern is matched with a logic that counts the number of FF set to 1 within a row, using a majority logic: that means that one could ask a minimum number of FF set

Don't Care bits

AMCHIP04: VARIABLE RESOLUTION



Fixed Threshold Menus

TDREta v3p3



Offline Thr.	Std Trigger Alg	Rate (kHz)	Trk Trigger Alg	Rate (kHz)
18	Single Mu	139	Single TkMu	14
14 10	DoubleMu	177	DoubleTkMu (vtx)	1.1
19, 10.5	isoEG + Mu	160	isoTkEle + tkMu (vtx)	0.66
31	Single EG	78	Single TkEle	16
27	Single IsoEG	89	Single isoTkEle	13
31			Single isoTkEM	30
22, 16	isoEG + EG	70	isoTkEle + EG	11
22, 16			DoubleTkEM	17
88	Single Tau	88	Single TkTau	41
56, 56	DoubleTau	53	tkTau + Tau	42
19, 50	isoEG + Tau	34	isoTkEle + Tau	7.5
45, 14	Tau + Mu	55	tkTau + tkMu (vtx)	5.4
173	Single Jet	42	Single tkJet	42
2@125	Double Jet	52	Double tkJet (vtx)	25
4@72	Quad Jet	185	Quad tkJet (vtx)	12
23, 66	isoEG + Jet	144	tkEle + tkJet (vtx)	16
16, 66	Mu + Jet	175	tkMu + tkJet (vtx)	9.0
23, 95	isoEG + HTM	60	tkEle + tkHTM	9.7
16, 95	Mu + HTM	64	tkMu + tkHTM	2.9
350	HTT	73	tkHTT	14
	Total LI Rate	1034	Total LI Rate	210