101° Congresso Nazionale SIF

24/9/2015

Come i raggi cosmici limitano l'affidabilità dei circuiti elettronici a livello terrestre e avionico

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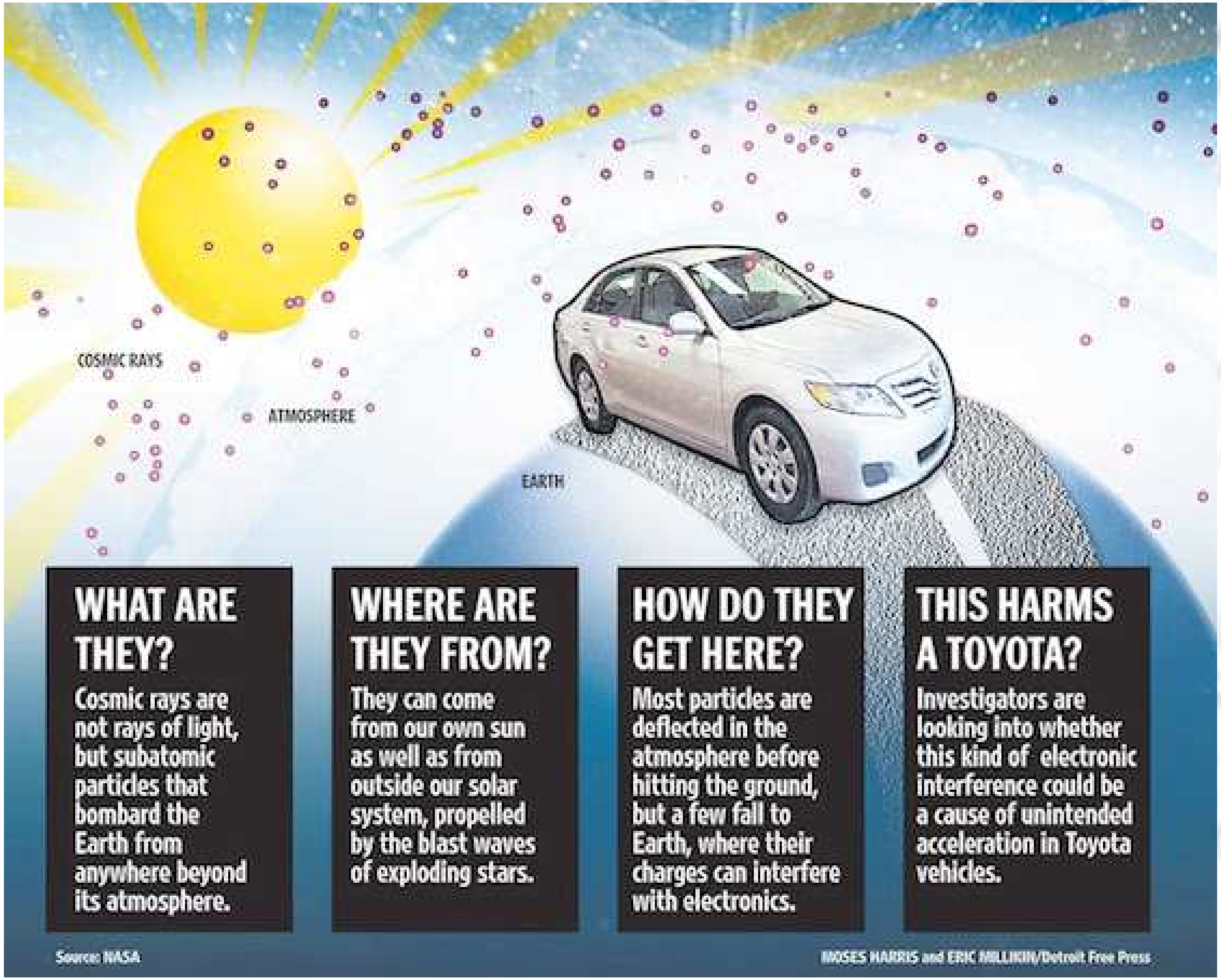
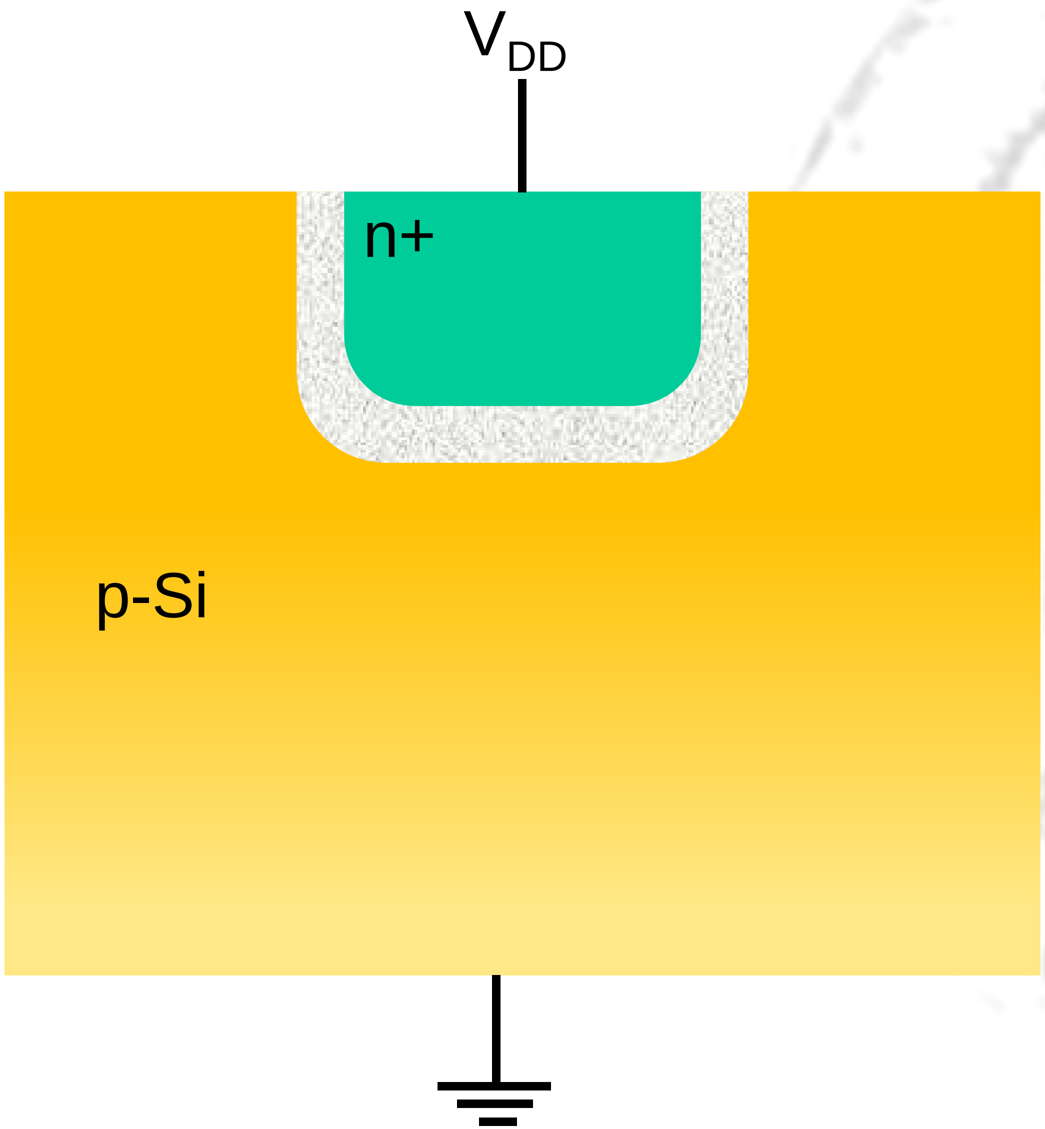
- Introduction
- Ionizing radiation effects in semiconductors
- Reliability issue: Single Event Effects (SEE's)
- Cosmic rays and atmospheric neutrons
- Accelerated testing of electronics with accelerators
- Microelectronics technology evolution and SEE's
- Summary

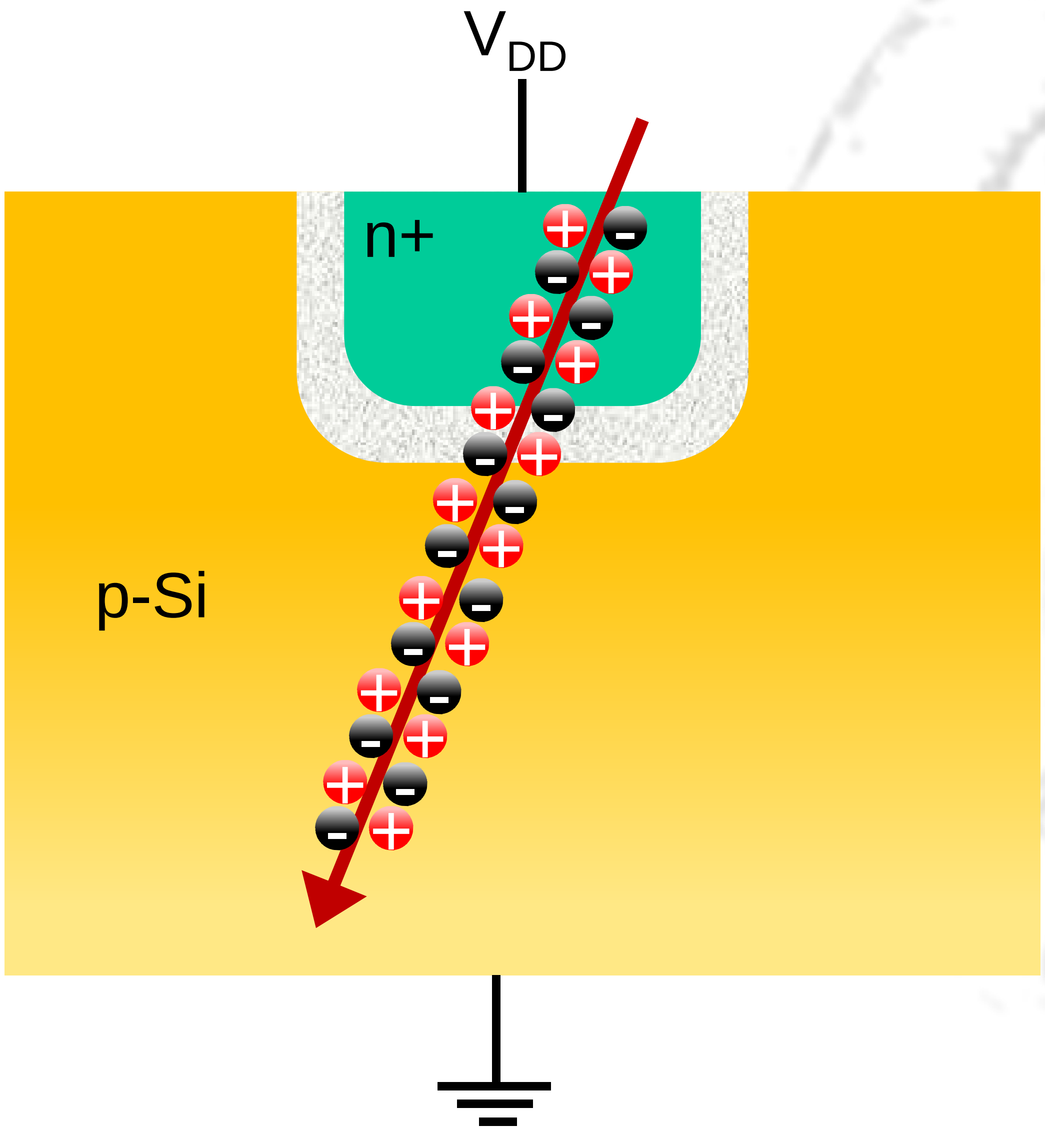


www.cars.com, 2010

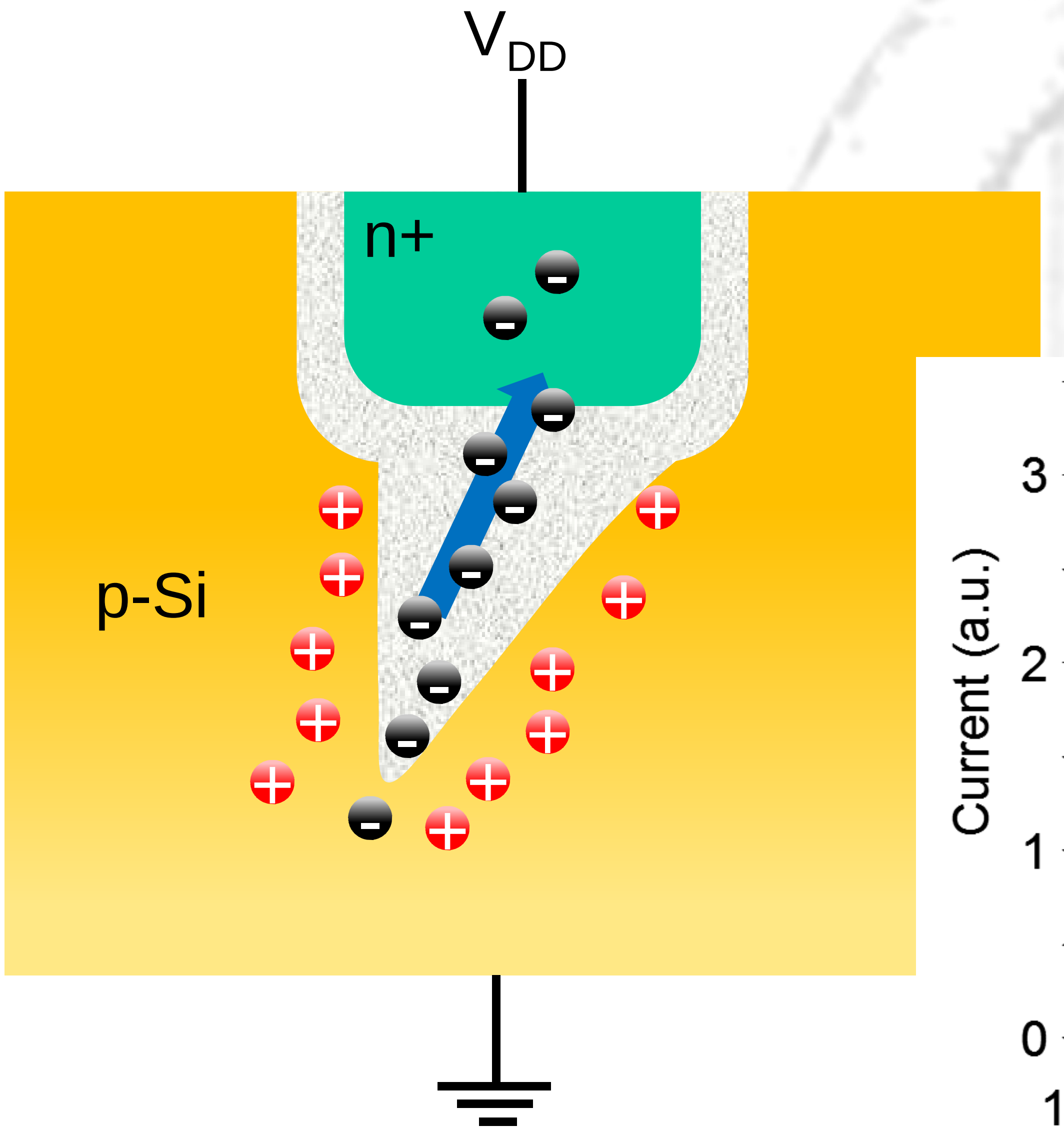
- *Societal needs for more reliable electronics*
- Reliability in advanced ICs is improving down to some **10-100 FIT**
- Electronics is present in **Active Security**, especially visible in everyday vehicles (airplanes, cars – **0 FIT goal**, trucks, railways,…)
- Ionizing radiation poses a threat on the electronics reliability, even at **sea level, on a variety of applications**
- **Avionic and space industries** have a long standing tradition of radiation testing, but this issue is being seriously investigated by:
  - Semiconductor *companies*: IBM (since'80s), Intel, STMicroelectronics, Texas Instruments, Cypress, Xilinx,…, but few SEE comprehensive data from companies are available
  - Semiconductor IC *customers*: even less prone to show their interest and results, basically no data available
- Radiation effects at sea level are dominated by **Soft Errors (SE)** → **Soft Error Rate (SER)** figure of merit; if not properly mitigated, SER may reach **10^5 FIT** → **high reliability requires extensive testing!**



- Reverse-biased pn junctions are very sensitive to radiation, because they can collect charge, giving rise to a spurious current pulse
- Three phases: onset, drift/funnel, diffusion

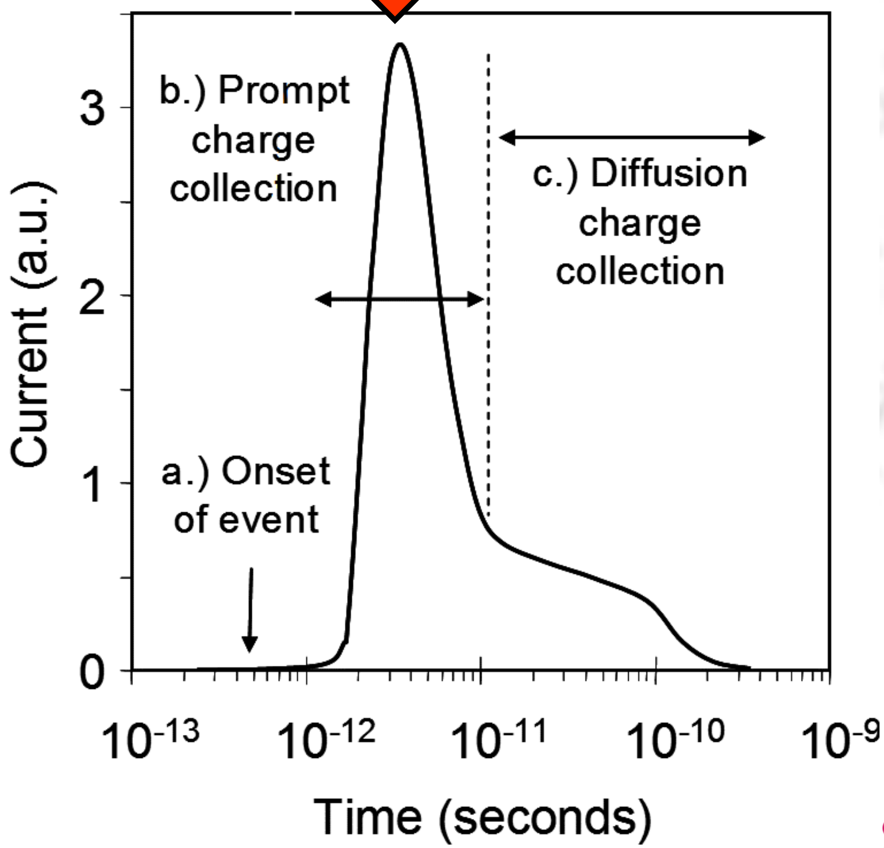


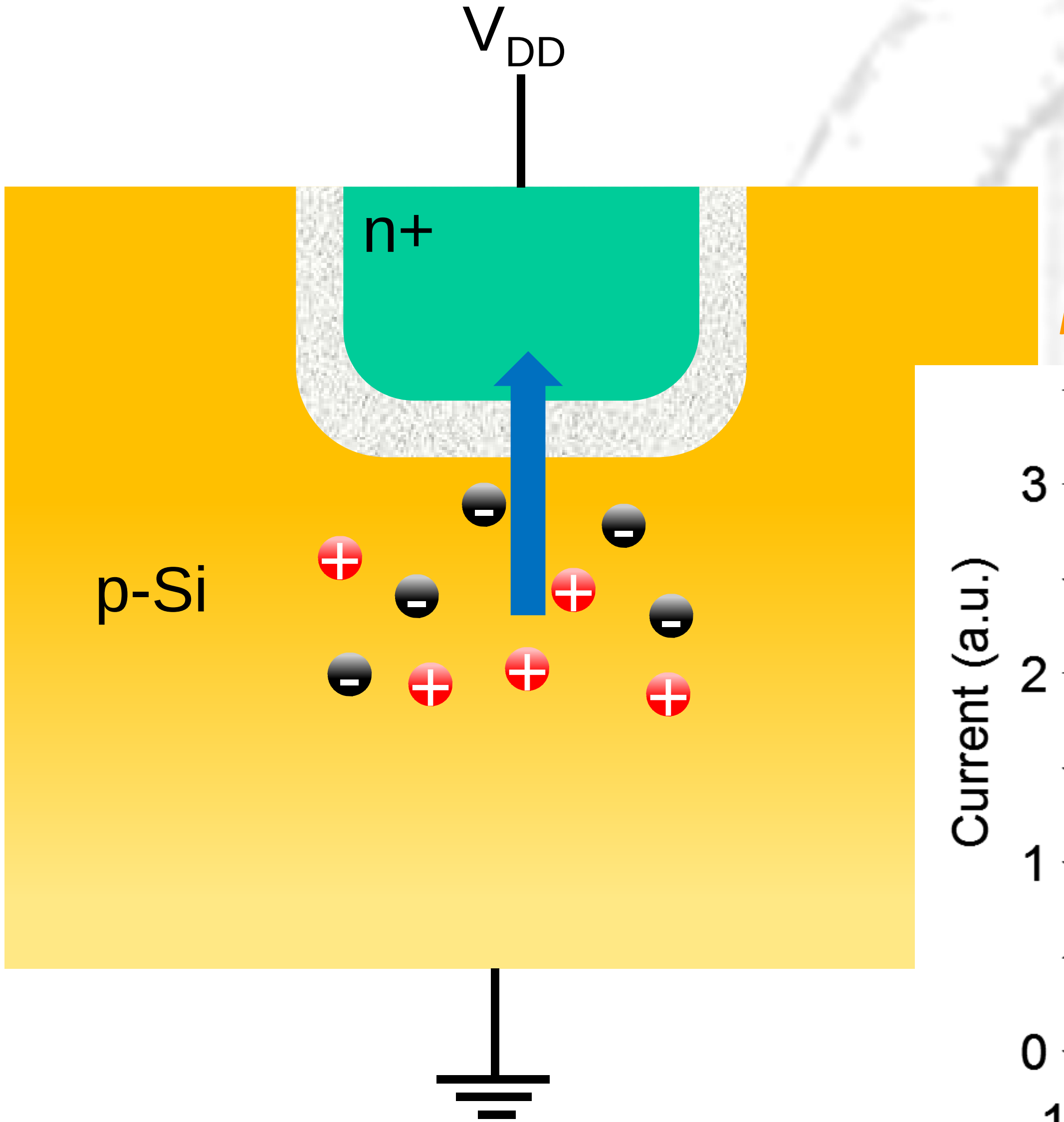
- Reverse-biased pn junctions are very sensitive to radiation, because they can collect the radiation generated charge, giving rise to a spurious current pulse at a sensitive node
- Three phases: **onset**, drift/funnel, diffusion



- Three phases: onset, **drift/funnel**, diffusion

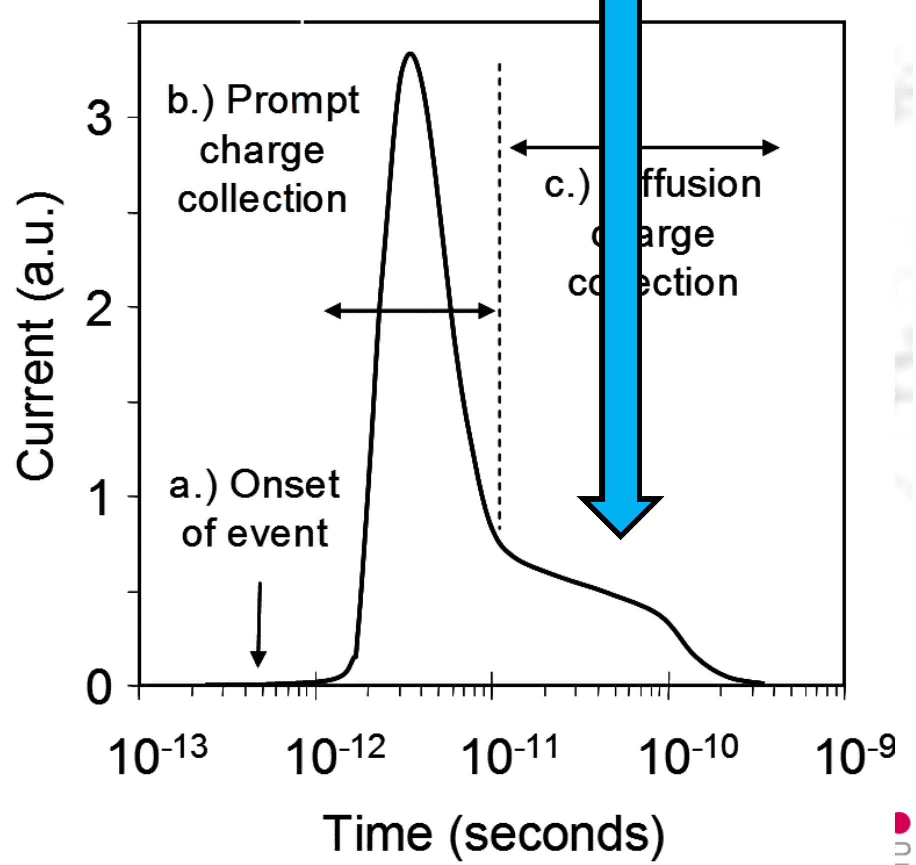
R. Baumann, IEEE-TDMR, 2005

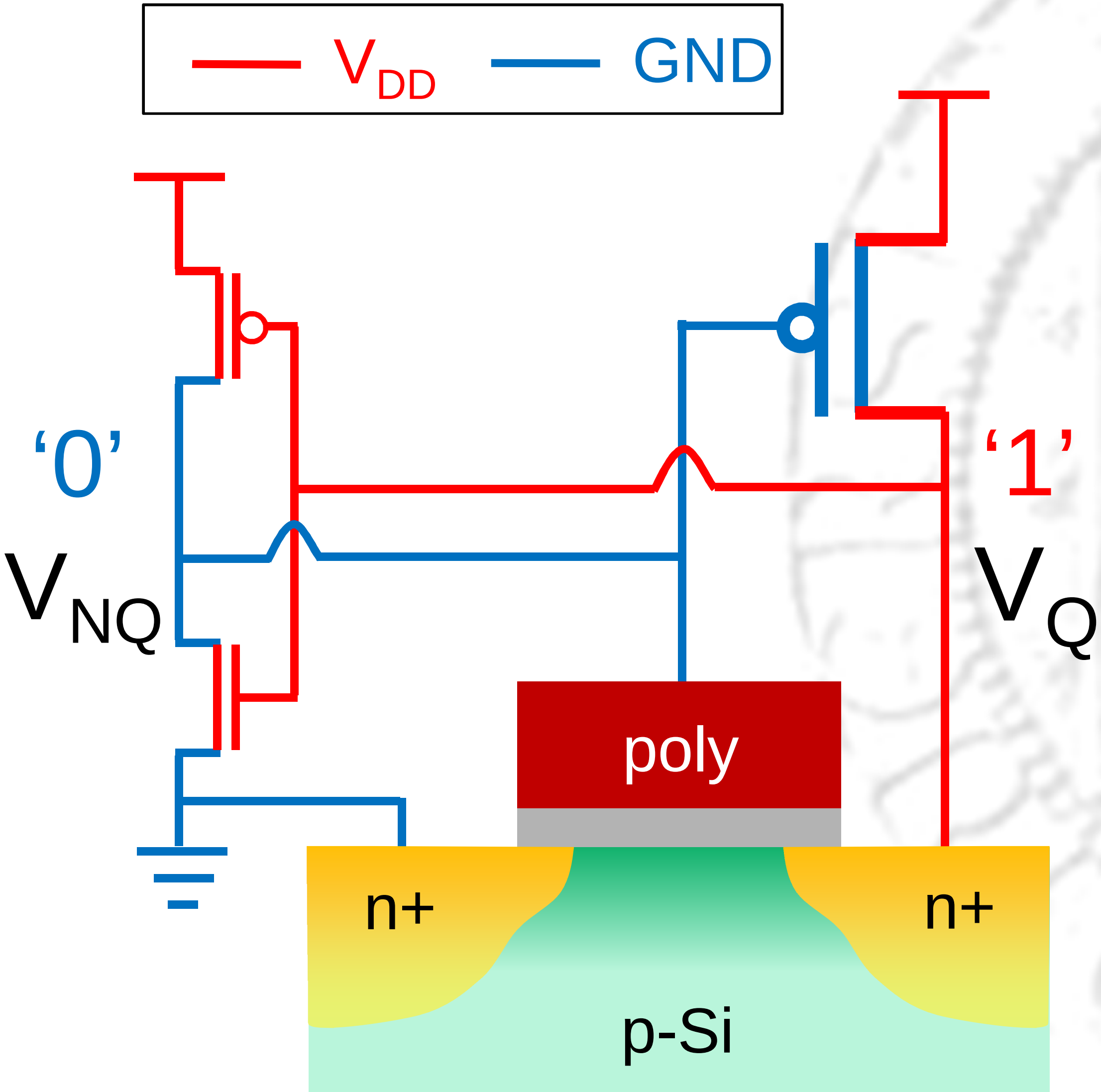




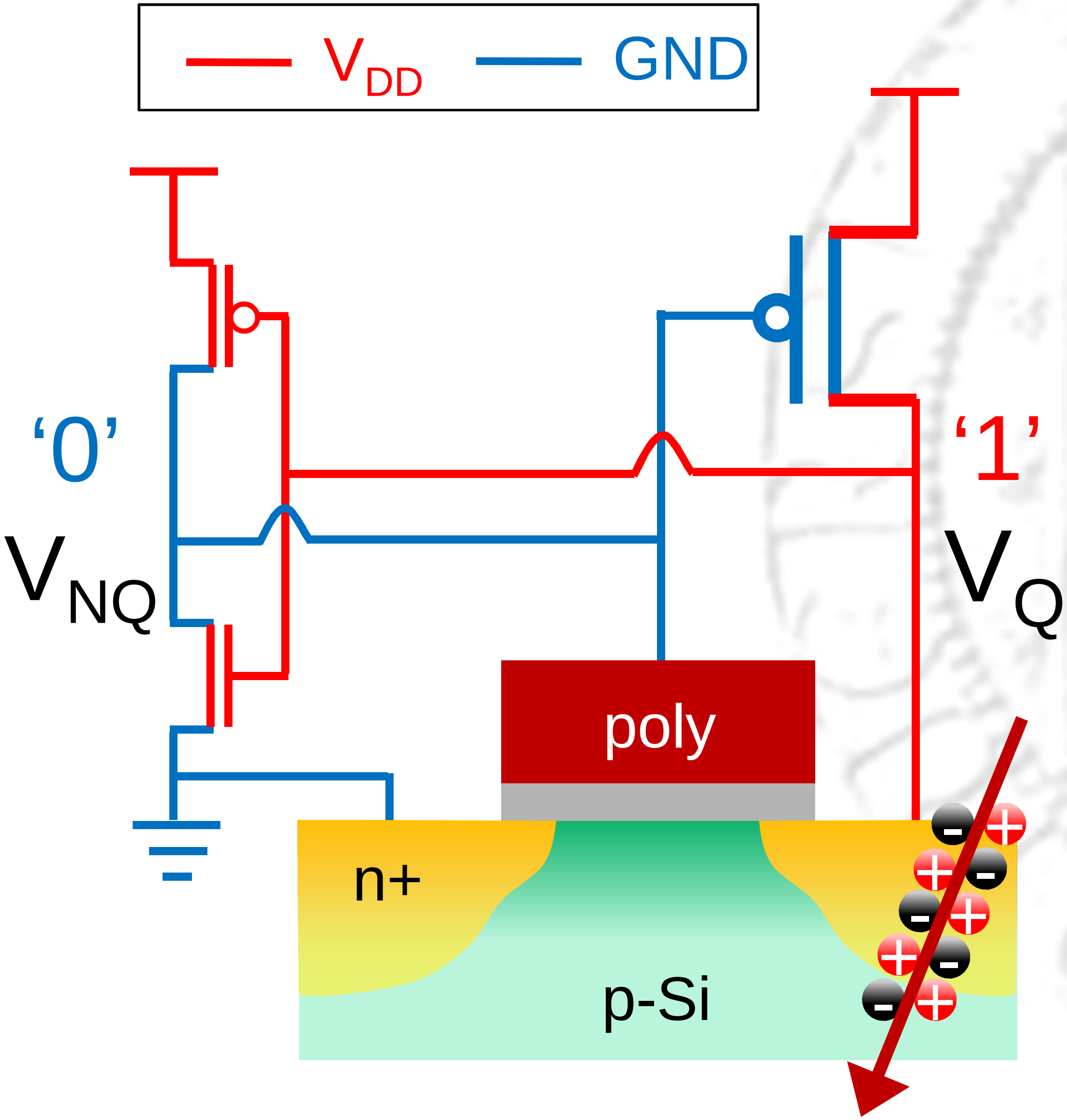
- Three phases: onset, drift/funnel, **diffusion**

R. Baumann, IEEE-TDN R, 2005

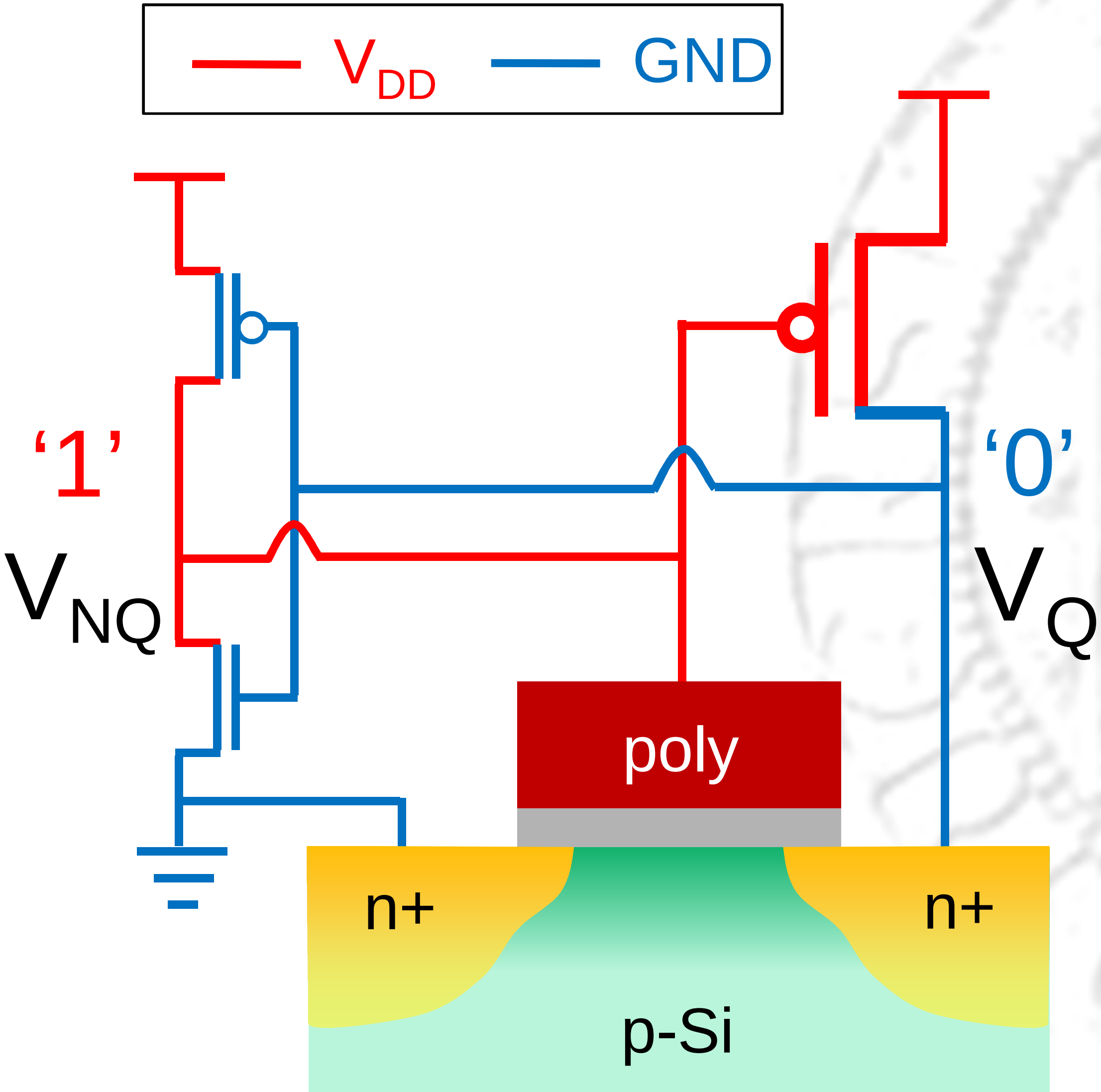


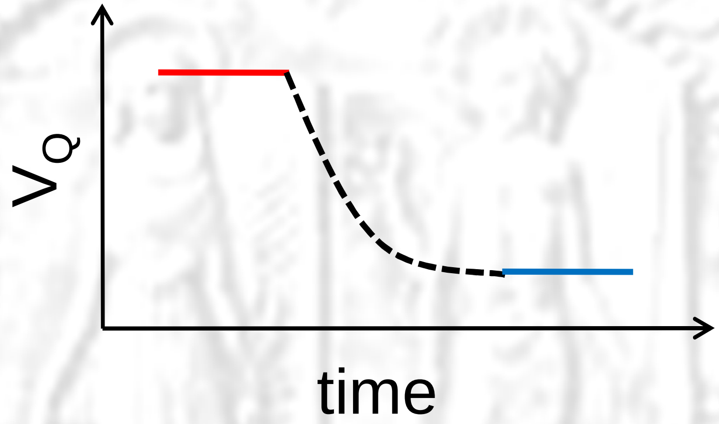


- SRAM: **benchmark** for SEE studies
- Initial state:
  $V_Q = V_{DD}$ (logic "1")
  $V_{NQ} = 0$ (logic "0")



A particle strikes the drain junction of the off NMOSFET: electrons are collected at the Q node, generating a **negative voltage pulse**





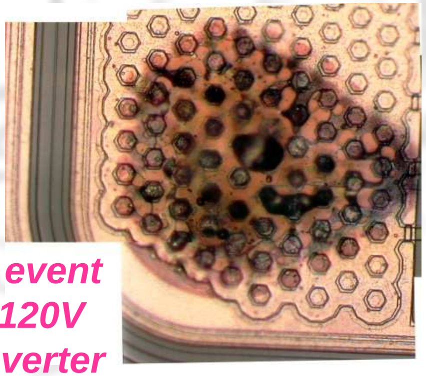
If the voltage transient is **long** and **ample** enough (in other terms, if the **collected charge** is larger than the **critical charge**), the cell flips:

Q: 1 → 0;

NQ: 0 → 1

SOFT ERROR!

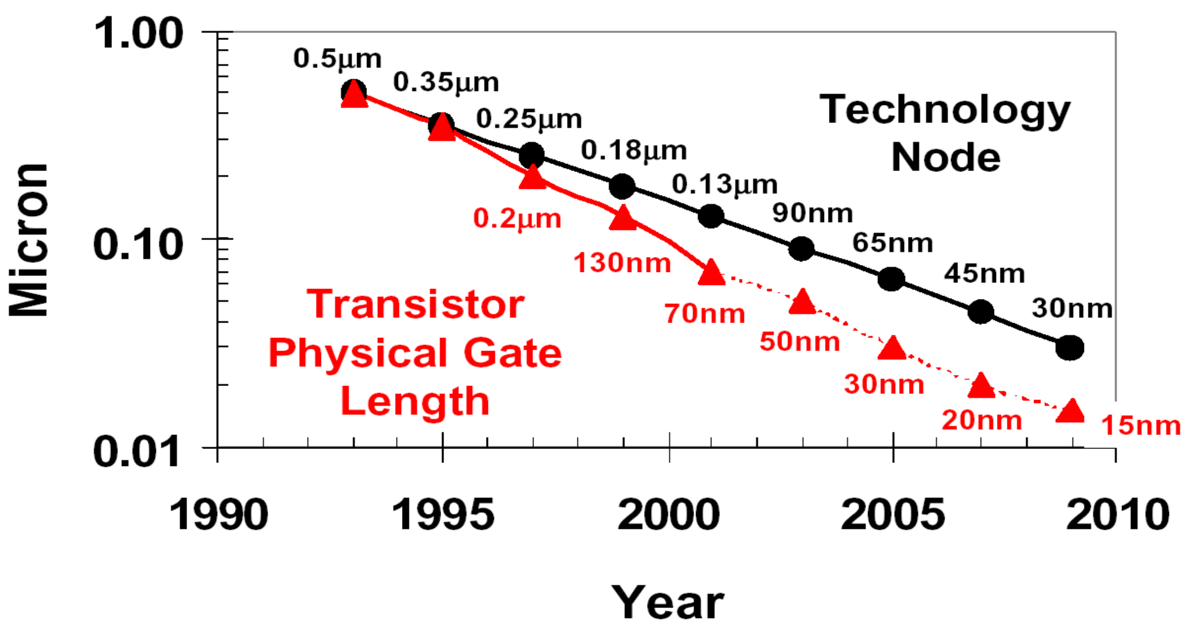
- **Non-destructive (Soft Errors, SE)**:
  - *Single Event Transient (SET)*
  - Single Event Upset (SEU)
    - Single Bit Upset (SBU)
    - Multiple Bit/Cell Upset (MBU/MCU)
  - Single Event Functional Interruption (SEFI)
  - Single Event Latchup (SEL or SELU)… *may be also destructive*
- **Destructive (hard errors)**:
  - Stuck Bits
  - Power, analog:
    - Single Event Burnout (SEB)
    - Single Event Gate Rupture (SEGR)



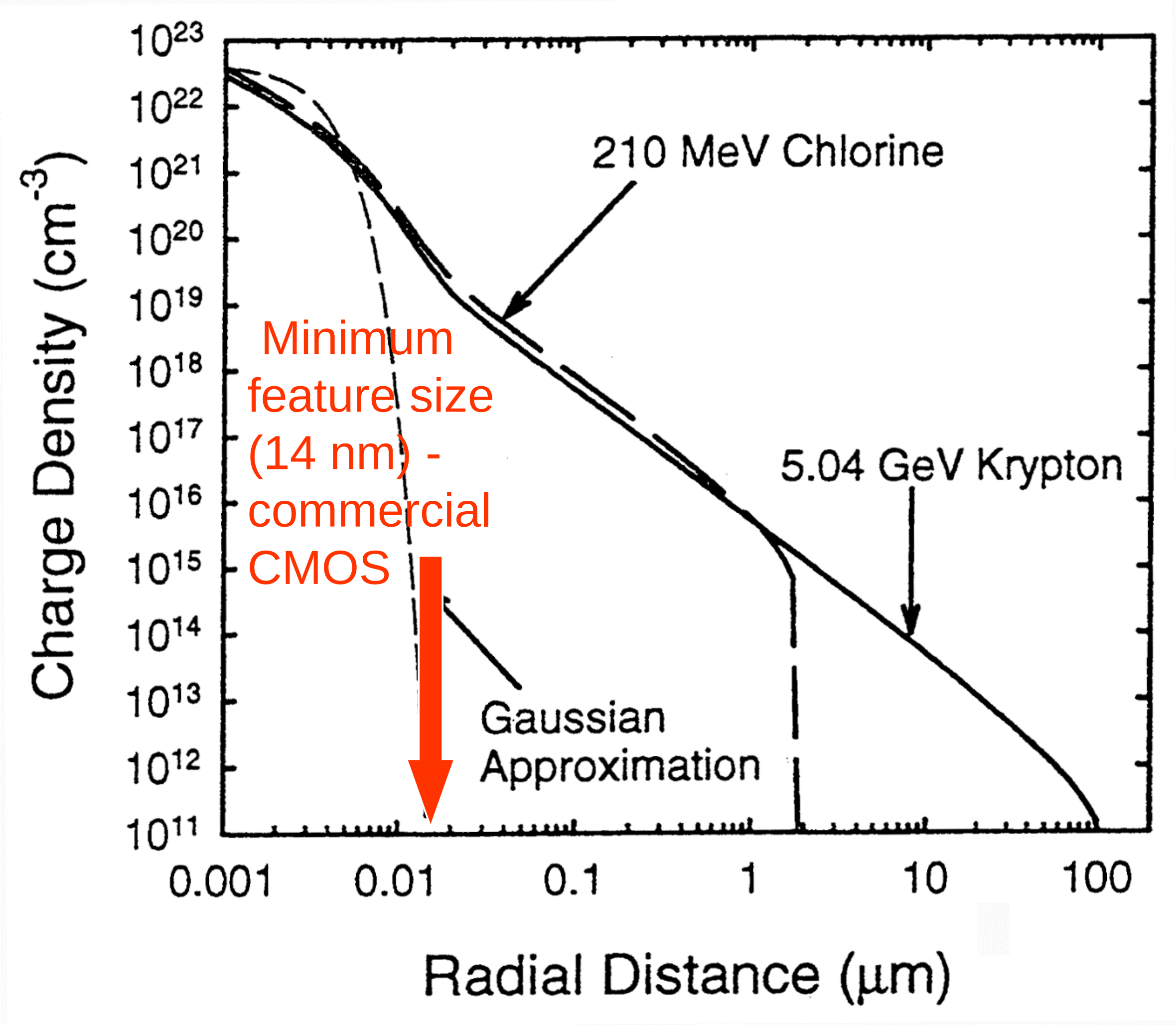
Destructive event in a COTS 120V DC-DC Converter

K. LaBel, EWRHE 2004

Moore’s law is (self-)validated by reducing the transistor dimension over the years, by scaling down the minimum feature size of the CMOS technology node (at present, the smallest feature size is 14 nm, microprocessors by INTEL and SAMSUNG)

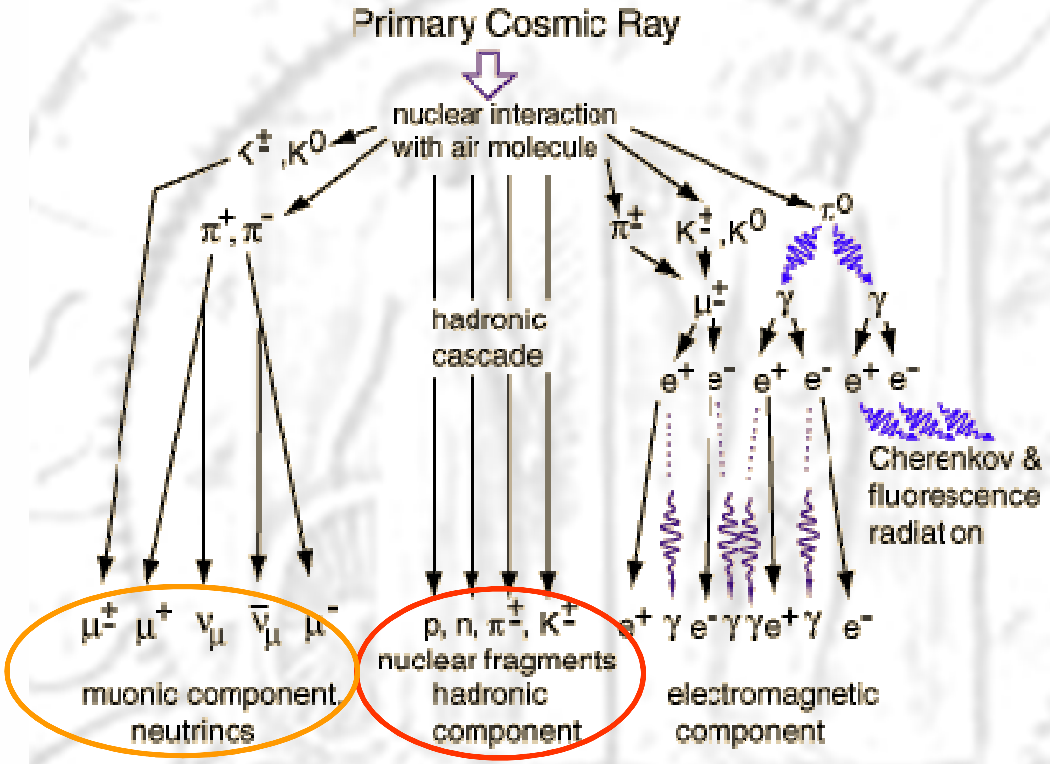


Source: INTEL

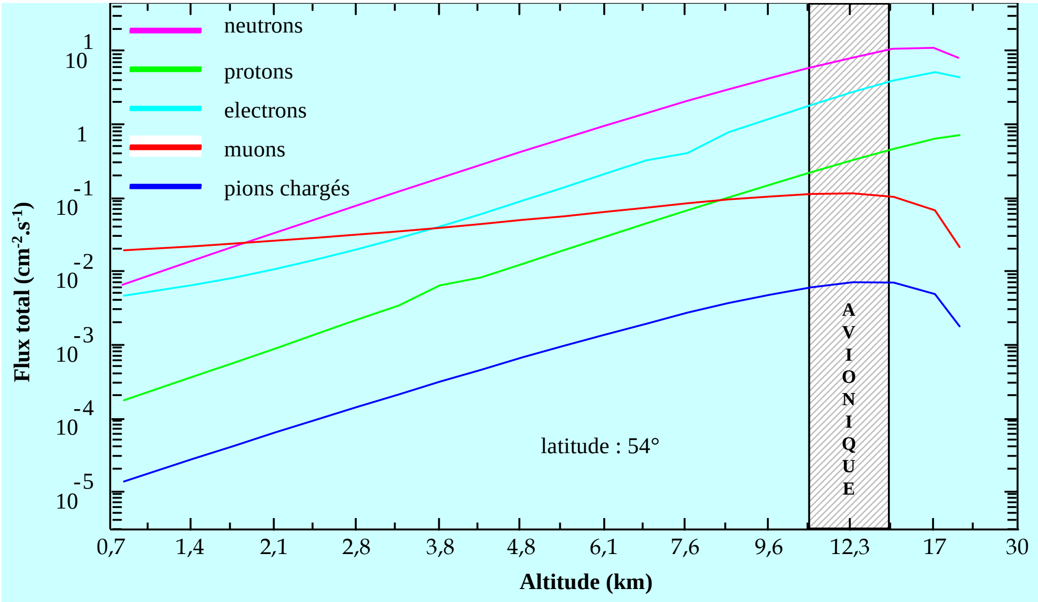


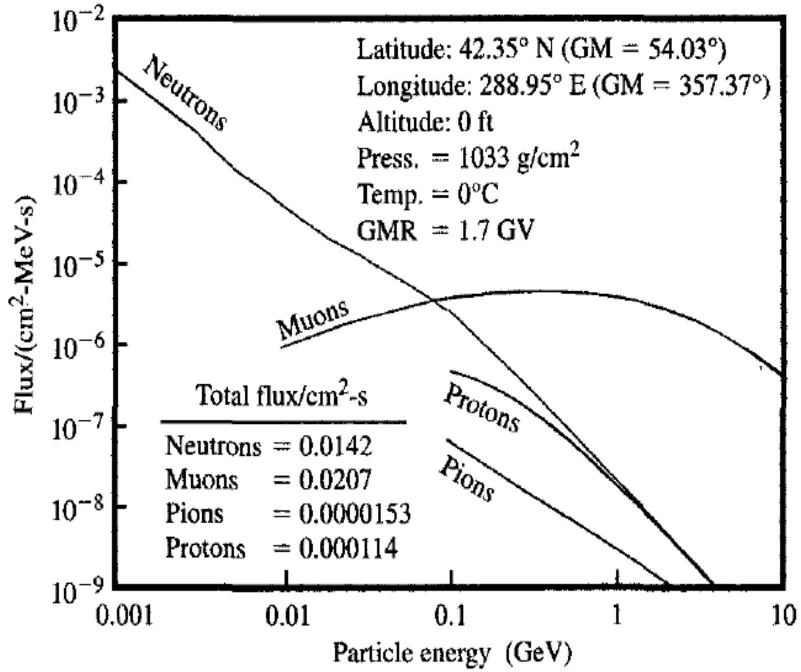
P. Dodd, et al., IEEE-TNS, 1998

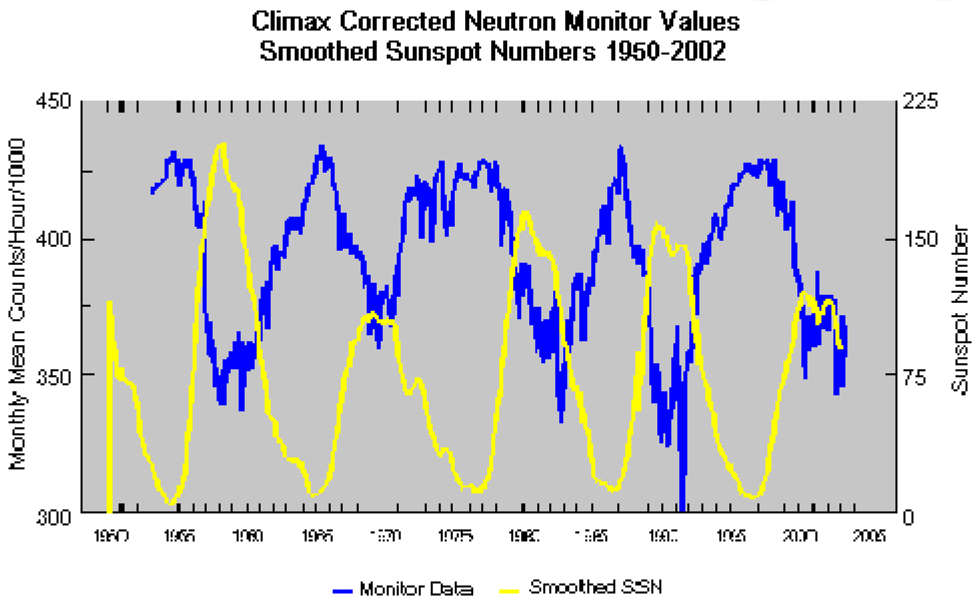
Victor Hess before his 1912 balloon flight in Austria, during which he discovered cosmic rays



Atmospheric particles flux

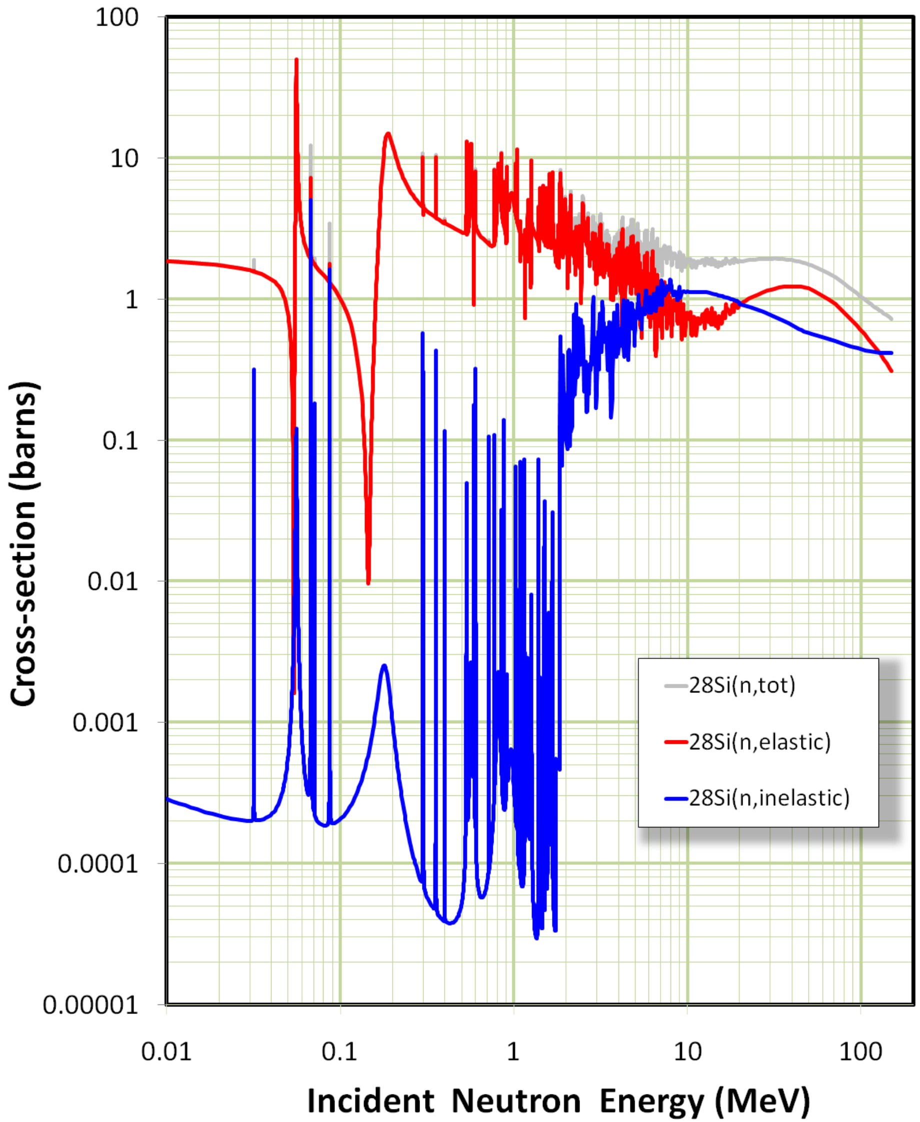






J. F. Ziegler, IBM J. Res. Develop., 1998.

- **Wide neutron energy spectrum**
- JEDEC JESD89A (standard flux): **~ 13 n/cm²-hr** @ sea-level, NYC, $E_n \geq 10$ MeV



Inelastic reactions $^{28}Si + n \rightarrow$

$^{25}Mg + \alpha$	2.75 MeV
$^{28}Al + p$	4.00 MeV
$^{27}Al + d$	9.70 MeV
$^{24}Mg + n + \alpha$	10.34 MeV
$^{27}Al + n + p$	12.00 MeV
$^{26}Mg + {}^{3}He$	12.58 MeV
$^{21}Ne + 2\alpha$	12.99 MeV

F. Wrobel et al., IEEE TNS, 2000

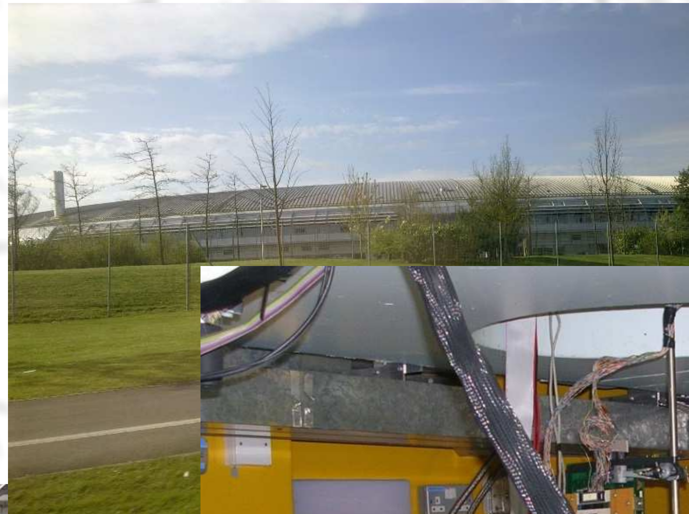
Plus reactions between n and O, Al, Cu, W, …

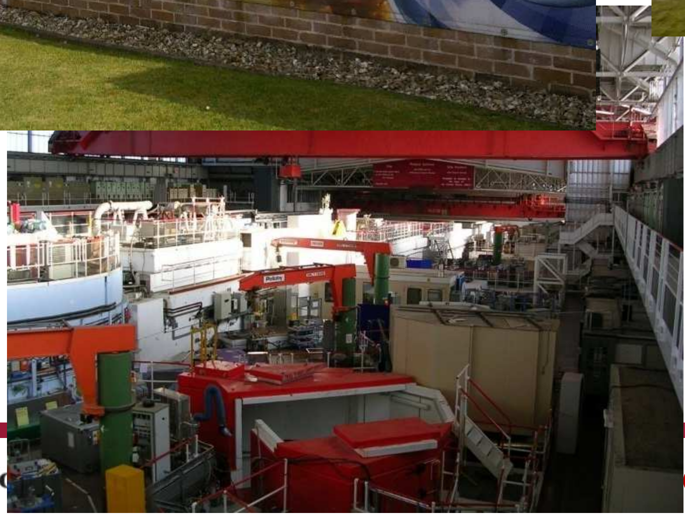
Testing with wide neutron energy spectrum: only **few accelerators** around the world may produce neutron beams at high intensity to perform accelerated testing of electronics:

- **VESUVIO (and shortly CHIPIR) at ISIS, Rutherford Appleton Laboratory, Didcot, UK**
- ANITA, The Svedberg Laboratory, Uppsala, Sweden
- CHARM facility, CERN
- *Petersburg Nuclear Physics Institute (PNPI), Gatchina, St Petersburg, Russia*

- Los Alamos Neutron Science Center (LANSCE), Los Alamos National Laboratory, Los Alamos, NM, USA
- TRIUMF, Vancouver, Canada
- *RCNP, Osaka, Japan*

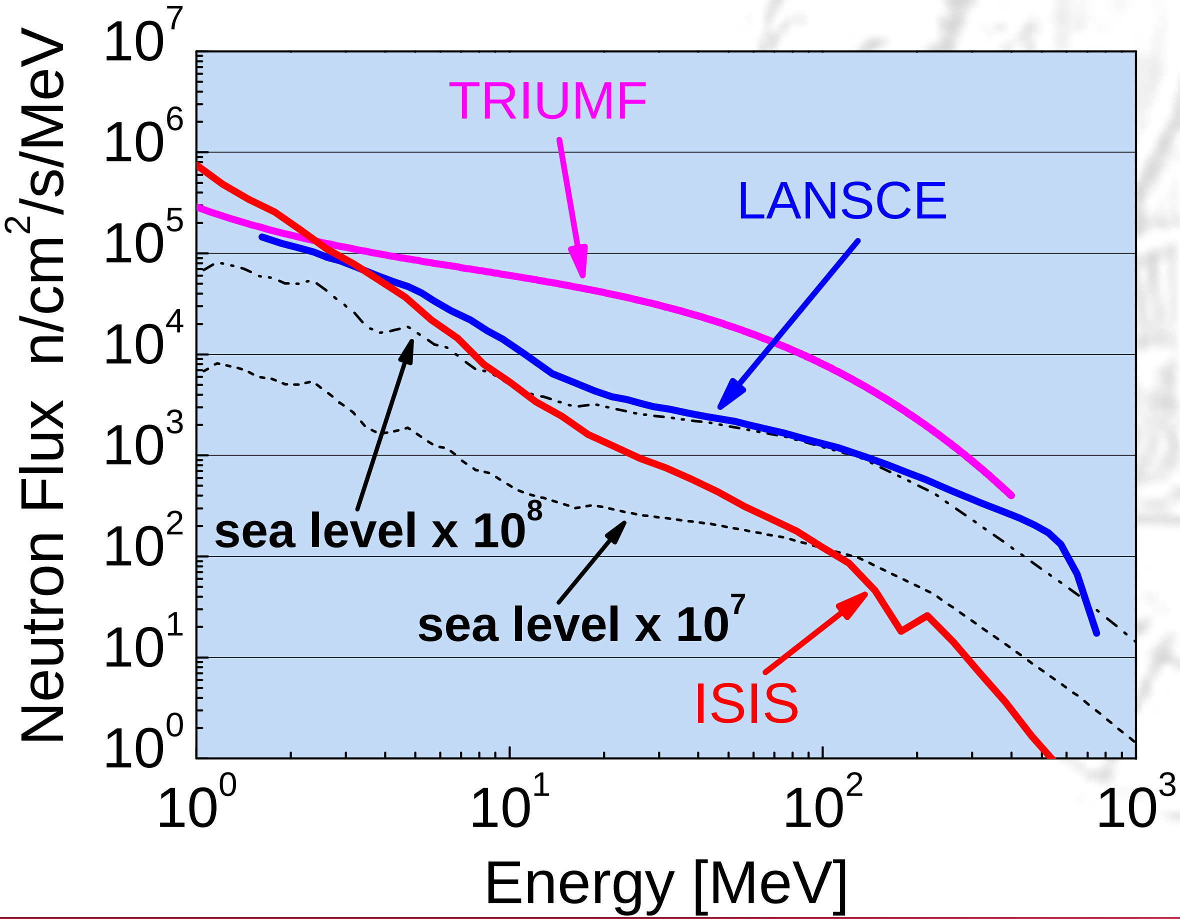
The first SEE testing of electronic components under a wide energy spectrum in Europe performed at the VESUVIO line, ISIS-RAL, Didcot, UK, by an Italian Collaboration (**Universities of Milano Bicocca, Padova and Roma2 Tor Vergata**) *(Andreani, et al, APL, 2008)*



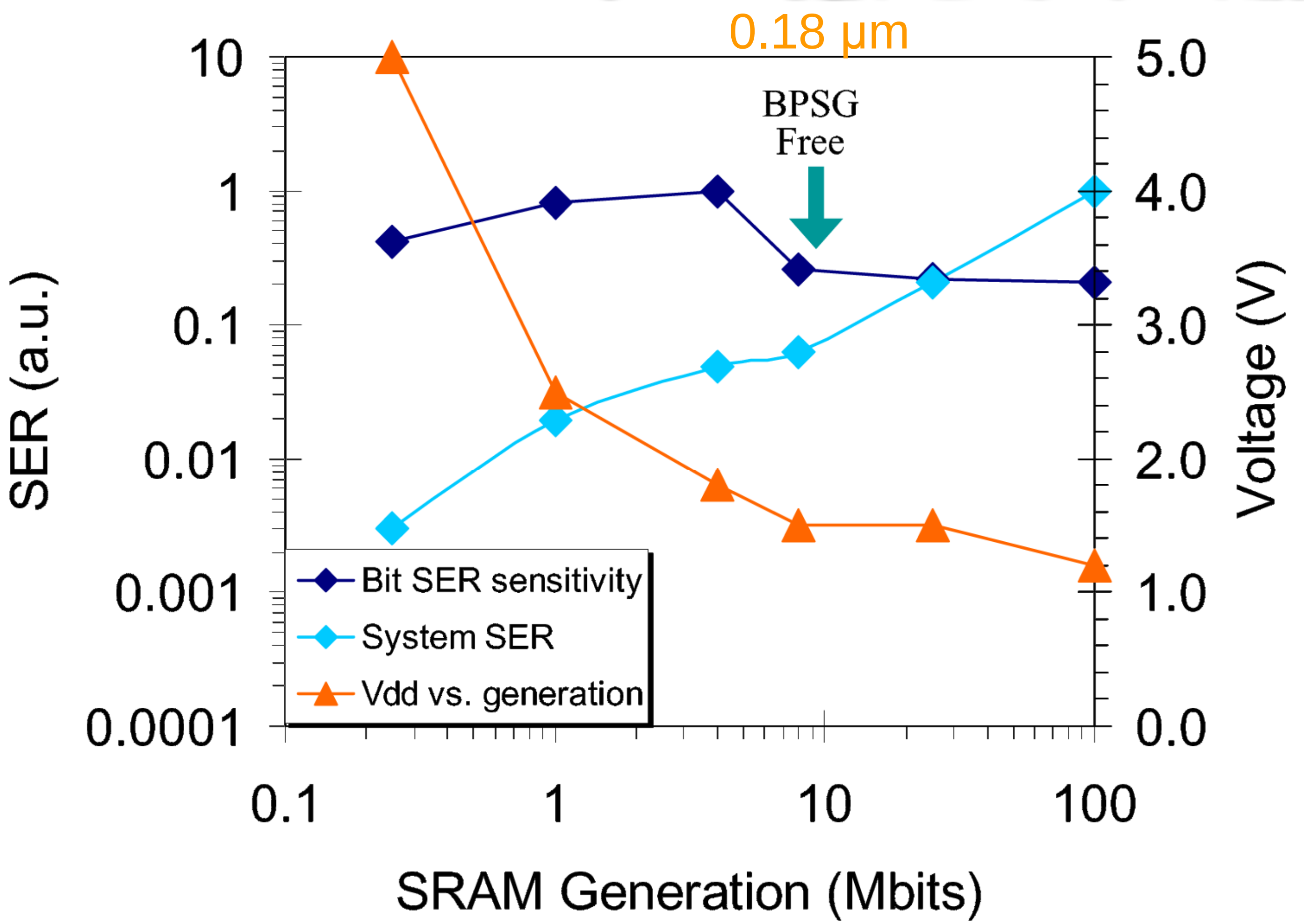


The ISIS neutron spectrum:

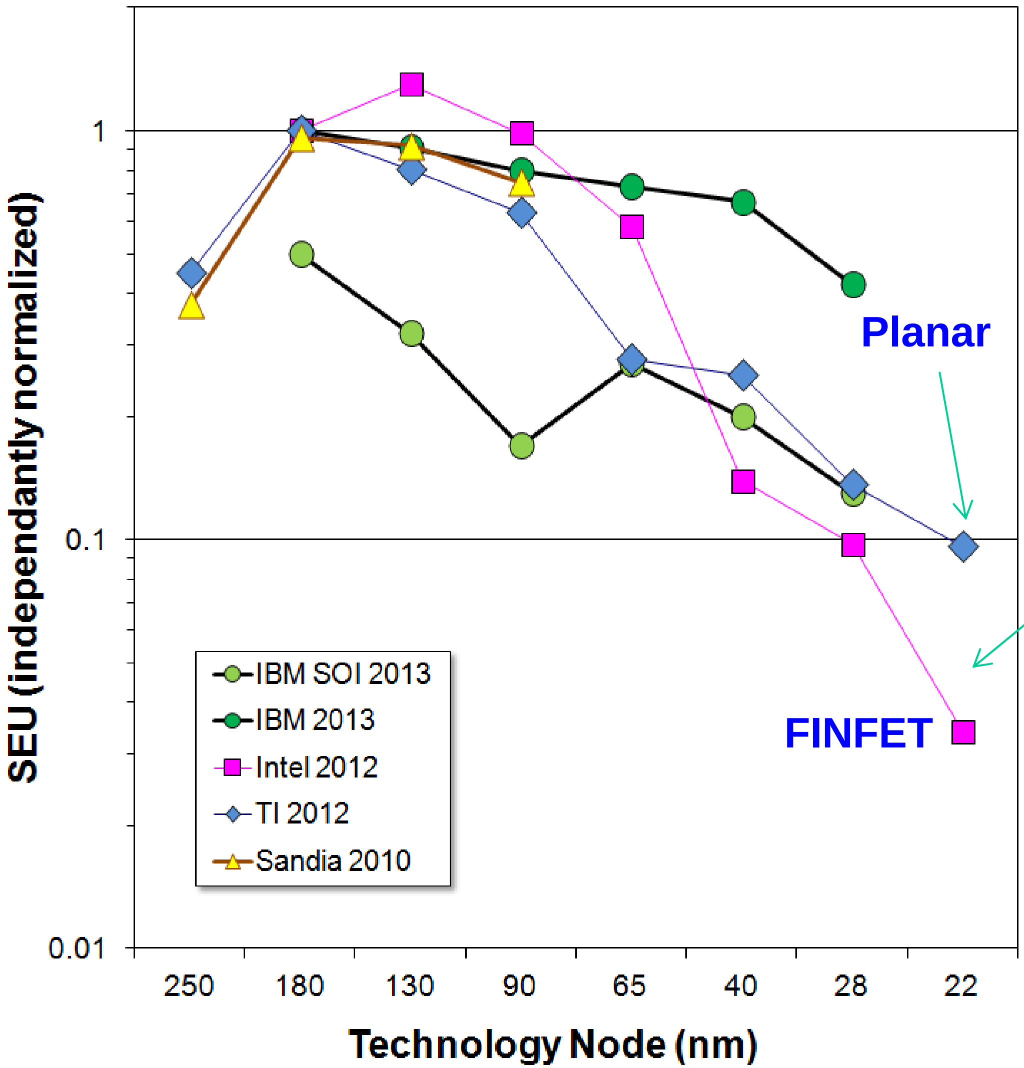
- $1/E^{\alpha}$ characteristic ($\alpha > 1$),
- flux similar to the terrestrial: **acceleration factor** over **10^7**



At ISIS a new line (**CHIPIR**), dedicated to neutron testing of electronics, is under commissioning, with a **higher intensity neutron flux**



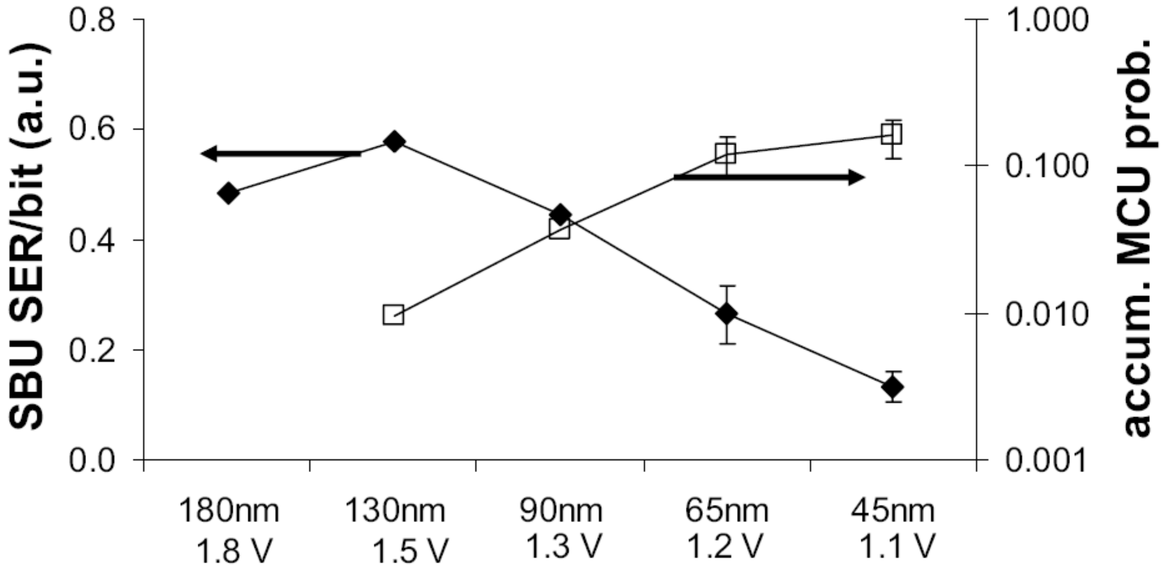
R. Baumann, RADECS Short Course, 2001



Courtesy: Robert Baumann, Texas Instruments, 2013

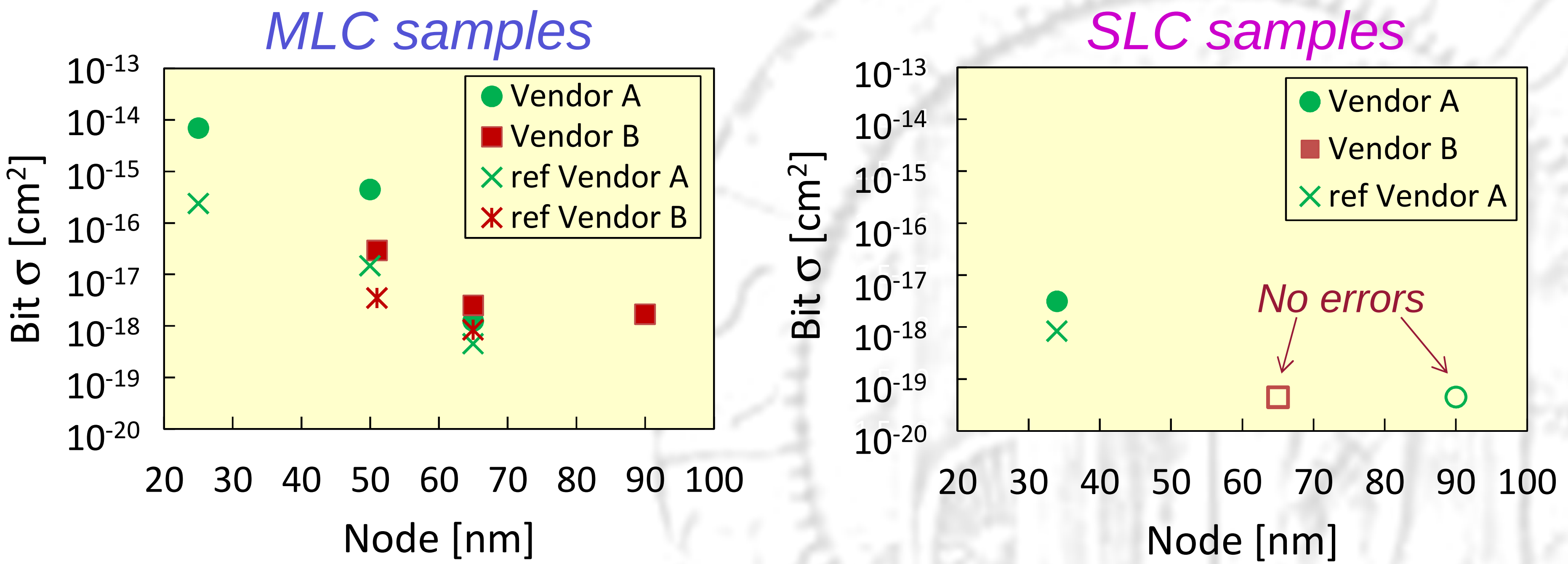
- Per bit, SEU is slightly going down with each generation (since 180 or 130nm)…
- …but system bit count is strongly increasing!

Atmospheric Muon induced SEEs may increase the bit SEU (significantly?) once Q_{crit} <0.1 fC: first tests performed at ISIS (Vanderbilt Univ, Padova Univ)



N. Seifert, et al., IRPS 2008

- **New Single Event Effects** are observed on state-of-the art IC's exposed to neutrons, due to the shrinking MOS size:
  - Multi-cell hits
  - Charge sharing
  - Grazing angle effects
  - SEU bursts
  - MBUs rising, more difficult to correct by onboard ECC



S. Gerardin, et al., TNS 2014

- In NAND Flash Memories, the neutron bit cross section σ exponentially increases as the cell feature size is reduced (*Multi Level Cell: MLC*)
- 34-nm SLC is one of the first generations of single-bit NAND cells (Single Level Cell: SLC) sensitive to neutrons

- Single event effects are produced by collecting the charge generated in the semiconductor by a single ionizing particle: charge > critical charge (CC)
- Different SEE's may occur depending on the device type, being either soft or hard in nature
- SEE's take place not only in radiation harsh environments but also at **sea and avionic levels**
- The SEE per bit sensitivity of current CMOS technologies is stable/decreasing, but the **overall system SER is increasing**
- Diverse SEE features appear in scaled CMOS IC's, needing suitable countermeasures to mitigate SEE's and reduce SER
- New concerns may arise from terrestrial muons when CC<0.1 fC

Keeping high reliability levels in IC's requires extensive neutron (and muon) testing by using accelerators!