Istituto Nazionale
di Fisica Nucleare
Sezione di Torino

# Readout triggerless per sensori a pixel ibridi al silicio

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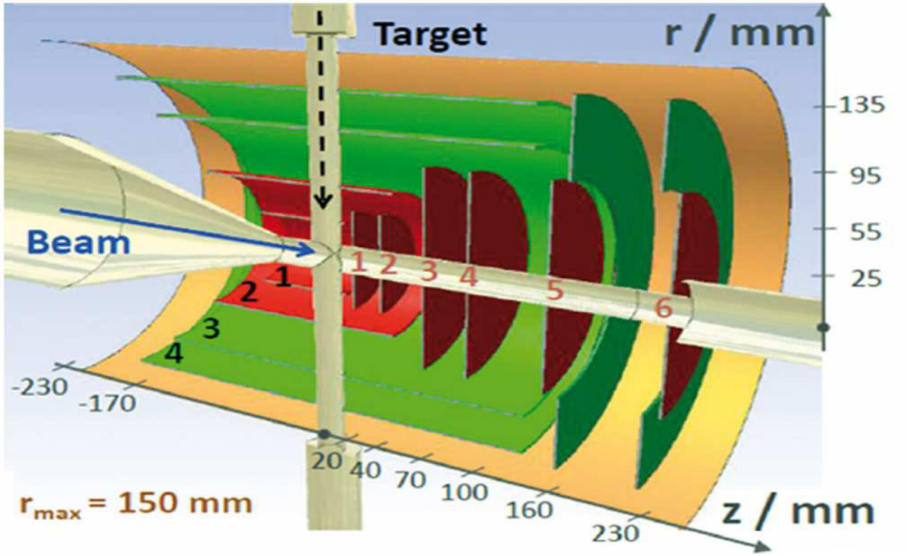
**on behalf of the Torino MVD pixel group**

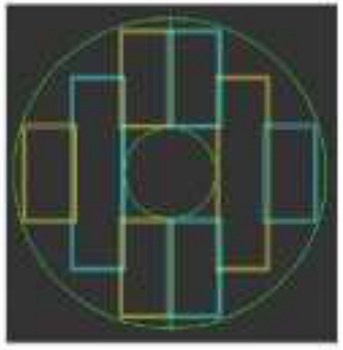
101° Congresso Nazione della Società Italiana di Fisica 2015
24 Settembre 2015 – Università la Sapienza, Roma



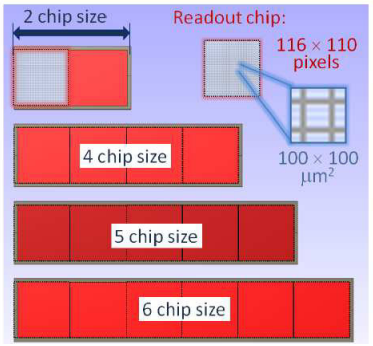

## Hybrid Pixel Sensors

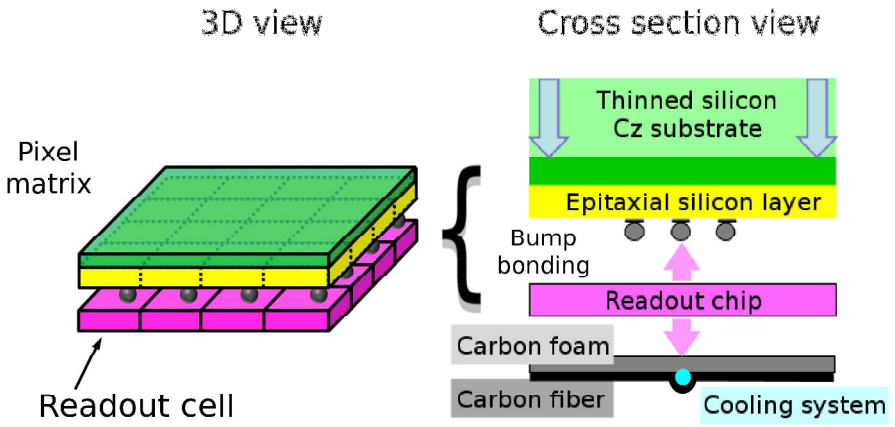
- The resolution depends on the pixel size.
- Compared with strip sensors, the hybrid sensors are not affected by the ghost effect problem but at the price of using more channels.
- Since these sensors are adapt for high rates, they are used to build the internal barrels and all the disks of the MVD.

### Forward Disk



### Modules

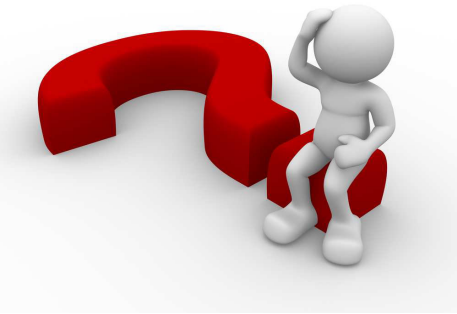


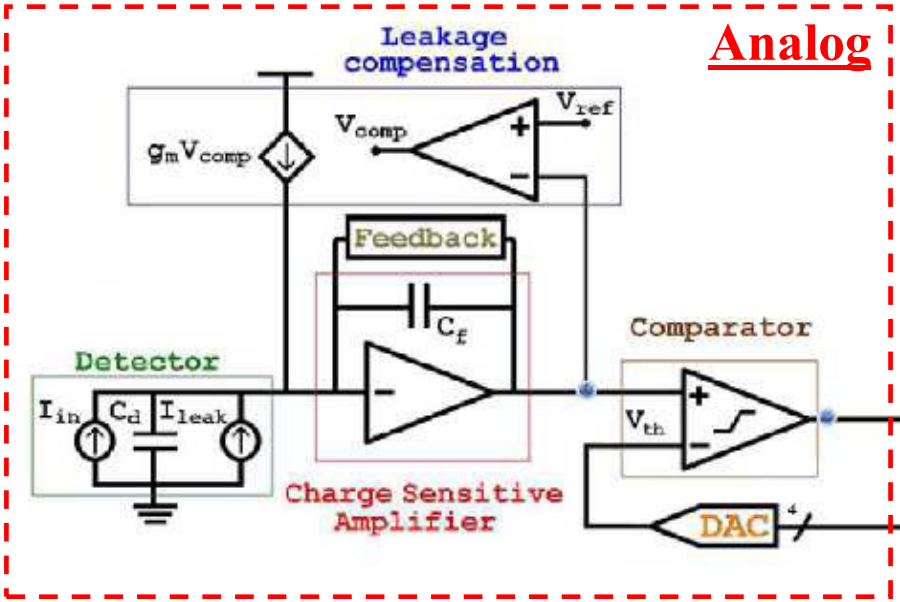
# The ASIC requirements

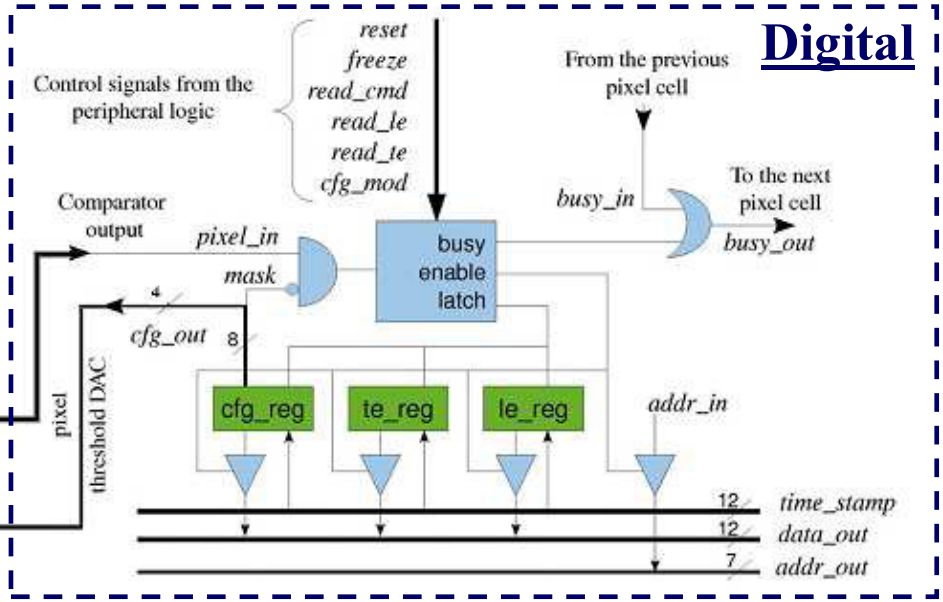
| | |
|---|---|
| **Measurements** | Position / Energy loss / Time |
| **Pixel Size** | 100 μm x 100 μm |
| **Time/charge digitization** | At pixel level |
| **Chip Active Area** | 11.4 x 11.6 $mm^2$ |
| **System Clock** | 160 MHz |
| **Power Consumption** | < 800$mW/cm^2$ |
| **Max event rate** | 6.1 x $10^6$ $hit/cm^2s$ |
| **Time resolution** | <10 ns |
| **Trigger** | Self triggering |
| **TID tolerance** | 10 Mrad |
| **Noise Level** | 200 $e^-$ rms |
| **Linear dynamic range** | Up to 50 fC |

**To satisfy the requirements it was necessary to develop an ASIC called ToPix. Currently the fourth version is under test.**

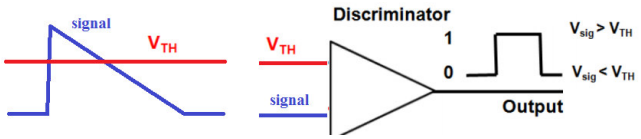


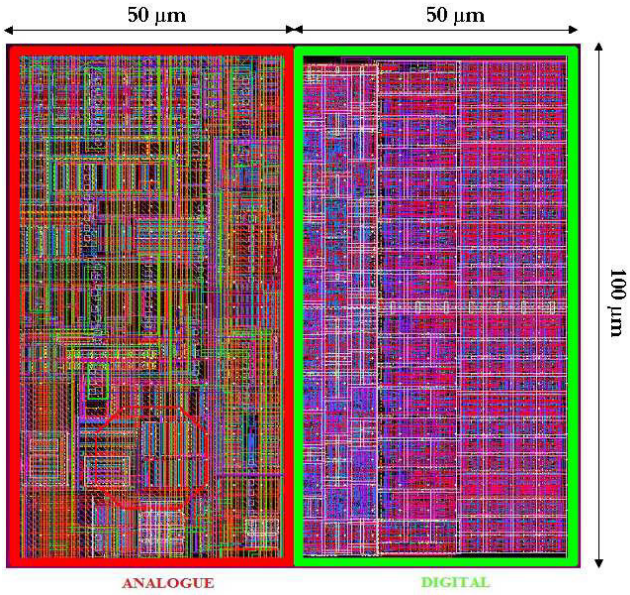
# The Pixel Architecture of ToPixV4




## Time Over Threshold

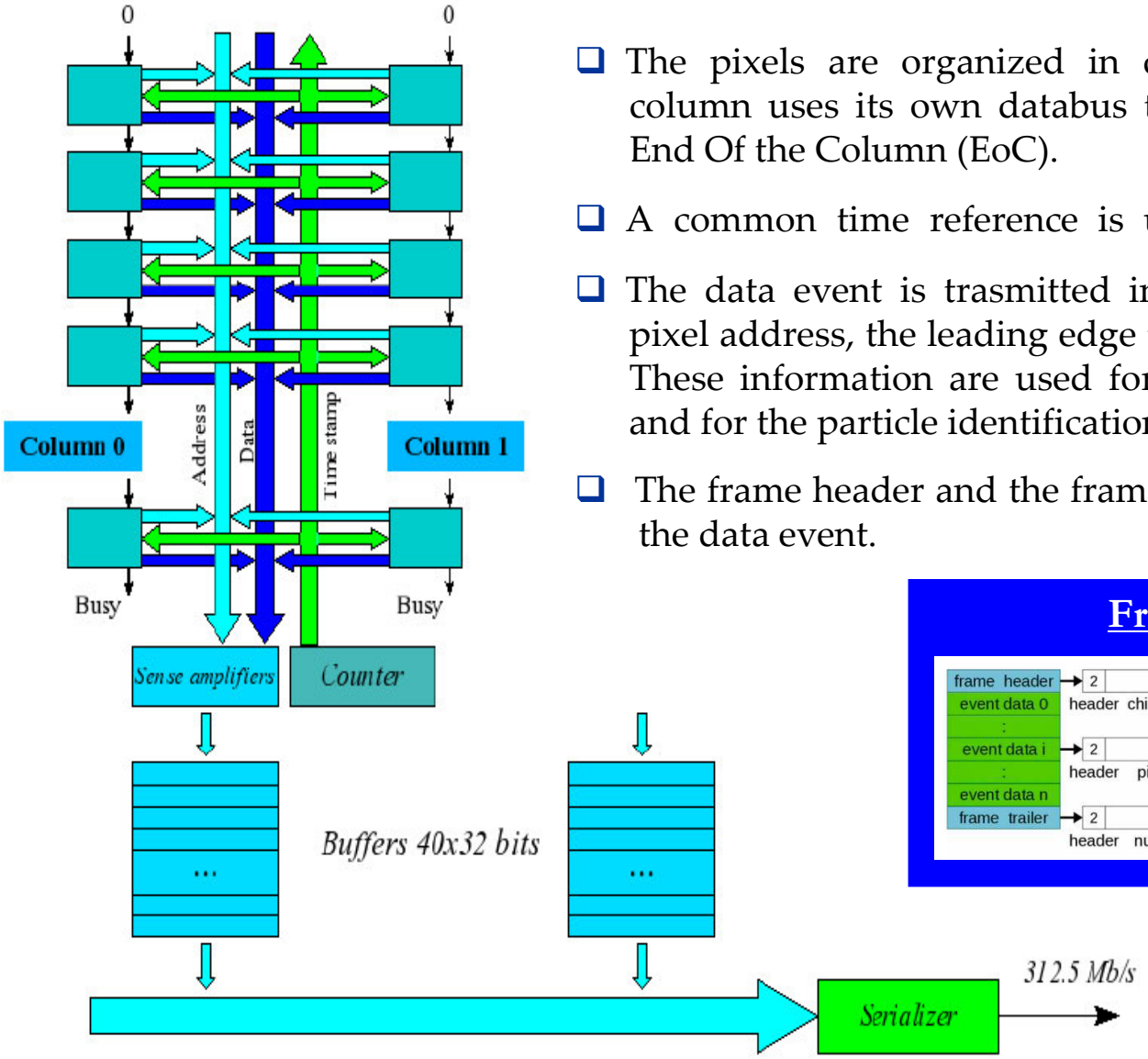



## SEU Protection @ pixel level

- The **leading and trailing registers** are protected via DICE latches.
- The **configuration register** is protected with TMR/Hamming.

# Readout Architecture of ToPix

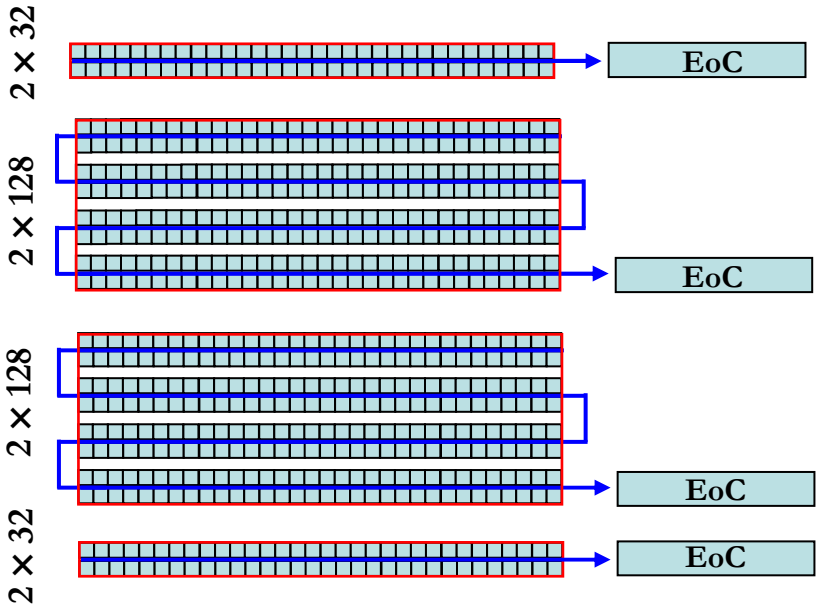


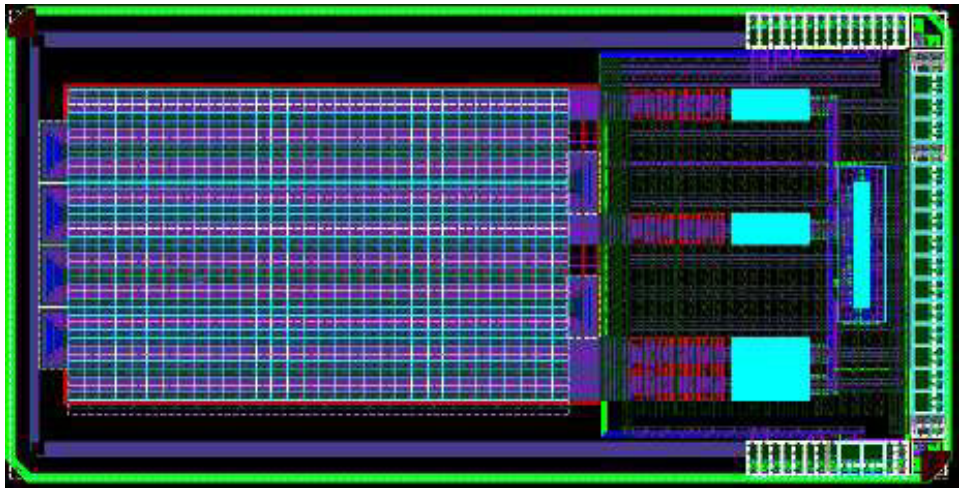

- The pixels are organized in double columns. Each double column uses its own databus to send the information to the End Of the Column (EoC).
- A common time reference is used to send the time stamp.
- The data event is trasmitted in a packet which contains the pixel address, the leading edge time and the trailing edge time. These information are used for the hit position identification and for the particle identification.
- The frame header and the frame trailer allow to identify easily the data event.

## Frame Format

| | | | | | |
|---|---|---|---|---|---|
| frame header | 2 | 12 | 8 | 12 | 6 |
| | header | chip address | frame counter | not used | ECC |
| event data 0 | | | | | |
| : | | | | | |
| event data i | 2 | 14 | 12 | 12 | |
| | header | pixel address | leading edge time | trailing edge time | |
| : | | | | | |
| event data n | | | | | |
| frame trailer | 2 | 16 | 16 | 6 | |
| | header | number of events | CRC | ECC | |

# Readout Architecture of ToPix V4



Size: 6 mm × 3 mm

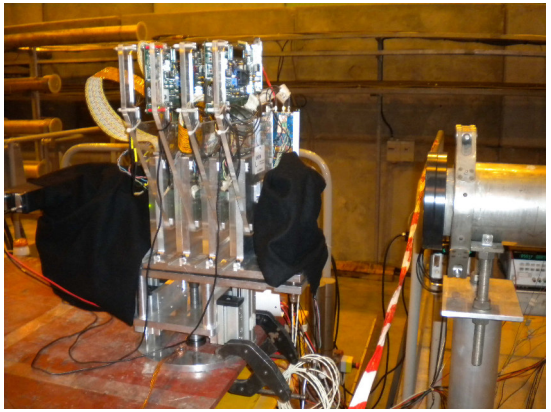
## Improvements in ToPix v4

- The front-end has been modified from version 3:
  - Analog gain increased to improve the ToT linearity with charges < 1fC
  - The threshold tuning system has been improved
- Some aspects of the readout:
  - Reduction of the bus capacitance to improve the performance @ 160 MHz
  - Double Data Rate (DDR) Mode
  - Frame based transmission
- Sensor: compatible with v3 sensors

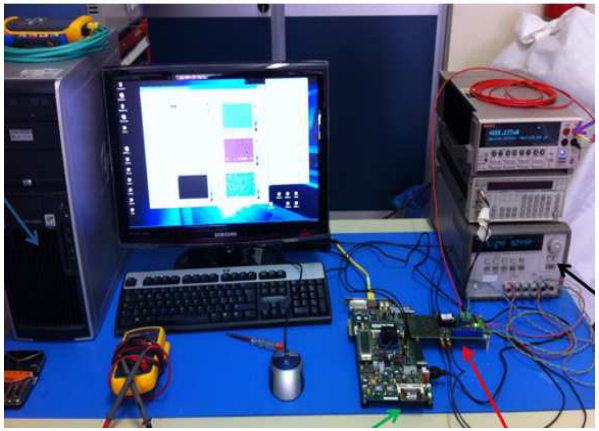
**TopixV4 received on 18° Feb 2014**

# Test & Results

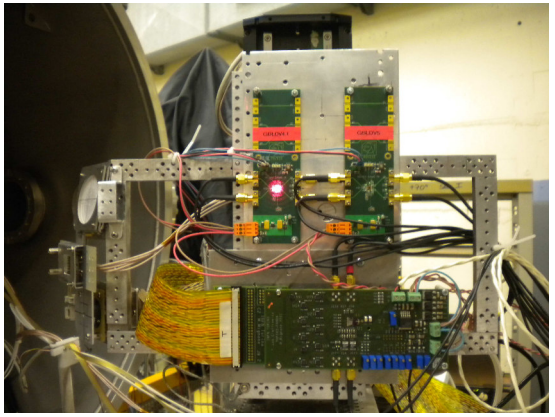
## Test beam



## Characterization

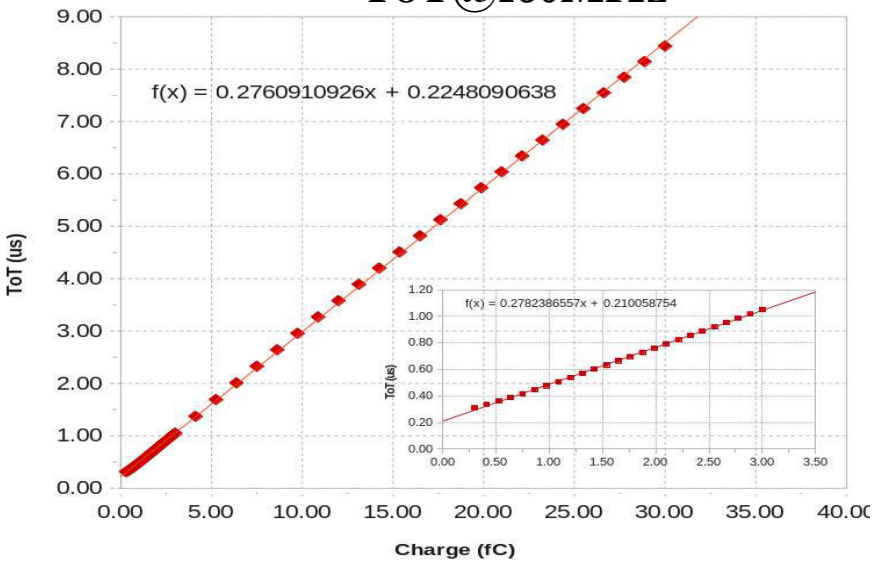


## SEU

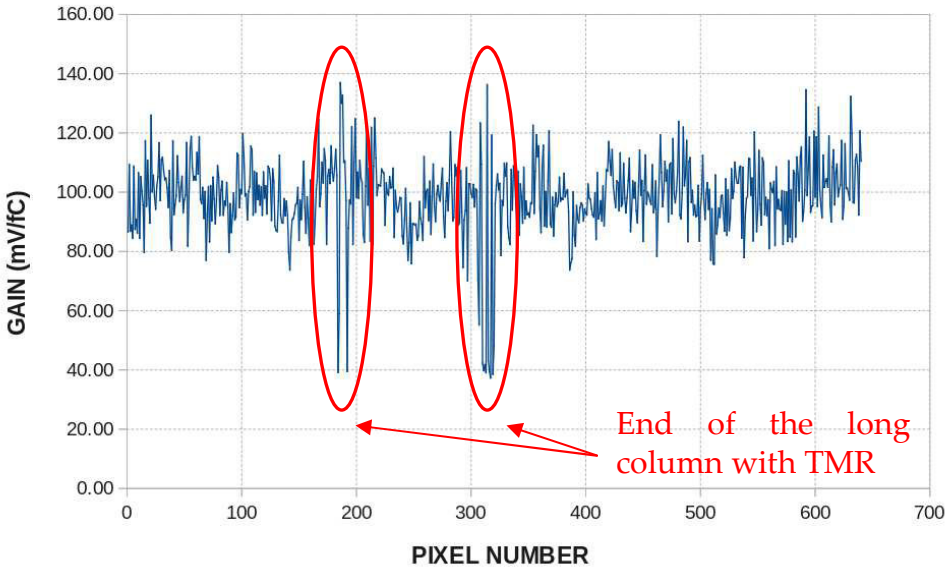


# TopixV4 Characterization

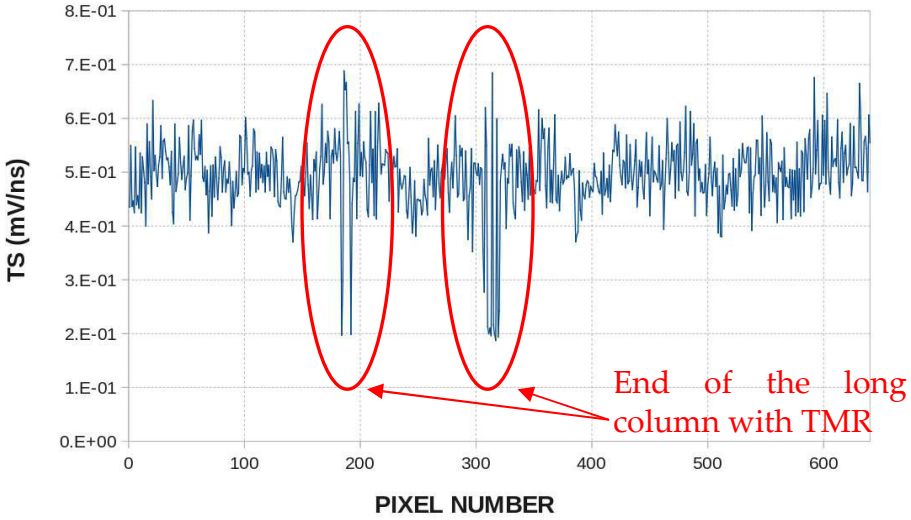
## ToT@160MHz




## Gain @160MHz

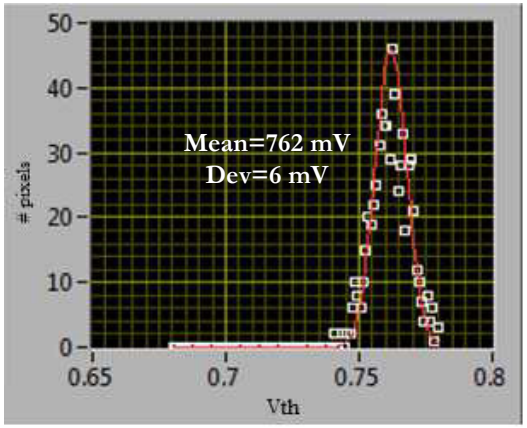



## Tail Slope @160MHz

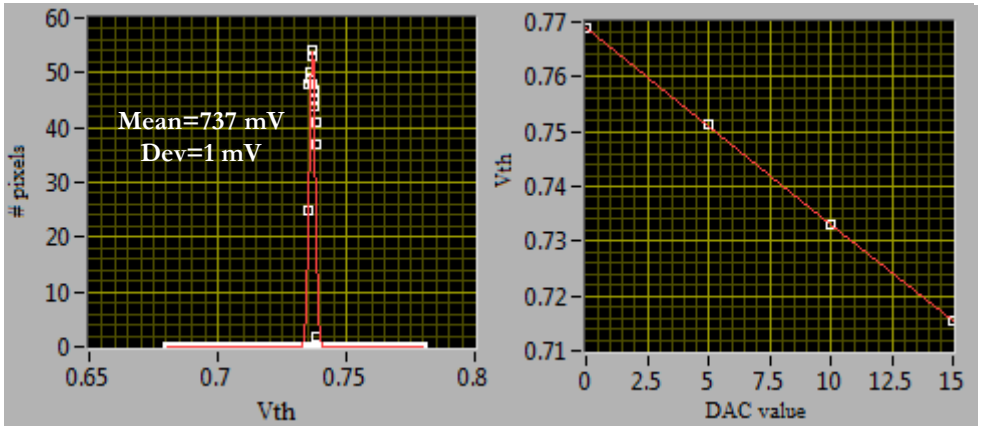



- The ToT is linear also for charges < 5 fC as expected from simulations.
- The gain measurement shows higher values than those obtained with Topix v3 (~ 55 mV/fC) as expected.
- The tail slope measurement shows a strange behavior at the end of the long columns protected by TMR. This effect is present only @ 160 MHz. This may be related to the bus capacitance which limits the data trasmission.

# The threshold tuning

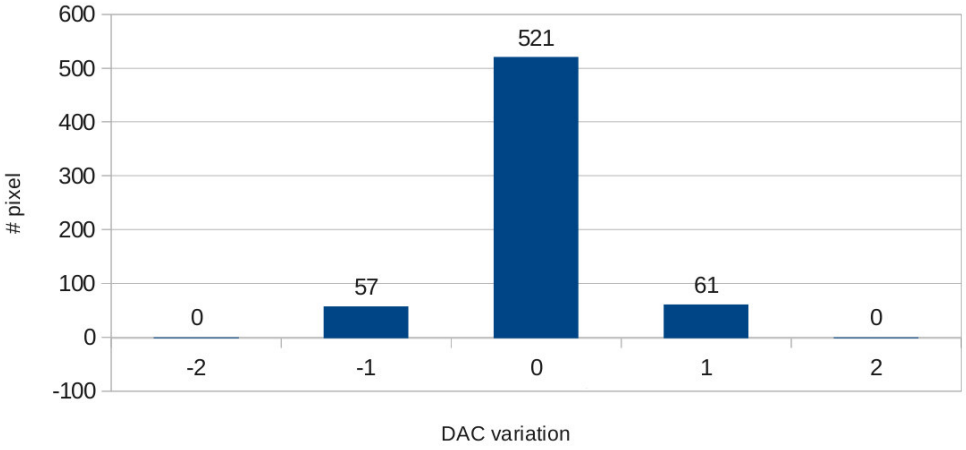



CORRECTION



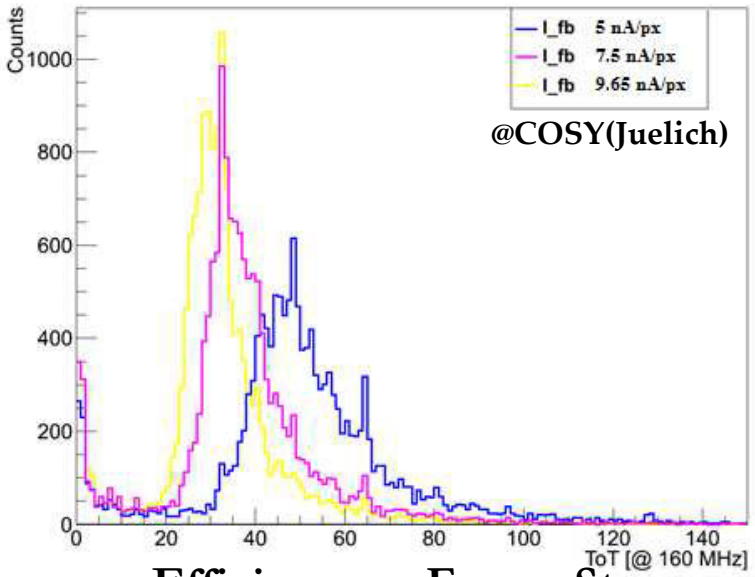

- The new threshold tuning system allows to reduce the standard deviation of the distribution from 6 mV to 1 mV and to set the mean value.
- Thanks to the tuning system linearity the calibration of the 640 channels can be done in few minutes.
- Only small variations of the calibration file are reported after a test beam.

## DAC values variation after a test beam

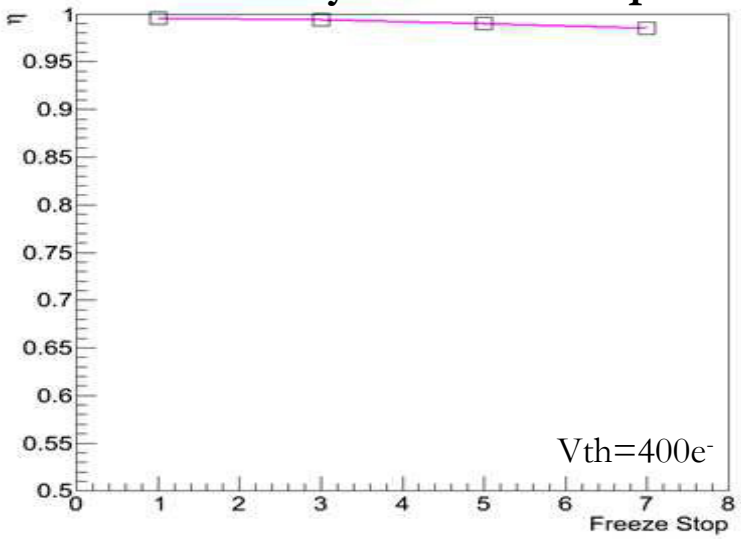


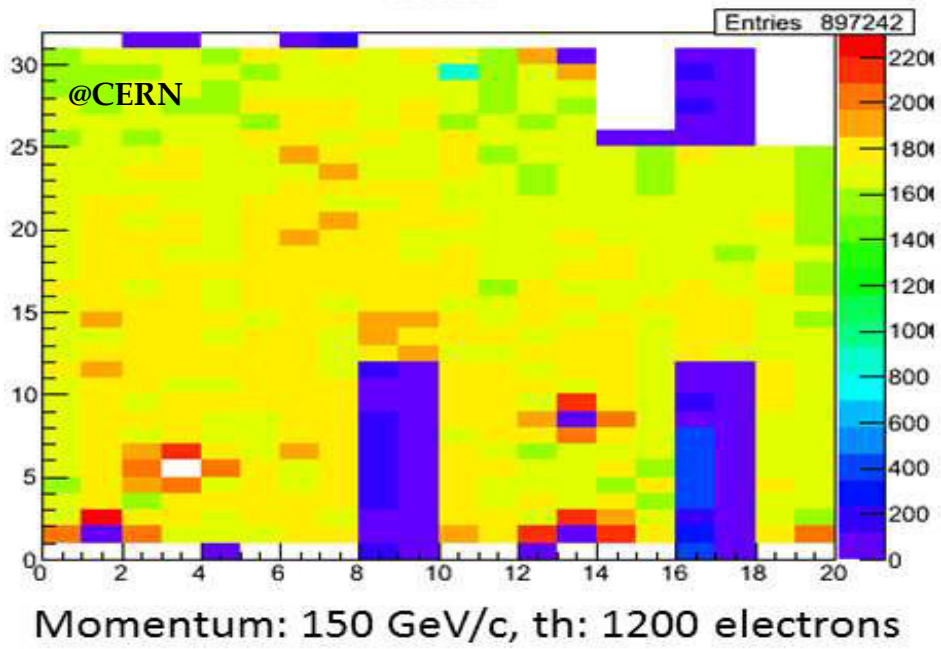
# Test Beam Results

## Ifb Scan



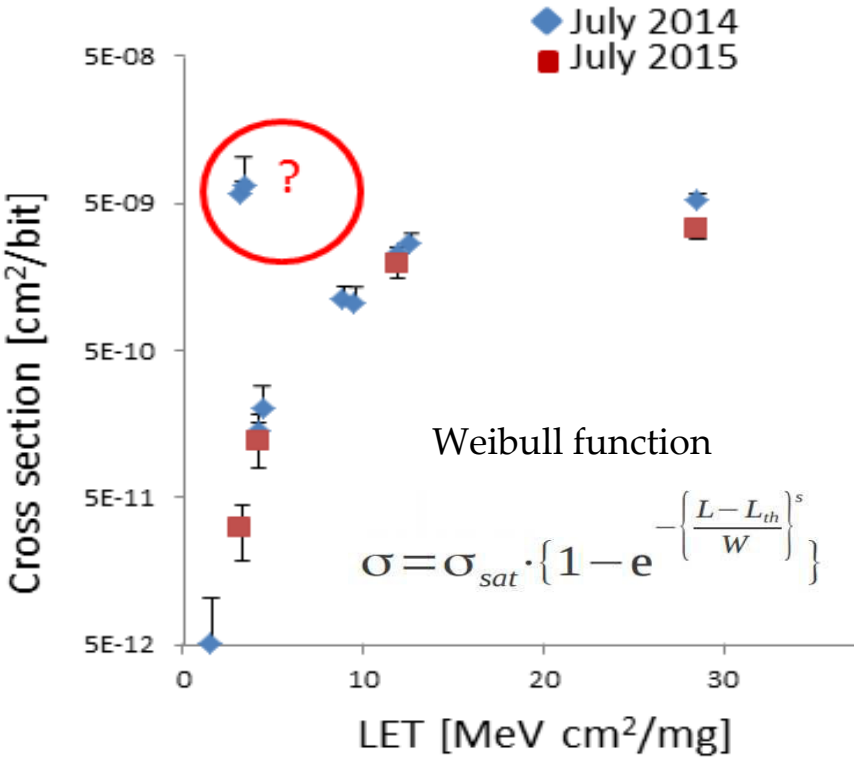

## Efficiency vs Freeze Stop

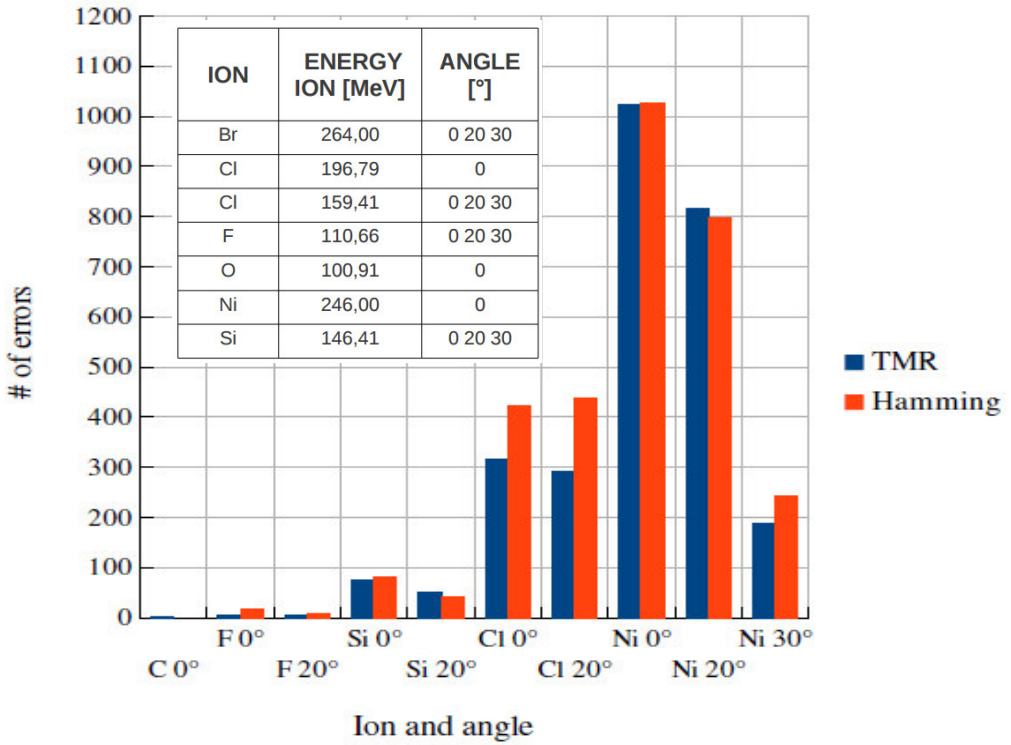



- The ToT distribution is tall and narrow with high values of I_fb.
- During the test, the furthest pixels in the long columns were masked but they reported events anyway. These ghost events may be generated in the EoC. This must be investigated.
- The efficiency has been studied in different working conditions.

# SEU@SIRAD-LNL




- The test @ SIRAD(LNL) in 2015 confirms the trend obtained in the 2014 and improves the statistic.
- All the pixels are SEU protected. Half of them use Triple Modular Redundancy (TMR) and the other part Hamming enconding. The test done shows that the effect of these two protections is similar. However, the readout presents some problems with the long column protected by TMR and so, from this point of view, the Hamming protection can be considered the best choice for the next version.

# CONCLUSION

- The analog performance in terms of ToT, gain and threshold tuning was tested. The results meet the requirements as desired.
- The operation @ 160 MHz shows a limit for the folded column of 128 pixels implemented with TMR. However this point is not so critical because for the final version of the chip is foreseen the use of columns of 116 pixels.
- The test beam gives good results but some effects must be still studied.
- The SEU test @ SIRAD has been done with good results.
- The test of the fourth version can be considered concluded. The design of ToPix v5 is started.

# THANK YOU

# FOR YOUR ATTENTION

# BACKUP SLIDES

# TID test