Design of a 64-channels current-to-frequency converter ASIC, front end electronics for high intensity particle beam detectors

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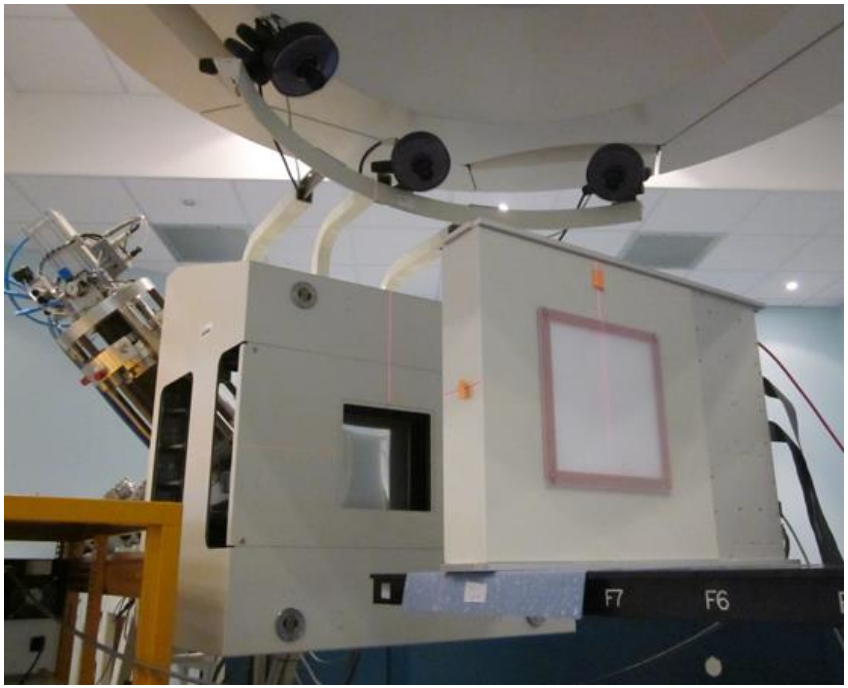
DETECTOR
DEVICES AND TECHNOLOGIES TORINO
Turin University spin-off

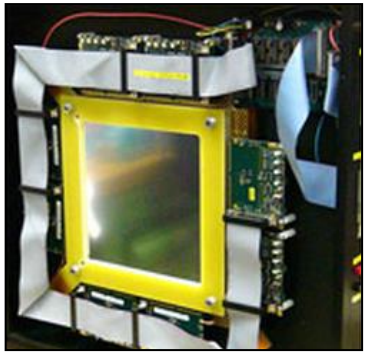
The application field: particle therapy



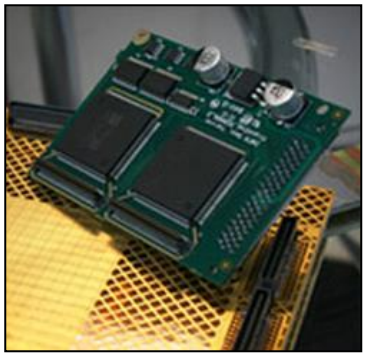
Technology trend:

Compact accelerators with pulsed high intensity beams

- Pulse frequency: 0.2 – 1 kHz
- Pulse length: 5 – 20 μs
- 10^7-10^8 protons/pulse (average current during the pulse of 1 - 25 μA)
- High dose rate

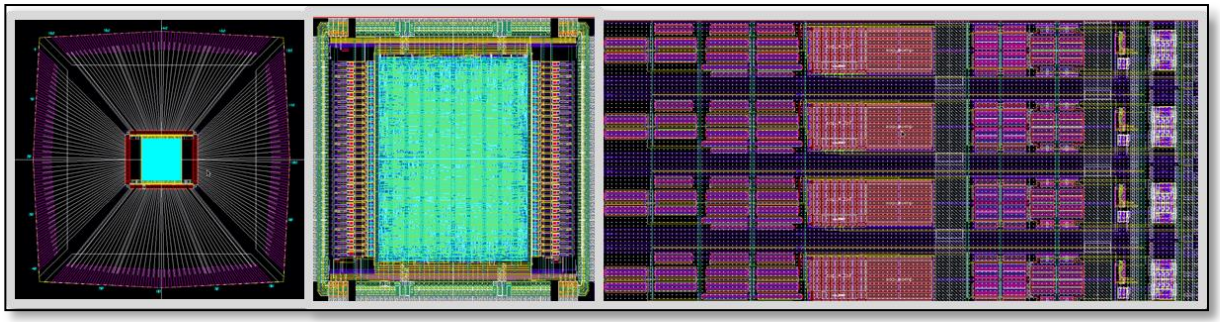


Modern version of detectors and thus new dedicated electronics are needed



An updated version of the TERA chip will be available soon

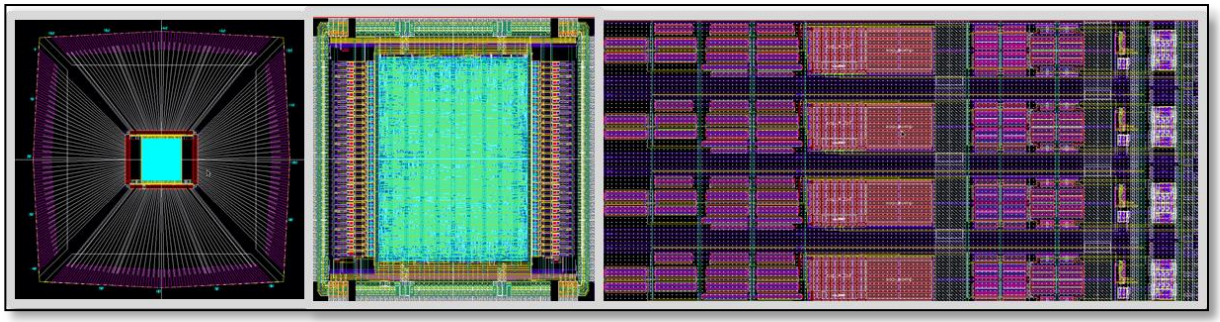
TERA09 DESIGN



Targets:

- Satisfy the new application requirements

TERA09 DESIGN



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- Satisfy the new application requirements
- Maximum backward compatibility

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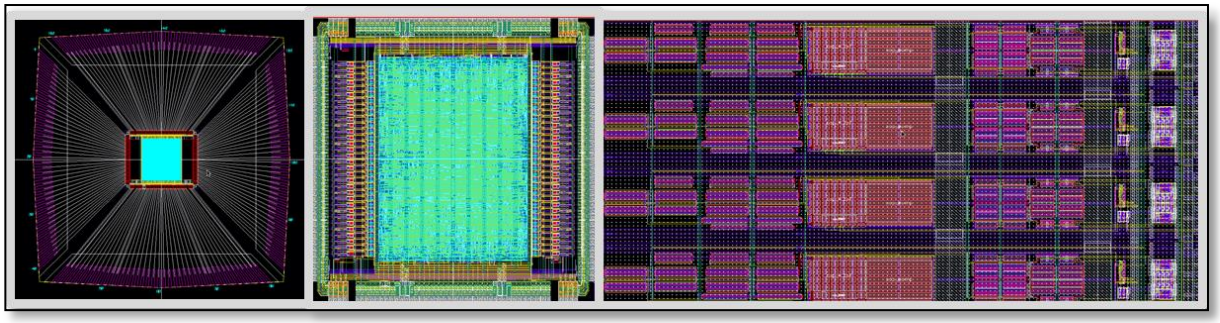
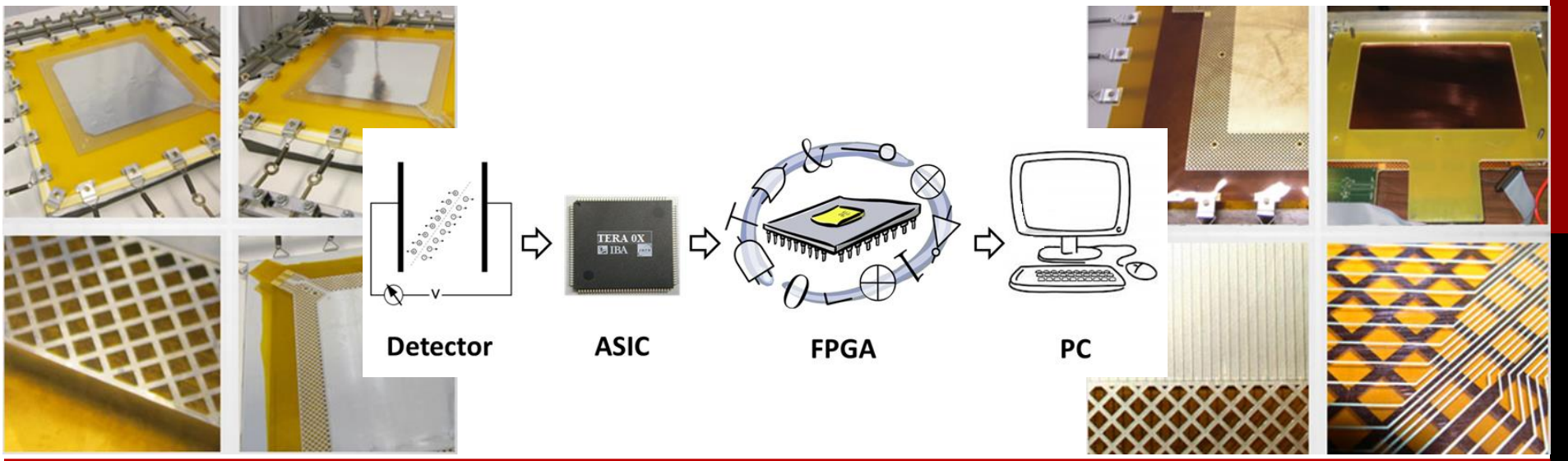


Targets:

- Satisfy the new application requirements
- Maximum backward compatibility
- Simplicity and flexibility maintained



The TERA09 ASIC is the upgrade of the last version of the chip designed in the VLSI group of Turin, the TERA08

TERA08

- Produced by iba (Louvain La Neuve, Belgium)
- Used for INFN research projects
- Installed by DE.TEC.TOR. S.r.l. in ionization chambers adopted by medical centres like CPO, PSI, CNAO and MedAustron

TERA09
Main features

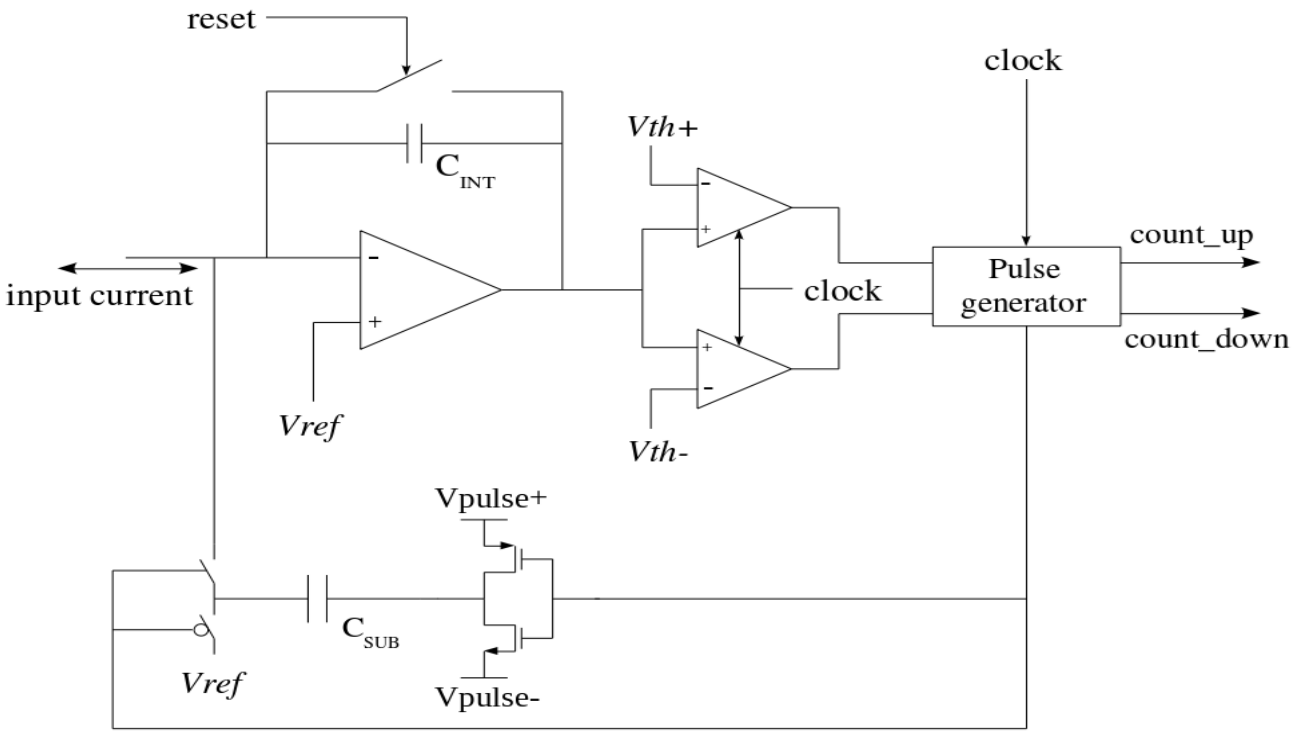
- 64 channels i/f converter
- VLSI CMOS AMS 0.35 μm technology
- Able to manage bipolar input currents in the range 0.1nA ÷ 3mA → 64 channels in parallel
- Single channel conversion linearity up to 15μA
- Integrated system of adders (single channel output, sum of 4, 16, 32 and 64 channels output)
- Warning signal (to overcome the registers overflow)

The TERA09 ASIC

Functional blocks:

- Current to frequency converter
- Digital logic
- Logic interface

The current to frequency converter scheme



Recycling integrator structure →dead time free data acquisition

i-v Converter: main changes

- Integration capacitance : 600 fF → 1.2 pF
  - ➔ *slower ramp gives more time to the circuit to react*

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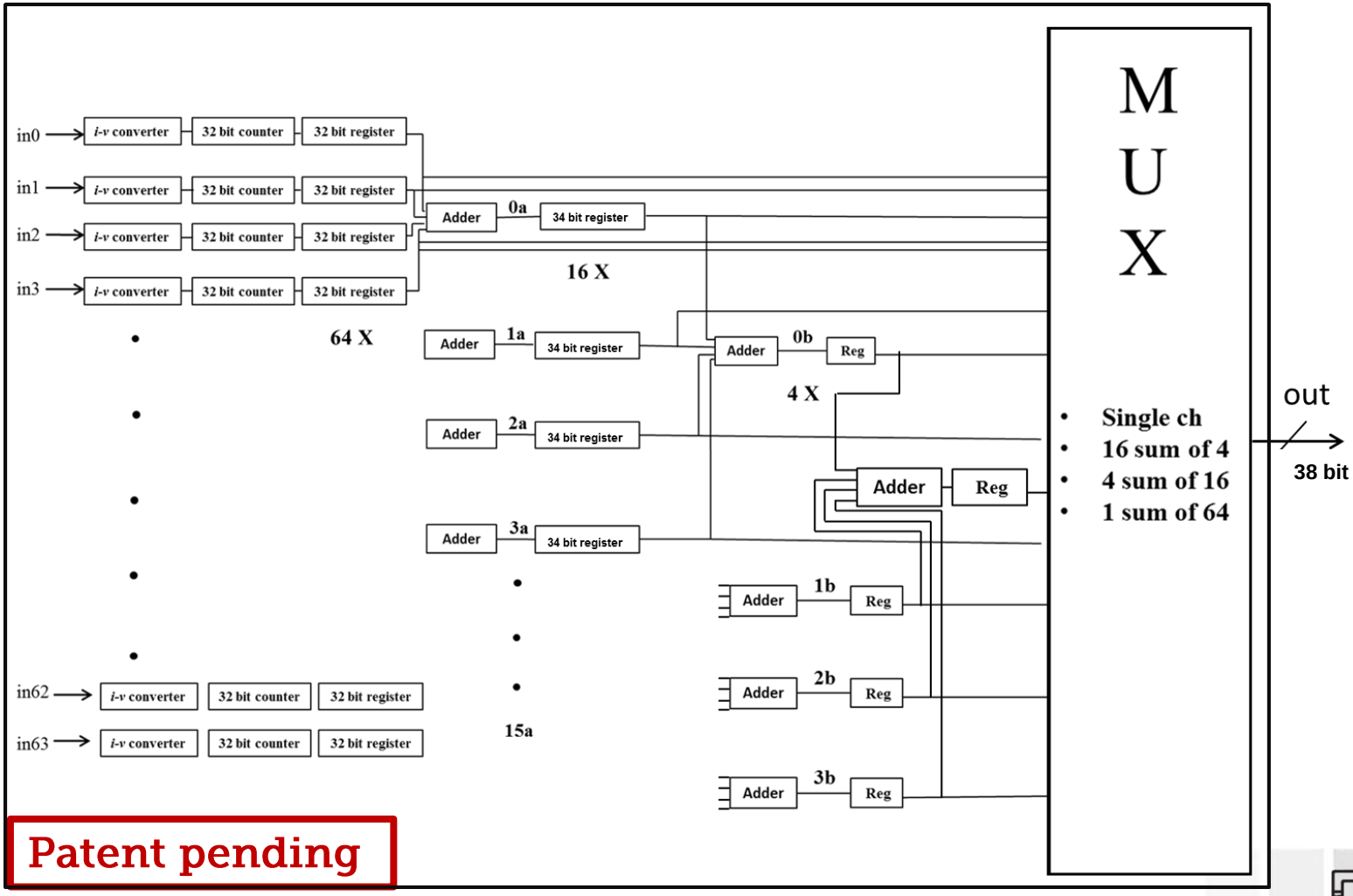
- Single 200 fC subtraction capacitor

Digital logic

- Sixteen 34-bits registers providing the result of the sum of 4 channels groups
- Four 36-bits registers providing the result of the sum of 16 channels groups
- One 38 bits register providing the result of the sum of all the 64 channels
- Sum operation triggered from the load signal
- 38-bit output bus

Block diagram of the chip structure



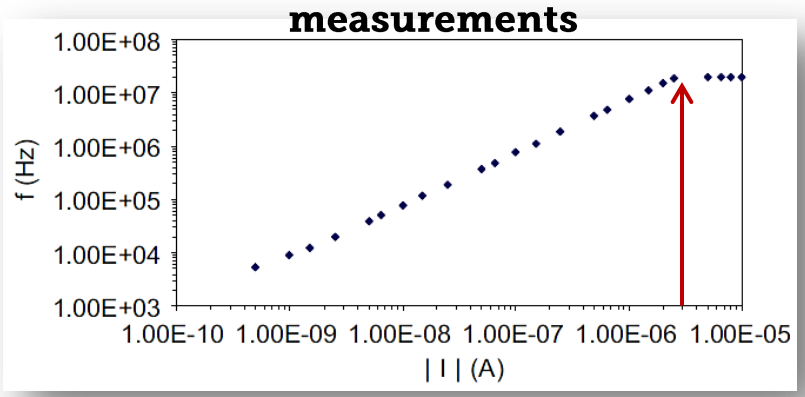
Patent pending

Interface logic

- Programmable bias generator
  - ➔ two internal modes : low power (same bias as the previous version) and high performance
  - ➔ external pin selection
- LVDS receiver
  - ➔ required to receive the 320 MHz clock

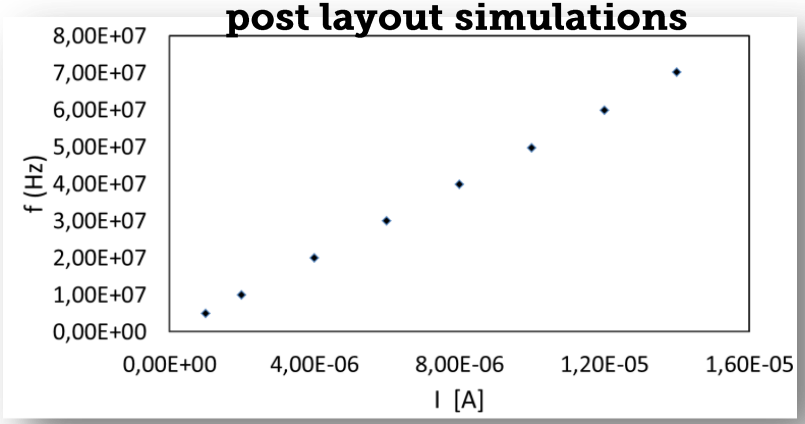
First linearity study

TERA08



A. La Rosa et Al., Nucl. Instr. and Meth. A 583 (2007) 461-468.

TERA09



Using a Q_c of 200fC (most used in therapy)

The single channel saturation point is moved from 4µA to 16 µA

The digital architecture (with an integrated channels parallel connection) permits to extend the current input range up to 1mA (and over, with a Q_c that can reach 660fC)

Project status and plans

- Submission date to Europractice: Sep. 14th 2015
- Submission date to AMS: Sep. 21st 2015
- Samples out from AMS: Nov. 6th 2015
- Packaged samples from Europractice: Nov. 23rd 2015
- PCB design: Oct.-Dec. 2015
- ASIC characterization: Dec.-March 2016
- Integration with detectors and beam tests

Conclusion

- The design of TERA09 is submitted
- The technical requirements are satisfied:
  high input current range (hundreds of pA to few mA)
- The backward compatibility is greatly accomplished:
  similar signals for data, controls, tests, almost equivalent area, selectable I_{bias} and conversion frequency…
- The ASIC architecture is quite simple therefore, the device remains versatile
- Waiting for the chip, we have to prepare the system for the test and the characterization of the prototypes

Thanks for your attention

BACKUP SLIDES

Addressing scheme

- Channel address via 7 bit bus
  - $0b_5b_4b_3b_2b_1b_0$: select register channel $b_5b_4b_3b_2b_1b_0$
  - $1b_5b_4b_3b_2x0$: select 1st level sum registers
  - $1b_5b_4xx01$: select 2nd level sum registers
  - 1xxxx11 : select 3rd level sum register

BACKUP SLIDES

Specifications comparison

TERA08

- VLSI CMOS 0.35 μm
- Bipolar input
- Digital output: 32 bit
- Clk 100 MHz
- Max counting rate 20 MHz
- Charge quantum: 50 ÷ 350 fC
- Saturation current 4-7 μA

TERA09

- VLSI CMOS 0.35 μm
- Bipolar input
- Digital output: 38 bit
- Clk 320 MHz (LVDS Rx)
- Max counting rate 80 MHz
- Charge quantum: 200 fC
- Integrated system of adders (single channel output, sum of 4, 16, 32 and 64 channels output)
- Saturation current until mA
- Warning signal (to overcome the overflow)