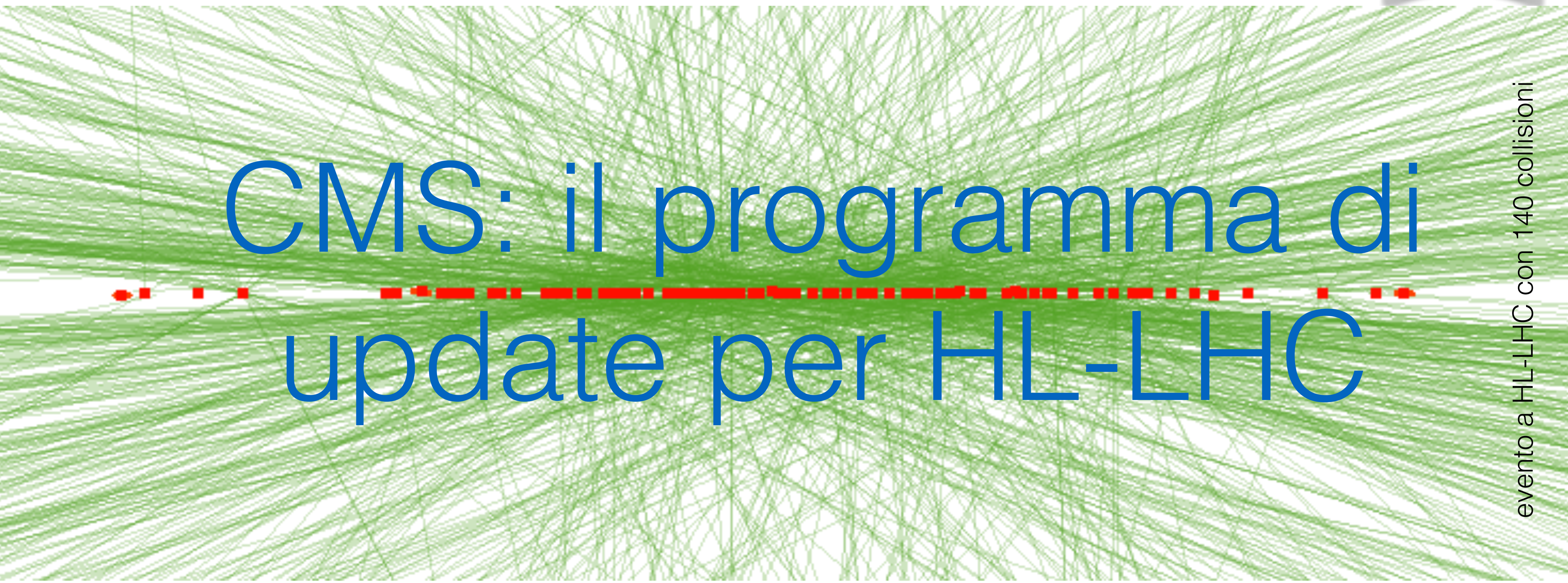
CMS: il programma di update per HL-LHC



evento a HL-LHC con 140 collisioni

L.Demaria, INFN Torino
per la Collaborazione CMS

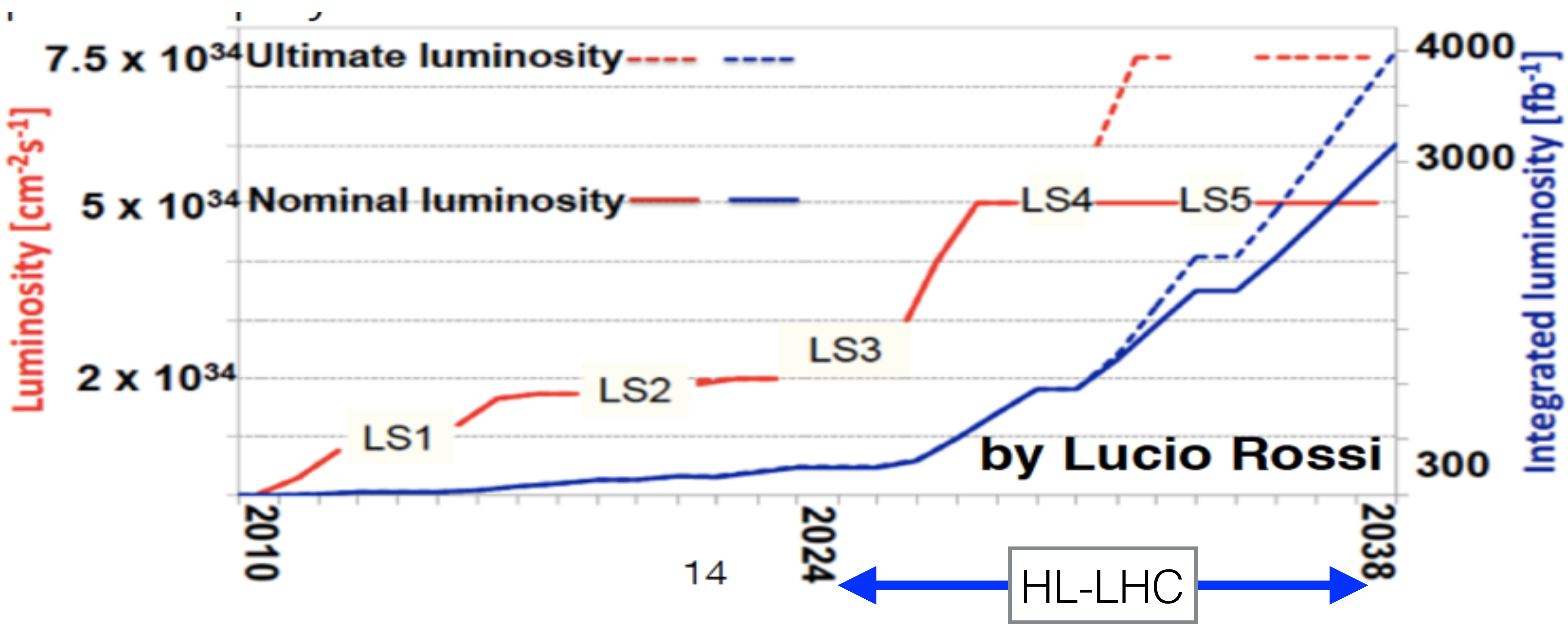
Societa' Italiana di Fisica, 101° Congresso annuale
Universita di Roma La Sapienza, Roma 25/09/2015

Talk layout

1. The HL_LHC challenge
2. The CMS challenge
3. Tracker Detector
4. Calorimetry
5. Muon Detectors
6. Trigger
7. Conclusions

HL_LHC challenge

- High Luminosity LHC, a natural extension of LHC program
  - goal is to reach 3000 fb^{-1} in 10 years
  - x10 LHC Integral Luminosity
  - x5 LHC-0 instant Luminosity (=higher particle flux)
  - x5 LHC PU (140) : now also perspective for x7 PU (200)



Why HL_LHC ?

- From F.Gianotti - Monday:

Full exploitation of LHC project with HL-LHC ($\sqrt{s}$ ~ 14 TeV, 3000 fb^{-1}) is mandatory

- ❑ Present highest-E accelerator:
- → detailed direct exploration of the TeV scale up to m ~ 10 TeV
- → measurements of Higgs couplings to few percent
- ❑ Results will inform the future

F. Gianotti, SIF, Roma, 21/9/2015

Future colliders will give physics data:

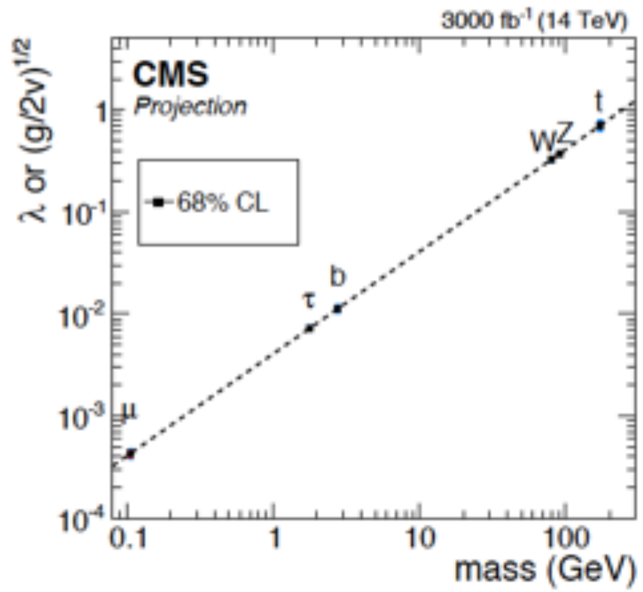
- CLIC (ee) > 2035
- ILC (ee) > 2030
- CepC (ee) > 2028
- SppC (pp) > 2052
- FCC (ee-pp) > 2030 ?
- muon-coll > ??

→ HL_LHC is the best accelerator for HEP after 2024 (and up to at least 2030)

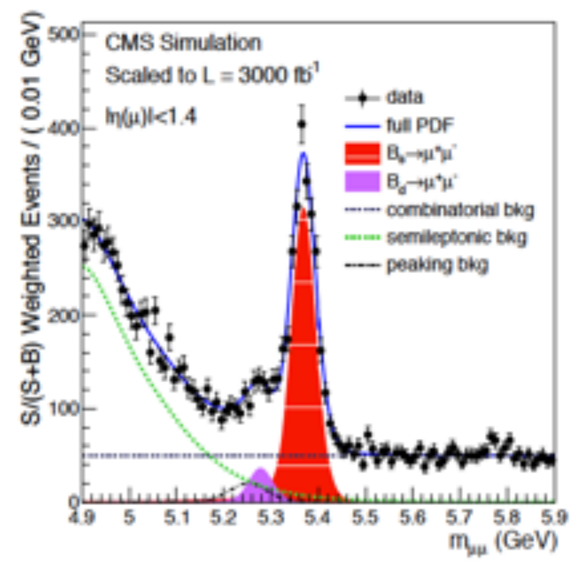
CMS physics@HL_LHC
few examples

Higgs Boson: precision measurements

Luminosity	300 fb⁻¹	3000 fb⁻¹
Coupling parameter	7-parameter fit uncertainties	
k_γ	5-7%	2-5%
k_g	6-8%	3-5%
k_W	4-6%	2-5%
k_Z	4-6%	2-4%
k_u	14-15%	7-10%
k_d	10-13%	4-7%
k_l	6-8%	2-5%
Γ_H	12-15%	5-8%



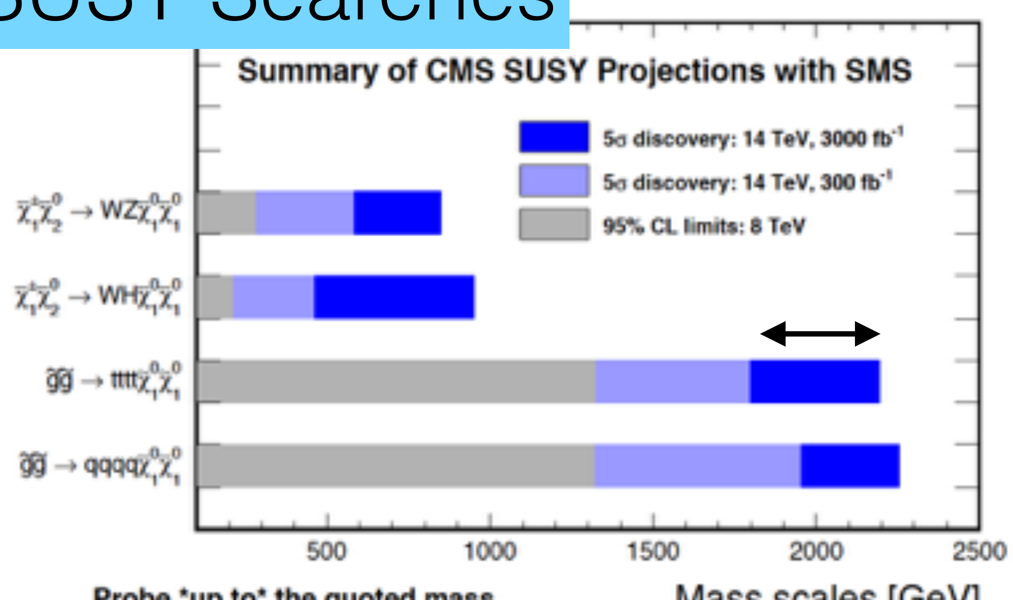
B physics



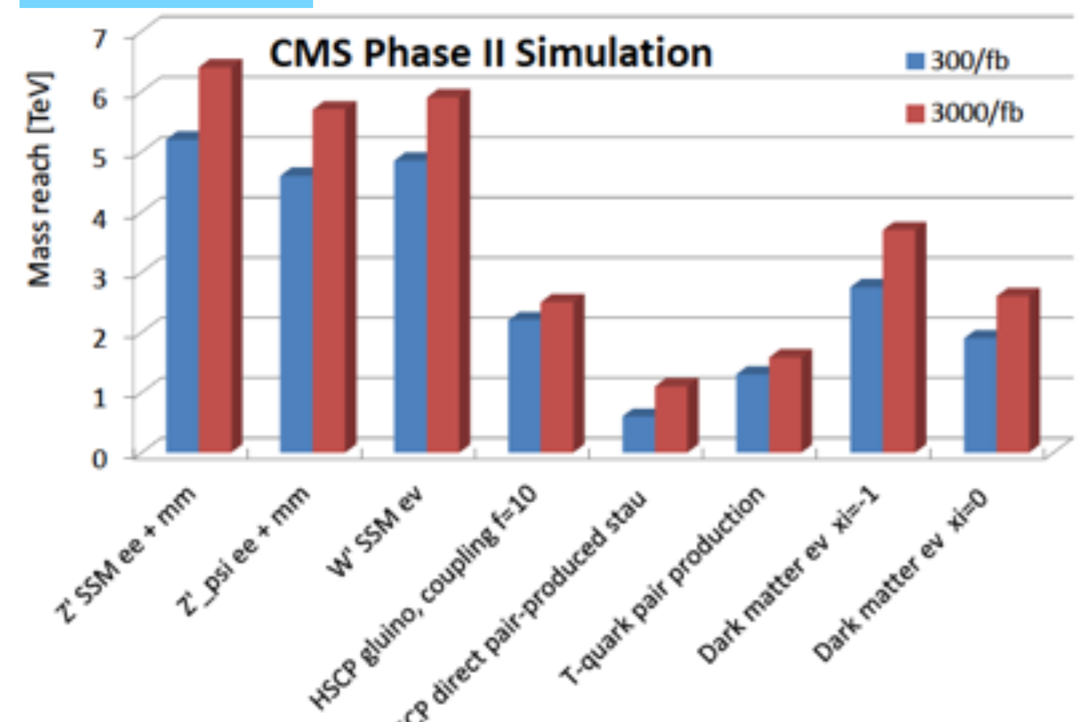
$B_s \to \mu^+\mu^-$ precision

$B_d \to \mu^+\mu^-$ $6.8\,\sigma$

SUSY Searches



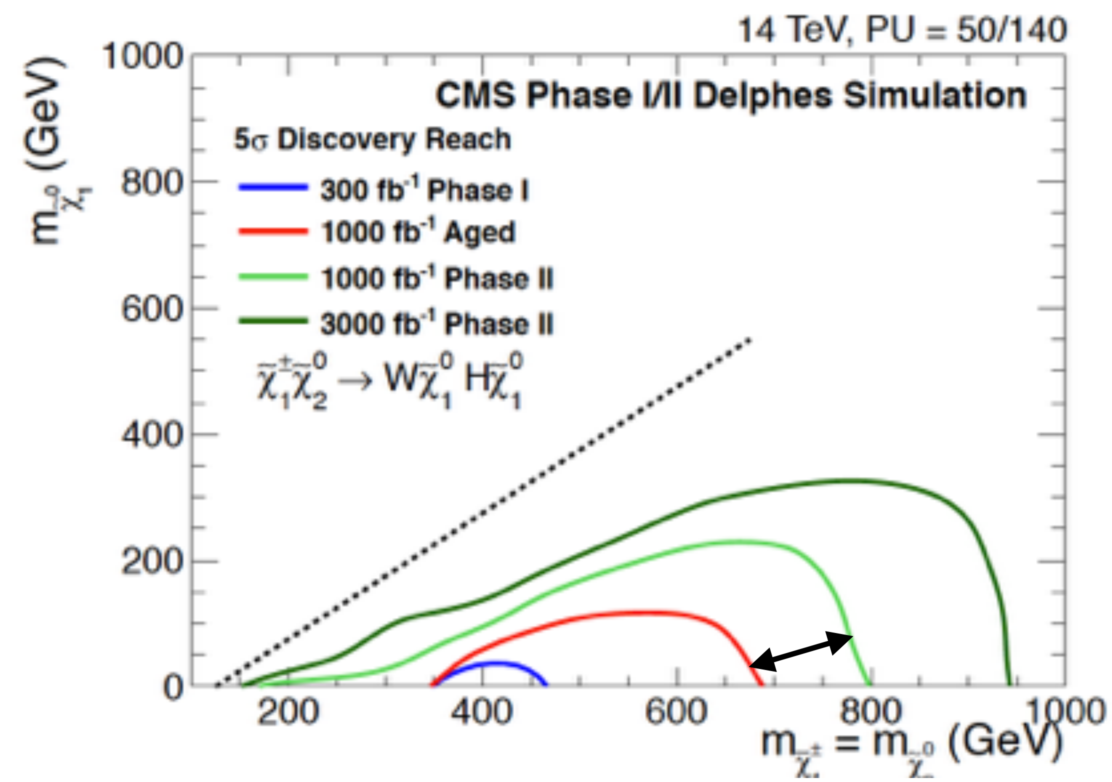
Exotica

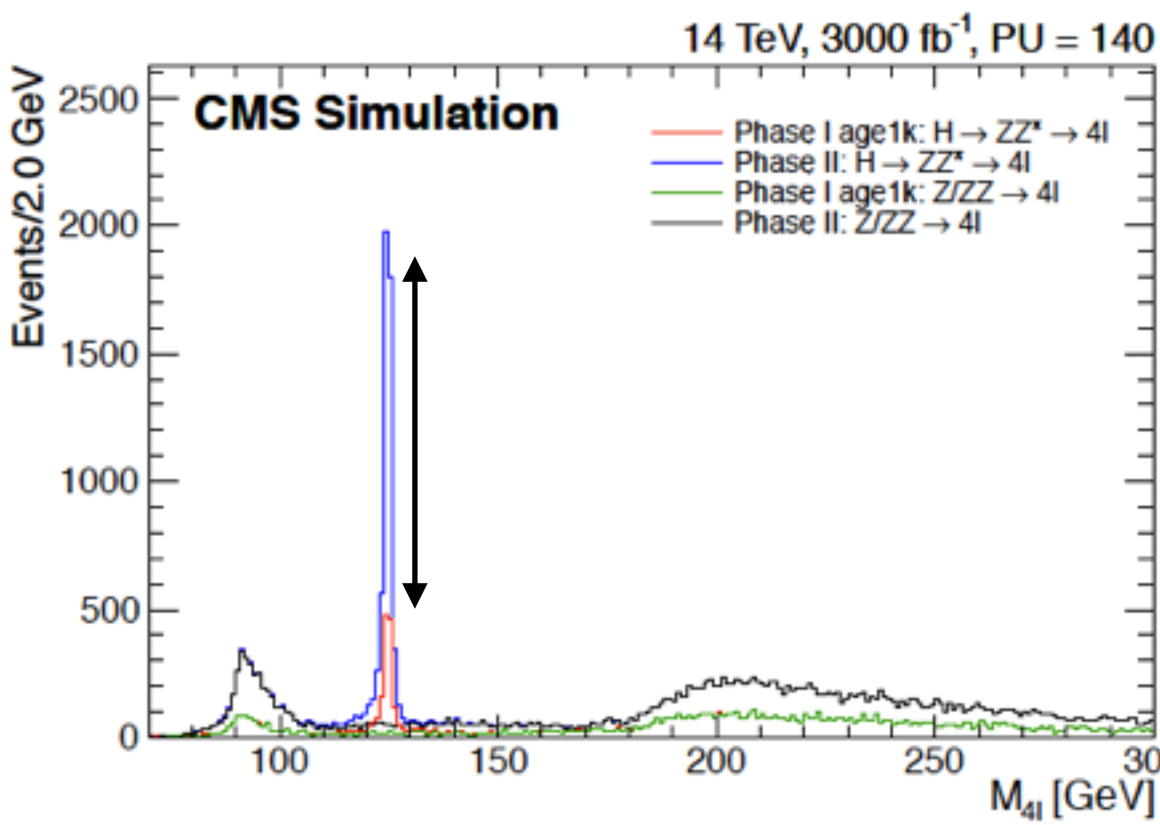


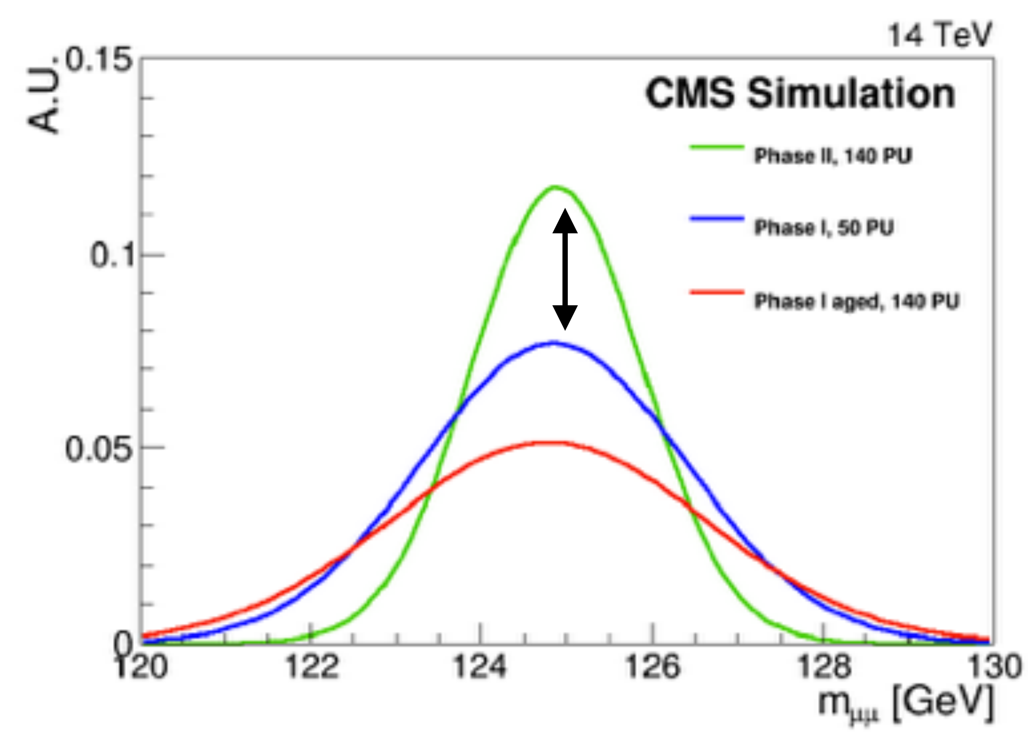
Why to upgrade CMS ?

Major limitation if NO upgrade
(list not complete)

- Reduced performances due to Radiation damage
- Tracking in too high particle density
- Pile-Up
- Data readout bandwidth







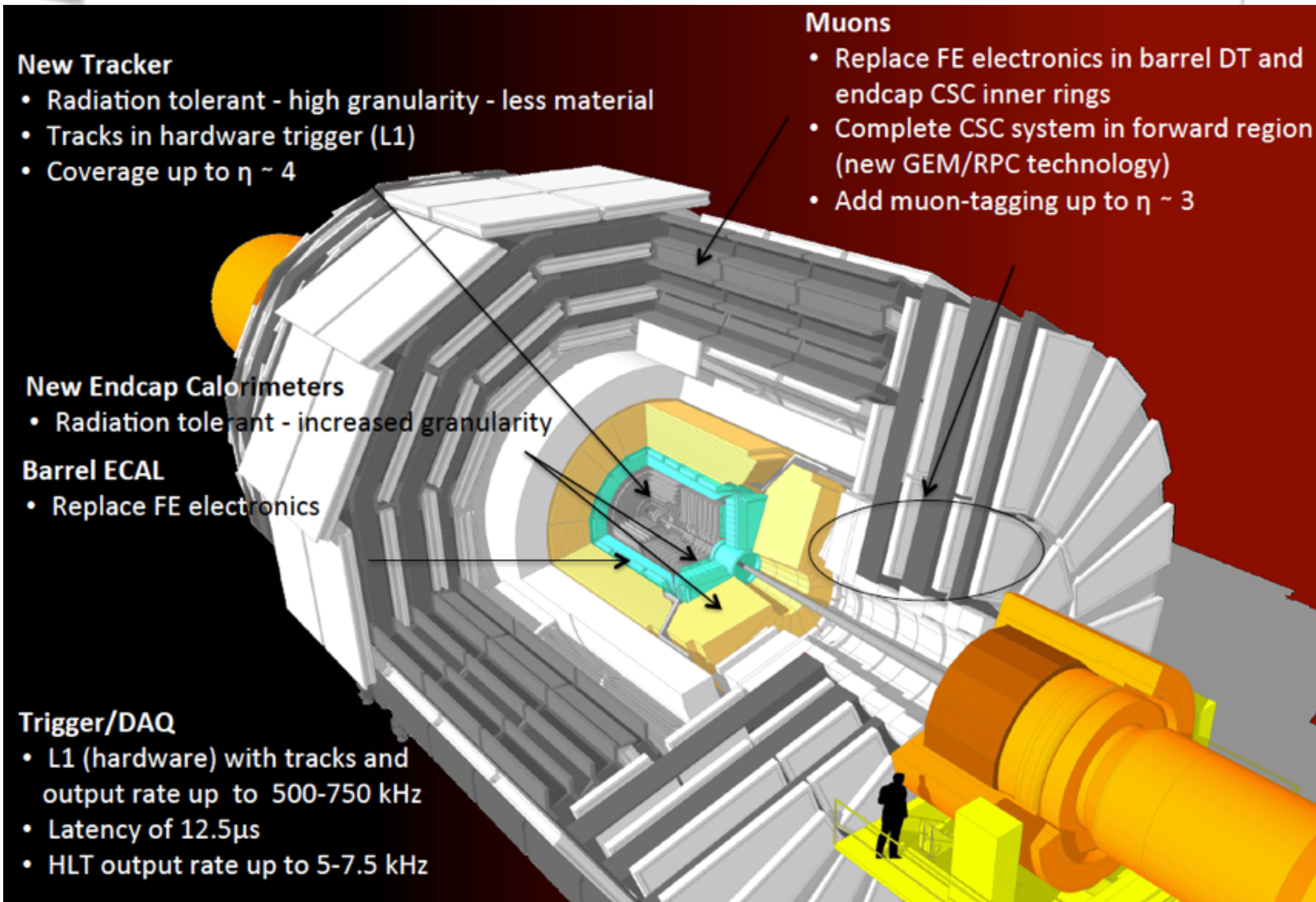
CMS challenge

- **Radiation Tolerance** 10x than LHC (from 300 to 3000 fb^{-1})
- **High Performance at 200 Pile Up** : more granular detector
- **Maintain or improve L1 Trigger performance**
  - Interesting events at 5-7 times larger rate : **750 kHz** (from 100 kHz)
  - **tracking trigger** at L1
  - longer latency : **12,8 us** (from 3,2 us)
- **Extended acceptance** up to $|\eta|$ ~ 4 for tracking / calorimetry / muon
- **Particle PileUp mitigation** : attribution of particles to primary vertex

Few facts:

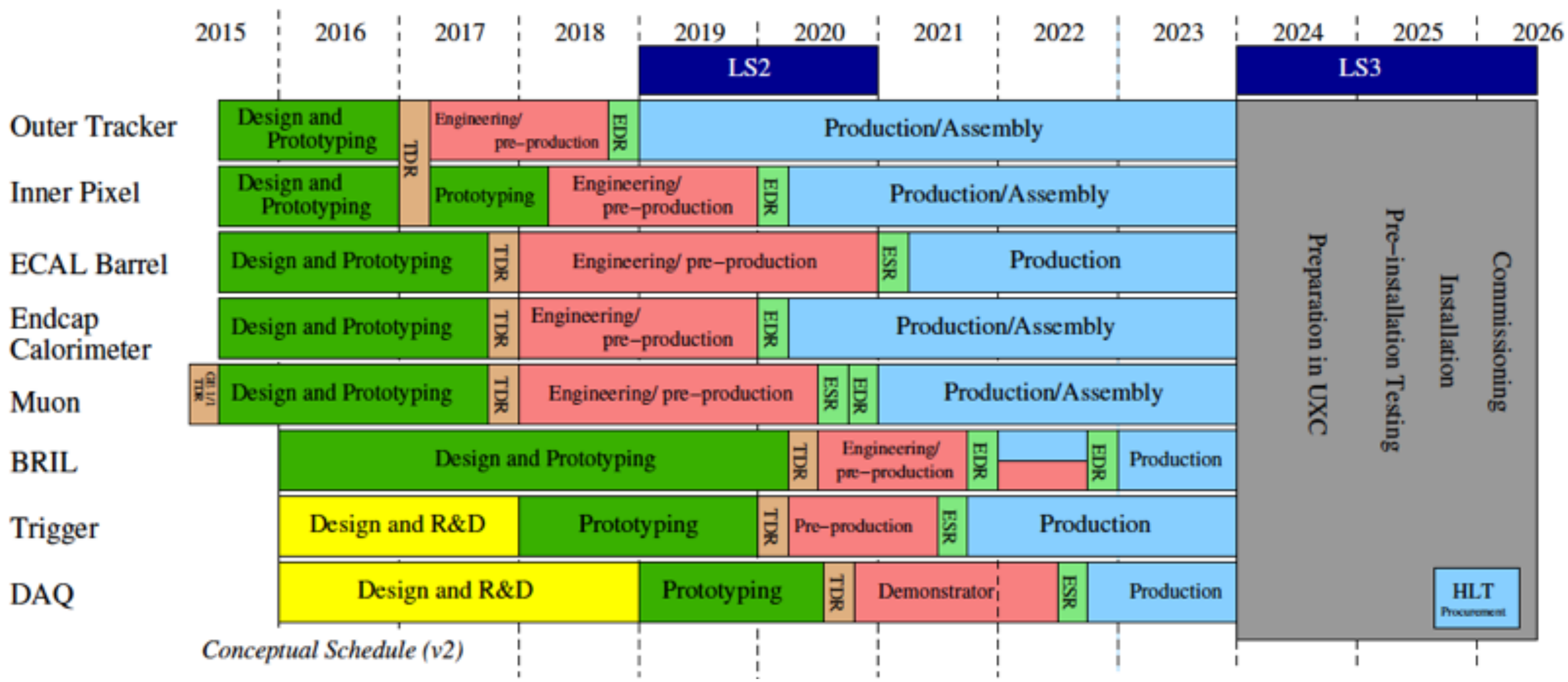
- Tracker detector needs replacement (radiation)
- Calorimeter needs replacement in the Forward region (radiation)
- Electronics needs refurbishment in many detectors

CMS Upgrade…
on a Nutshell



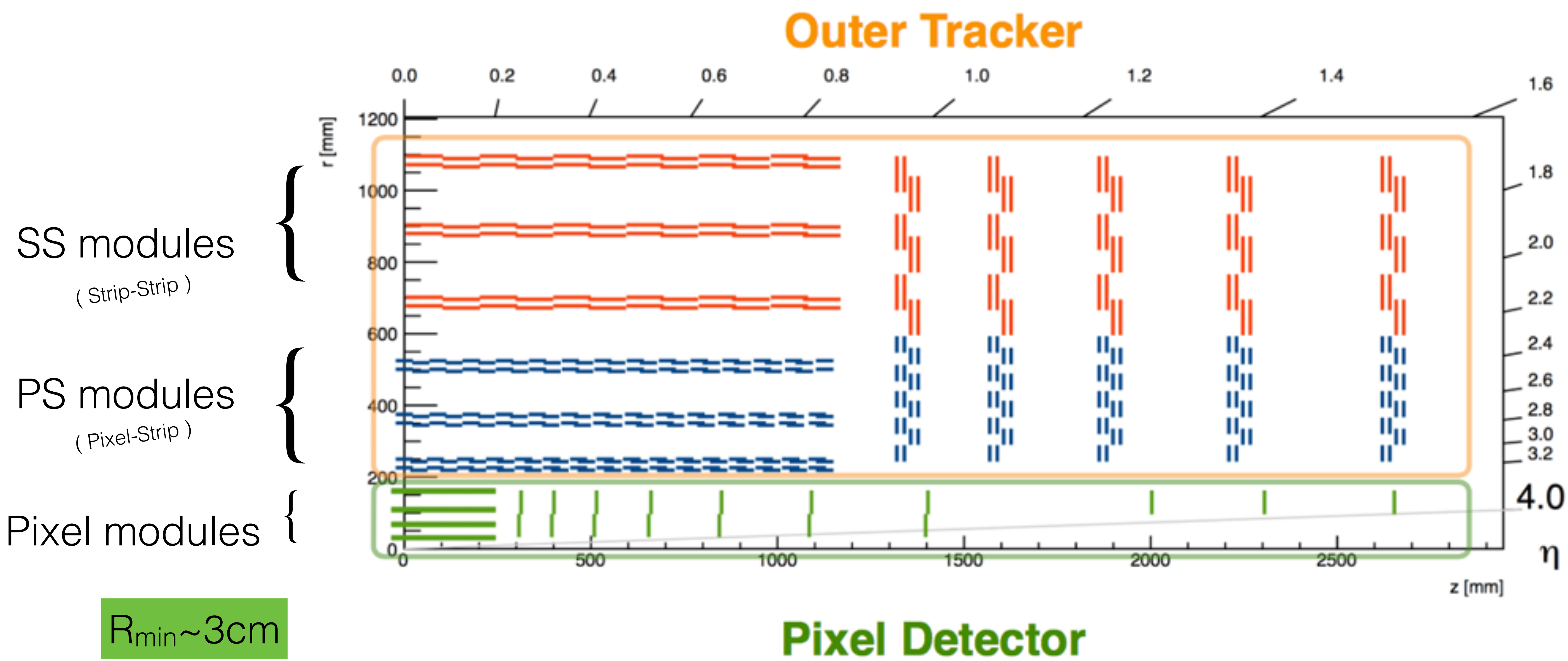
Upgrade start now !

- Despite the new CMS sub-detectors will be inserted on 2024, the time-schedule for construction is tight



Tracker Detector

- **OUTER TRACKER** : momentum resolution, tracking trigger (up to $|\eta|$ =2,4)
  - 6 'double-sensor' in barrel (10 single now); 5 double sensors disks (9 now)
- **PIXEL DETECTOR** : tracking seeding, vertex reconstruction, tracking extension
  - 4 barrel layers (as Phase-1); 10 disks (3 in Phase-1)



R_{min}~3cm

Pixel Detector: principles

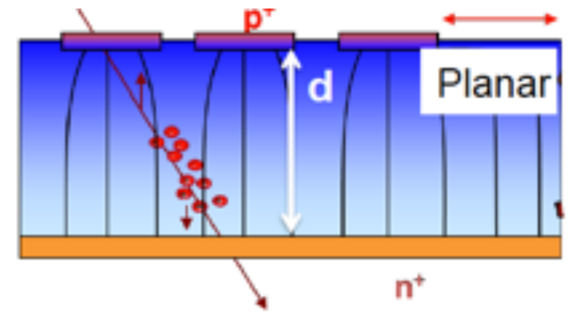
Major worries:

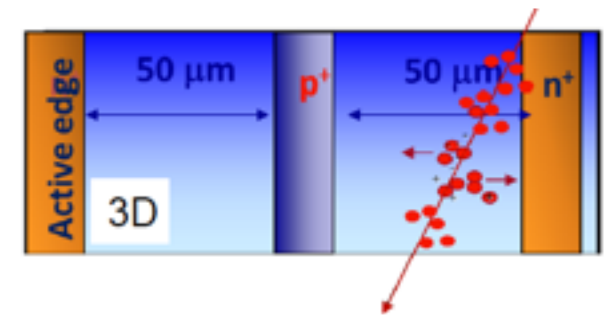
radiation damage (up to 2 10^{16} n/cm^2); 1-Grad

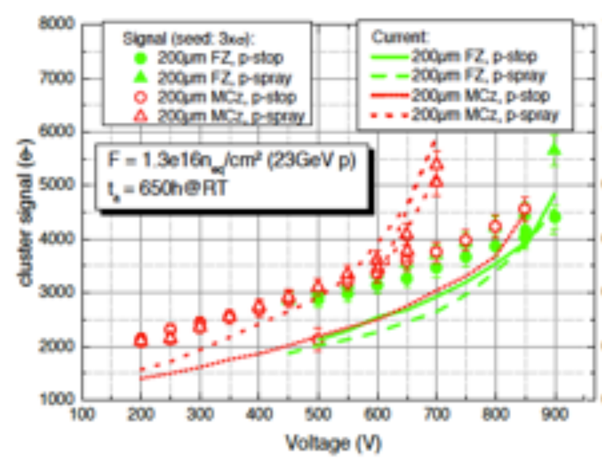
particle flux up to 3 GHz/cm^2 pix-hit

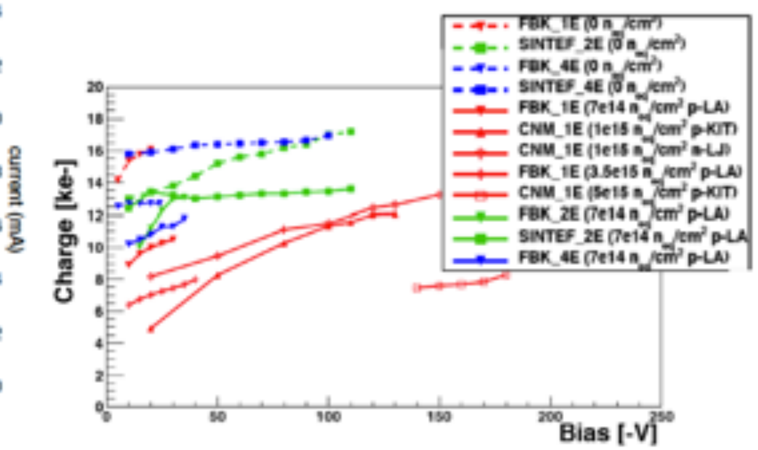
Sensors :

- dimensions (x1/4): 25x100 um^2 to 50x100 um2
- on-going R&D on : thin planar / 3D-silicon
  - reduce drift distance to minimize trapping
- small signals



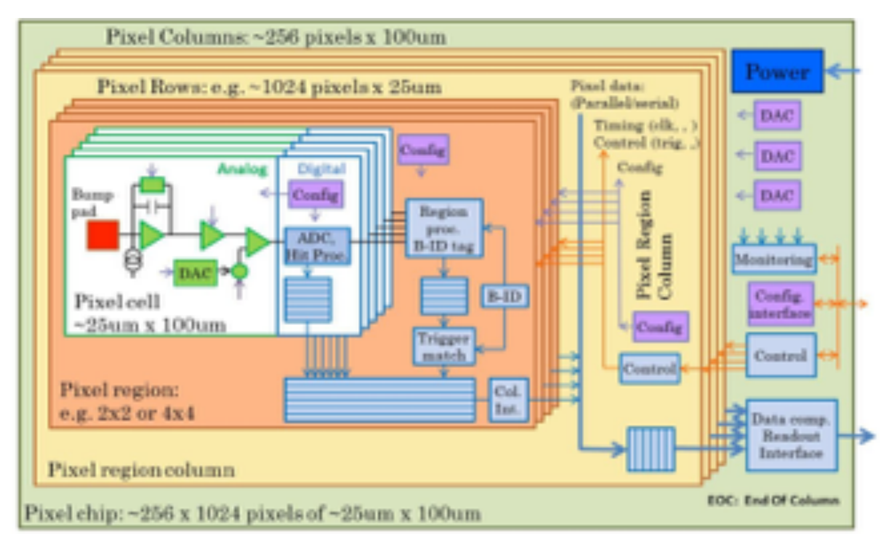






Read Out Chip (ROC) :

- low noise, low threshold : <1000 e$^-$
- compact : 50x50 um^2
- low power consumption : ~0,3-0,5 W/cm^2
- digital local storing : x7 (rate) x4 (latency)
- readout : up to 5 Gbps data out
- Large ASIC ~ 2x2 cm^2



ROC R&D in RD53 using CMOS 65nm (HEP novelty)

(faster, smaller, lower noise, more rad-hard)

Pixel Detector

Readout Elements

- ROC contains 4 E-Links, up to 1.2 Gbps.
- 8 E-Link connected via 1-2m twisted to LP-GBT

Modules Readout

- L1, L2 (25x100um^2)
  - 4 ROCs ; 16 E-LINks, 2 LP-GBT
- L3, L4 (50x200um^2) ;
  - 8 ROCs, 8 E-Links ; 1 LP-GBT

IMPORTANT that ROC can reduce power when 1/4 channels are connected

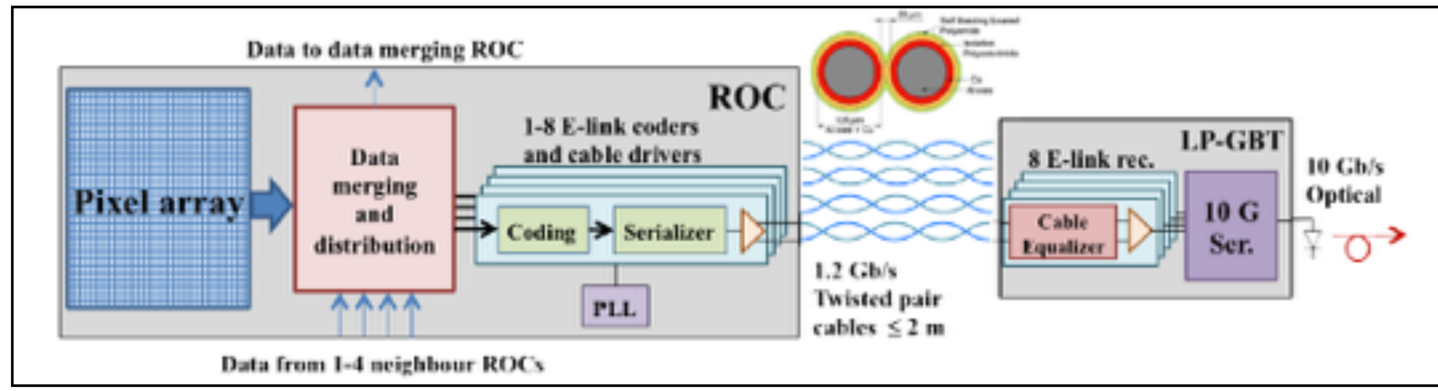
Module Power

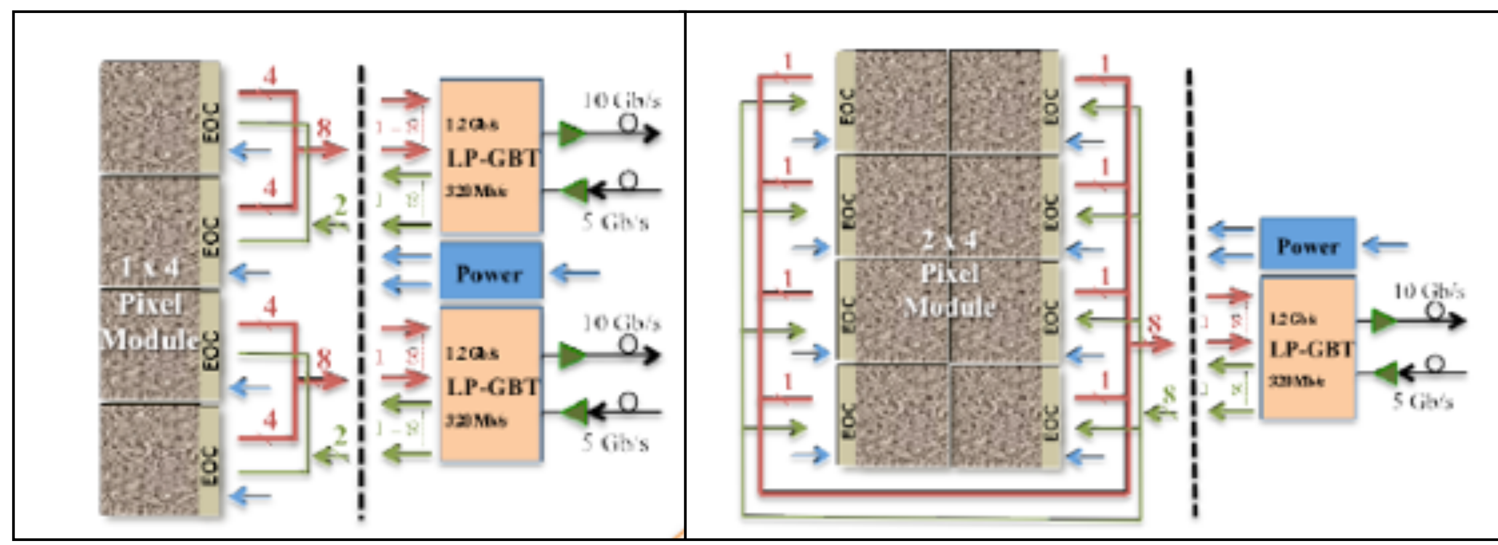
- DC-DC: problem of rad-hardness;
- R&D on Serial Powering

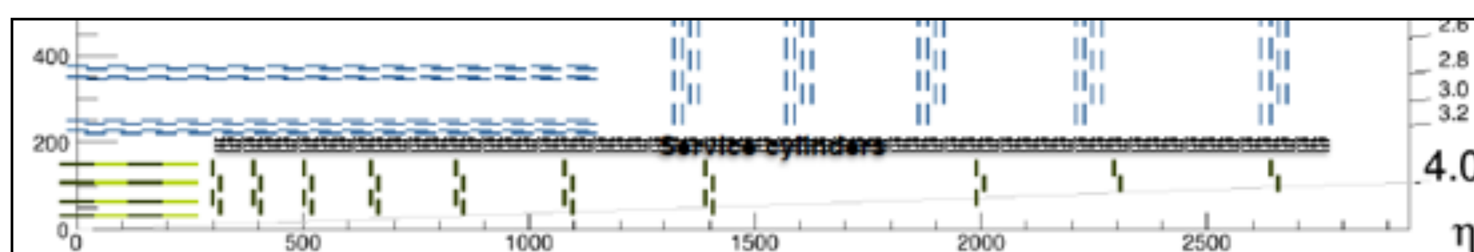
Service aspects

rapidity estention imply material inside acceptance: optimisation studies needed

Development of LP-GBT at high speed crucial (9-10 Gbps ?)



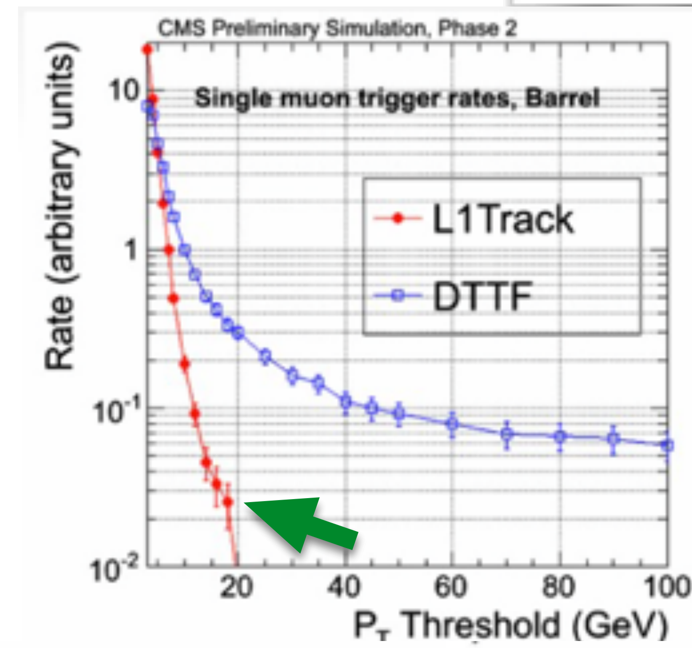


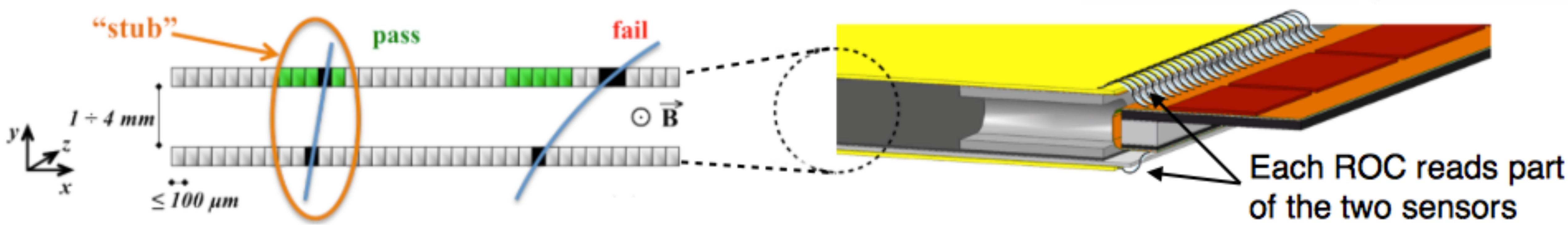


N.B. The service cylinders are completely inside the tracking volume

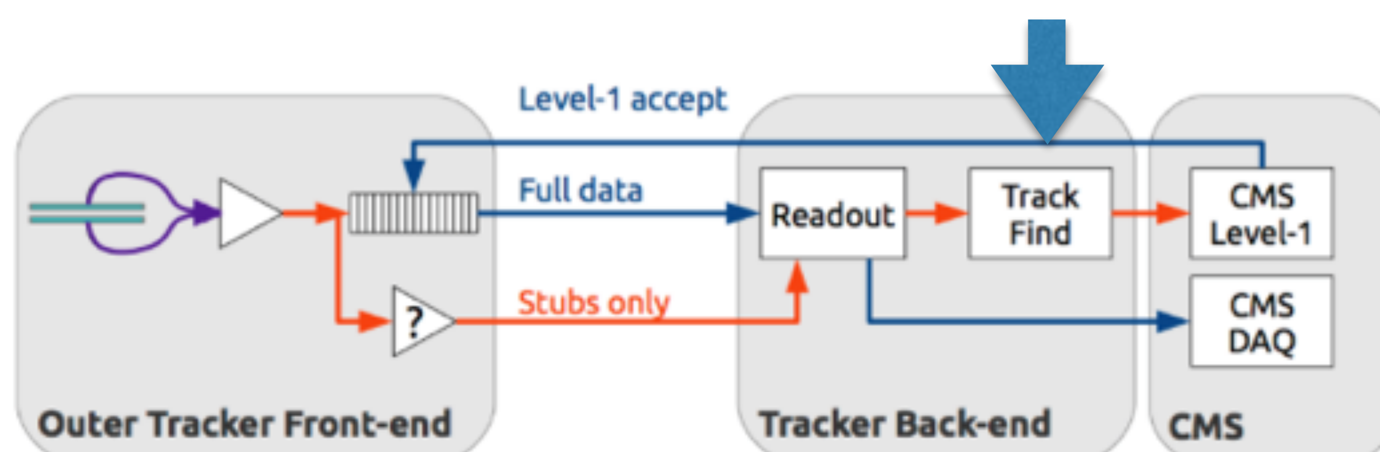
Outer Tracker concept

- Rate of **single muon** strongly suppressed by using the momentum measurements of the Tracker at L1 (muon detectors are inside the coil therefore suffer from large scattering) - **THIS IS a MUST**
- Tracker@L1 help ALSO: el-ID, isolation, vertex-ID of lepton and jets
- Design based on the L1-tracking trigger concept : the **Pt-Layers**
  - made of 2 silicon sensors, distant of 1 - 4 mm
  - **tracks above 2 GeV** are more pointing





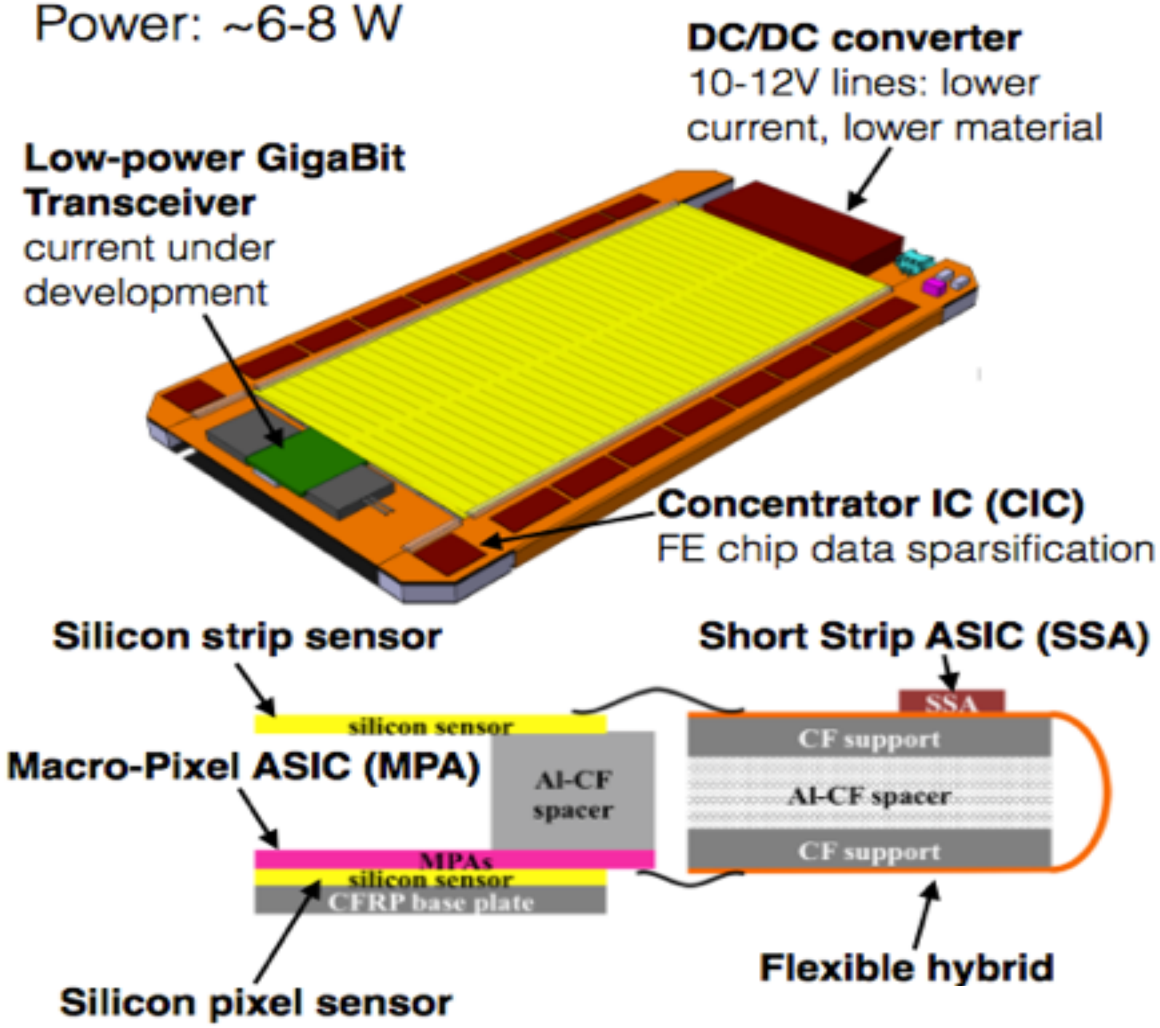
OUTER- TRACKER DATA:
- A stub is a track segment constituted by 1 TK-layer and provides position and Pt measurements (~1% relative) - 40 MHz to L1
- full data readout: hit position per module at L1-rate - up to 1 MHz



Outer Tracker modules

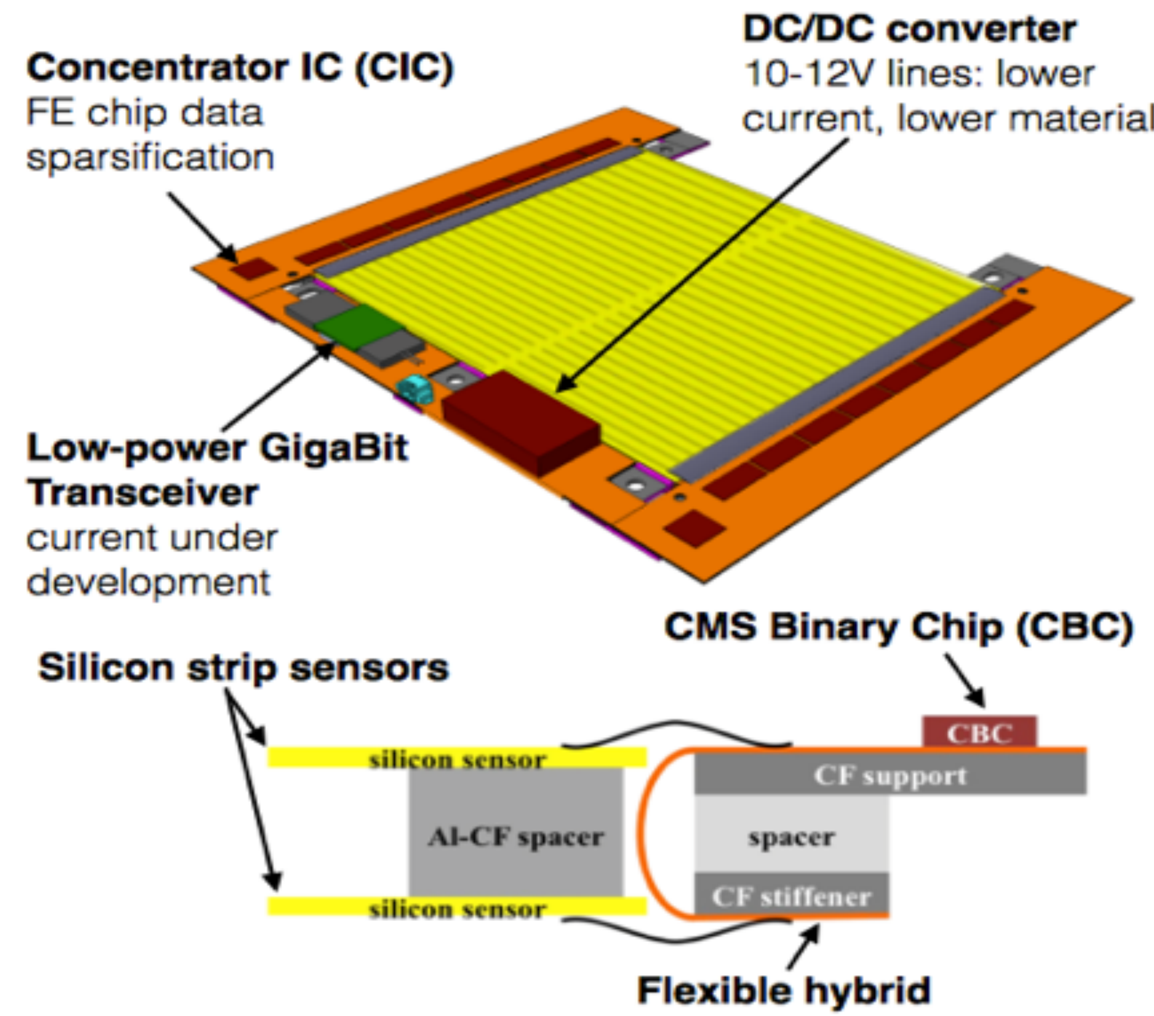
PS modules: Macro Pixel + Strip

Macro Pixel: 1.5 mm × 100 μm DC coupled
Strip: 2.4 cm × 100 μm AC coupled
Module area: ~5 × 10 cm²
Power: ~6-8 W



2S modules: Strip + Strip

Strip: 5 cm × 90 μm AC coupled (both sides)
Module area: ~10 × 10 cm²
Power: ~4-5 W



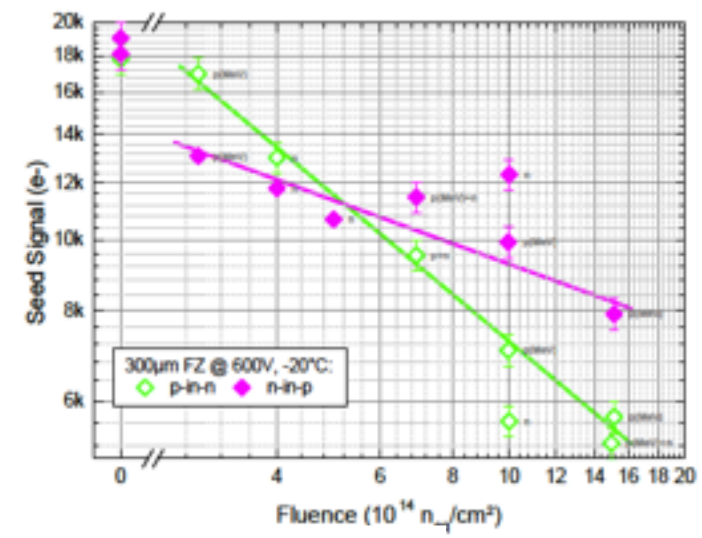
First Small MPA exists and under test

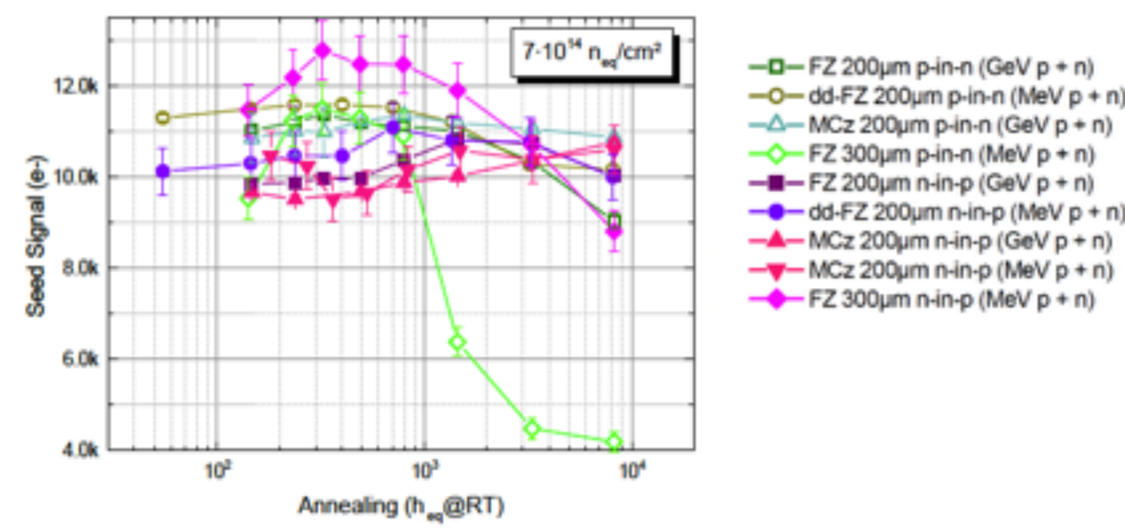
First SS prototypes exist

Outer Tracker sensors

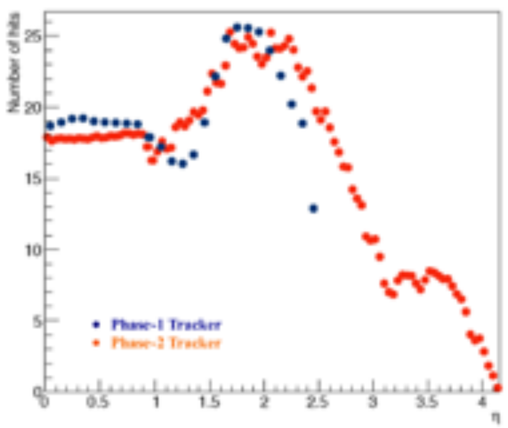
Basic R&D essentially finished: the main properties of the sensors are defined

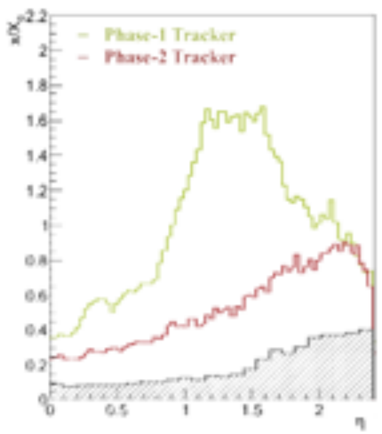
- **Polarity**
  - n-in-p is the selected option, as it offers robust performance (i.e. graceful degradation) after heavy irradiation
- **Material**
  - MCz is the preferred option (but FZ is OK)
    - ★ Allows for long annealing times with no adverse effects
    - ★ Could be (eventually) operated at lower V_{bias}, mitigating the requirements on the cooling
- **Thickness**
  - 200 µm active and physical thickness is the preferred option
    - ★ Sufficient charge, good annealing behaviour, lower I_{dark} and V_{bias}
  - 200 µm active 320 µm physical is a good backup
    - ★ Adds 60 kg of inactive material uniformly distributed in the tracking volume
    - ★ Active thickness can also be fine-tuned…



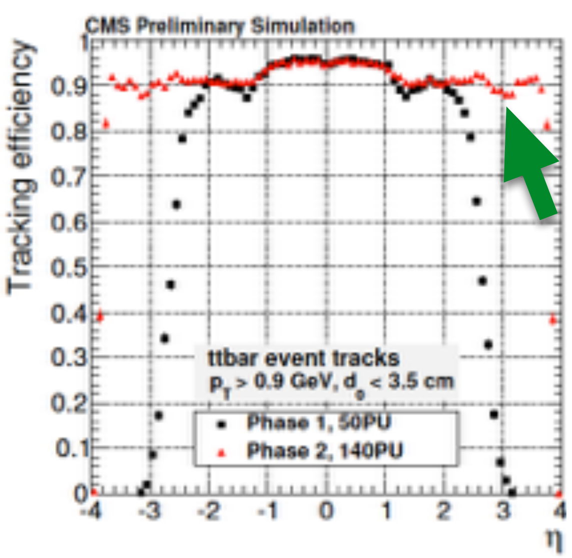


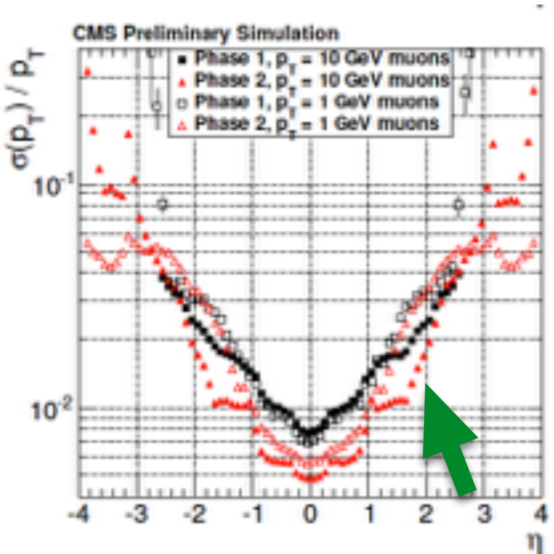
Tracking performance





Ph-2@140PU =(better) Ph1@50 PU

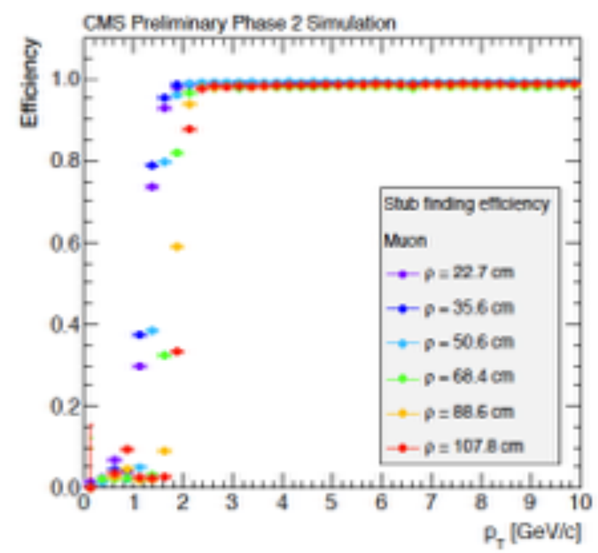


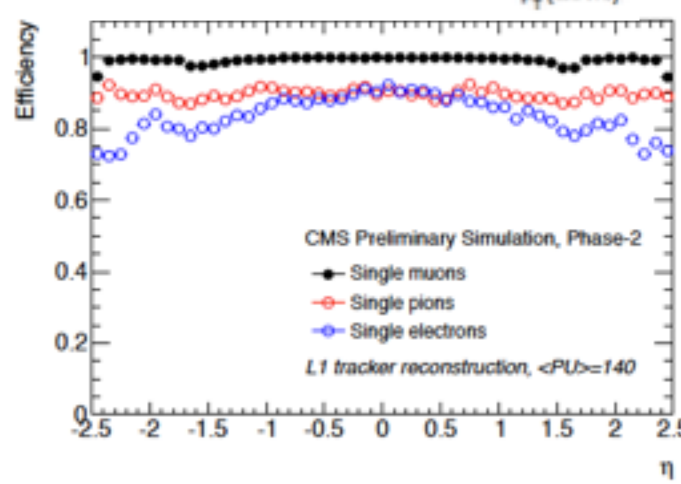


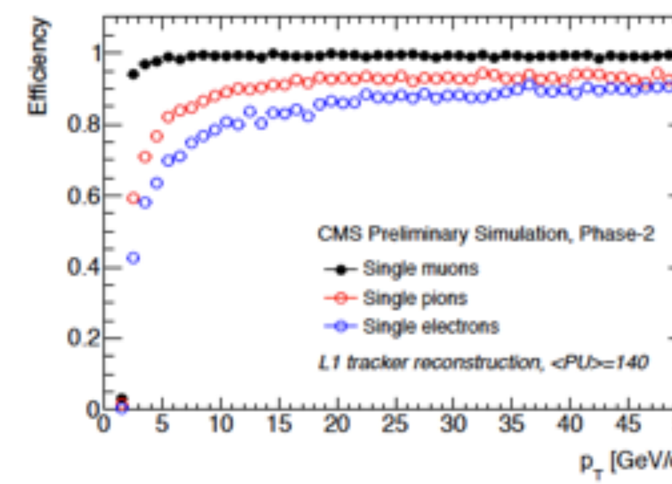
- Less material than Ph-1
- same/better performance
- extension up to eta=3.8

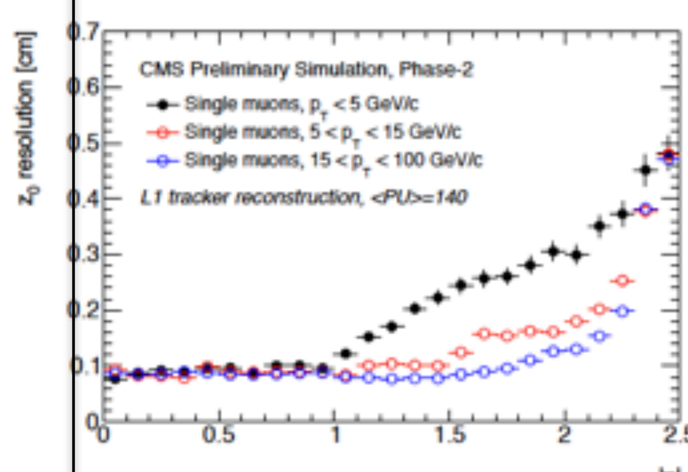
L1Tk-stub performance

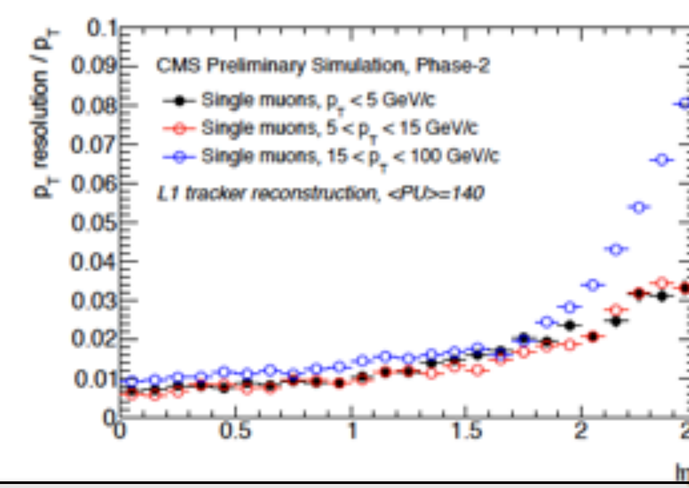
- eff=1 for muon p_t> 2 GeV/c
- sligthly better for low radii









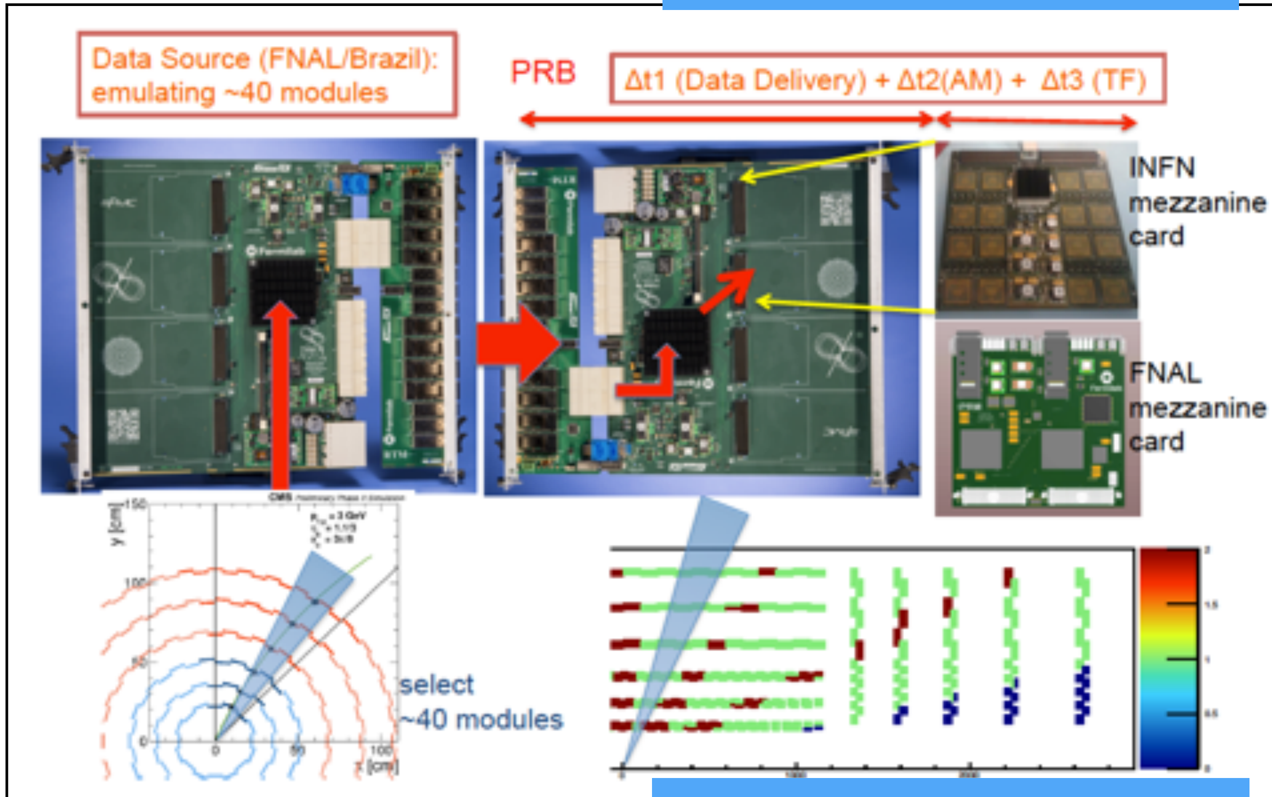


Tracking Trigger: 3 methods

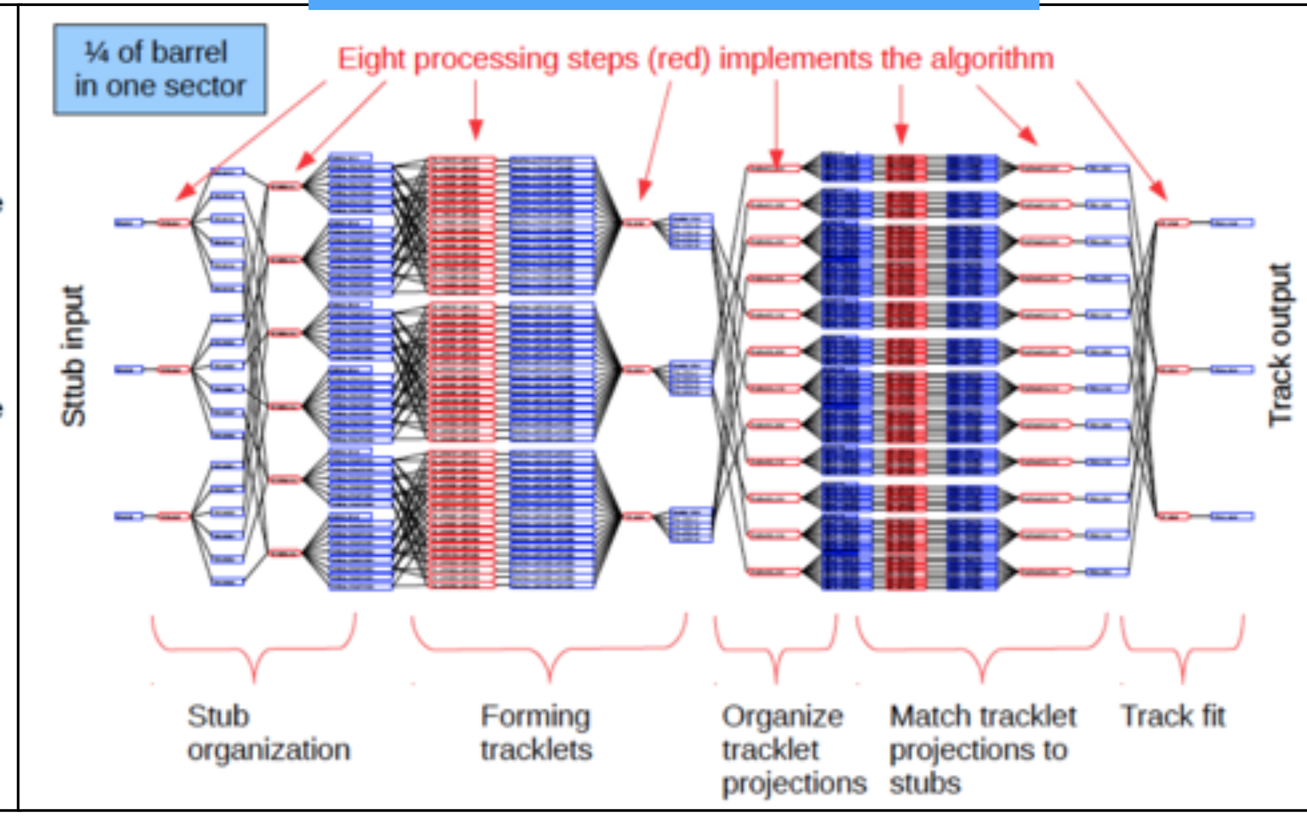
- **Associative Memory (AM)**
  - large bank of patterns stored in a dedicated Associative Memory chip (similar to FTK solution)
  - processing time linear with number of hits
  - Tracker = 48 angular regions; about 200 stubs per event / region are expected
  - stub coordinates loaded in Memory and matched patterns are considered as track candidates: **100 Million patterns** recorded in AM chip (2 Million each)
  - refit track candidates with full-resolution coordinates
- **Time-Multiplexed architecture**
  - uses Hough Transform
  - all data from one event goes to one processing node; the node redirect one event to a single destination for complex process
  - 5 secotrs in Phi and time multiplexing of 24
  - uTCA processing board using Virtex-7 FPGA
- **Tracklet-seeded road search**
  - conventional road-based track search using FPGA
  - pairs of stubs in neighbouring layers (tracklets) projected to other layers; 168 triggering towers

Tracking Trigger

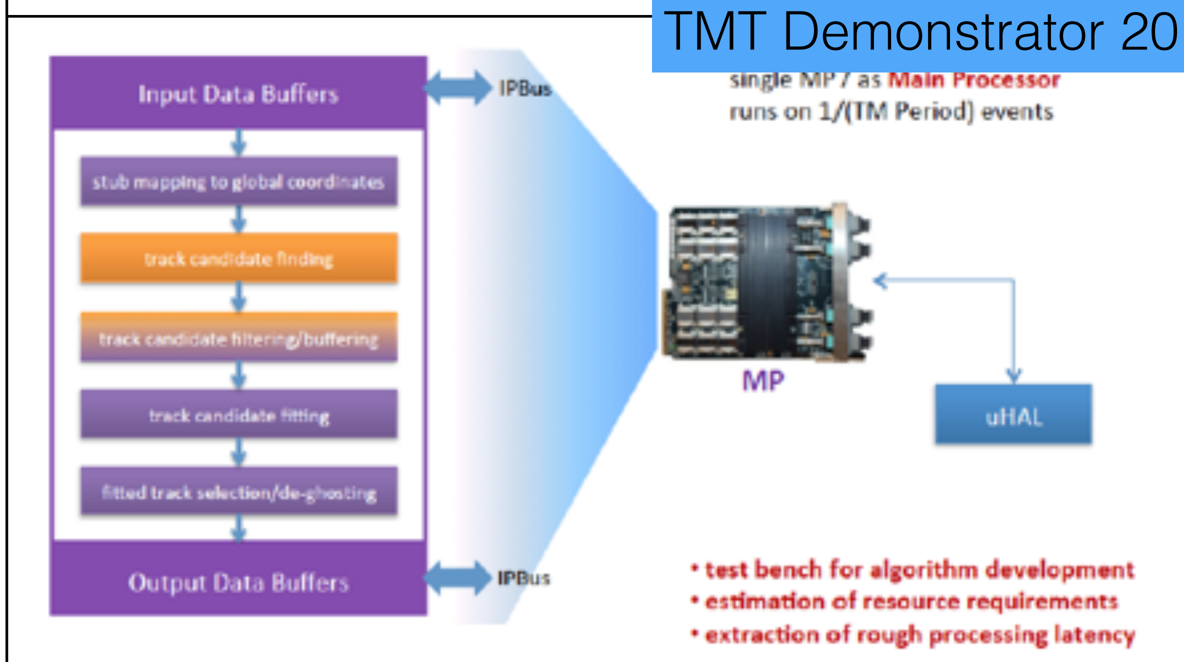
AM Demonstrator 2015



Tracklet FPGA impementation



TMT Demonstrator 2015

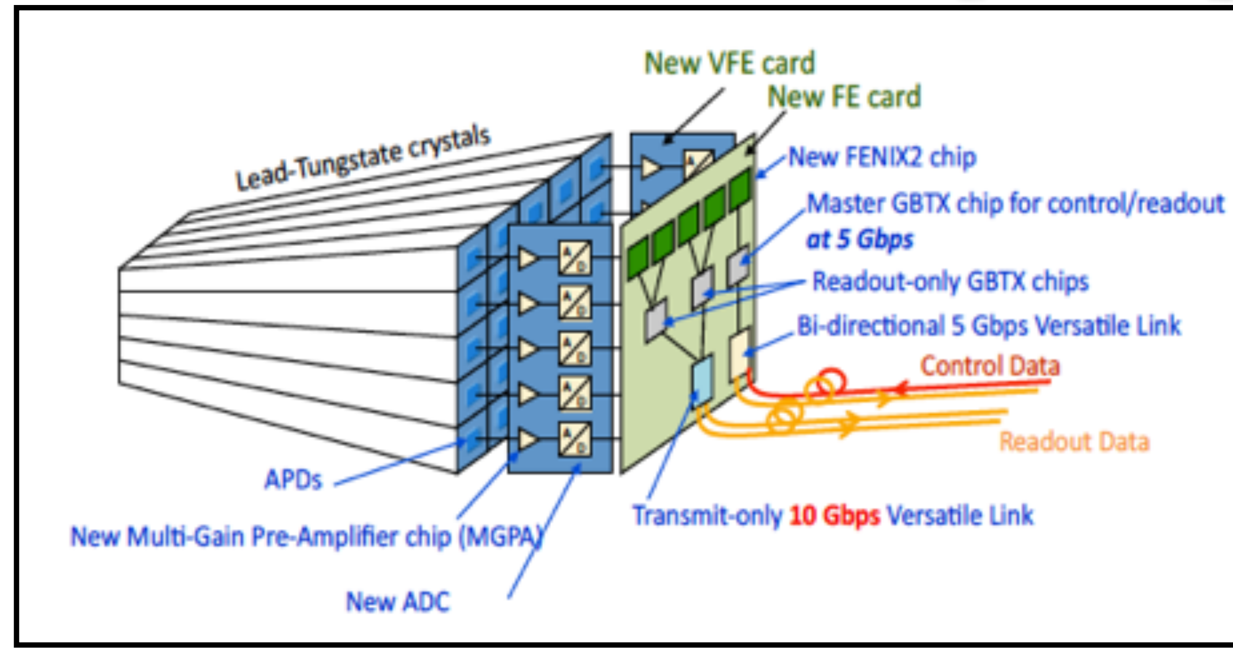


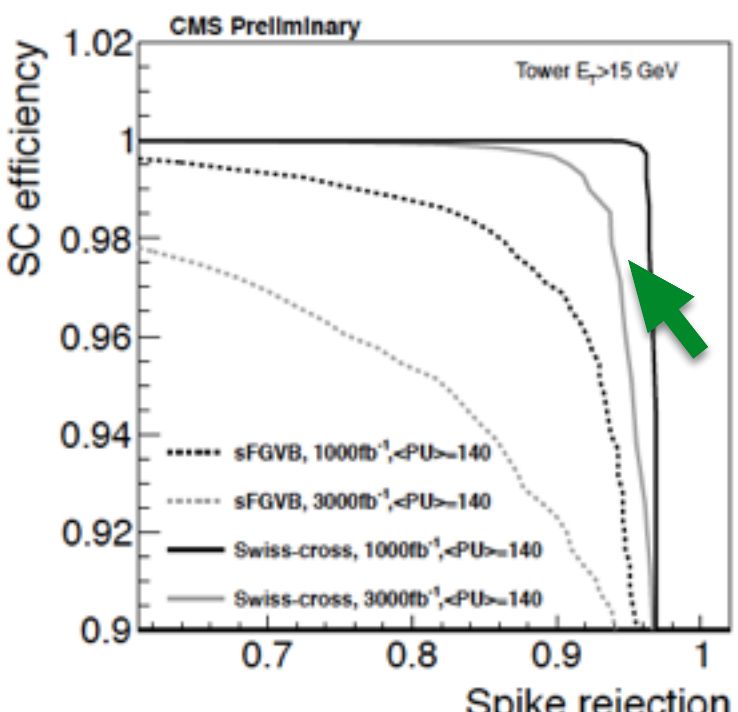
A final solution will be taken after complex demonstrators will be realised on 2015 - 2016

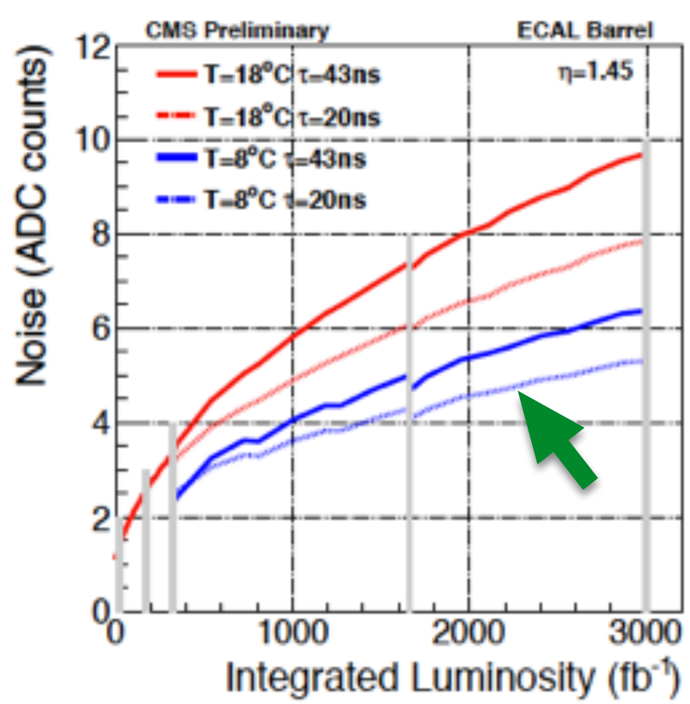
ECAL

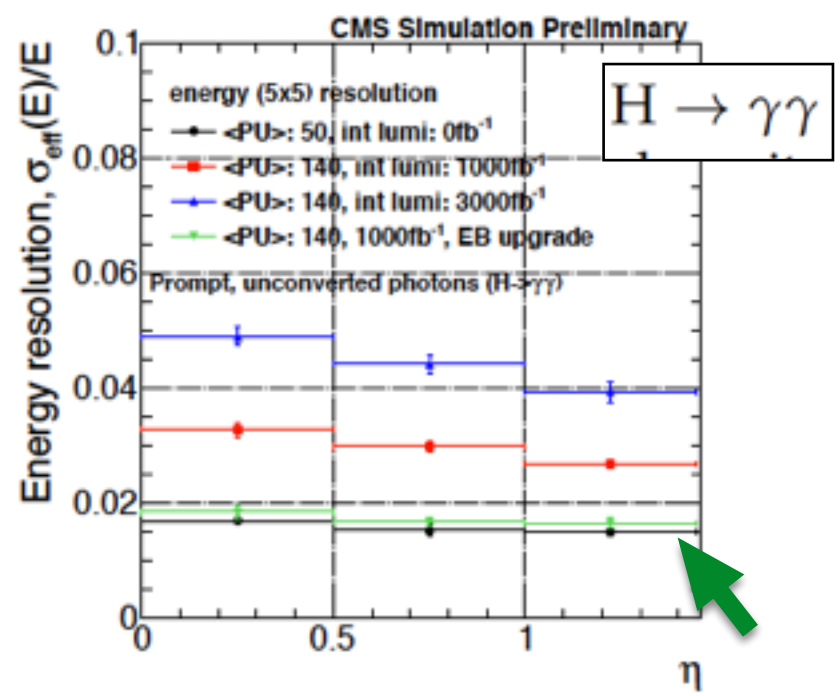
Replacement of electronics obligatory to meet trigger requirements. This gives opportunity to revise the crystal supermodules

- **Readout of single crystals** - allowed by GBT bandwitdth (now 5x5 crystal only)
- **VFE replacement**: shorter shaping time (20ns instead of 40ns) - allow to discriminates spikes
- **Lower temperature**: 8°C instead of 18°C - APD noise reduction





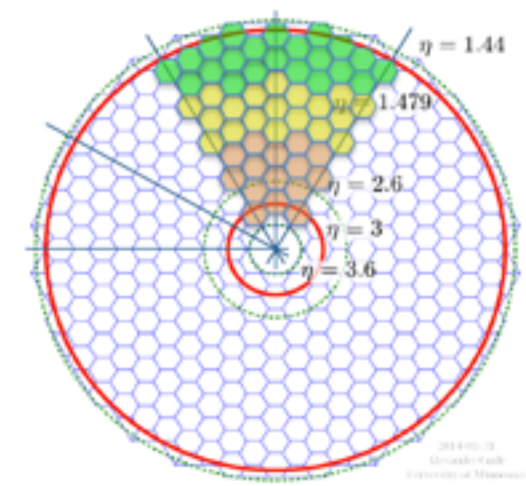


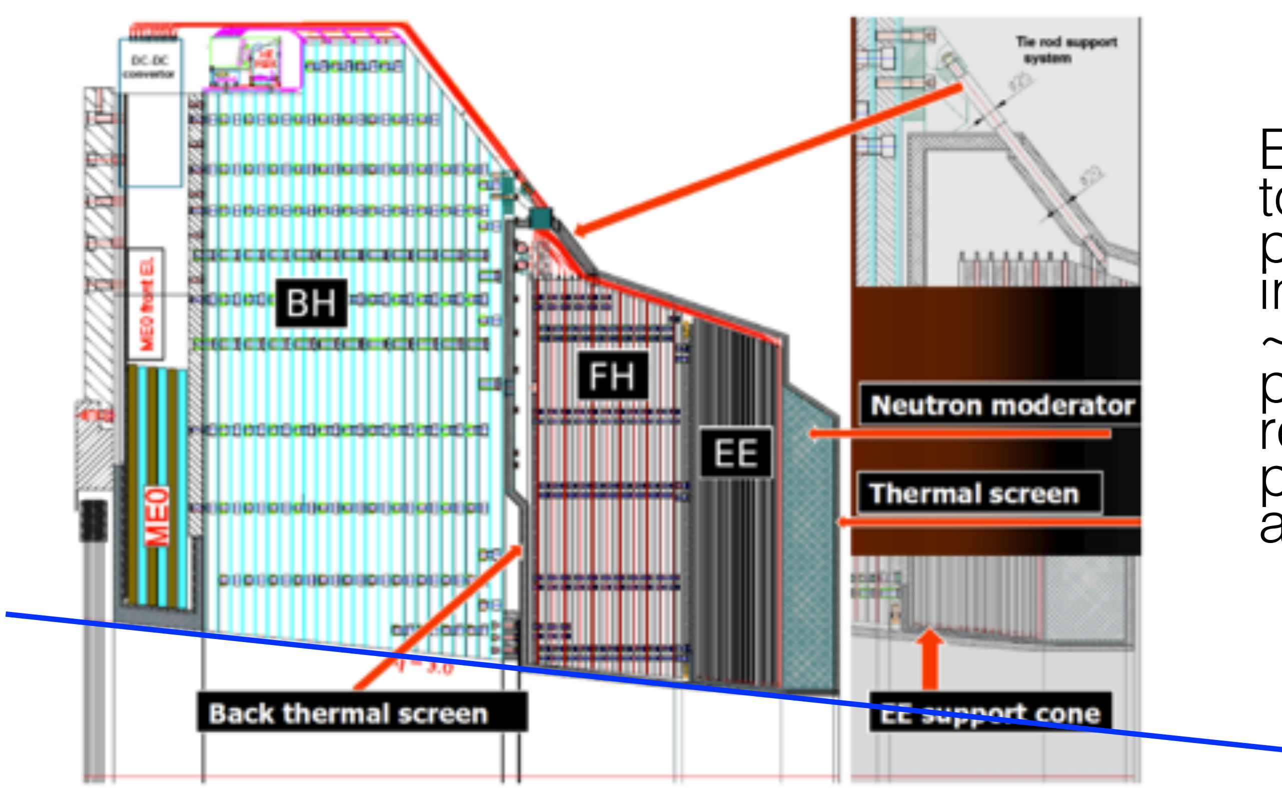


Forward calorimeters

Radiation damage and increased pile-up require detector REPLACEMENT. Foreseen a highly granular design of a sampling calorimeter (**HGC**) covering rapidity from 1,5 to 3. Already studied from CALICE Coll., provide single particle resolution and particle flow.

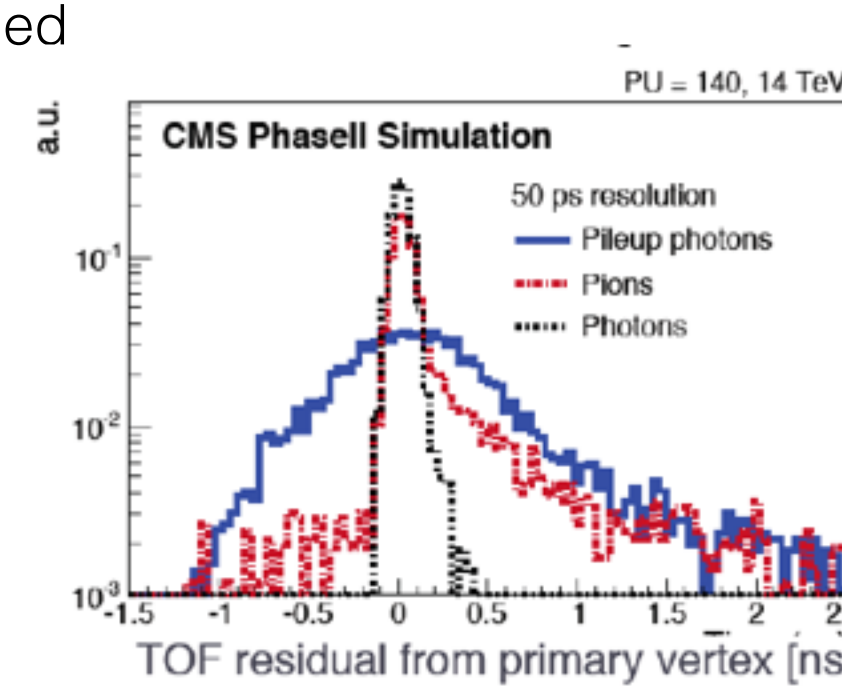
- **EE**: Si/W; 26 X_0 , 1.5 λ ; 28 samplings
- **FH** : Si/Brass; 3.5 λ ; 12 samplings
- **BH** : Plast/Brass; 5 λ; 12 sampling





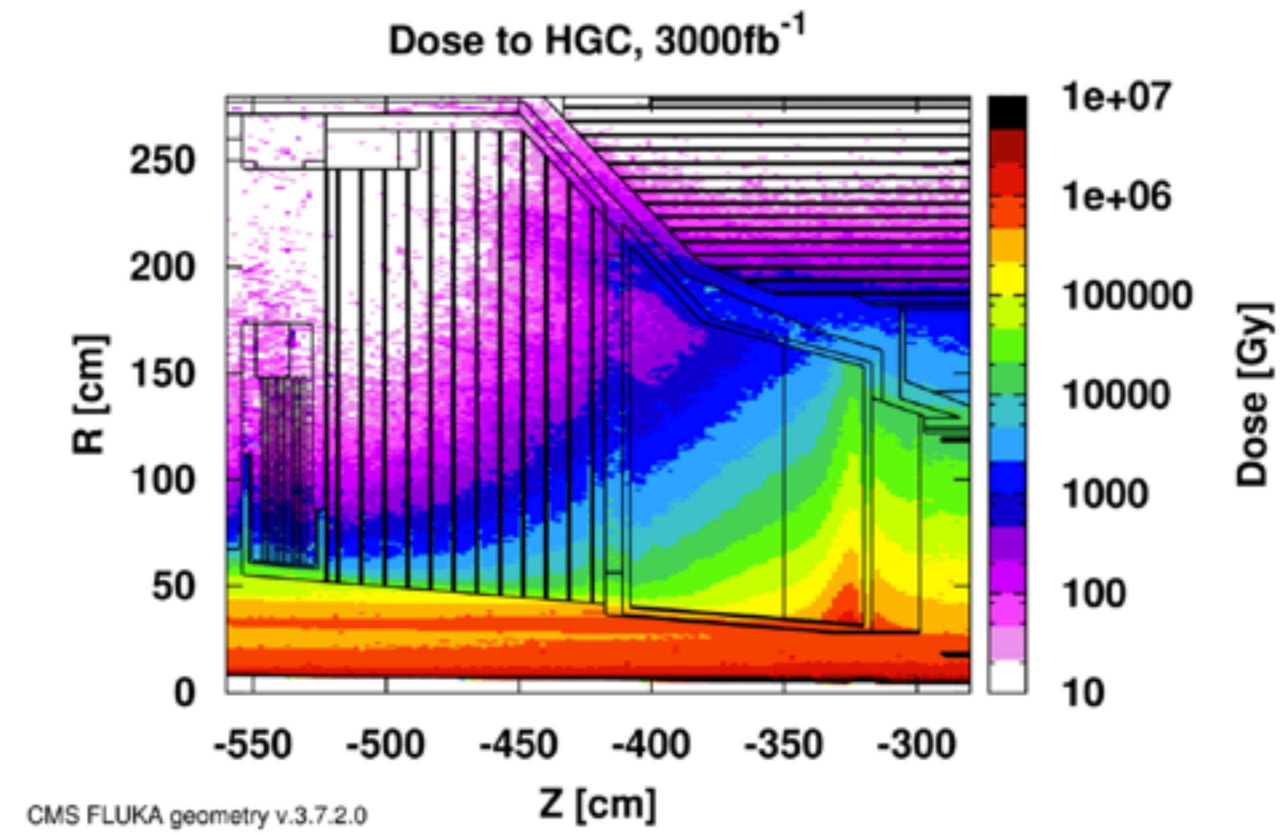
$|\eta|=3$

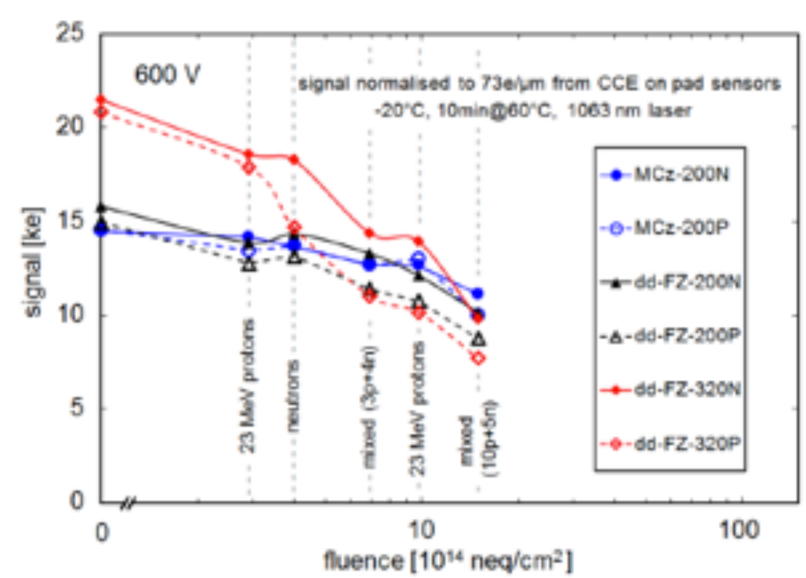
Electronics studied to provide very precise timing information of ~**50-100 ps** to provide pile-up reduction and primary vertex association

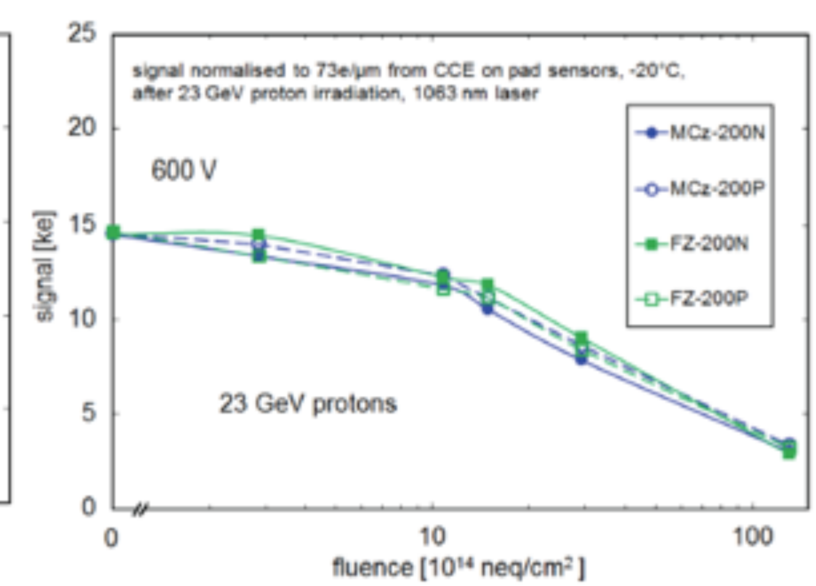


HGC sensor & front-end

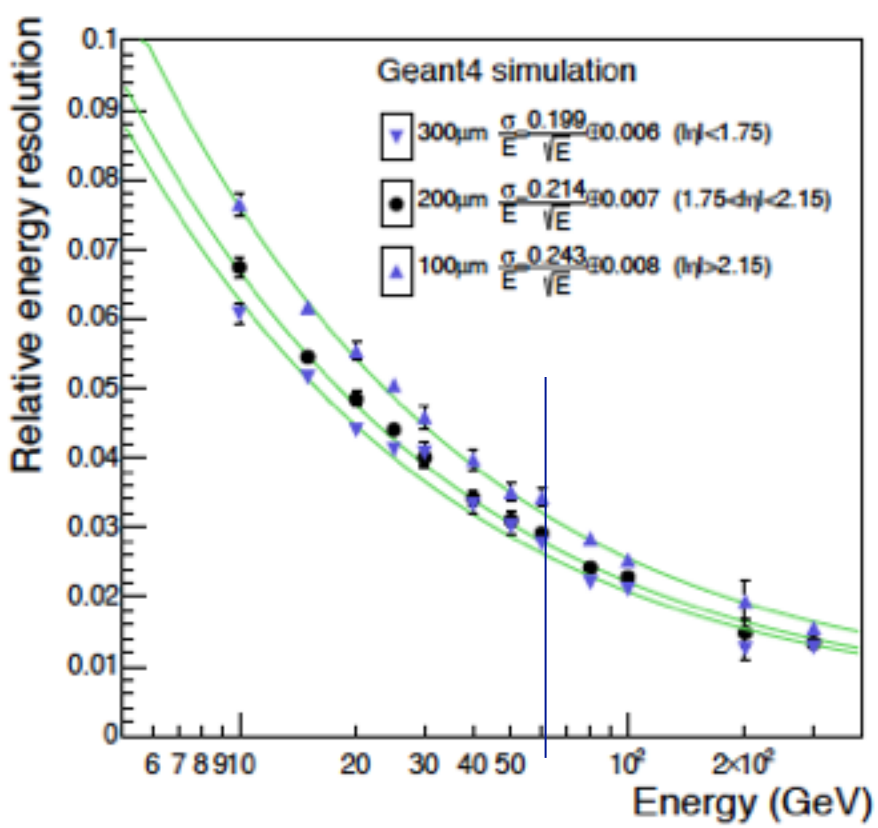
- Radiation fluency up to 1.6 10^{16} n/cm^{2} (higher rapidity) but dominated by neutron (TK is proton)
- Si-Sensors:
    - Baseline design based on 100 um thick detectors for rap < 3
    - Options for an extended HGC (rap < 4) considering 50um planar or 3D sensors
- Front End ASIC
    - assumption is 130nm CMOS
    - to be verified rad-hard up to 400 MRad and above

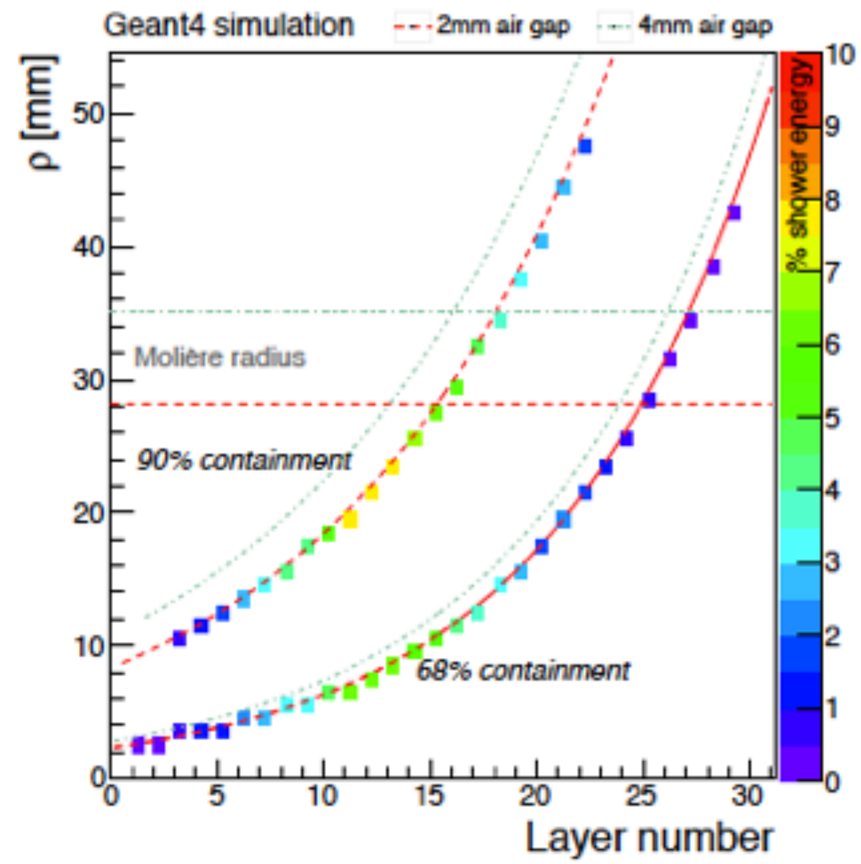


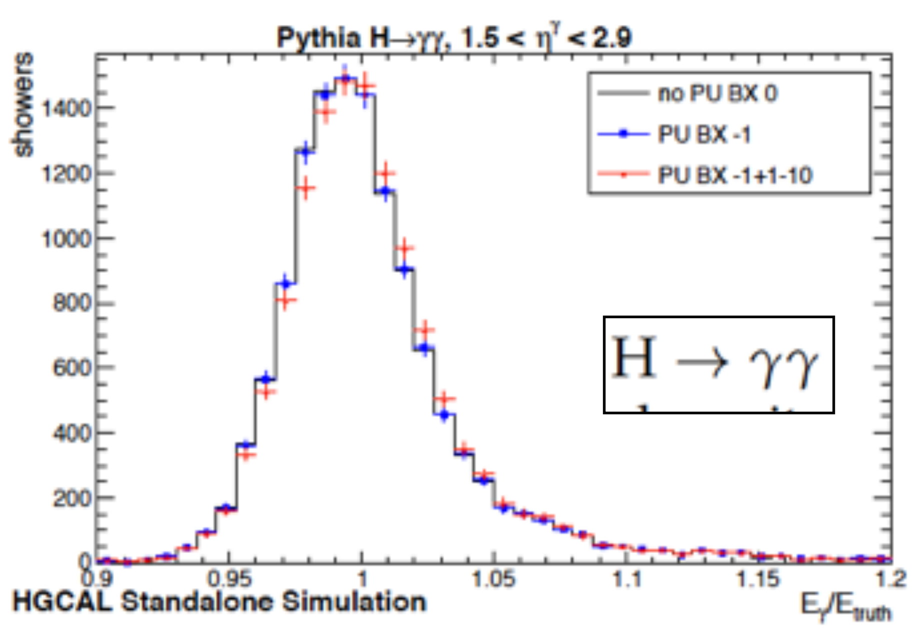


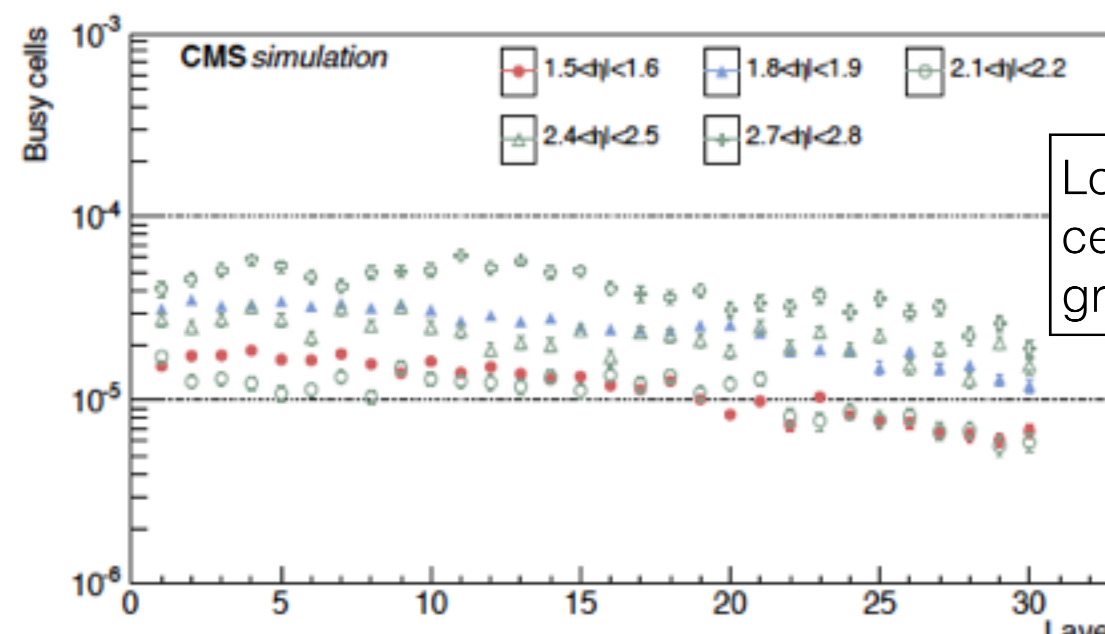


HGC Performance









Low level of busy cells due to high granularity

Muon Detectors

Barrel (DT) electronics upgrade

- L1 Trigger & Readout upgrade (Minicrates)

Forward (CSC)

- Front End electronics replacement

Gas mixture test for CSC and RPC

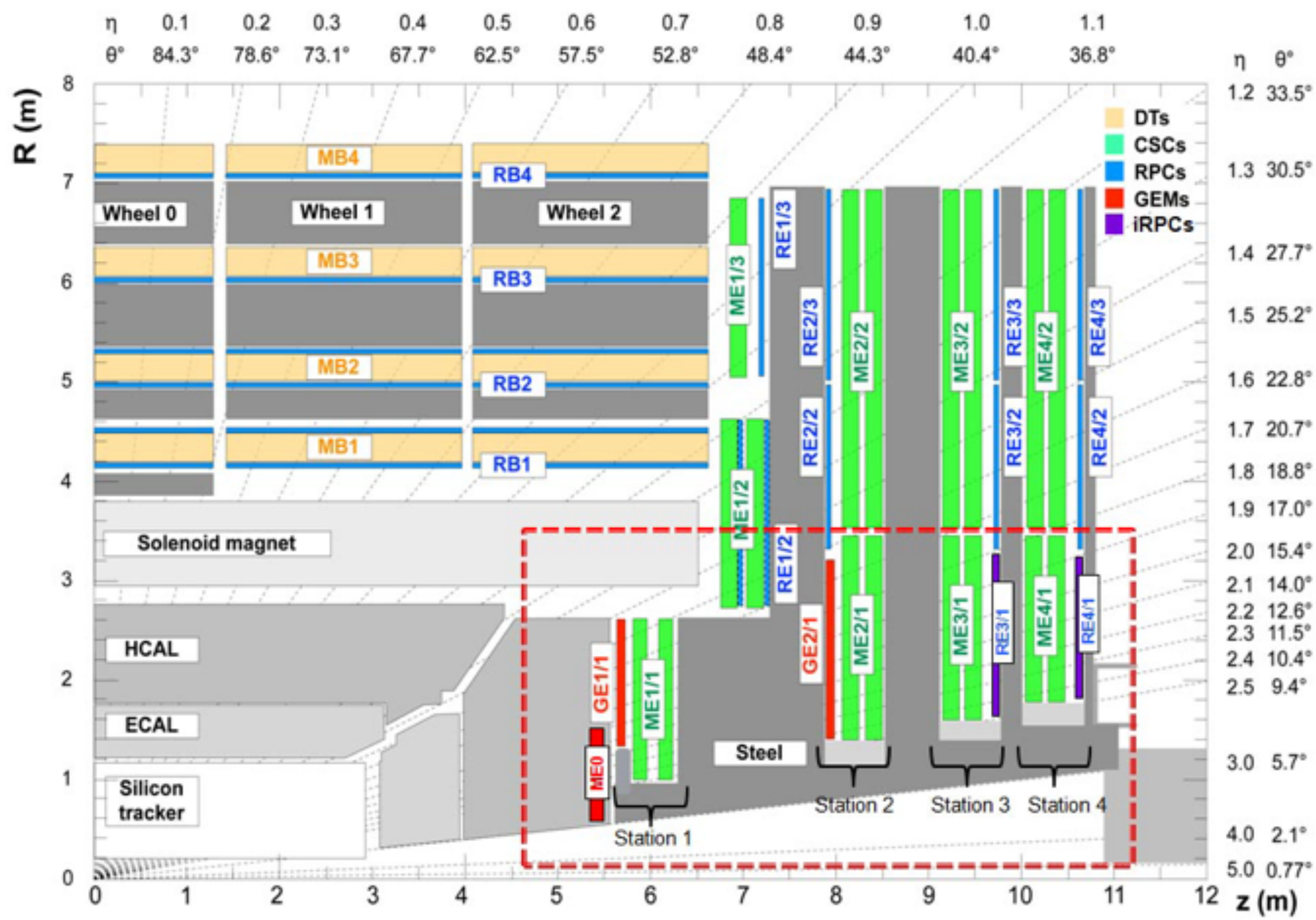
- problem of greenhouse gas regulation

Adding redundancy to CSC

- RPC: RE3/1, RE4/1 possibly with 100ps precision
- GE1/1, GE2/1 : GEM detectors

EXTENSION in rapidity (to eta 3)

ME0 with GEM detectors



Muon Det upgrade

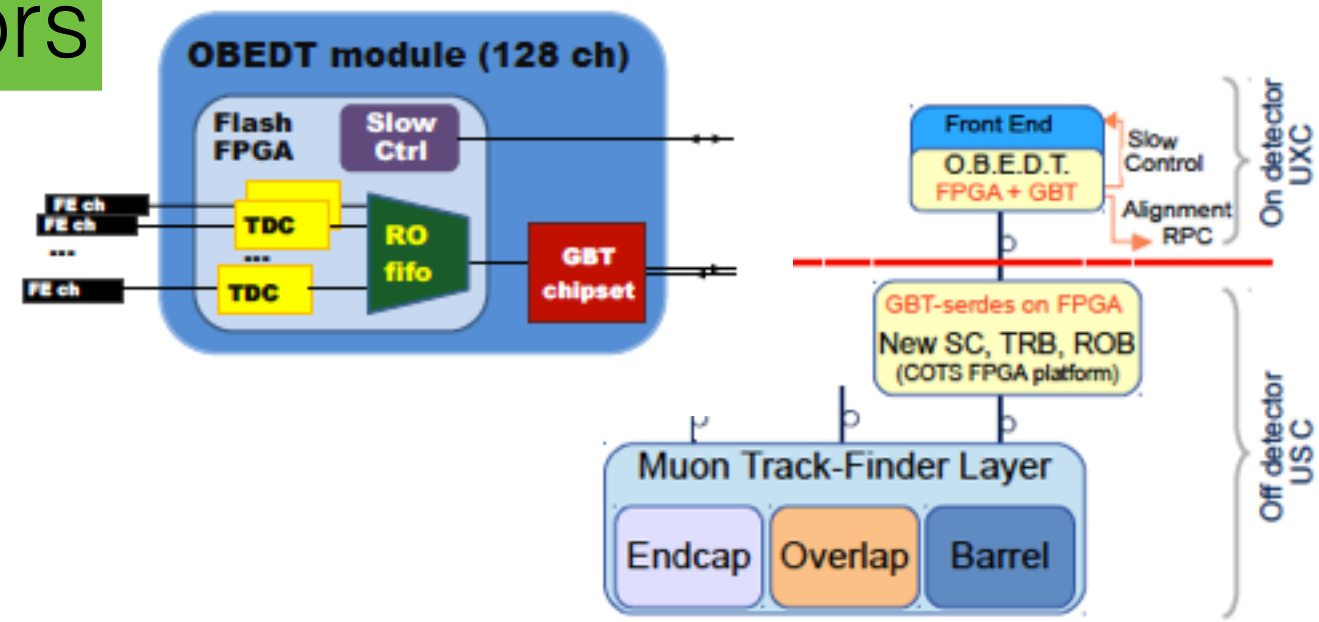
DT-detectors

Front End - New Minicrates:

- TDC (using a FPGA), control, monitoring only
- All data will be sent to BackEnd using GBT

Back End analysing full chambers information

- better BCO-ID, z-resolution, better tracking elements



CSC-detectors

New Front End

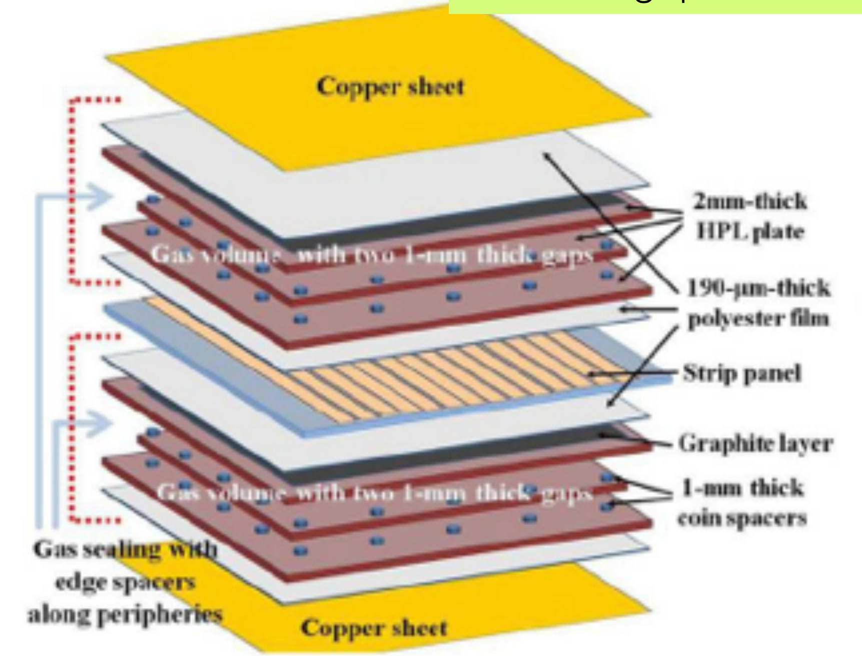
- New cathode electronics to improve rate and latency capabilities

RPC-detectors

New Forward detectors   RE3/1, RE4/1

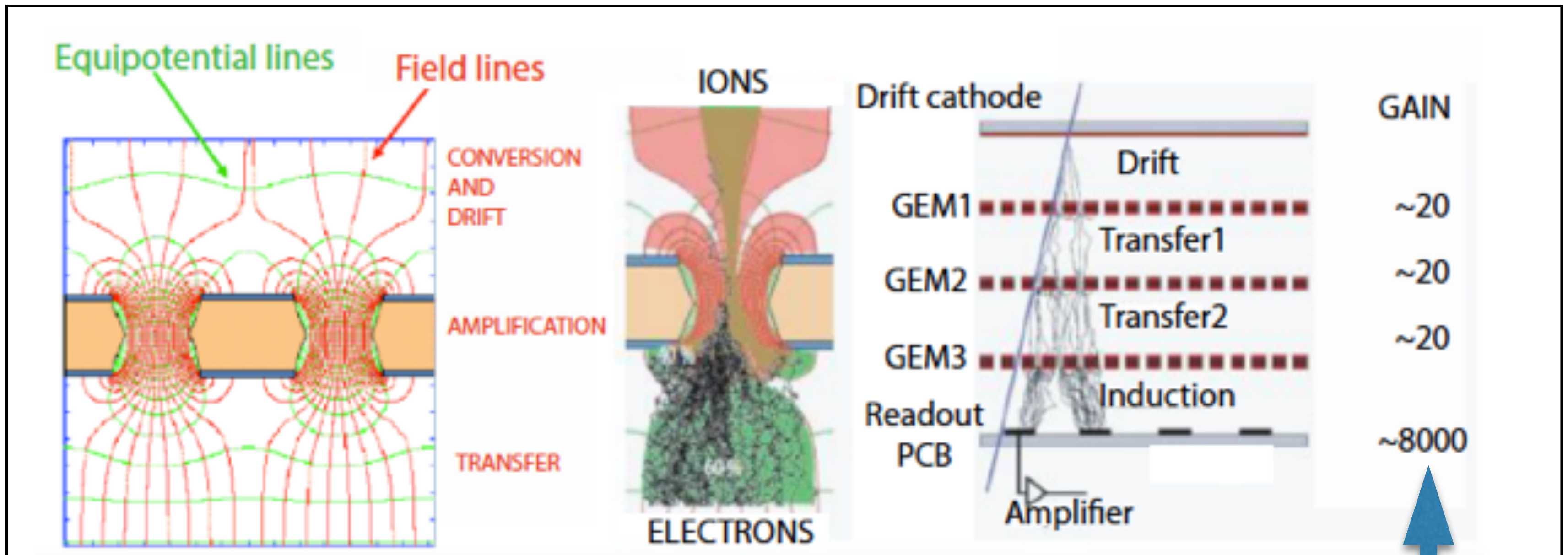
- Improvement in rate capability
  - lower electrode resistivity: RD on new material (silicate glass,) or improved production of bakelite
  - lower average charge in avalanches: compensated with higher electronics gain (like SiPM
  - detector configuration: thinner electrodes, multigap HPL RPC

multigap HPL RPC



GEM detectors

- Super chambers made of double layer of trapezoidal triple-GEM chambers
  - Single GEM : x (20-25) , **TRIPLE GEM:** gain of 8000-15000 !



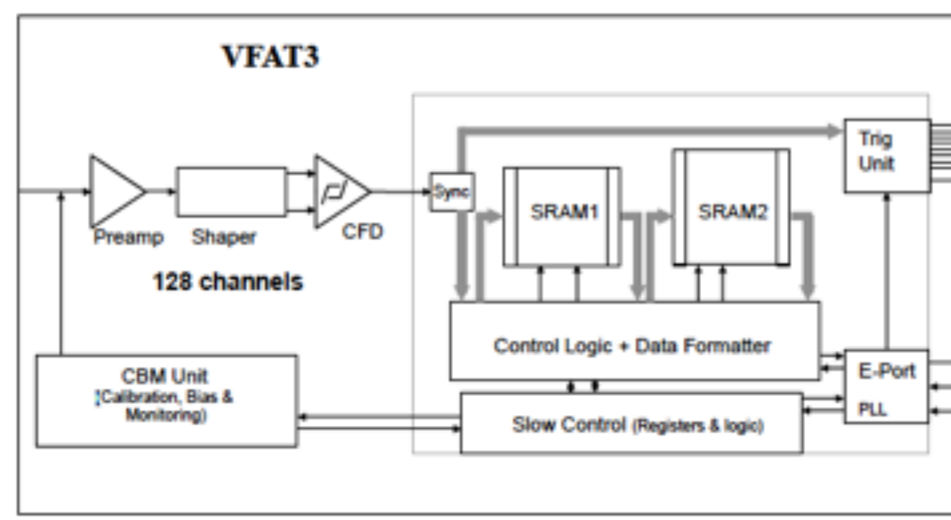
1 layer: Cu-Polyimide-Cu
hole: 70um, pitch 140 um
50-80 kV/cm @ hole
4000V for triple-GEM
gas: Ar-CO_2, Ar-CO_2-CF_4

dx ~200 um, dt ~ 5-8 ns
1 MHz/cm^2 rate

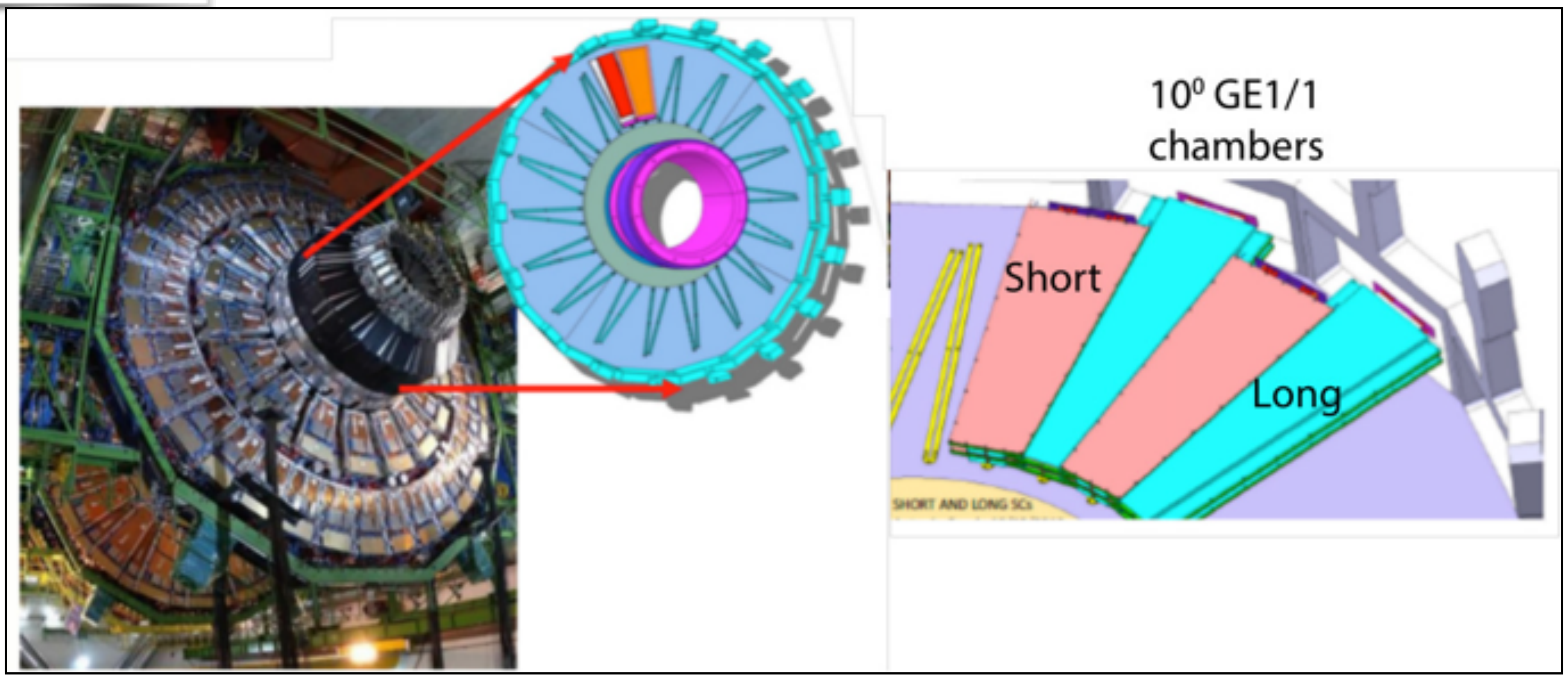
Challenge of building LARGE-size GEM !

NEW FE-ASIC: VFTA3 designed in CMOS 130nm technology:

- signal both polarities
- interface to GBT at 320 MHz
- up to 25 usec trigger latency
- time resolution < 7.5 ns

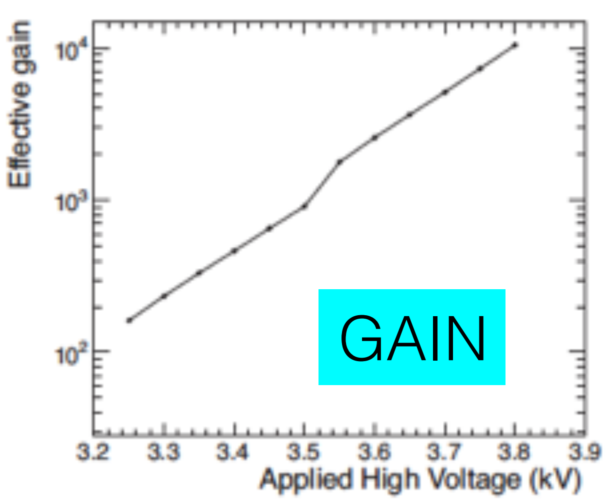


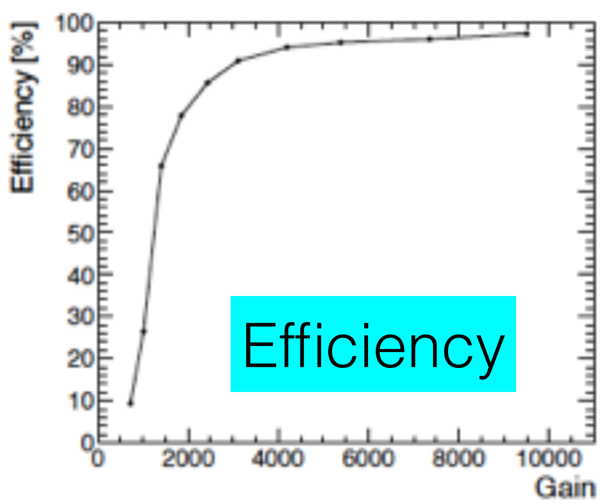
GE1/1, GE2/1, ME0

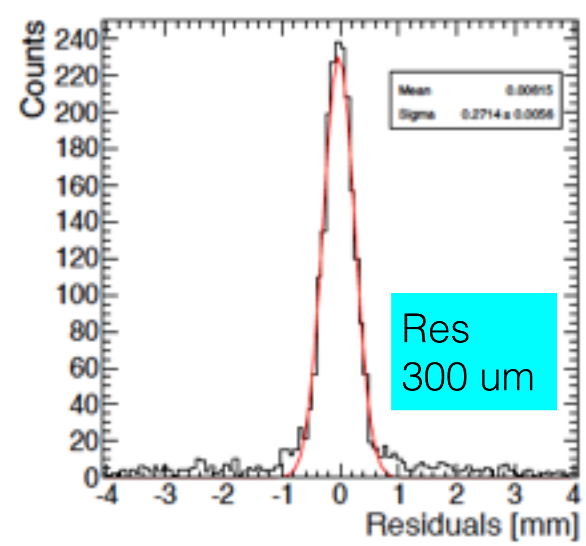


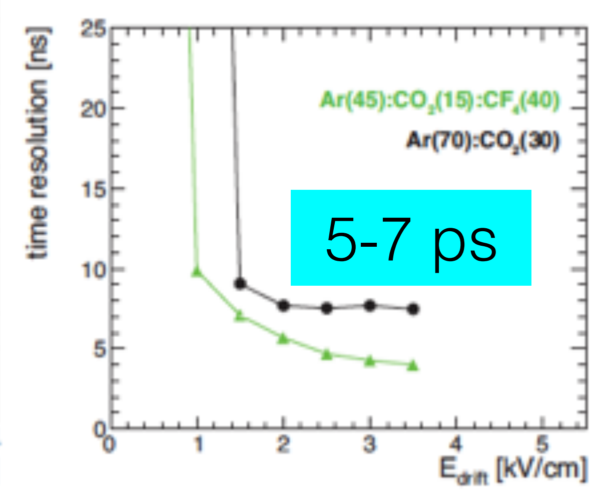
10 proto-**GE1/1** constructed already

GE1/1, GE2/1 could be already installed during LS2



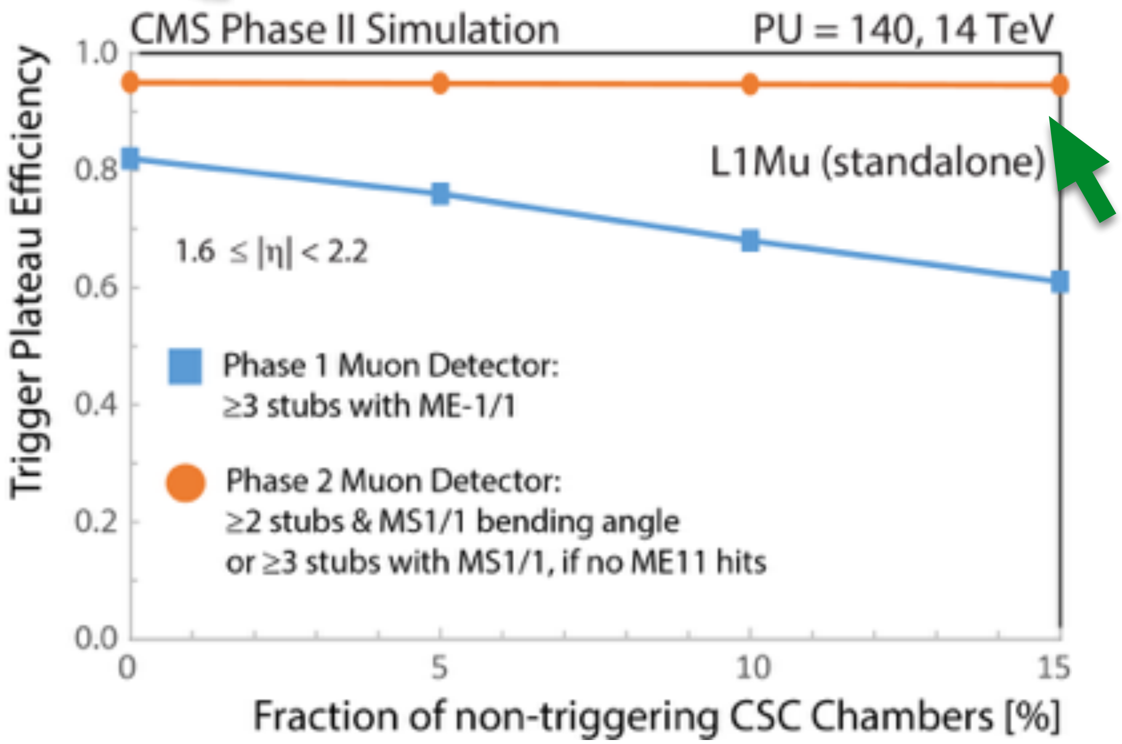


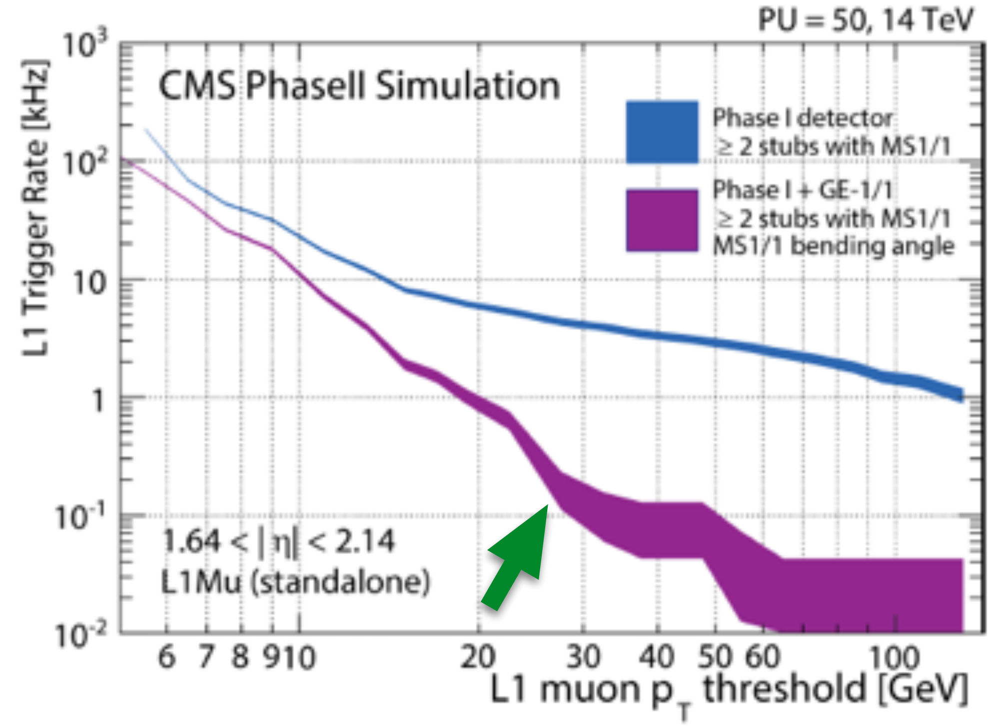




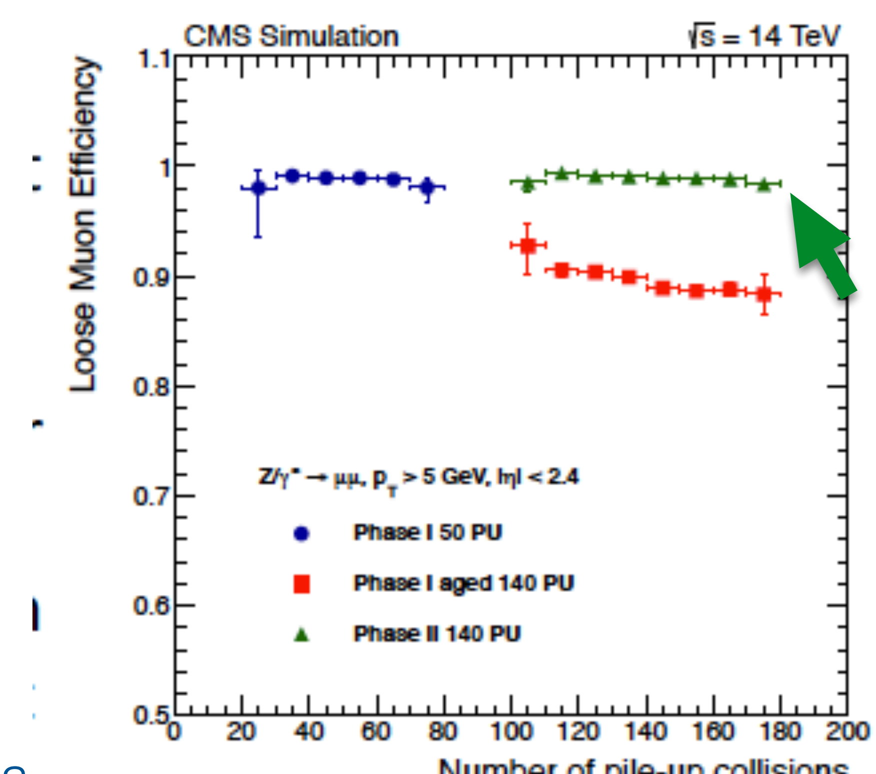
- **ME0** : GEM detector covering rapidity up to 3 (or more) depending on HGC boundaries

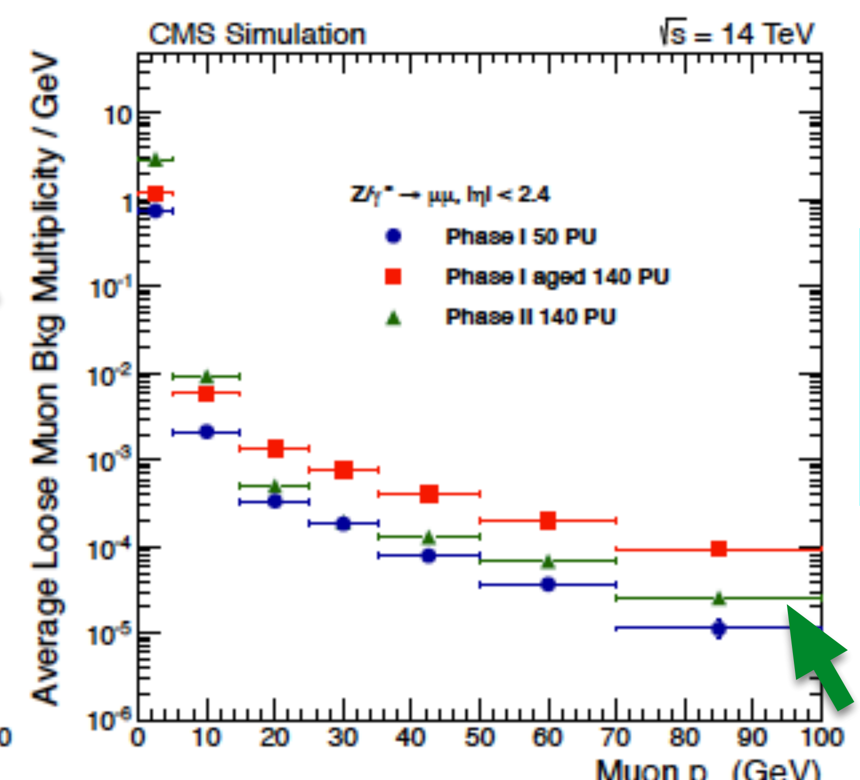
Muon Performance





Forward

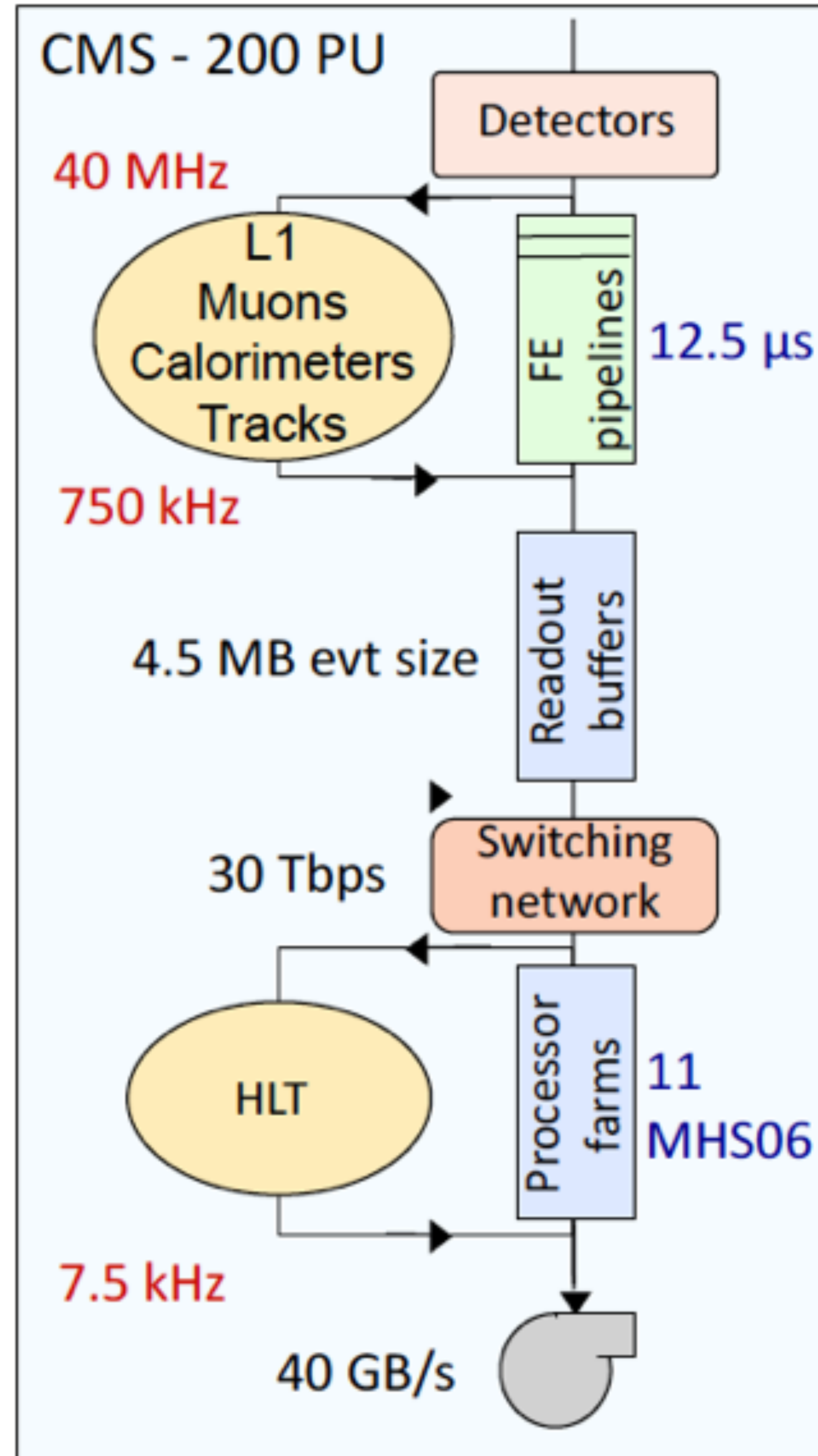




Barrel

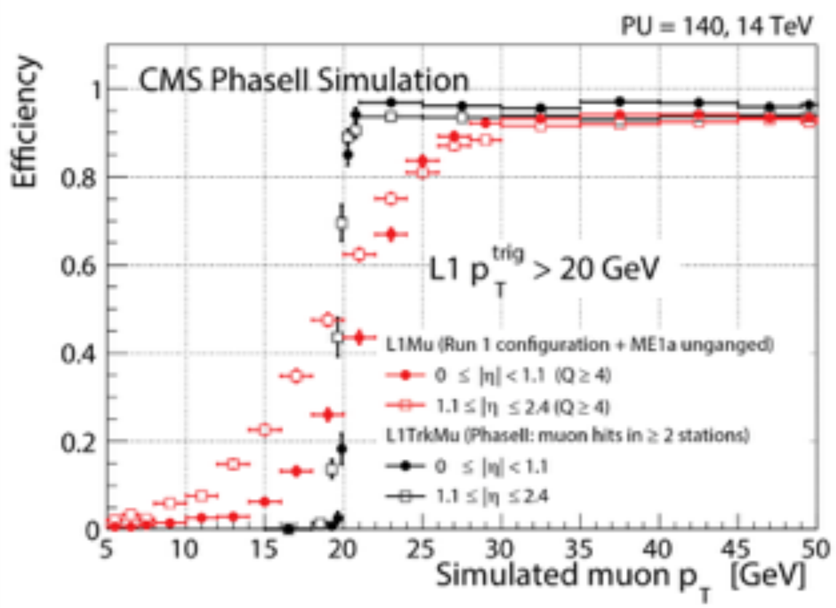
L1-Trigger / HLT / DAQ

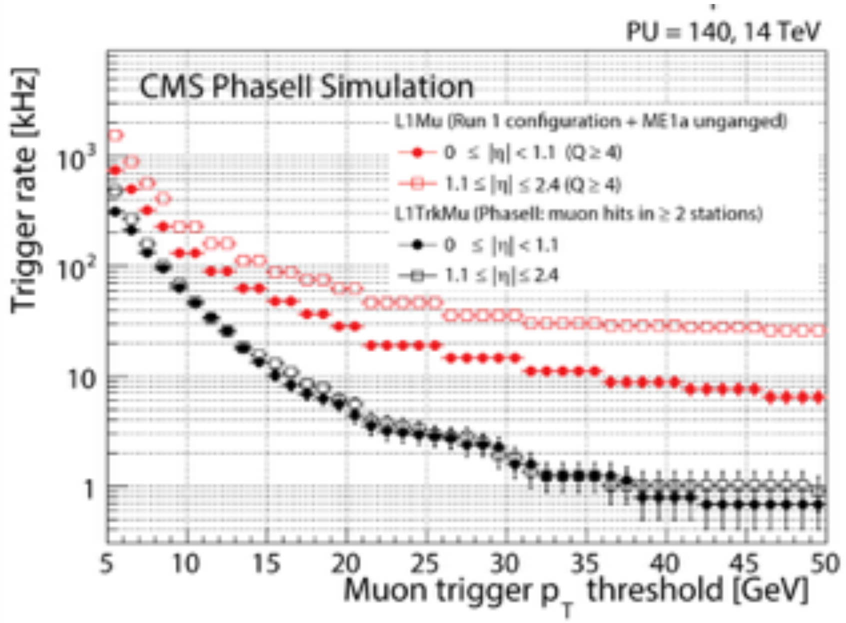
- L1-Trigger
  - High BW and processing power boards
  - First layer to match detector information
  - Second layer to produce Trigger objects
- Trigger timing, throttling and control
  - High Band Width bi-directional link allowing trigger information to steer readout
- DAQ
  - Similar evt builder, HLT and storage as present Increase Band Width - 800 links x 100 Gbps with 30% occ. will provide 30 Tbps evt building throughput
- HLT
  - Processing power scales as PU x L1 rate - need increase by a factor ≃ 52 wrt Run 2 at 200 PU



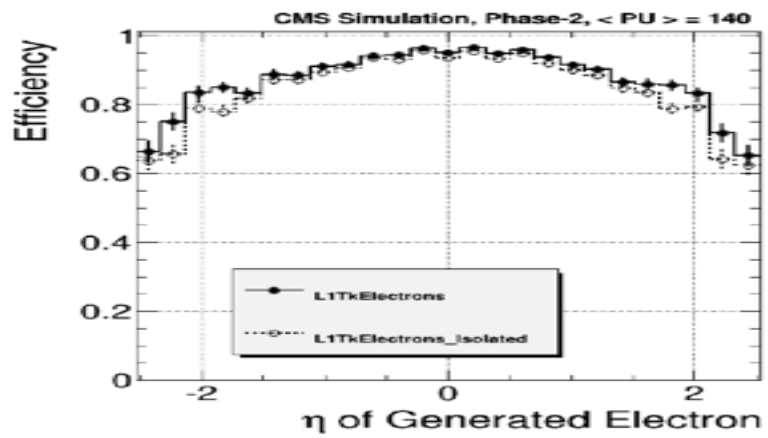
L1-Trig Performance

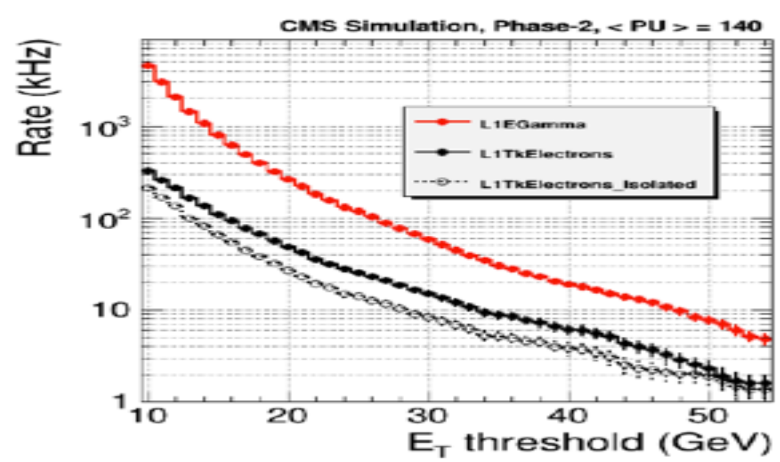
Muons

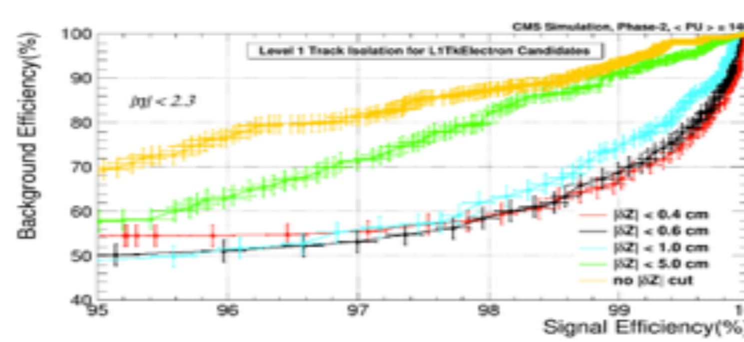




Electrons

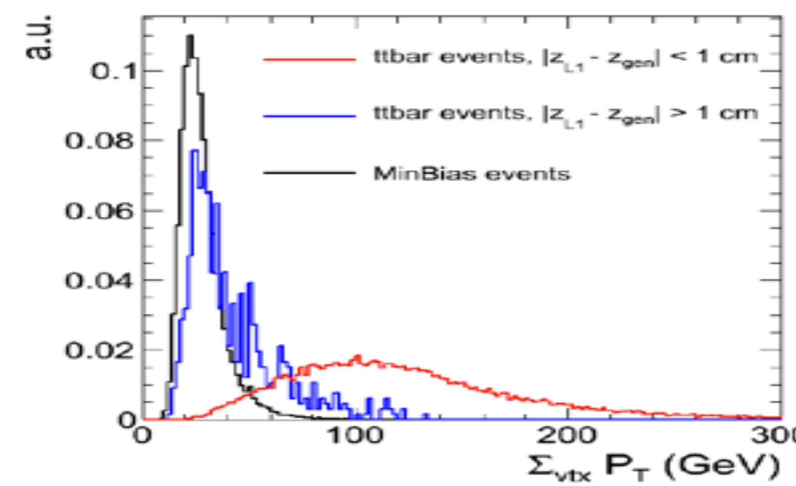




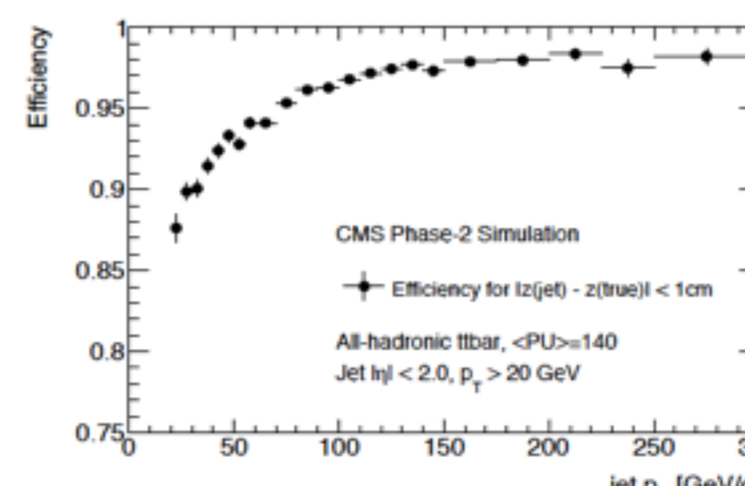


Isolation Eff.

Vertex-ID and jets



tt events: effect of Vtx-ID of jet



Eff. for jet @<1cm from True-Vtx

Italy involvements

- **TRACKER** : Ba, Ct, Fi, Mib, Pd, Pv, Pi, Pg, TO (21%) - 100 FTE
- **ECAL :** Mib**,** Rm1, To, Ts
- **RPC** : Ba, LNF, Na, Pv (27%) - 11 FTE
- **DT** : Bo, Pd, To (58%)
- **GEM** : Ba, Bo, LNF, Na, Pv - 17 FTE

Conclusions

- HL-LHC is (right now) provides the major HEP program after year 2024
- Experiments have to survive to hostile conditions and achieve unprecedented performance to fully exploit the physics potential offered by HL-LHC
- A solid upgrade program is under his way for the CMS experiment
- Looking forward still for new surprises and excitement from LHC and to continue even deeper in HL-LHC, both for important measurements and possible new discoveries

CHIPIX65 INFN Project

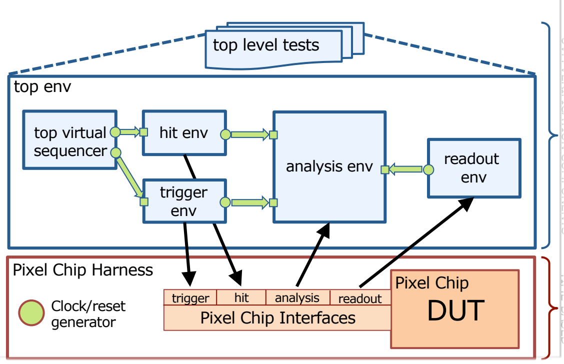
R&D on CMOS 65nm (CMS+ATLAS), part of RD53

Radiation characterisation

- x-ray machine at LNL / Pd-INFN
  - Total Ionising Dose (TID)
  - 1 GRad in ~ 2 weeks
- Low-p at CN accelerator LNL
  - TID and Total Displacement damage
- TANDEM / SIRAD
  - Single Event Effects - with Heavy Ion
- Studies on n-MOS, p-MOS
- Irradiation of IP-block, Noise-measurements vs Irradiation

Digital Electronics:

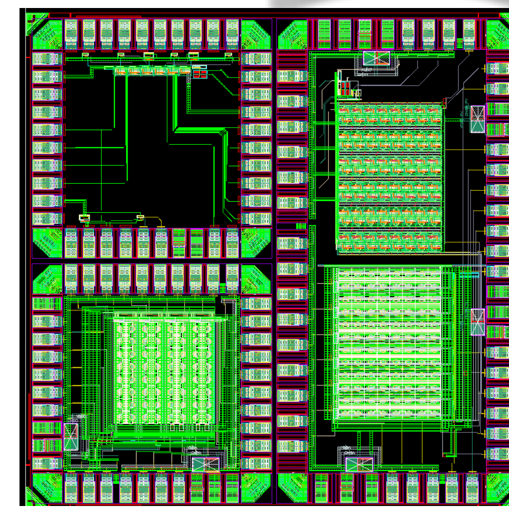
- Simulation Framework
  - System-Verilog-UVM (VEPIX53)
- Digital Architecture Studies
- Input protocols definition
  - fast/efficient/continuos (while readout)
  - SEE robust



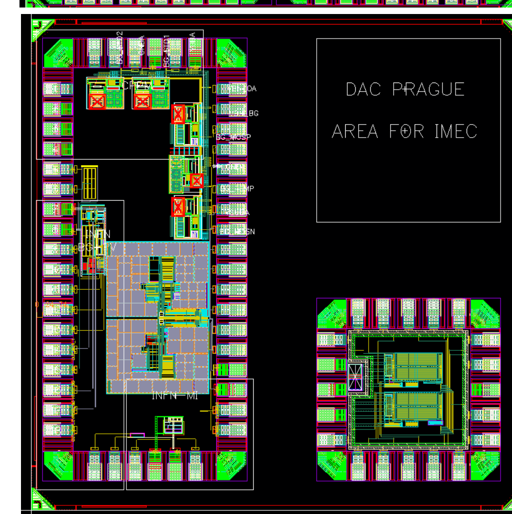
Activities of 2014 - now

Design in 65nm

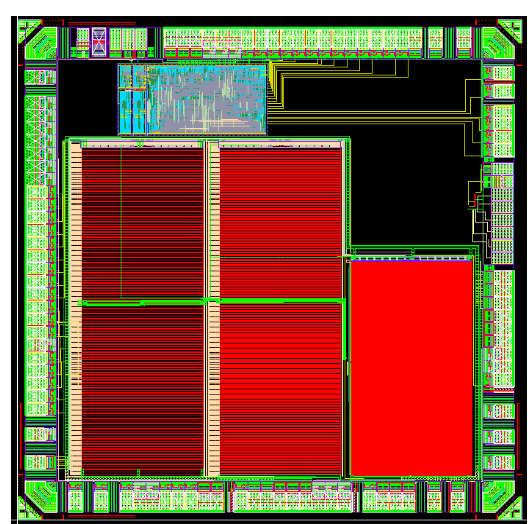
- 6 silicon dies 2x2mm2 submitted
- CHIPIX65 IP-blocks
  - DAC-curr, ADC, SRAM,
  - SER/DES, sLVDS(TX/RX)
  - BandGap, D2RA digital cells
  - JTAG
- CHIPIX65 Analog Very Front End
  - Synchronous chain
  - Asynchronous chain
- Integration of other RD53 IPs
  - DAC-volt (Prague)
  - SER (Bonn), BandGap (CPPM, CERN)

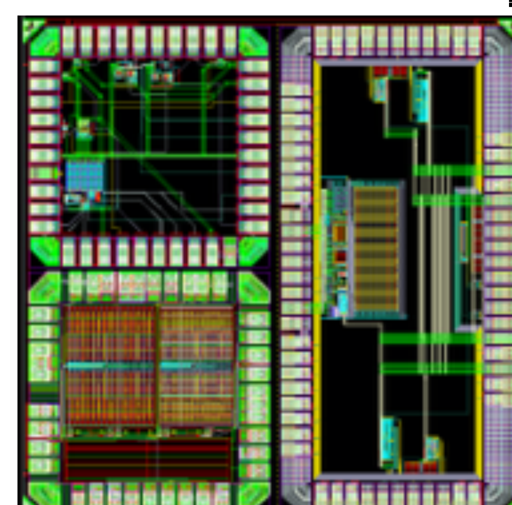


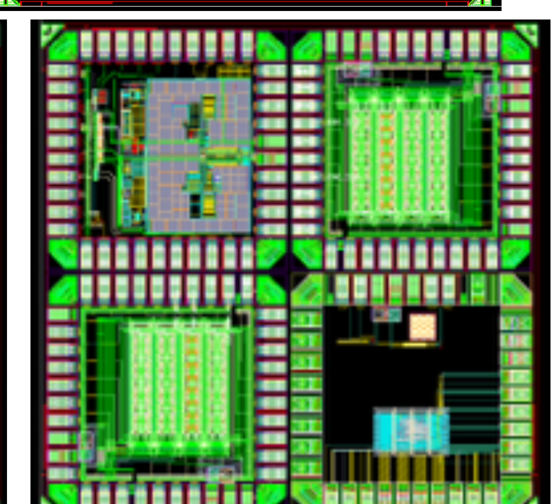
CHIPIX_VFE_1



CHIPIX_BIAS





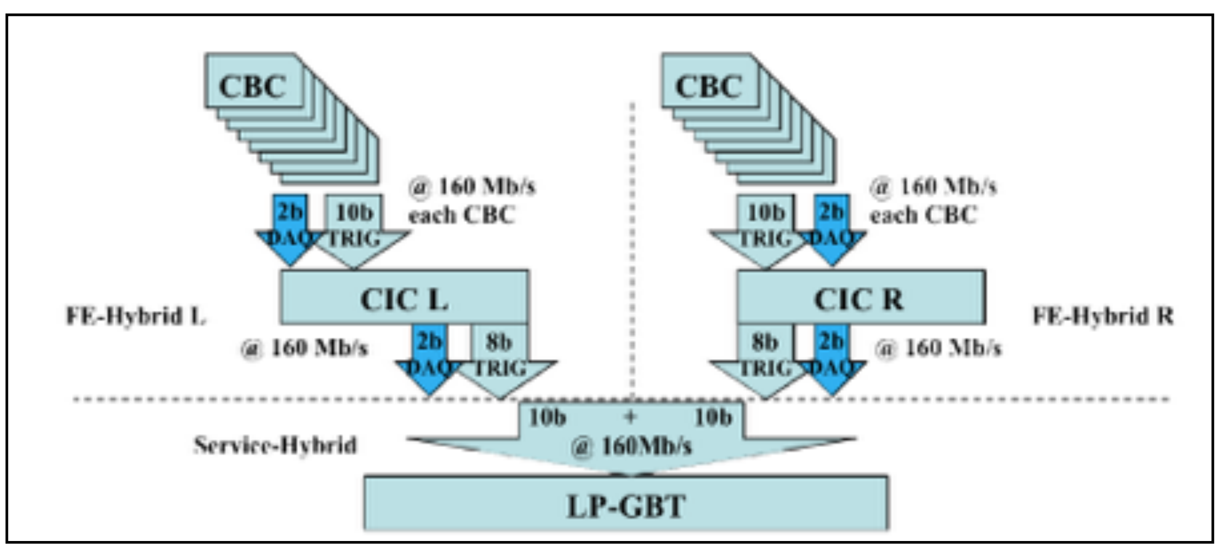


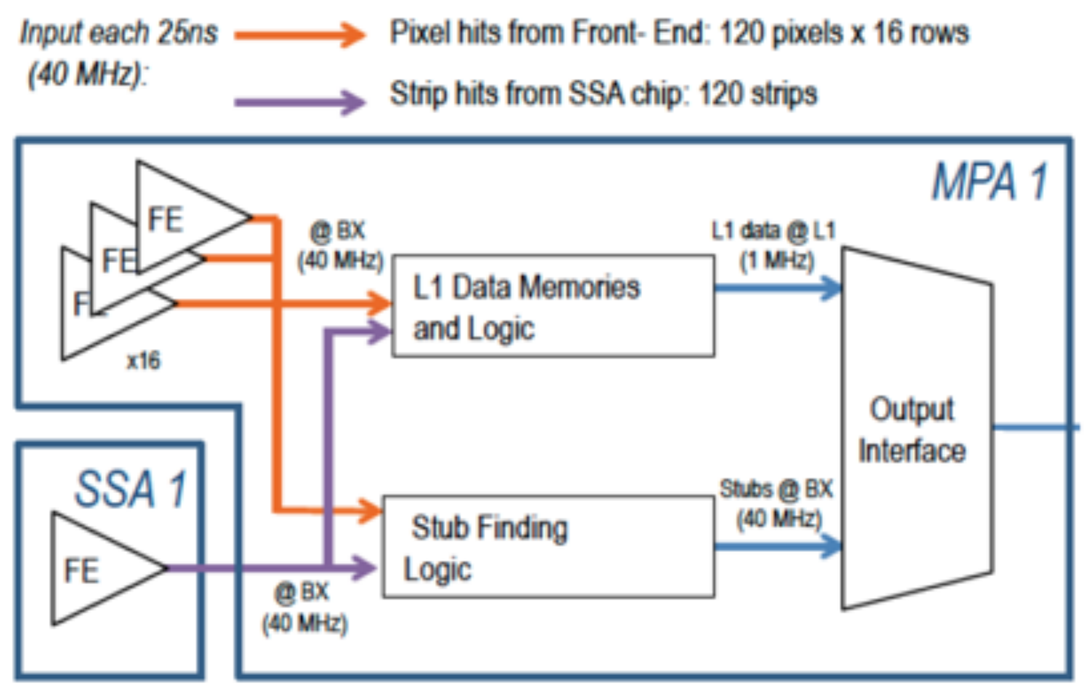
CHIPIX_SRAM, CHIPIX_IP_3, CHIPIX_VFE_2

Backup Slides

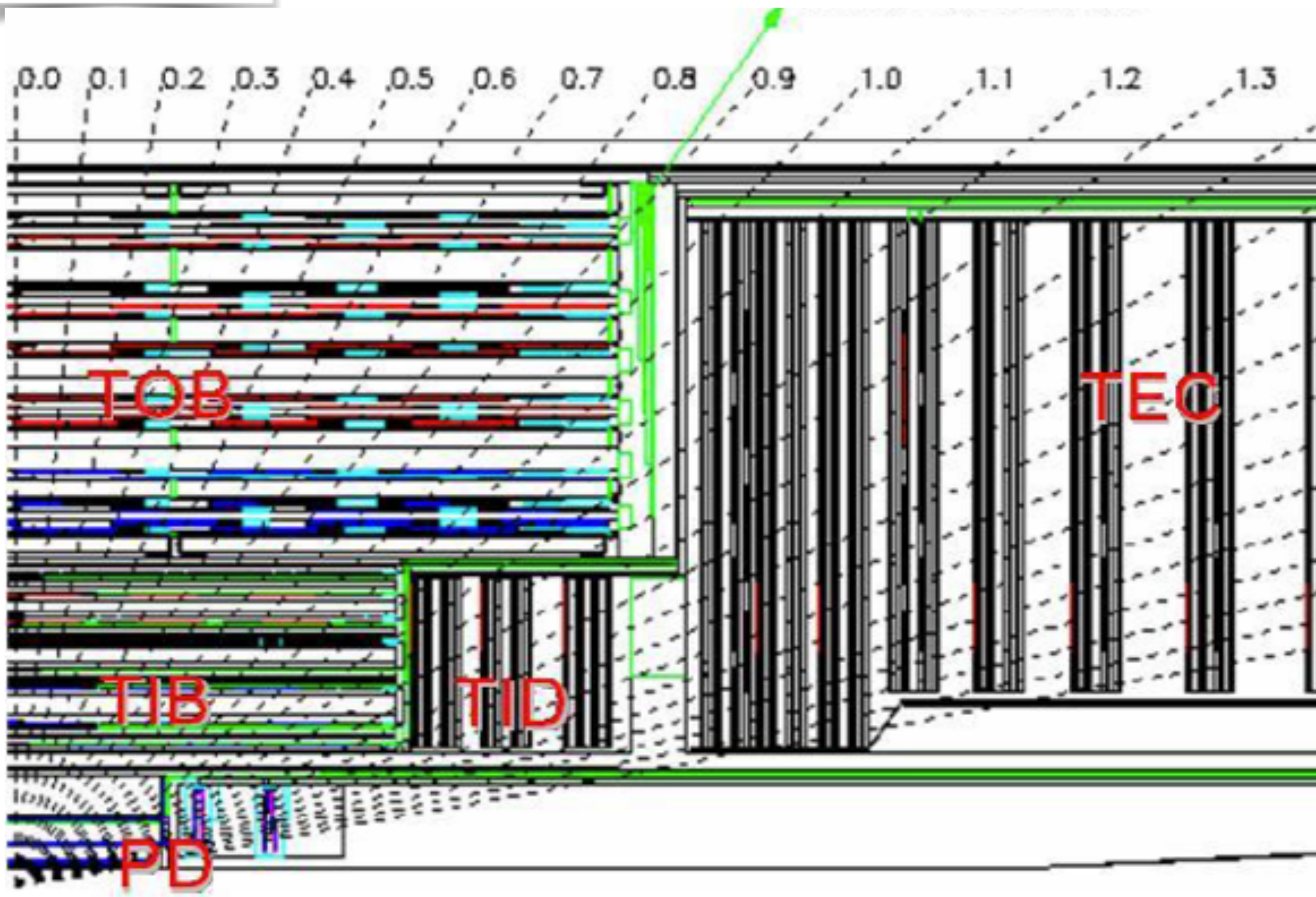
Outer Tracker ASICs

- CBC (CMS Binary chip):
  - 130nm CMOS
  - data inputs: 127 bottom-ch; 127 top-ch
  - correlation top / bottom + unsparsified binary readout
- CIC (Concentrator Integrated chip):
  - 65nm CMOS
  - buffer and sparsifies CBC data
- MAP (Macro Pixel Asic):
  - 65nm CMOS
  - data inputs: 2000 pixels + SSA data
  - correlation top / bottom + sparsified binary data readout and stubs
- SSA (Short Strip ASIC):
  - 65nm CMOS
  - process sensor signal and send unsparsified data





Present Tracker



Modules:

- 3112 + 3024 Thin modules (ss +ds)
- 5496 + 3600 Thick modules (ss +ds)

Silicon:

- 6,136 Thin sensors = $48 m^2$
- 18,192 Thick sensors = $162 m^2$

198 m^2 of silicon microstrip sensors
(~420 m^2 of silicon wafers)

FE Electronics:

75,376 APV chips

9,648,128 strips = electr. Channels

Tracker Inner Barrel (TIB): 4 layers: 2 Rϕ (2D), 2 Rϕ-Stereo (3D)

Tracker Outer Barrel (TOB): 6 layers, : 4 Rϕ (2D), 2 Rϕ-Stereo (3D)

Tracker Inner Disks (TID): 3*2 disks, : 1 Rz (2D), 2 Rz-Stereo(3D)

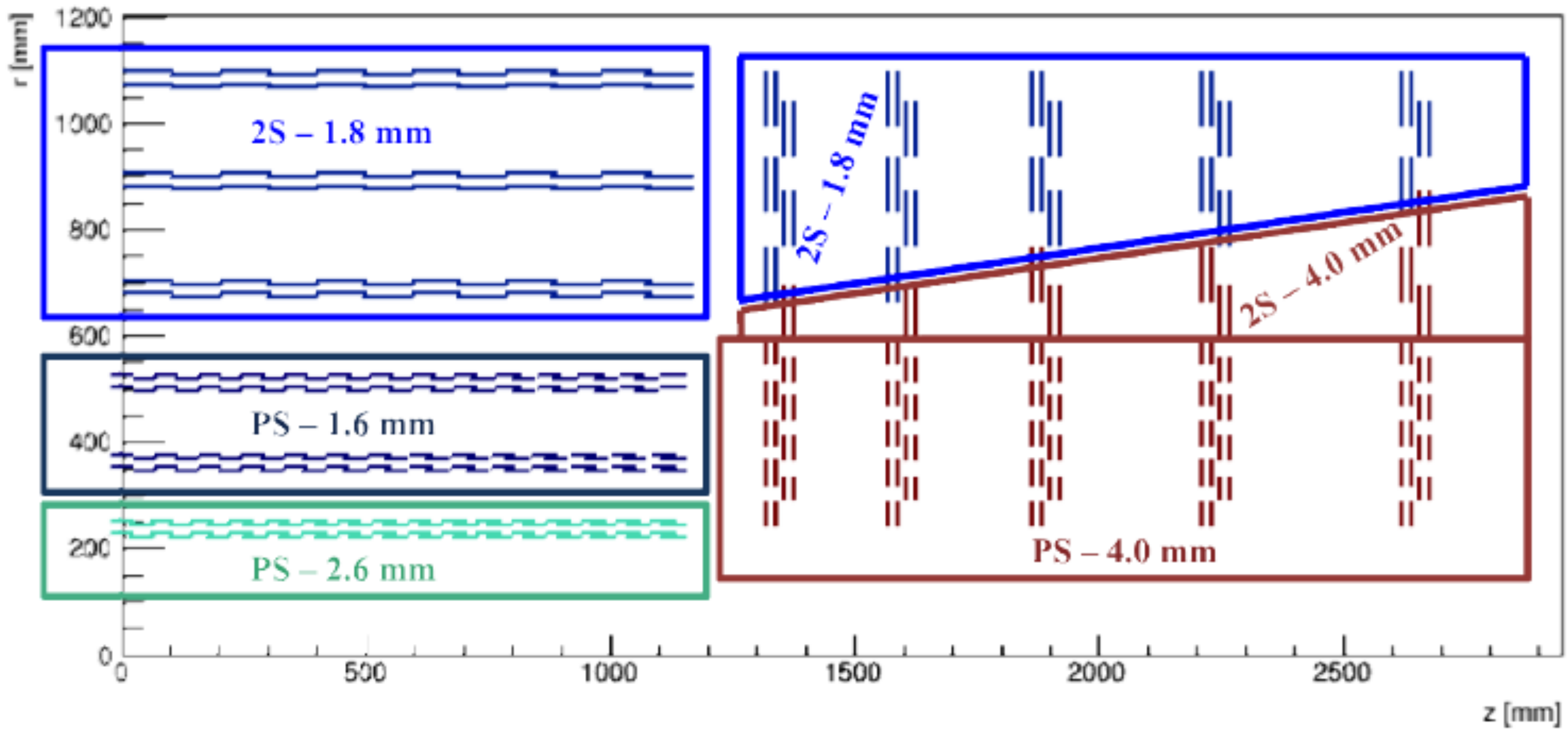
Tracker EndCap (TEC): 9*2 disks, : 4 Rz (2D), 3 Rz-Stereo(3D)

Each Track has at least 10 high precision measurements for Pt and 4 in Θ

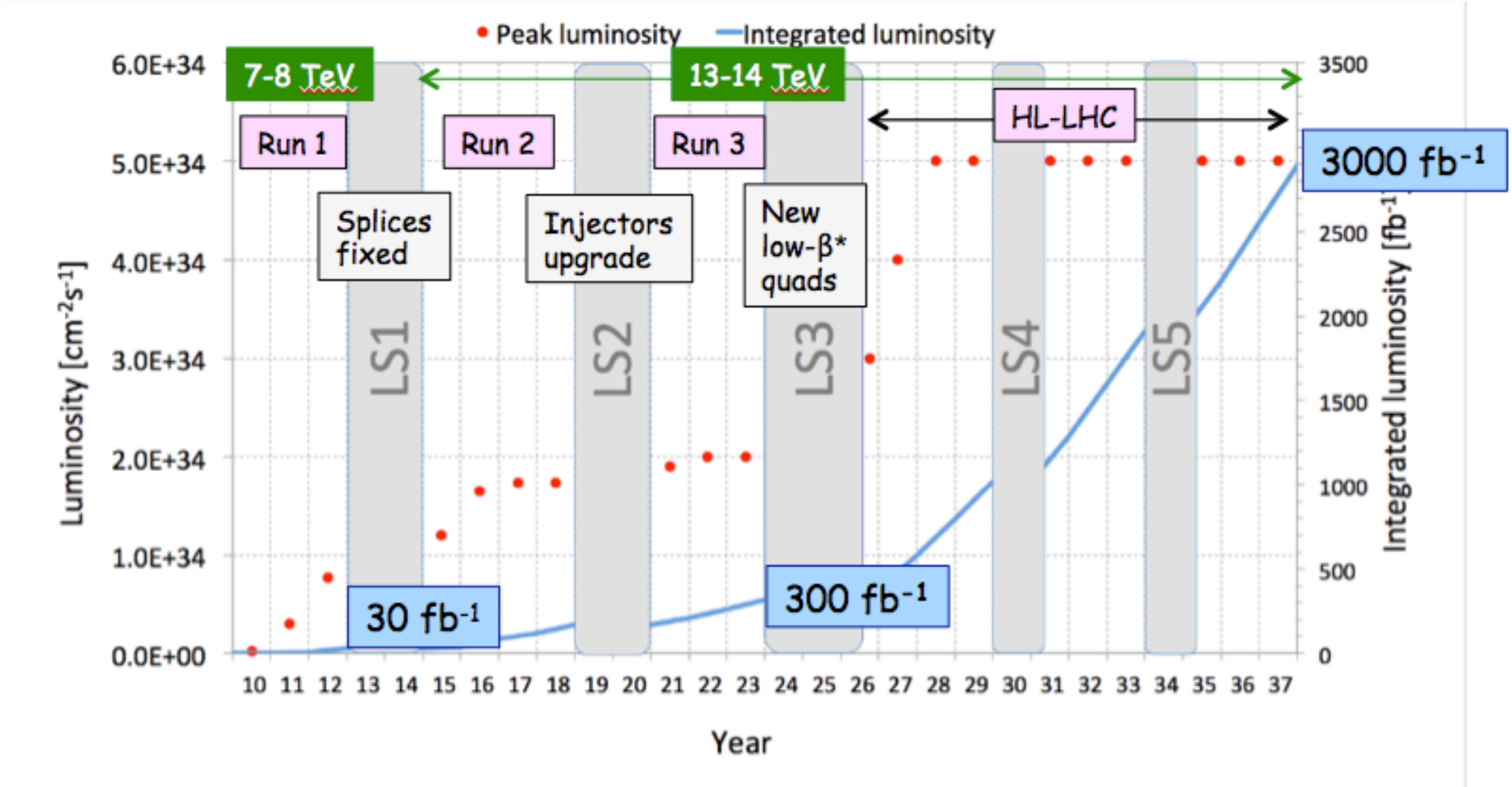
Coverage: | η | < 2.5

5

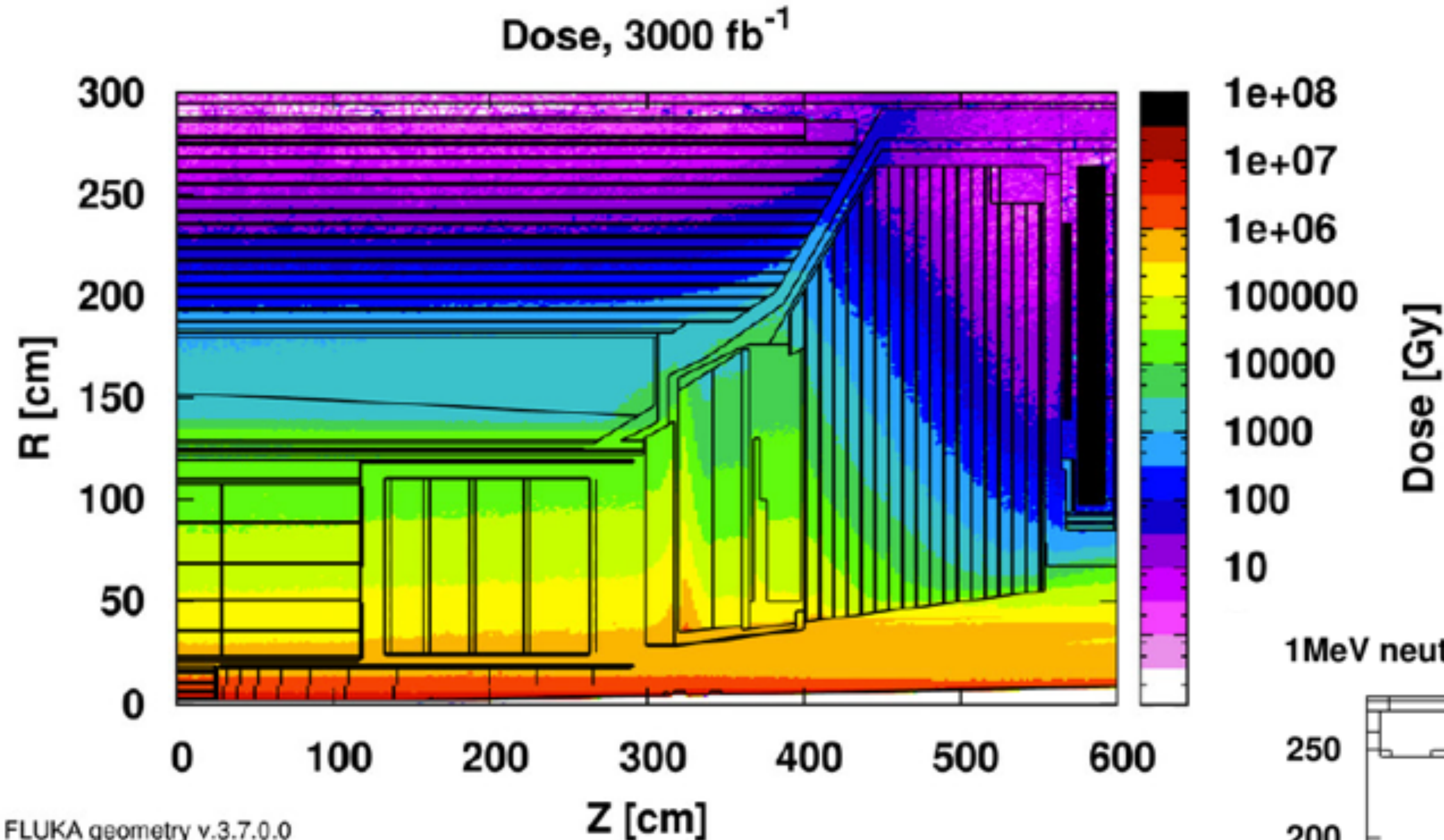
Outer Tracker spacing



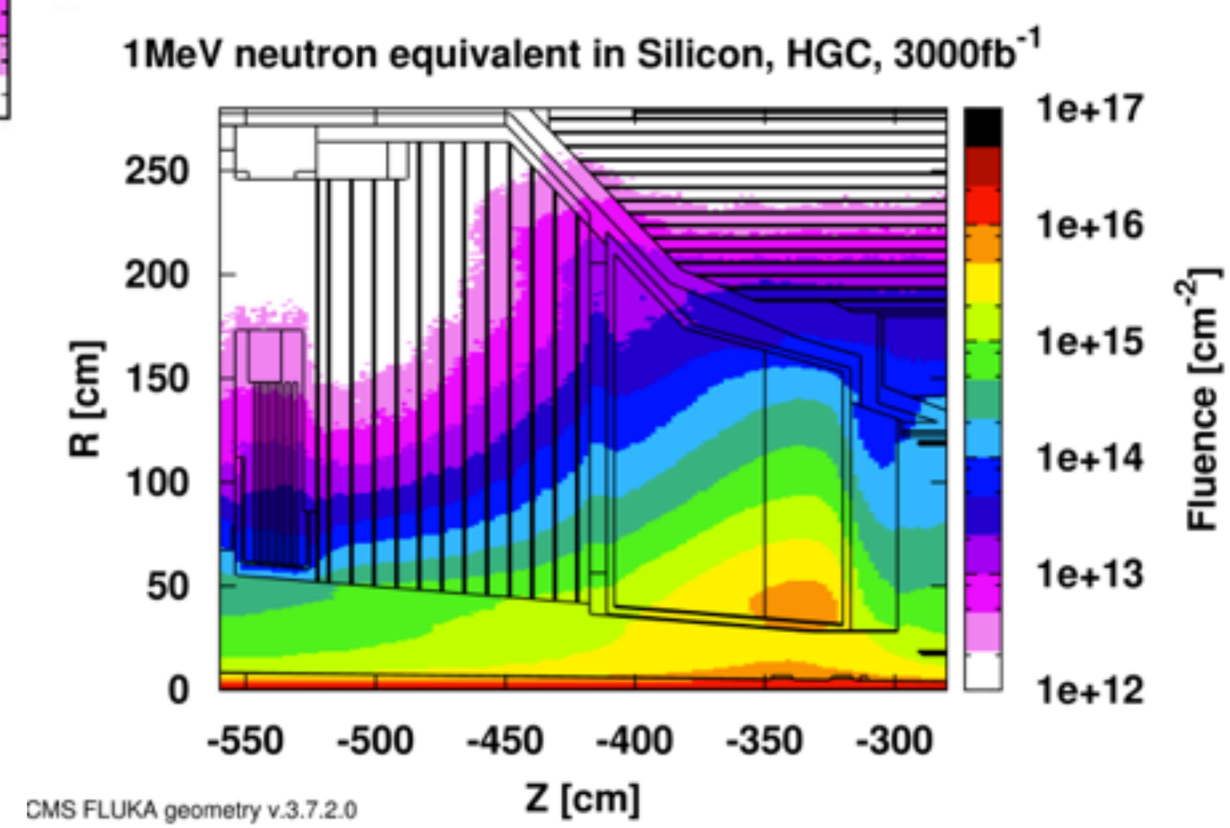
LHC time-scale



Radiation

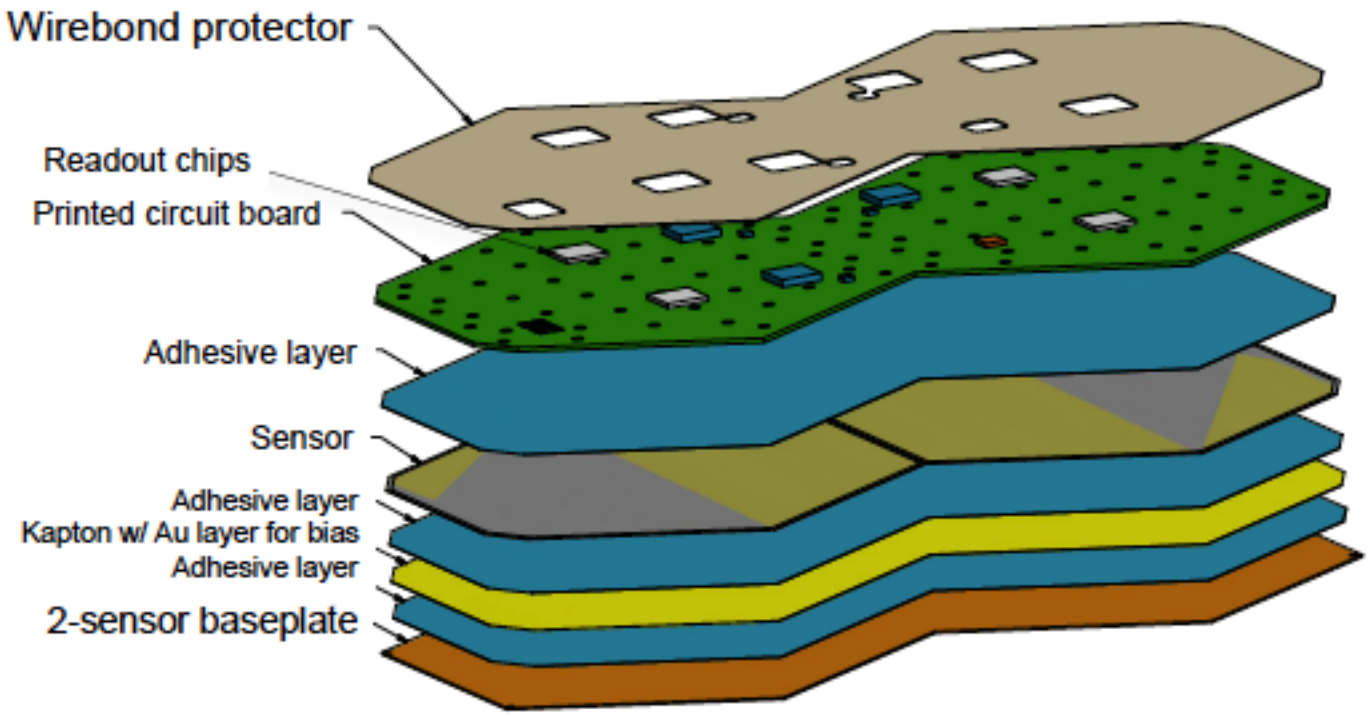


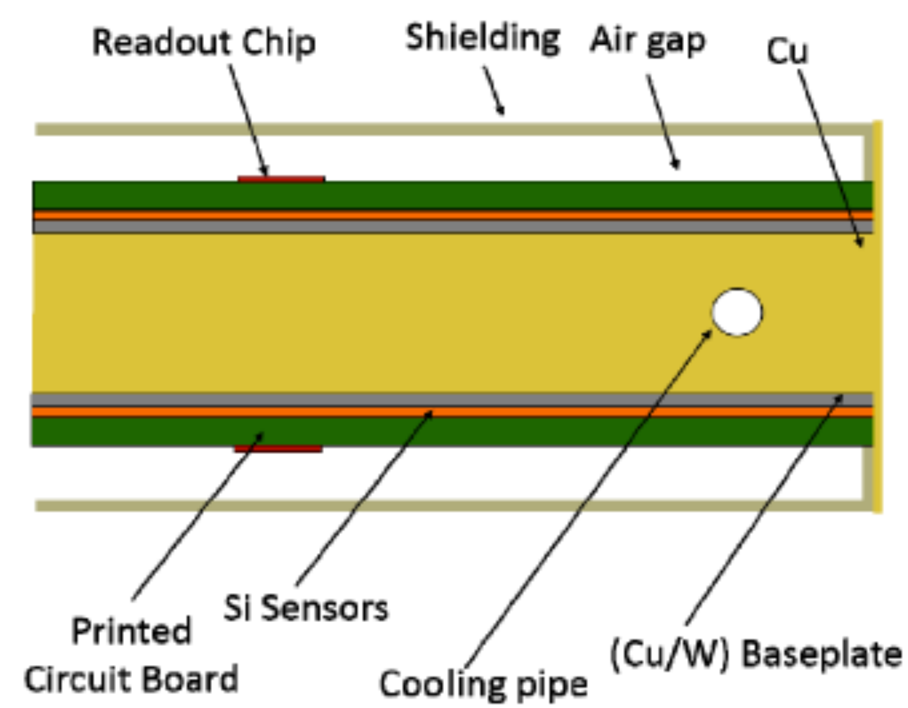
Dose, 3000 fb^{-1}
R [cm]
Z [cm]
Dose [Gy]
1e+08
1e+07
1e+06
100000
10000
1000
100
10
CMS FLUKA geometry v.3.7.0.0



1MeV neutron equivalent in Silicon, HGC, 3000fb^{-1}
R [cm]
Z [cm]
Fluence [cm^{-2}]
1e+17
1e+16
1e+15
1e+14
1e+13
1e+12
CMS FLUKA geometry v.3.7.2.0

HGC Modules


Wirebond protector
Readout chips
Printed circuit board
Adhesive layer
Sensor
Adhesive layer
Kapton w/ Au layer for bias
Adhesive layer
2-sensor baseplate


Readout Chip
Shielding
Air gap
Cu
Printed Circuit Board
Si Sensors
Cooling pipe
(Cu/W) Baseplate