Upgrade del sistema di trigger e readout per la stazione di test delle camere RPC di ALICE

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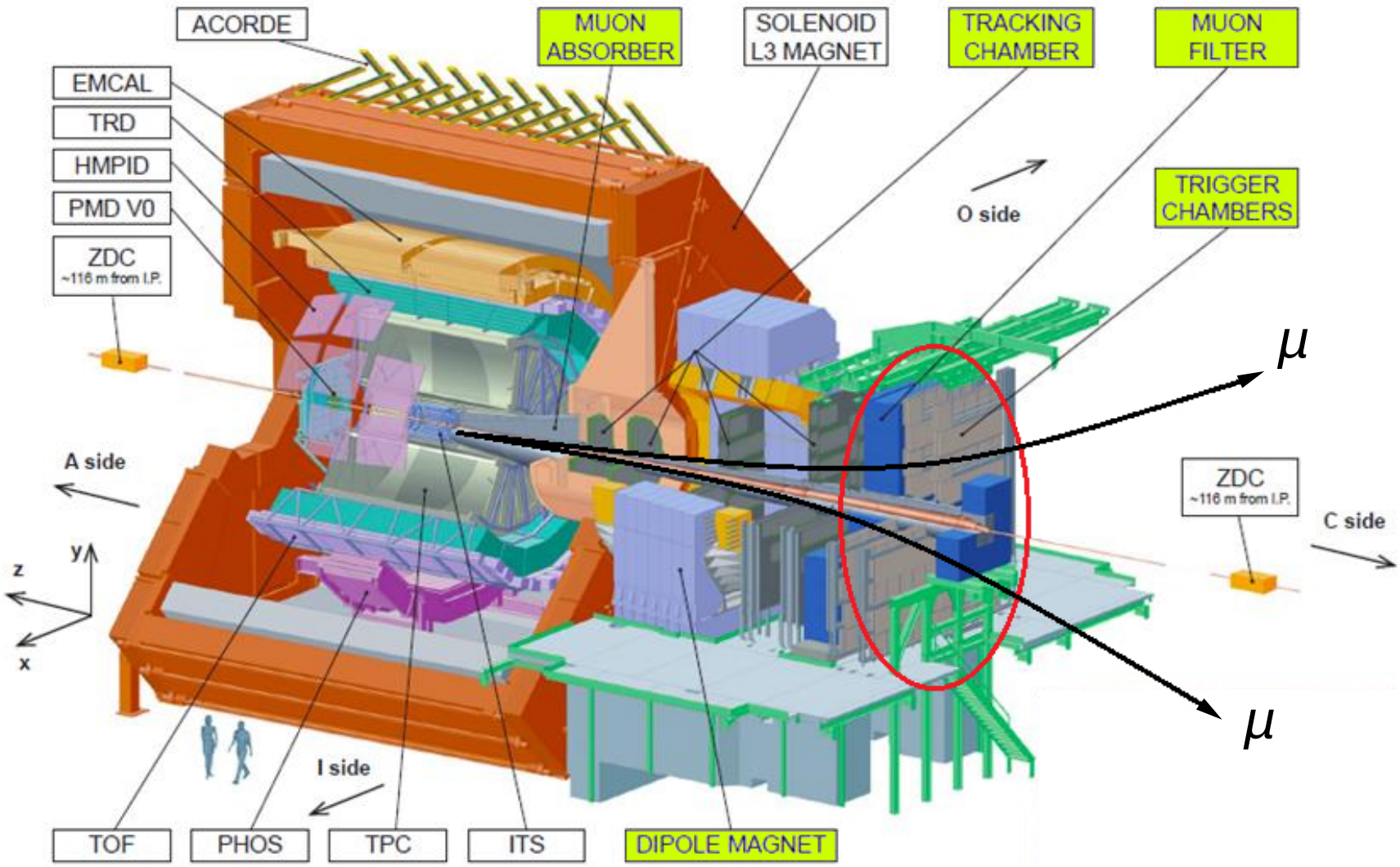
Roma, 25 Settembre 2015

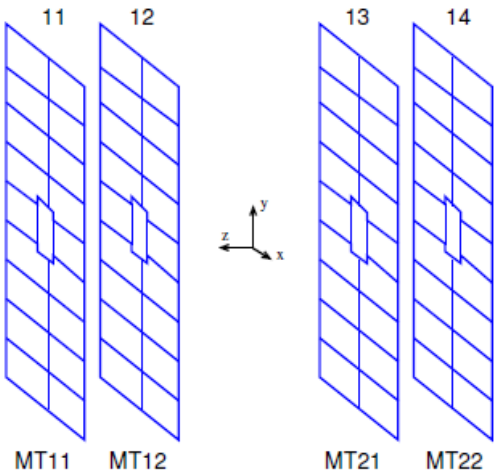
The ALICE Experiment

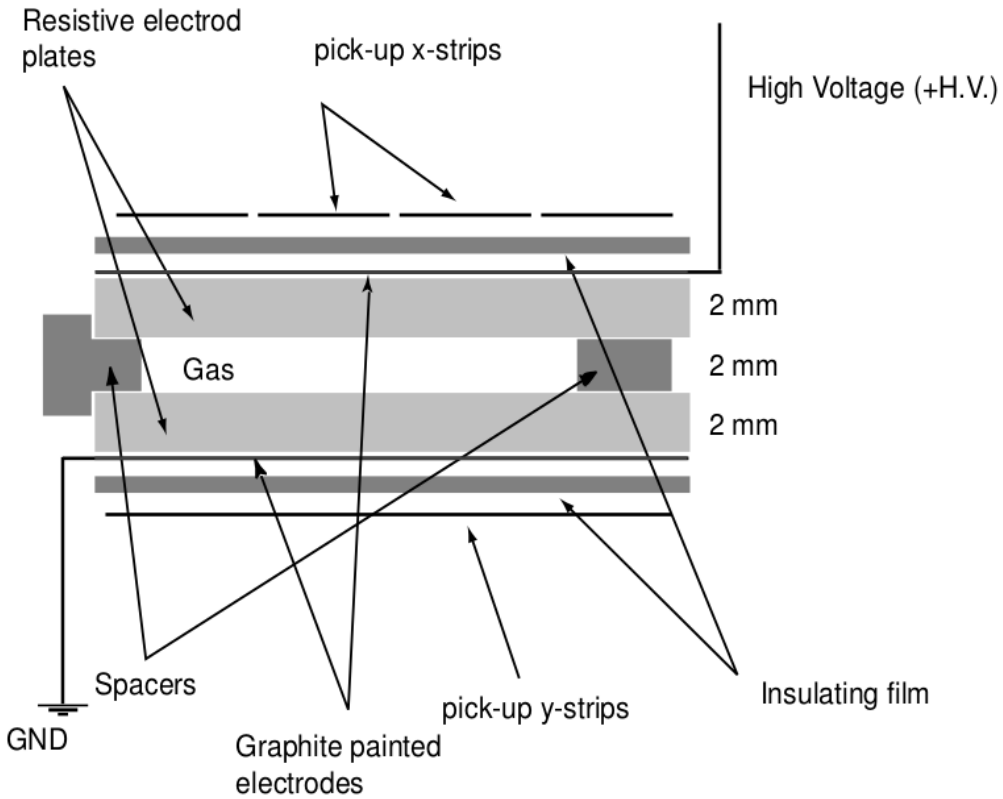
ALICE (A Large Ion Collider Experiment) $\longrightarrow$ heavy-ion collisions (Pb-Pb)



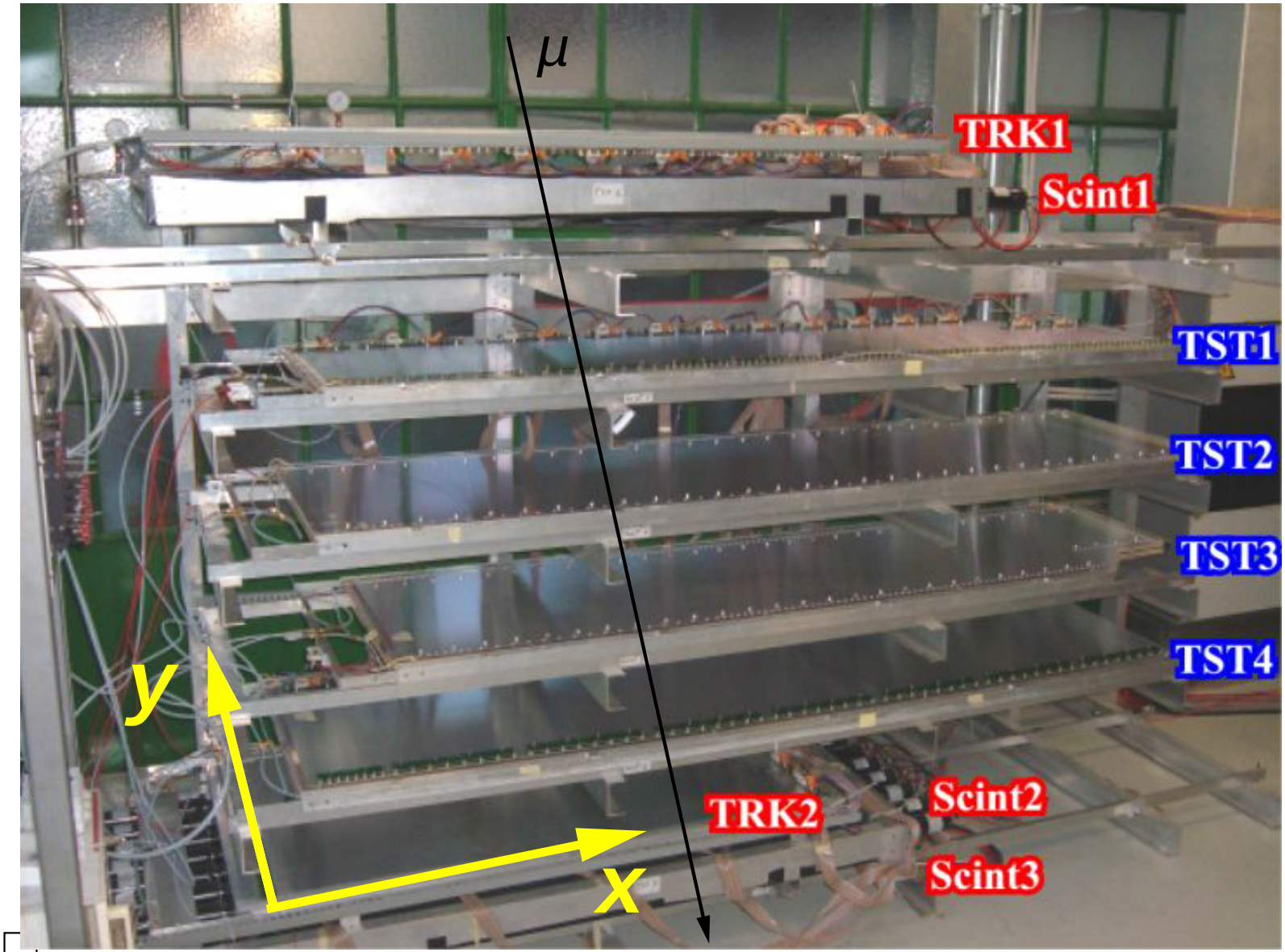
Resistive Plate Chamber (RPC)

- Gaseous single-gap detector
- Parallel plates made out of bakelite ($\rho \simeq 10^{10} \Omega$ cm)
- Area $\sim$ 270 x 70 cm^2
- Gas mixture: 89.7% $C_2H_2F_4$ 10% i-C_4H_{10} 0.3% SF_6
- Strips readout by FE discriminators (V_{th} = 7 mV)





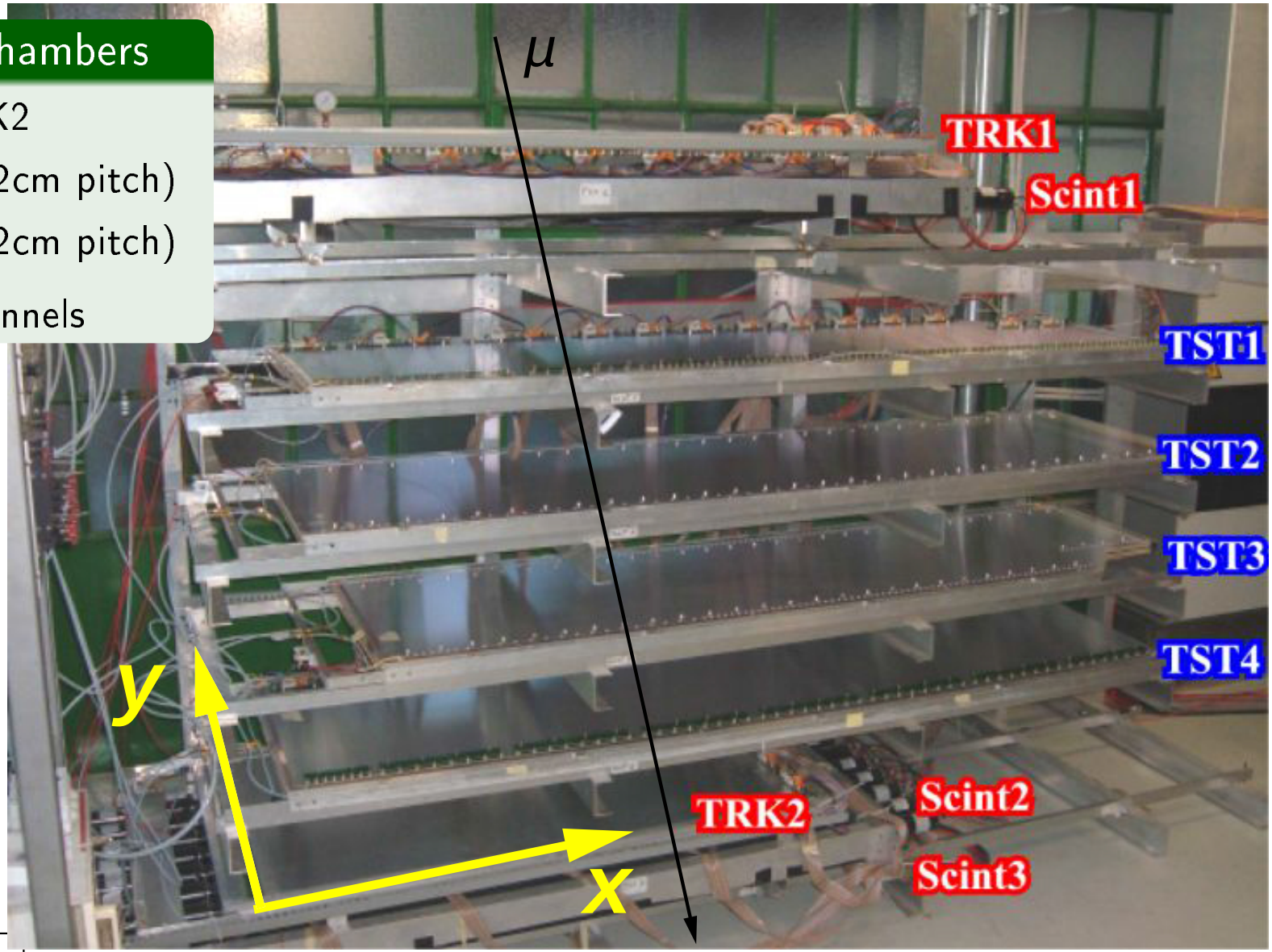
RPC Test Bench Setup



RPC Test Bench Setup

2 Tracking Chambers

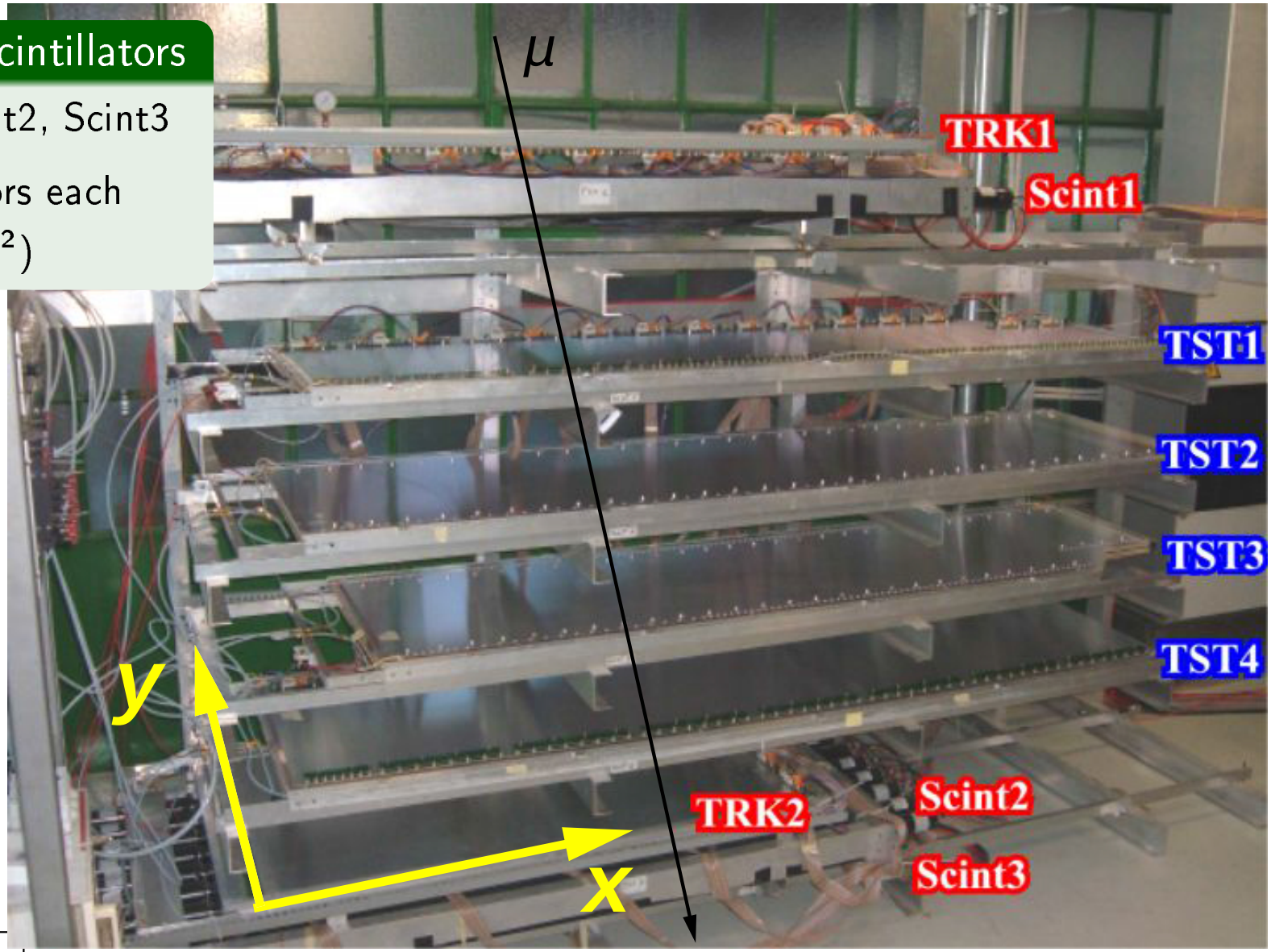
- TRK1, TRK2
- 40 strip x (2cm pitch)
- 72 strip y (2cm pitch)
- 112 x 2 channels



RPC Test Bench Setup

3 planes of Scintillators

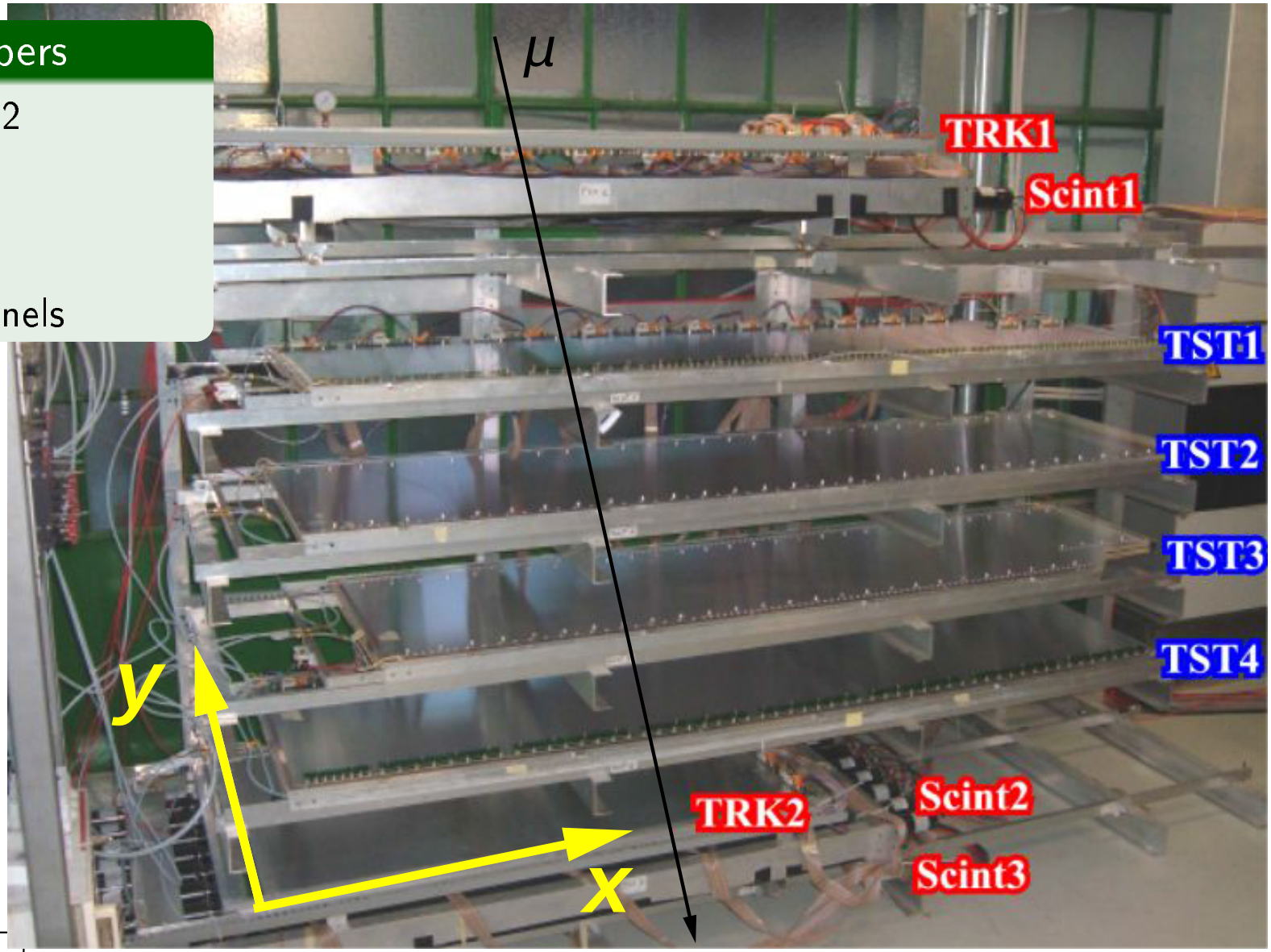
- Scint1, Scint2, Scint3
- 9 Scintillators each (10x150 cm^2)



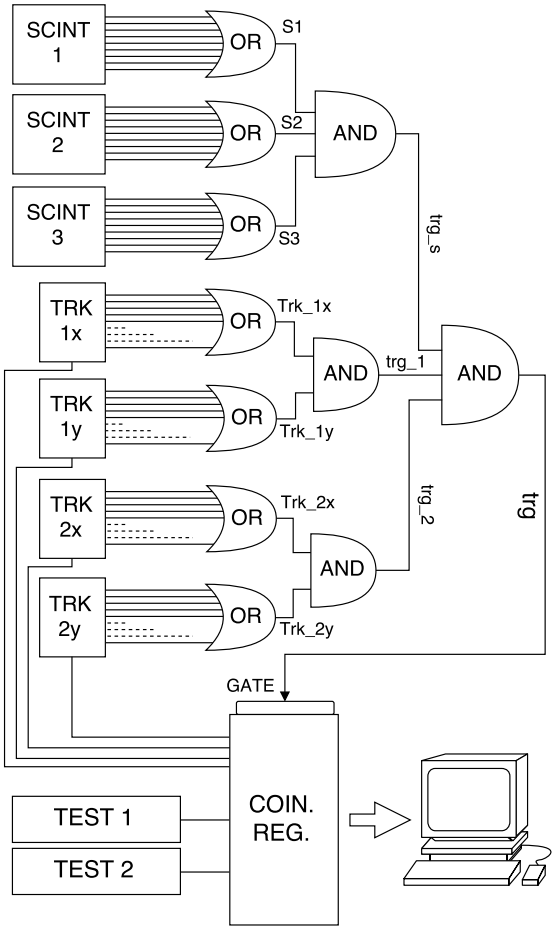
RPC Test Bench Setup

2 Test Chambers

- TST1, TST2
- 16 strip x
- 32 strip y
- 48 x 2 channels



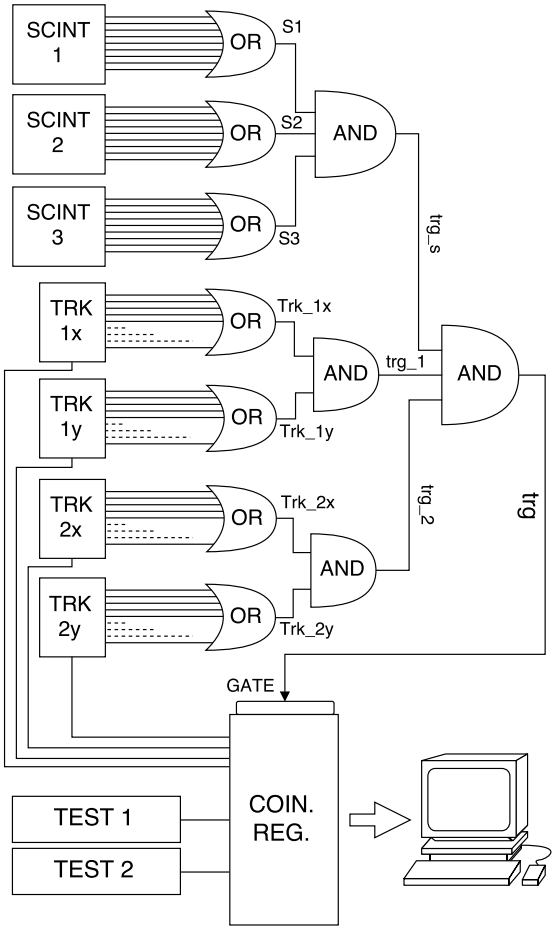
Efficiency Trigger



- global and local efficiency

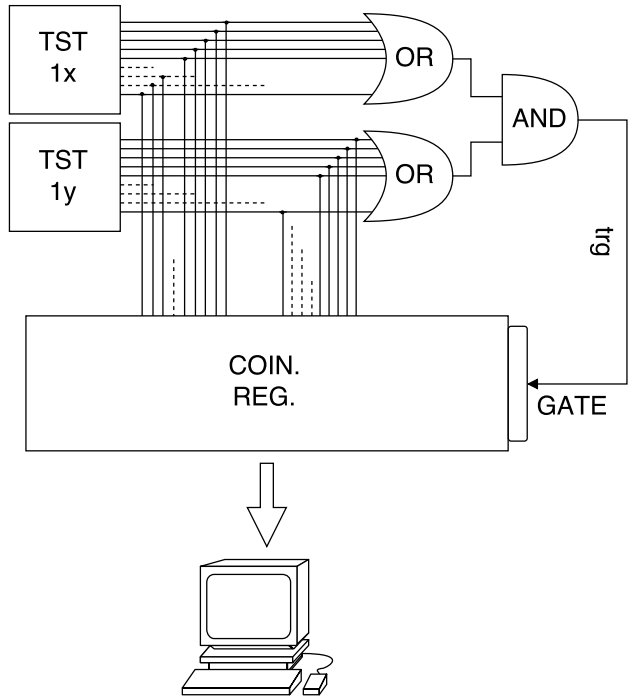
RPC Test Bench Setup

Efficiency Trigger



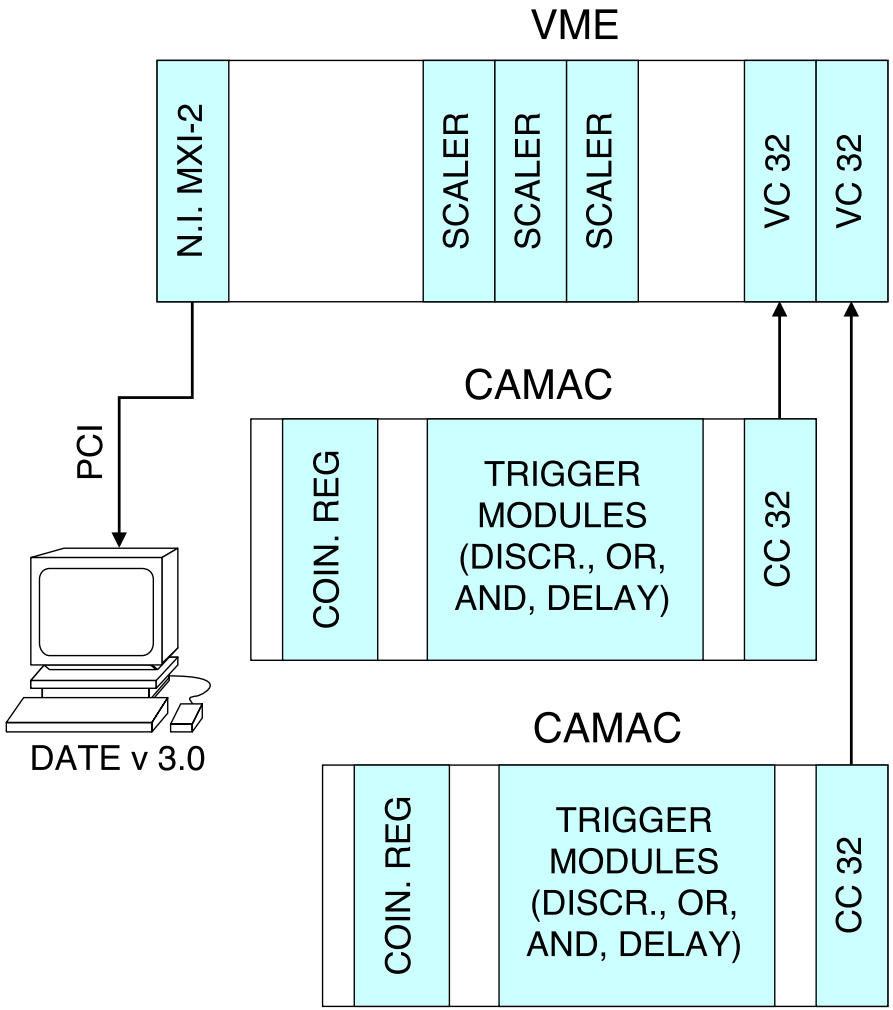
- global and local efficiency

Auto-Trigger

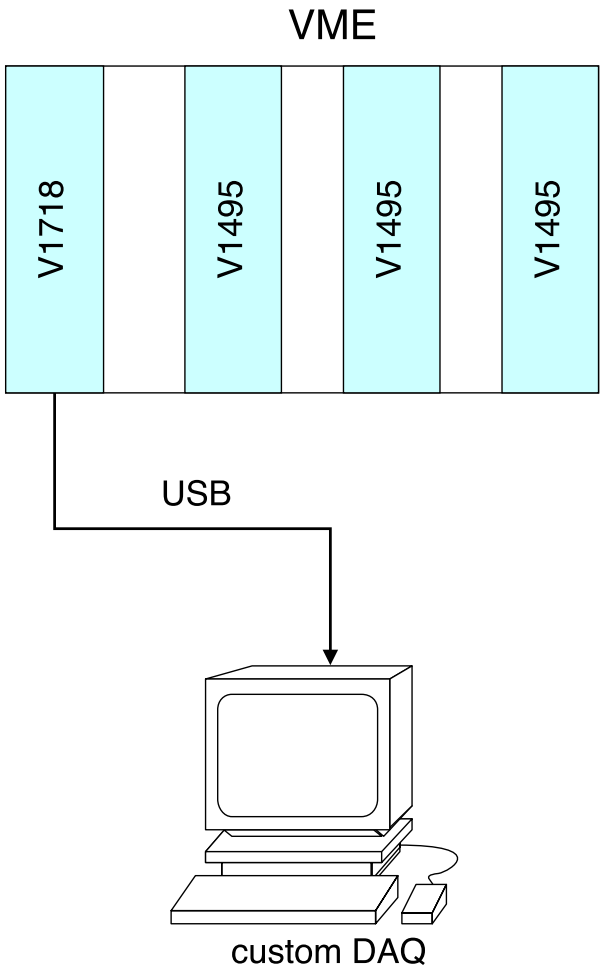


- monitoring background noise
- detecting “hot-spots”

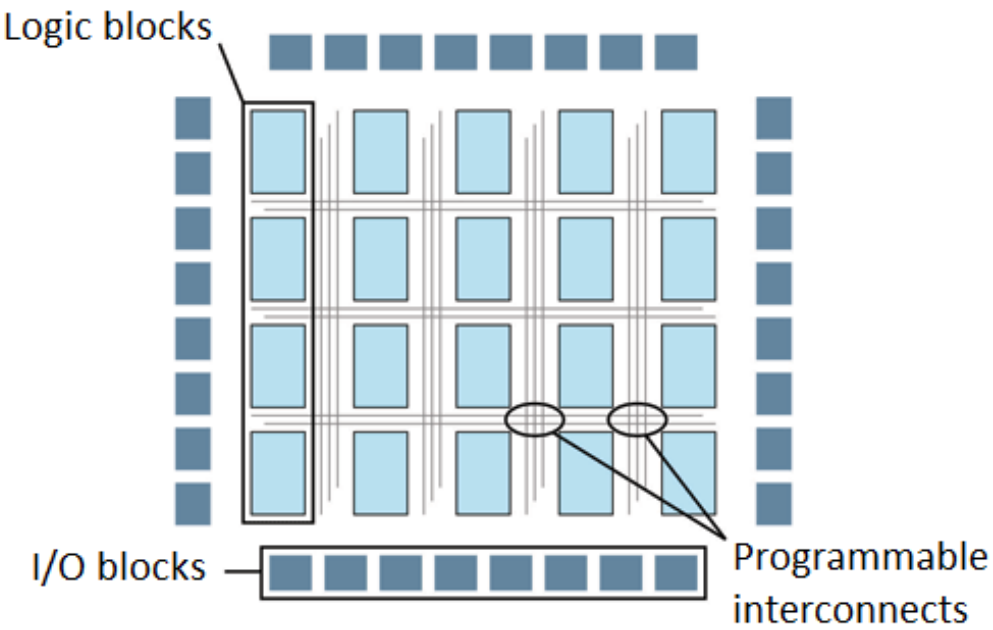
Before the Upgrade...



...After the Upgrade



FPGA (Field Programmable Gate Array)



Integrated circuit designed to be programmed by the user after manufacturing.

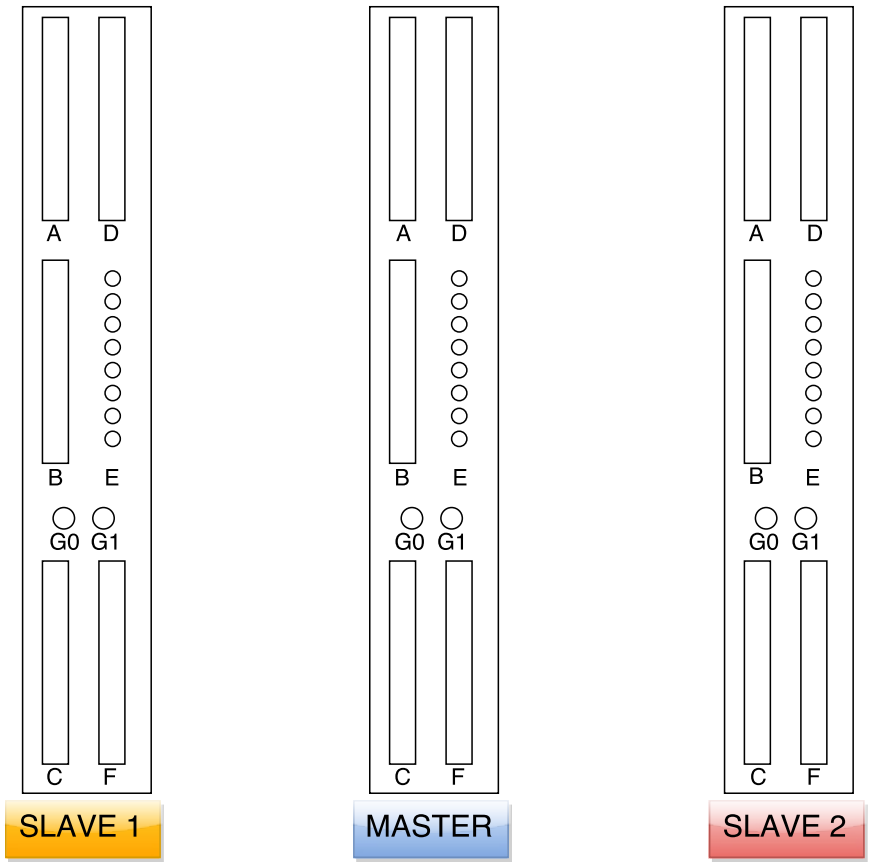
- Very fast custom logic (digital domain)
  - massively parallel operation
  - faster than microprocessors
- Reprogrammable at any time
  - more flexible than dedicated chipsets
  - easy and fast design

User FPGA

- ALTERA Cyclone I EP1C204F400C6
- Programmable with Altera Quartus II software (VHDL)

DAQ System

1. **Trigger**: generate a signal when a muon crosses the test stand
2. **Readout**: store strips hit-pattern data
3. **Scaler**: count pulses coming from RPC channels



320 input channels

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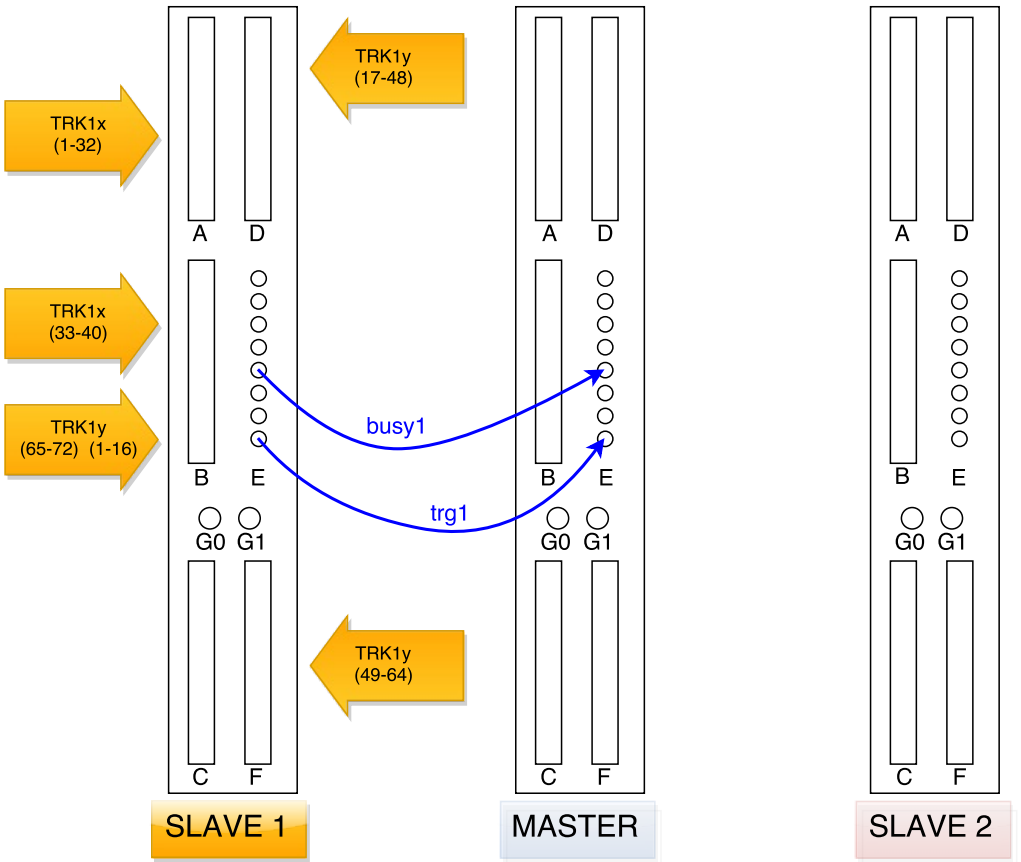

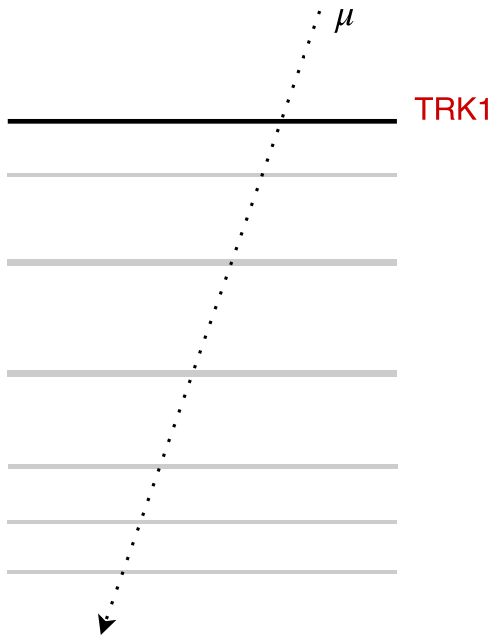

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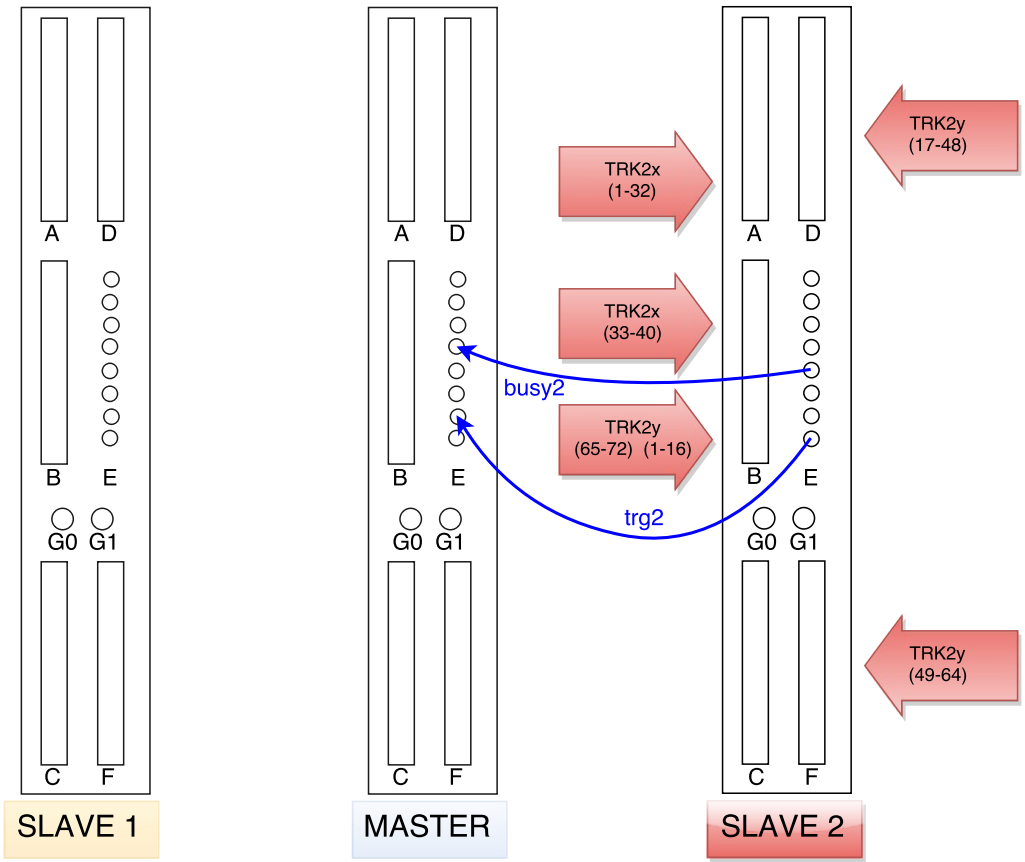

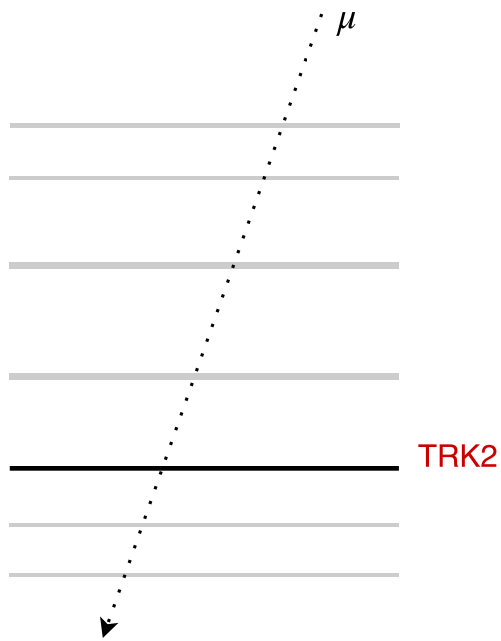

DAQ System

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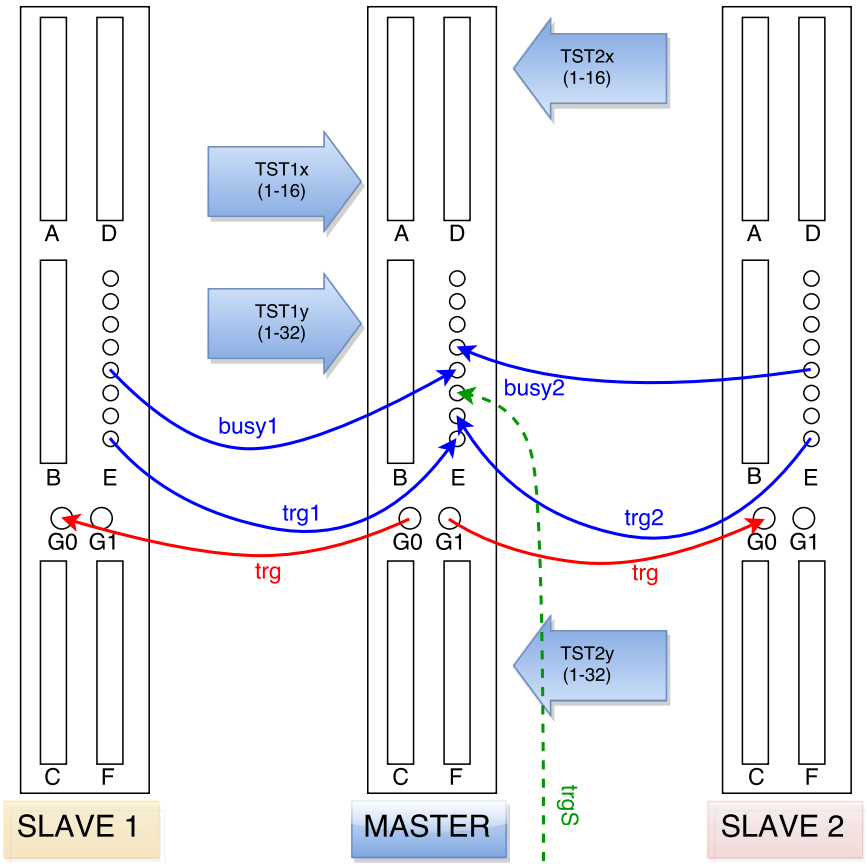

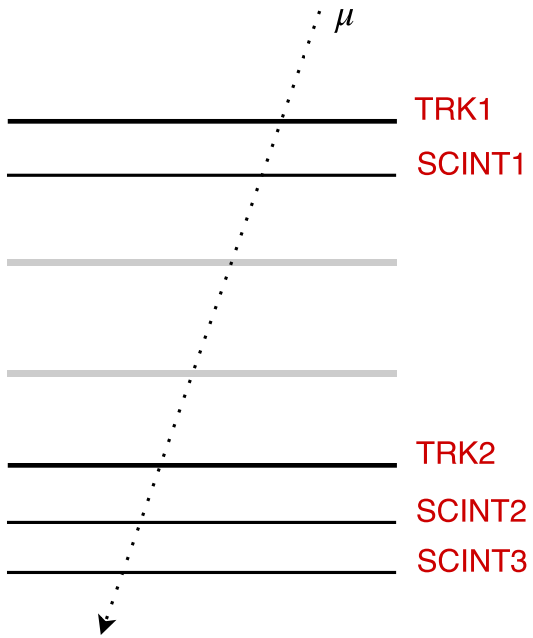

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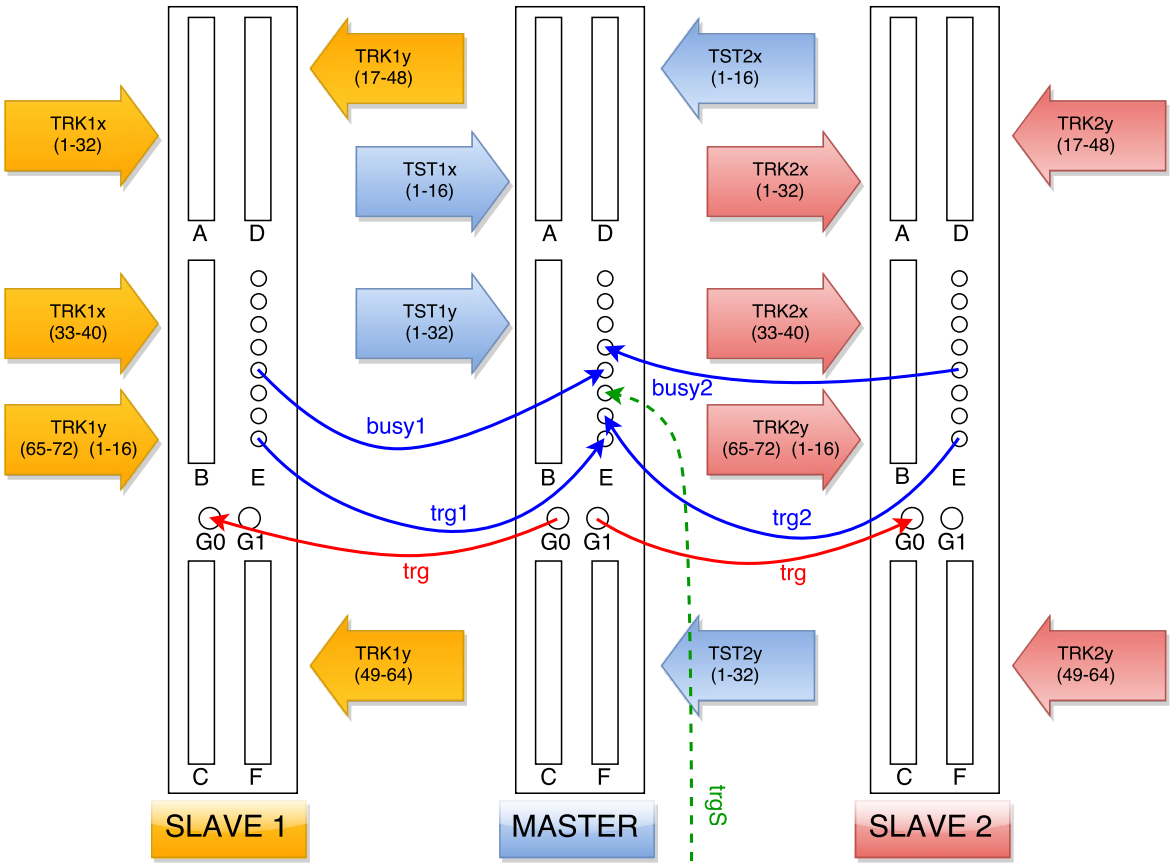
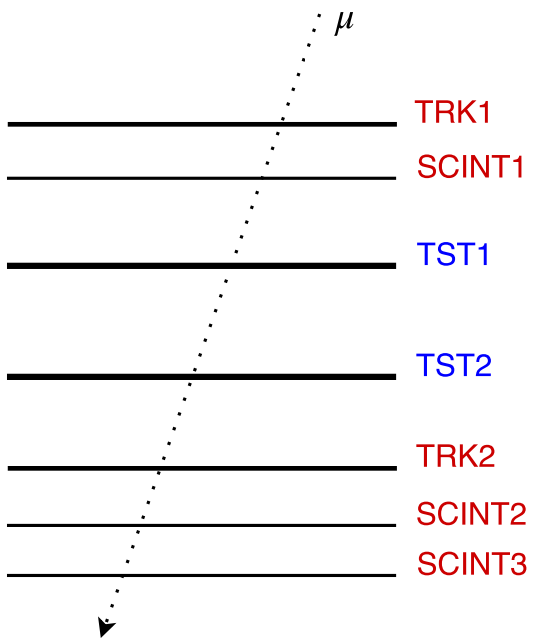
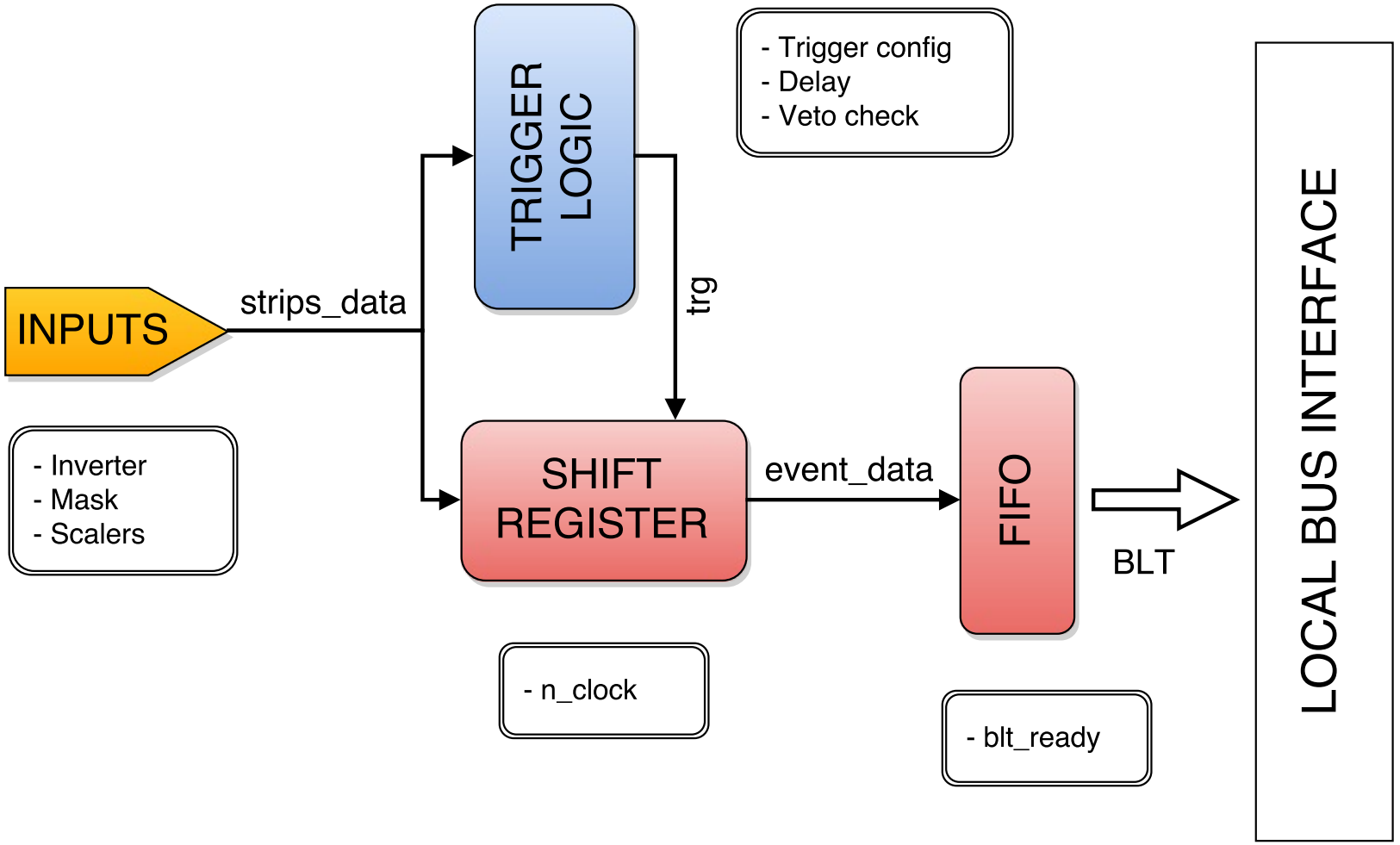




DAQ System



BLock Transfer: $\sim$ 320 ev/s (7.5 kB/s)

DAQ Software

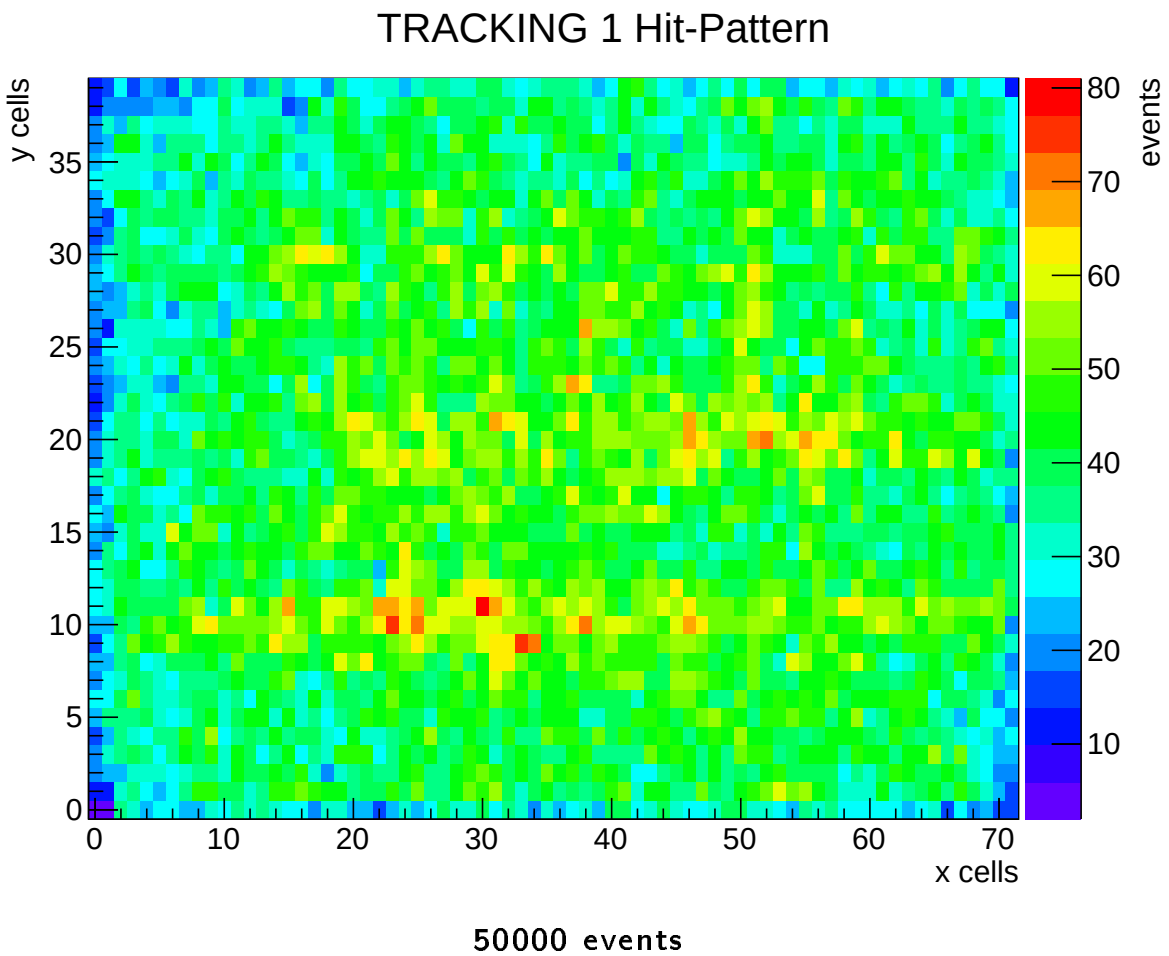
C++ / ROOT acquisition program

Setup

- Write Registers (Mask, Delay, n_clock)
- Start, Stop, Reset control

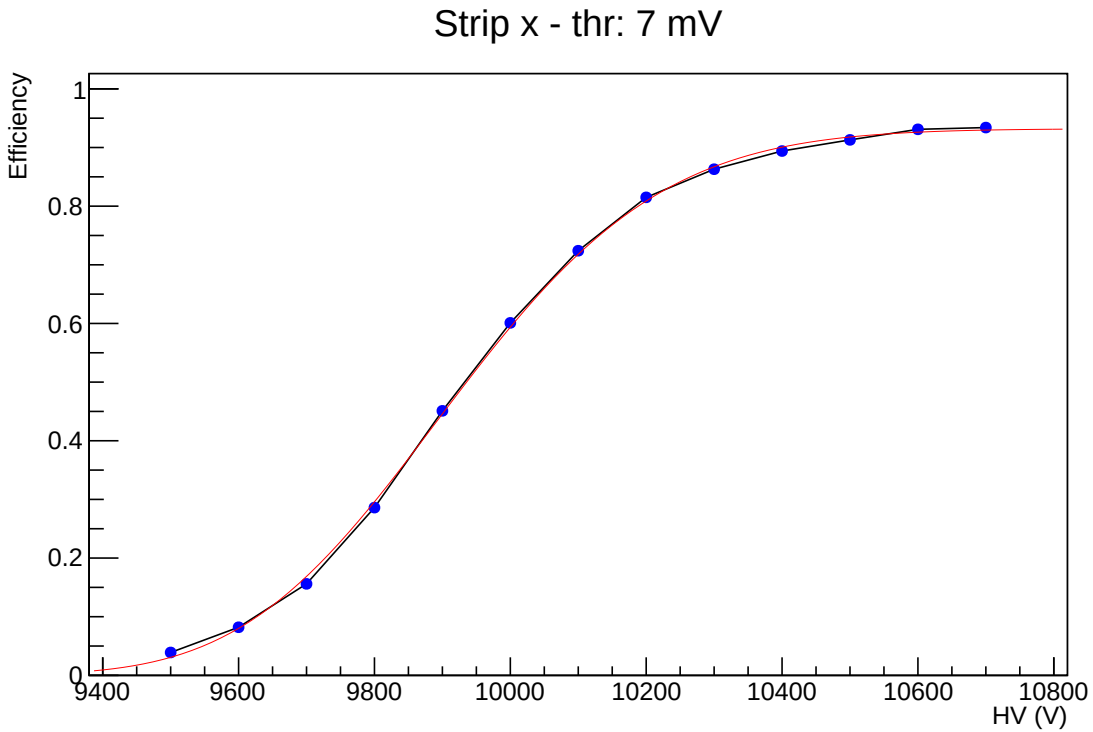
Readout

- Check blt_ready signal
- Block Transfer (BLT)
- Event Building
- ▷ Store Data (bin file)
- ▷ Online histograms



Results

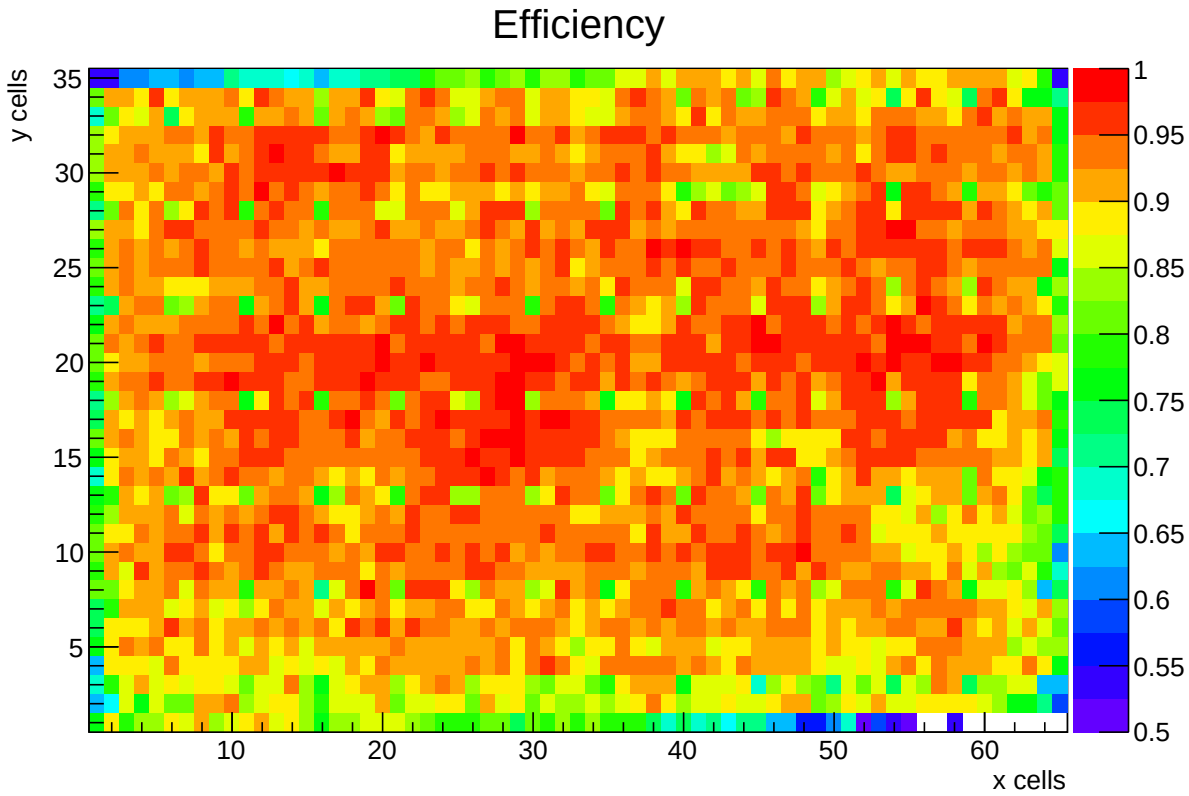
1. HV working point



- HV Scan (20000 events / run)
- ▷ Efficiency plateau at HV = 10700 V

Results

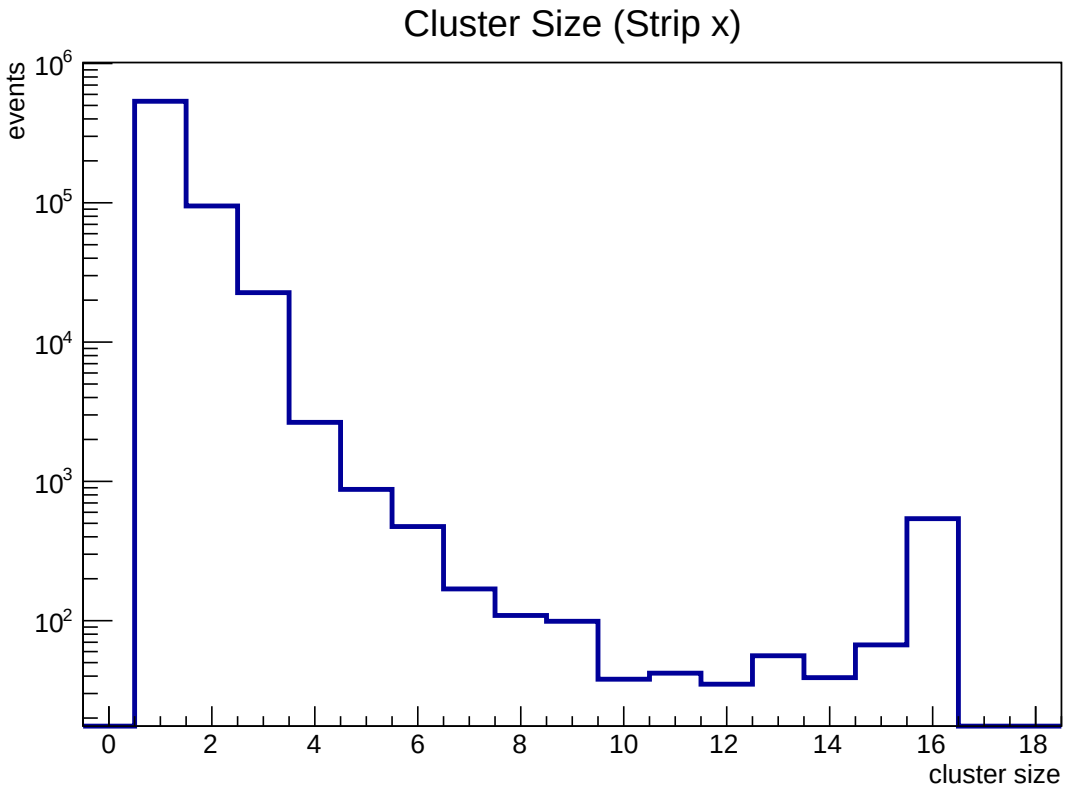
1. HV working point
2. Local Efficiency



- High Statistics run (1000000 events)

Results

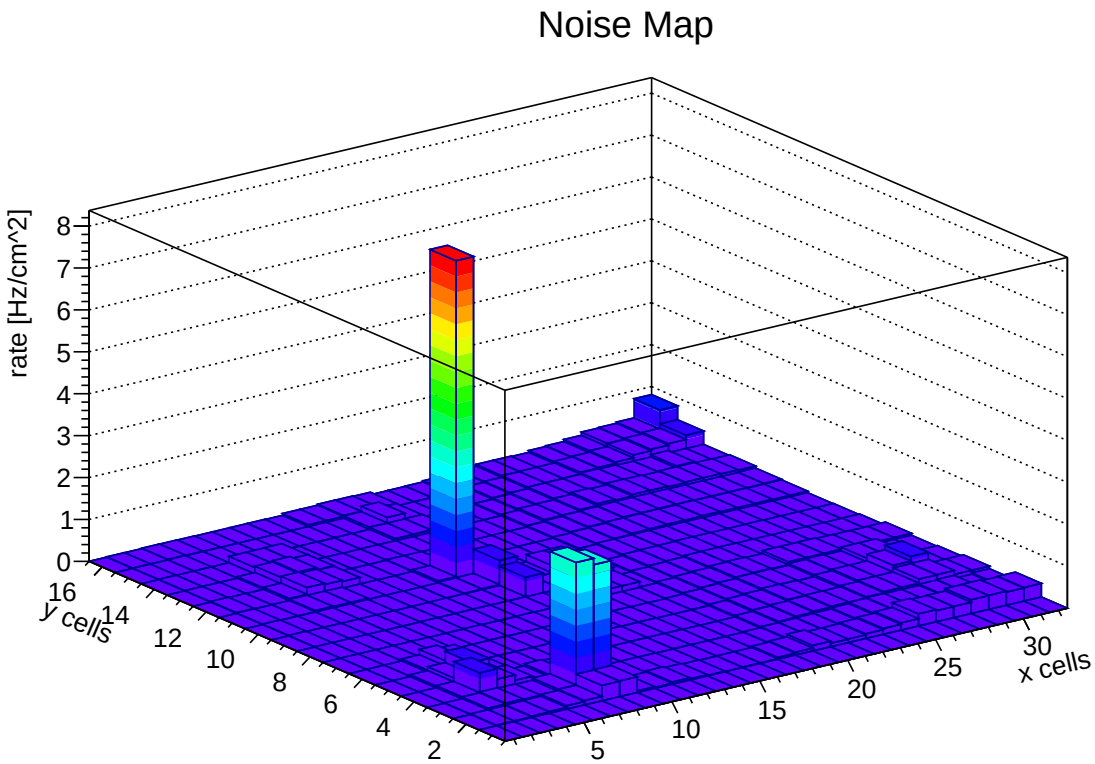
1. HV working point
2. Local Efficiency
3. Cluster Size



- High Statistics run (1000000 events)

Results

1. HV working point
2. Local Efficiency
3. Cluster Size
4. Noise Map



- AutoTrigger run (20000 events)
  - ▷ "Hot-Spot"

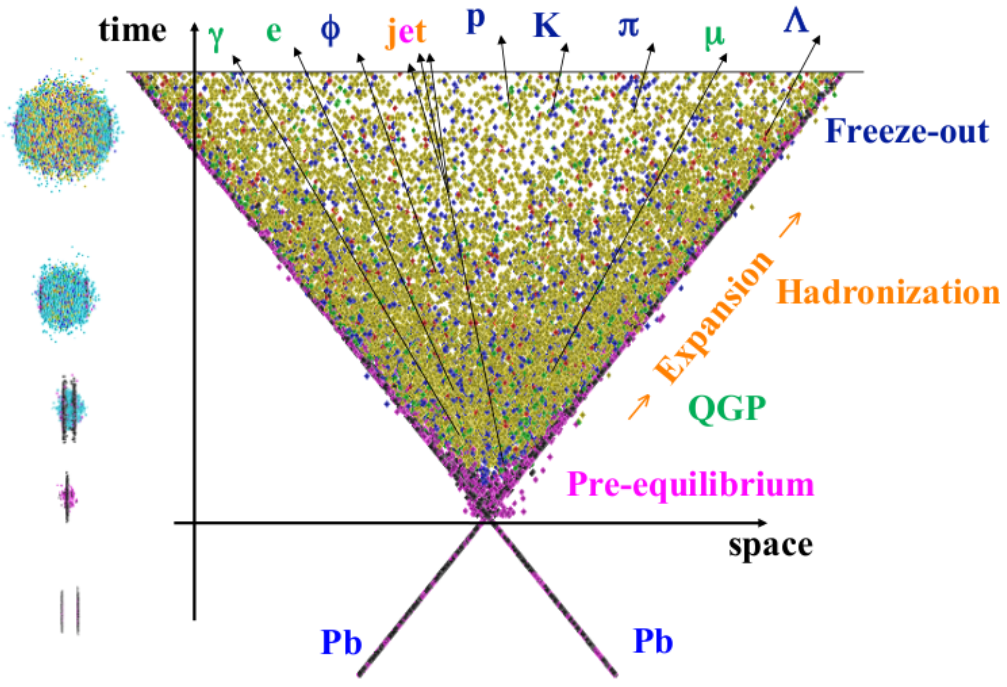
Conclusions

- New Trigger and Readout System successfully developed, integrated and tested.
- Faster (FIFO+BLT) and easily monitored (online histograms).
- Efficiency–AutoTrigger selection easier, simpler and reliable.
- 3 RPCs tested: one already mounted on the ALICE Muon Spectrometer at CERN.

Backup

QGP in heavy-ion collisions

Quark Gluon Plasma is a state of strongly interacting matter in which quarks and gluons are no more confined into hadrons.



QCD predictions:

- $\varepsilon > 1$ GeV/fm^3
- T > 170 MeV

- Heavy Quarkonia: J/Ψ, Ψ', $\Upsilon(1S)$, $\Upsilon(2S)$, $\Upsilon(3S)$
- Open heavy flavours: D and B mesons

} QGP "signatures"

Muon Spectrometer

Study the production of heavy quark resonances via their muonic decay.

Absorbers

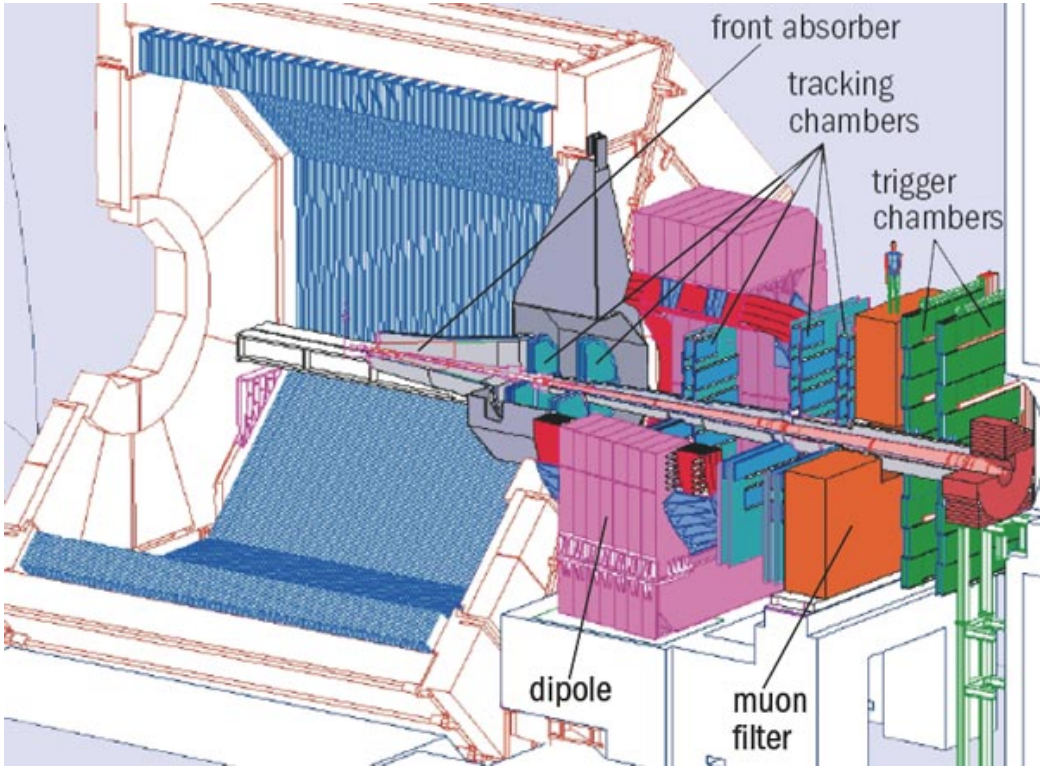
- Front Absorber
- Beam Shielding
- Iron Wall

Muon Tracking System

5 stations of 2 planes of Cathode Pad Chambers (CPC)

Muon Trigger System

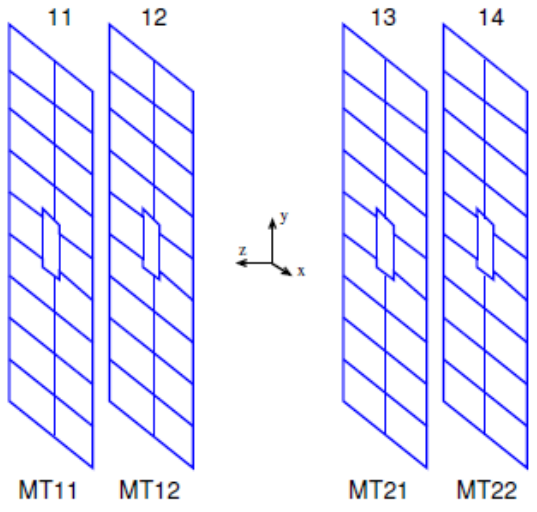
2 stations of 2 planes of **Resistive Plate Chambers (RPC)**

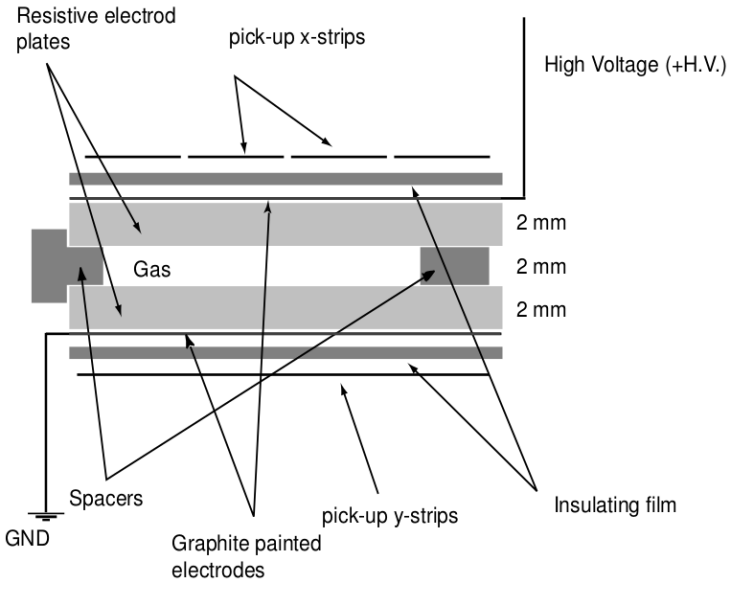


Trigger System

Setup

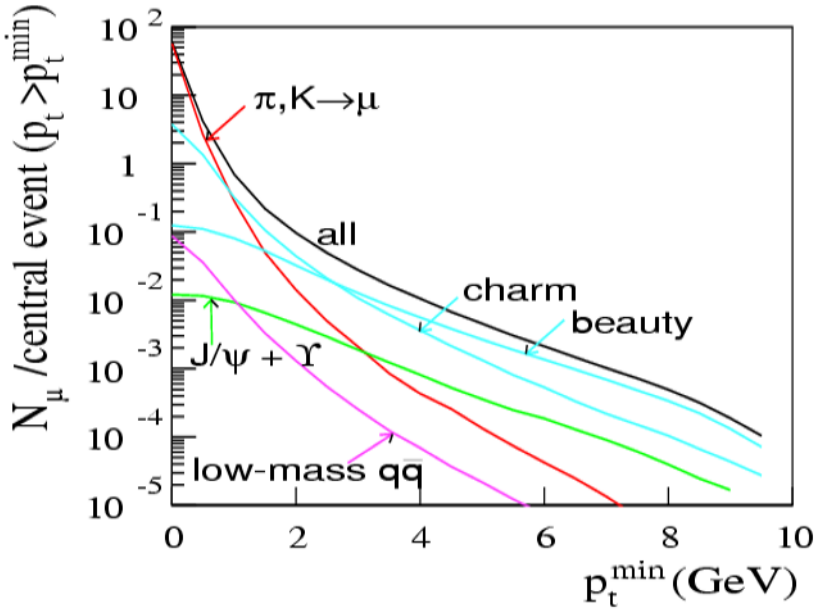
- 4 planes of detector arranged in 2 stations of 2 planes each
- Each plane $\sim 5.5 \times 6.5 m^2$, with $\sim 1.2 \times 1.2 m^2$ central hole (beam pipe and shielding)
- 18 RPCs per plane, read on both sides with orthogonal strips
- 21k strips (1, 2, 4 cm pitch) readout by FE discriminators (LVDS output)
- Projective Geometry: different strip pitch and length on each plane

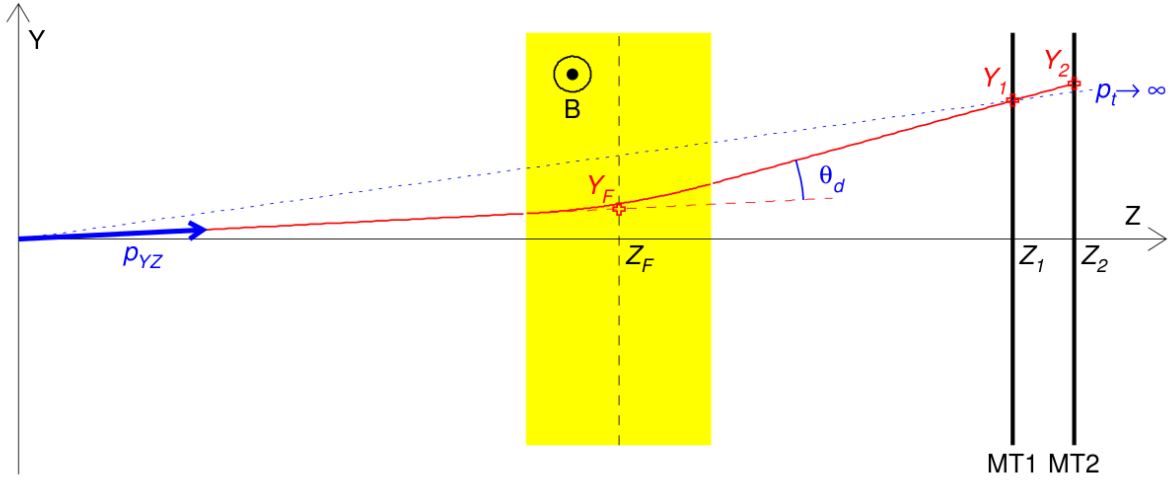




Trigger System

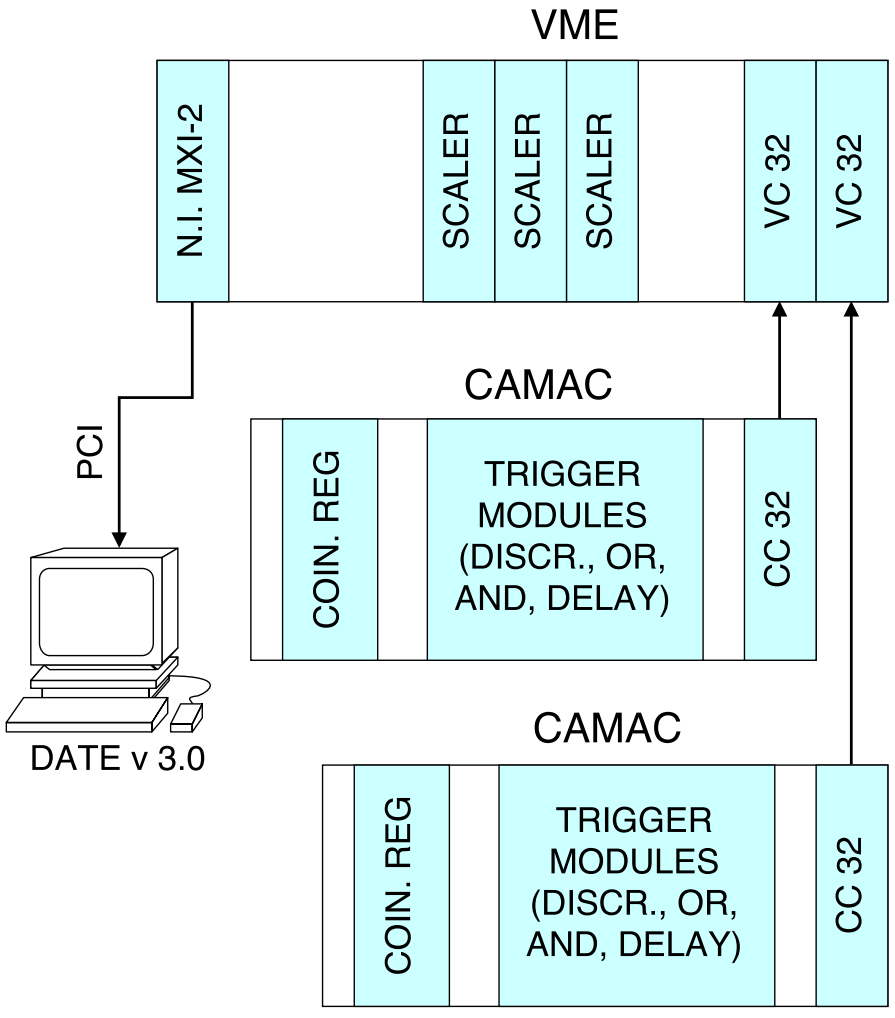
Muon p_t cut to reduce background from light meson decays

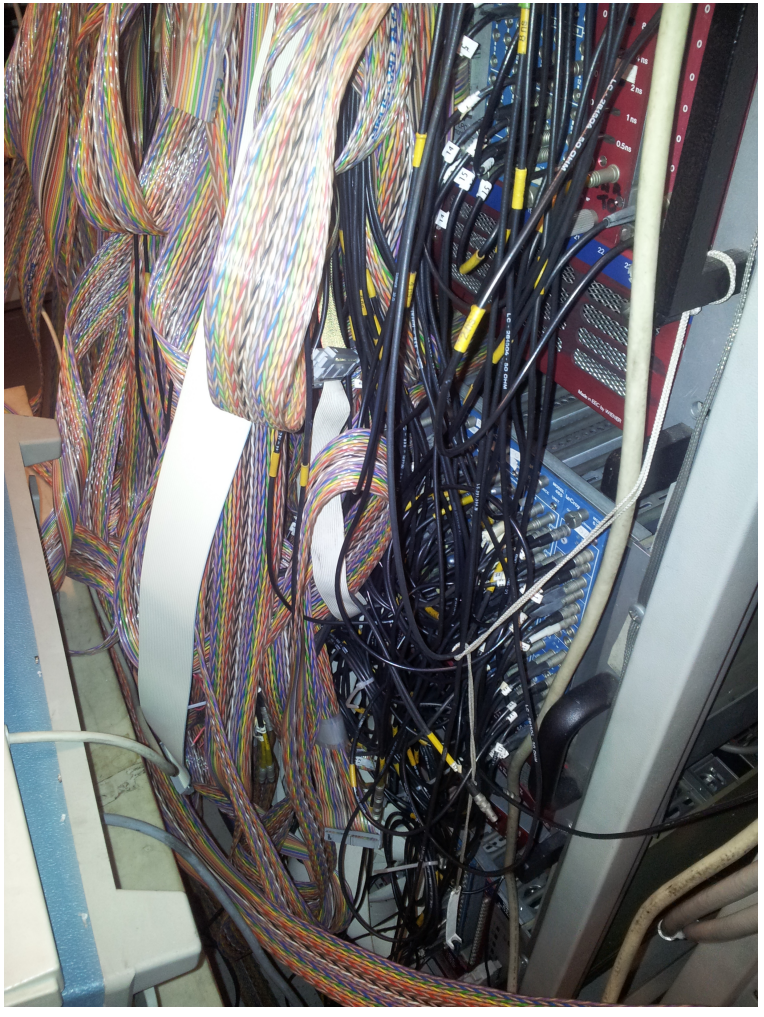




$$\delta y = (Z_2 - Z_1)\frac{eBL}{Z_1}\frac{y_F}{p_t}$$

Before the Upgrade...





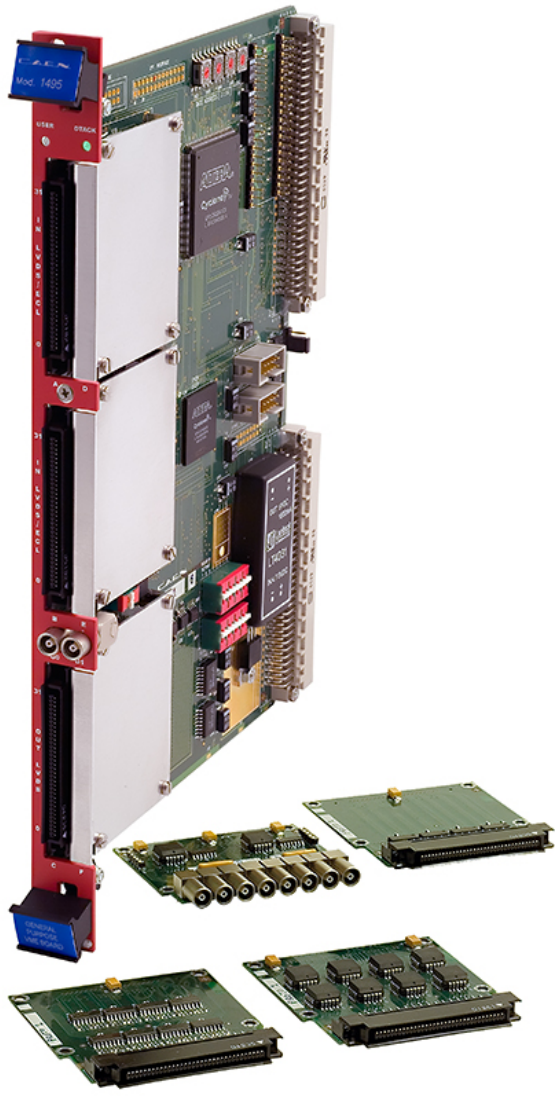
V1495

Specifications

- VME 6U board, 1U wide
- I/O Channels: support for NIM, TTL, ECL, and **LVDS**
- Internal **Clock** = 40 MHz (default)
- 405 MHz maximum frequency support for PLL (Phase-Locked Loops) synthesis
- **User** and Bridge **FPGAs** (Field Programmable Gate Array)

I/O Interface

- ▷ 64 dedicated differential LVDS, ECL inputs (A, B)
- ▷ 32 dedicated LVDS outputs (C)
- ▷ 2 bidirectional NIM, TTL ports (G)
- ▷ 3 optional expansion card module slots (D, E, F)



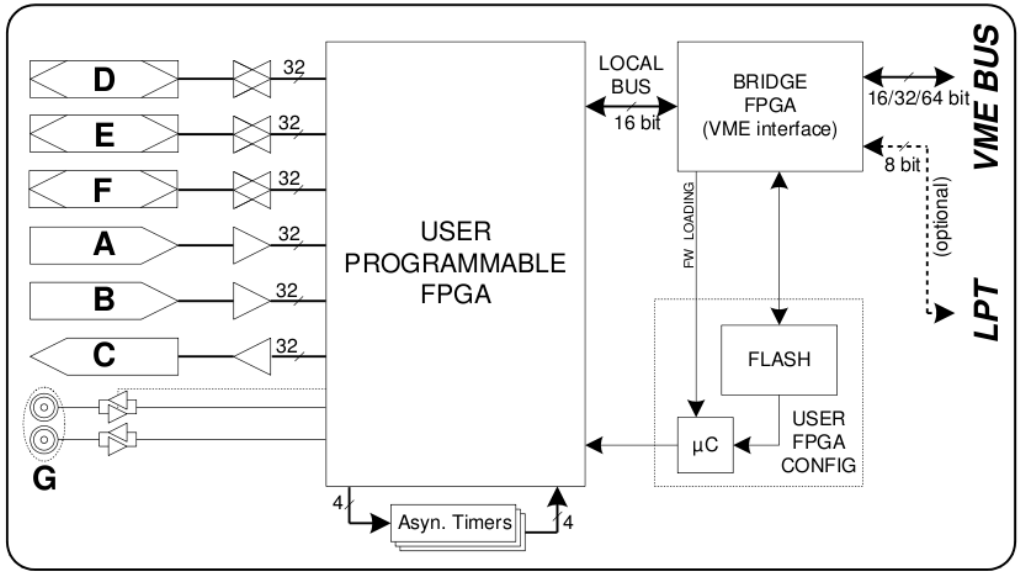
Programming V1495

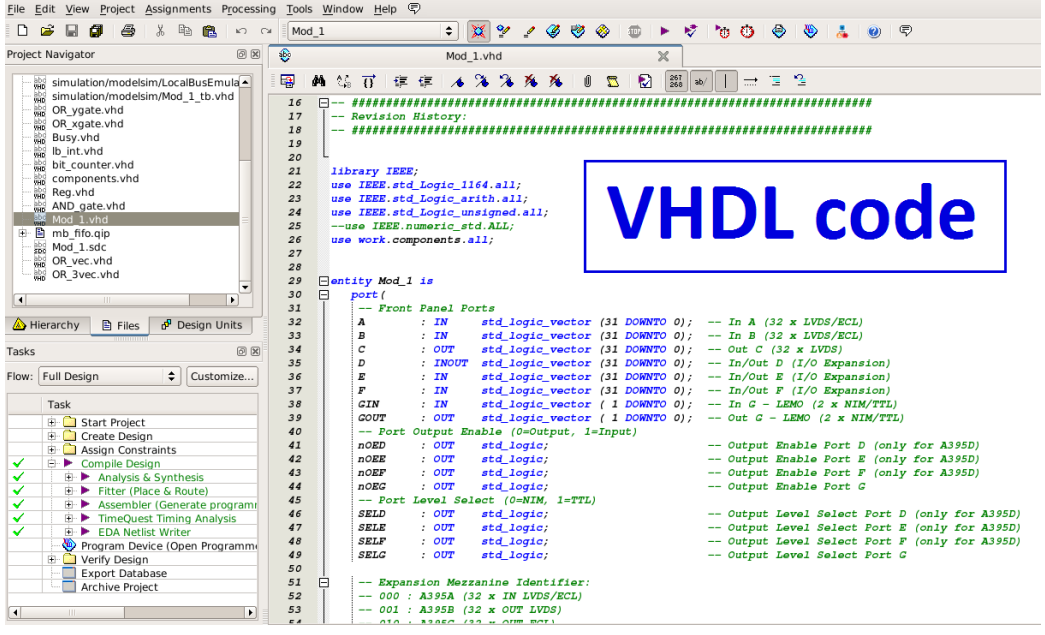
User FPGA:
ALTERA Cyclone I
EP1C204F400C6

Programmable with Altera Quartus II software:

1. Analysis & Synthesis
2. (Simulation)
3. Place & Route
4. Assembler
5. Timing Analysis

VHDL = VHSIC Hardware Description Language





Synchronous circuits

Clock based design

All logic elements are synchronized with a clock signal allowing them to simultaneously perform their intended function.

- input signals width = 20 ns

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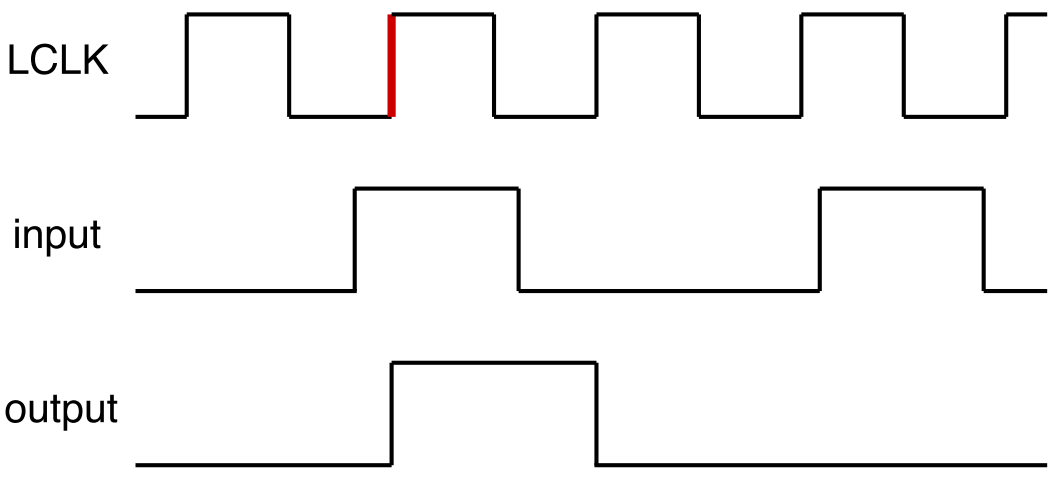

Positive-edge-triggered circuit

- input signals width = 20 ns

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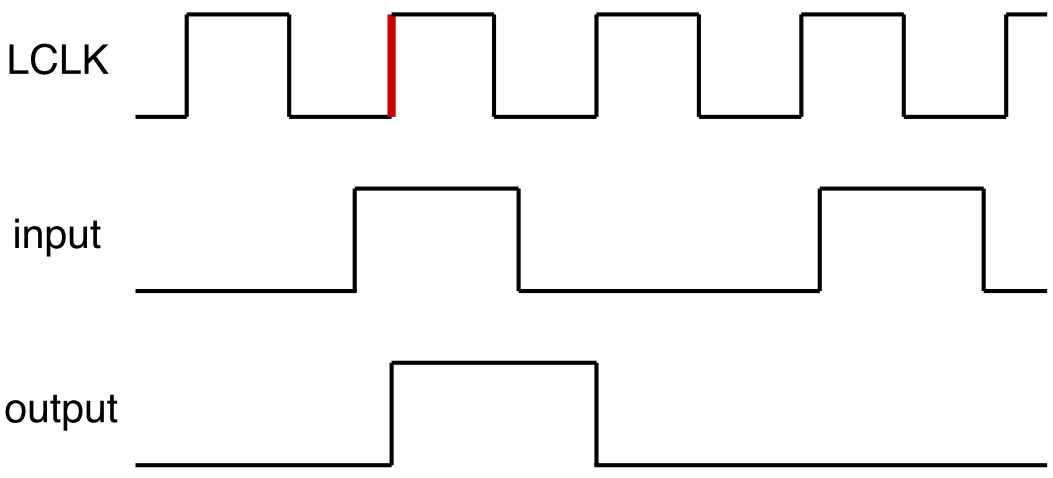

Positive-edge-triggered circuit

- $T_{LCLK} = 25$ ns
- input signals width $= 20$ ns

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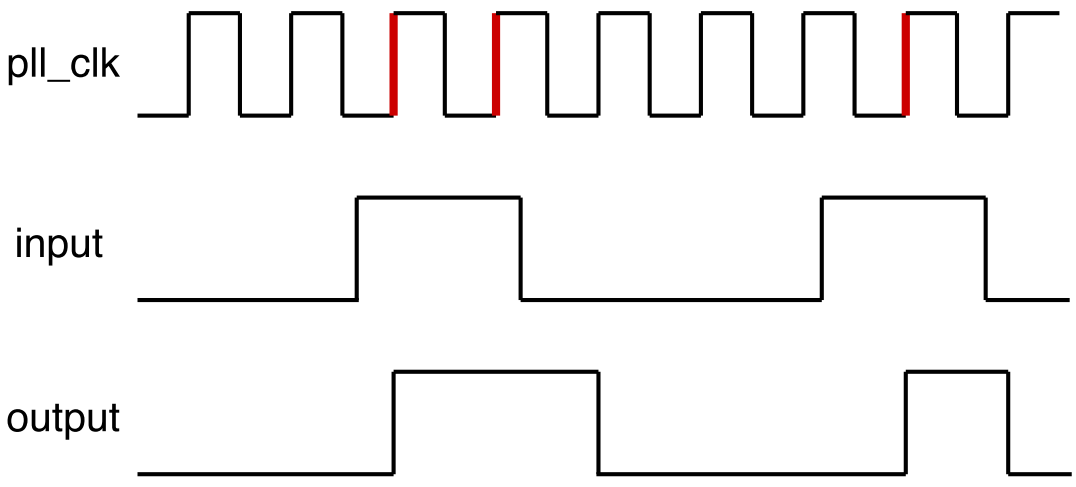
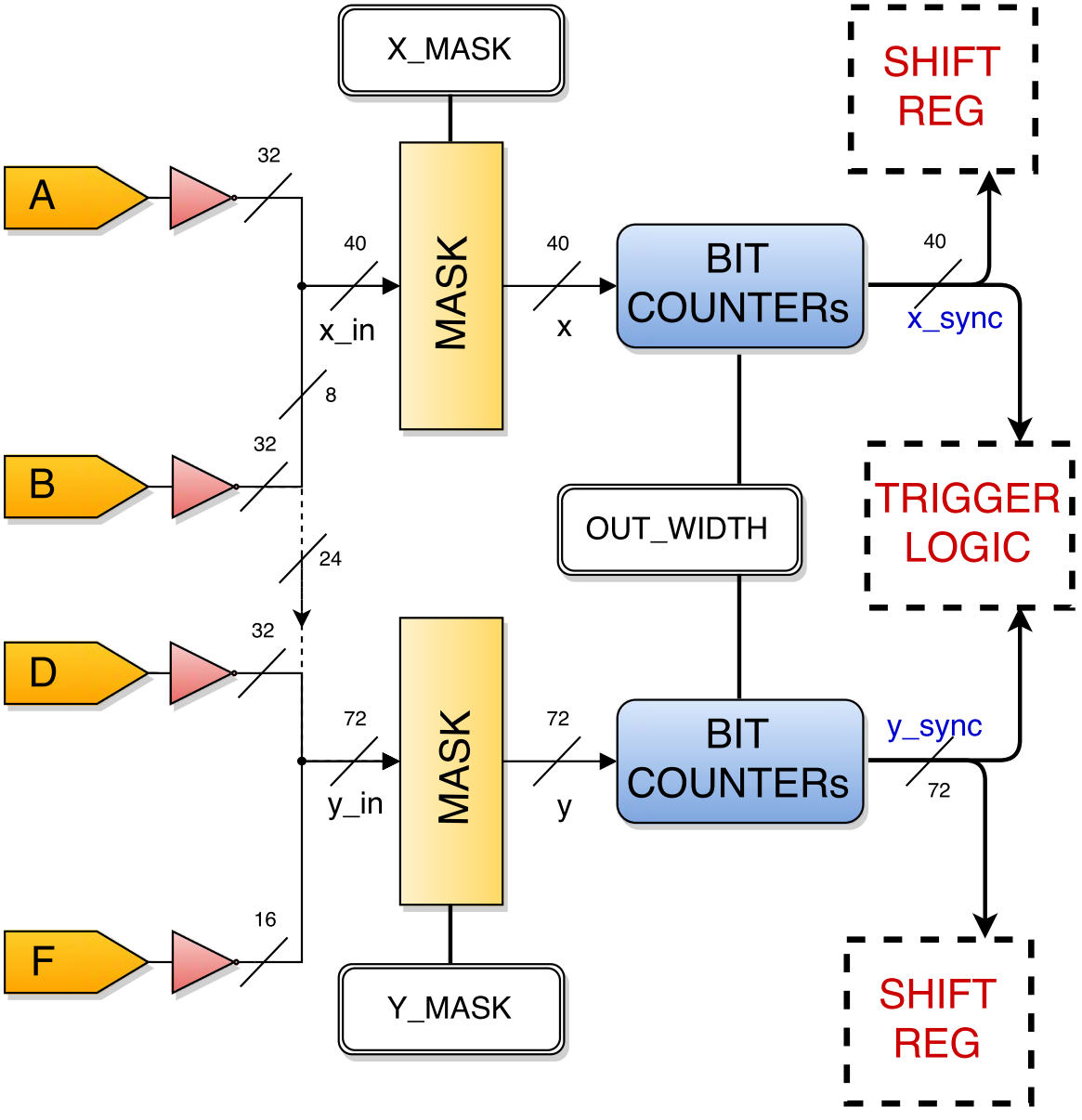


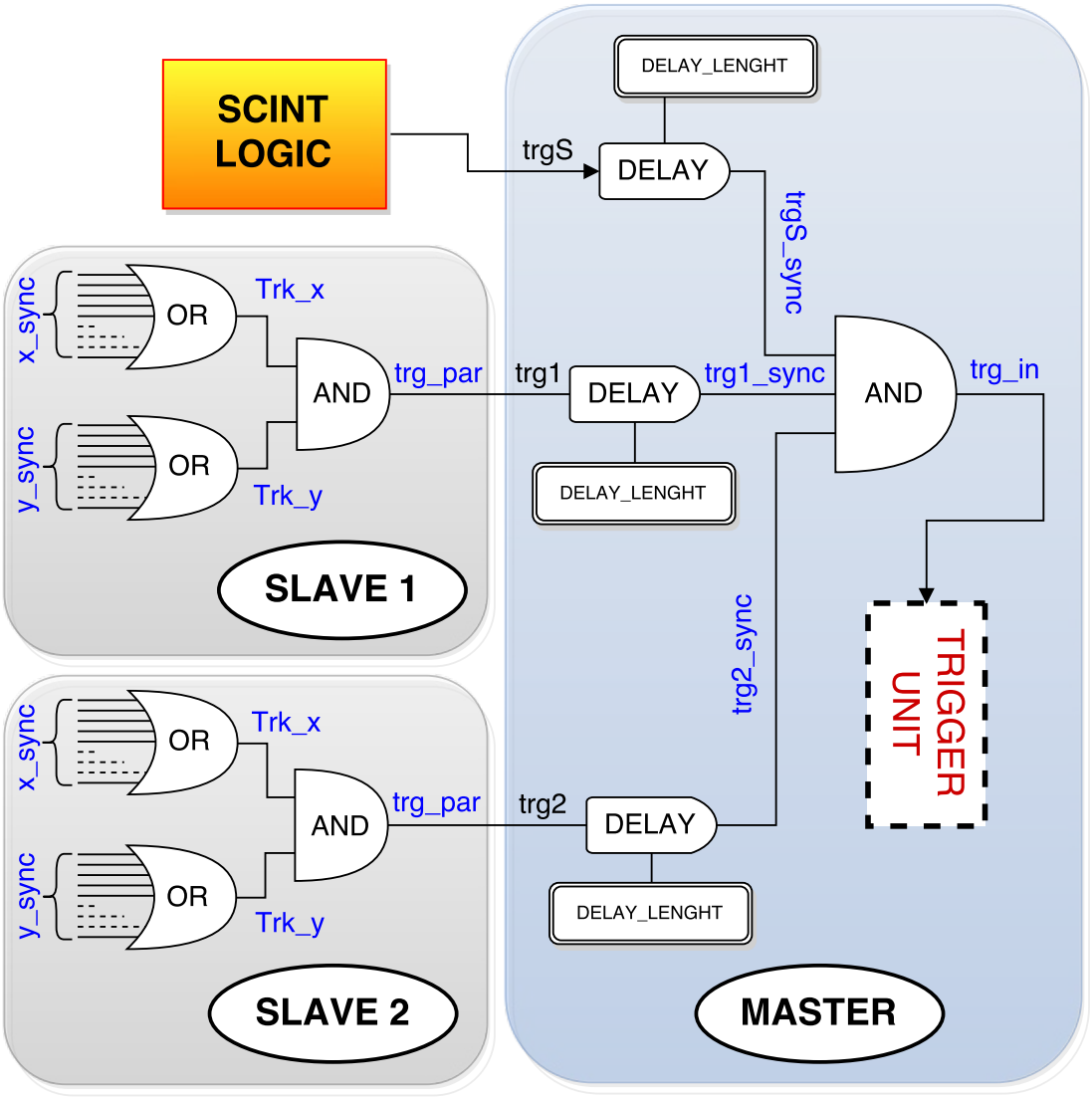
Positive-edge-triggered circuit

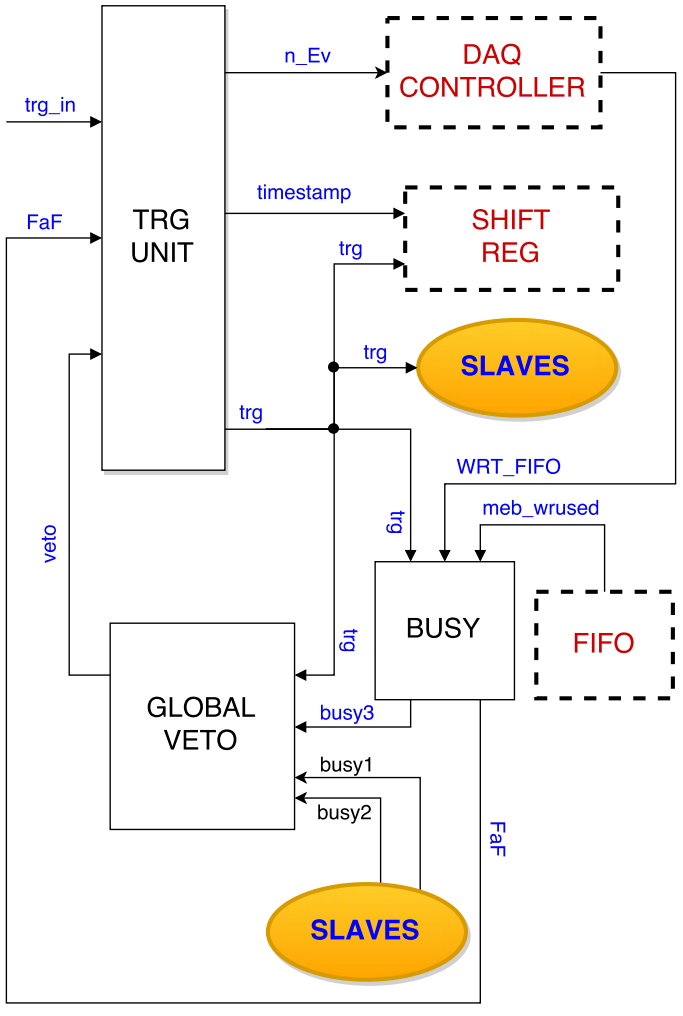
- pll_clk $\longrightarrow$ T = 12.5 ns
- input signals width = 20 ns

SLAVEs input stage

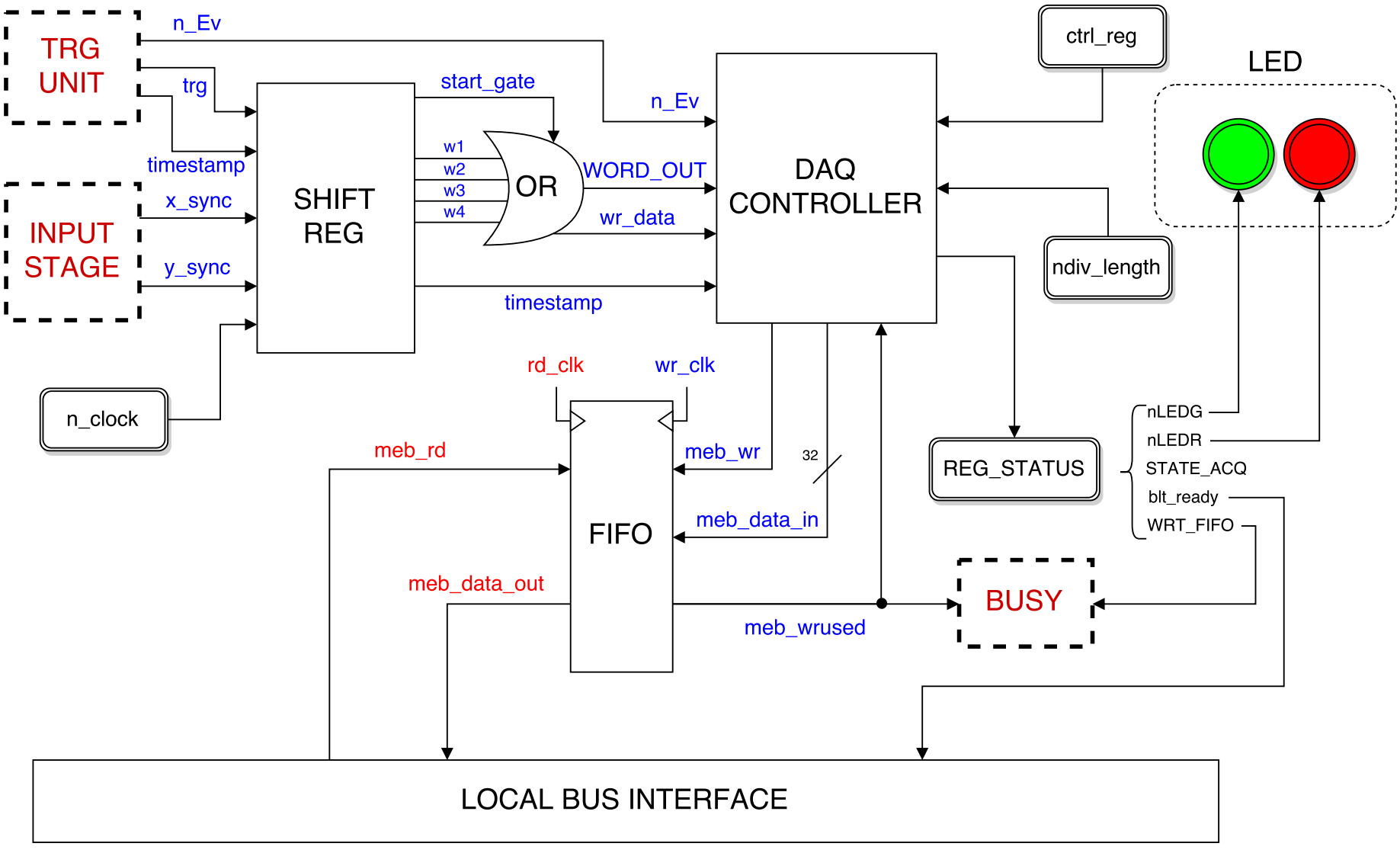


Trigger Logic

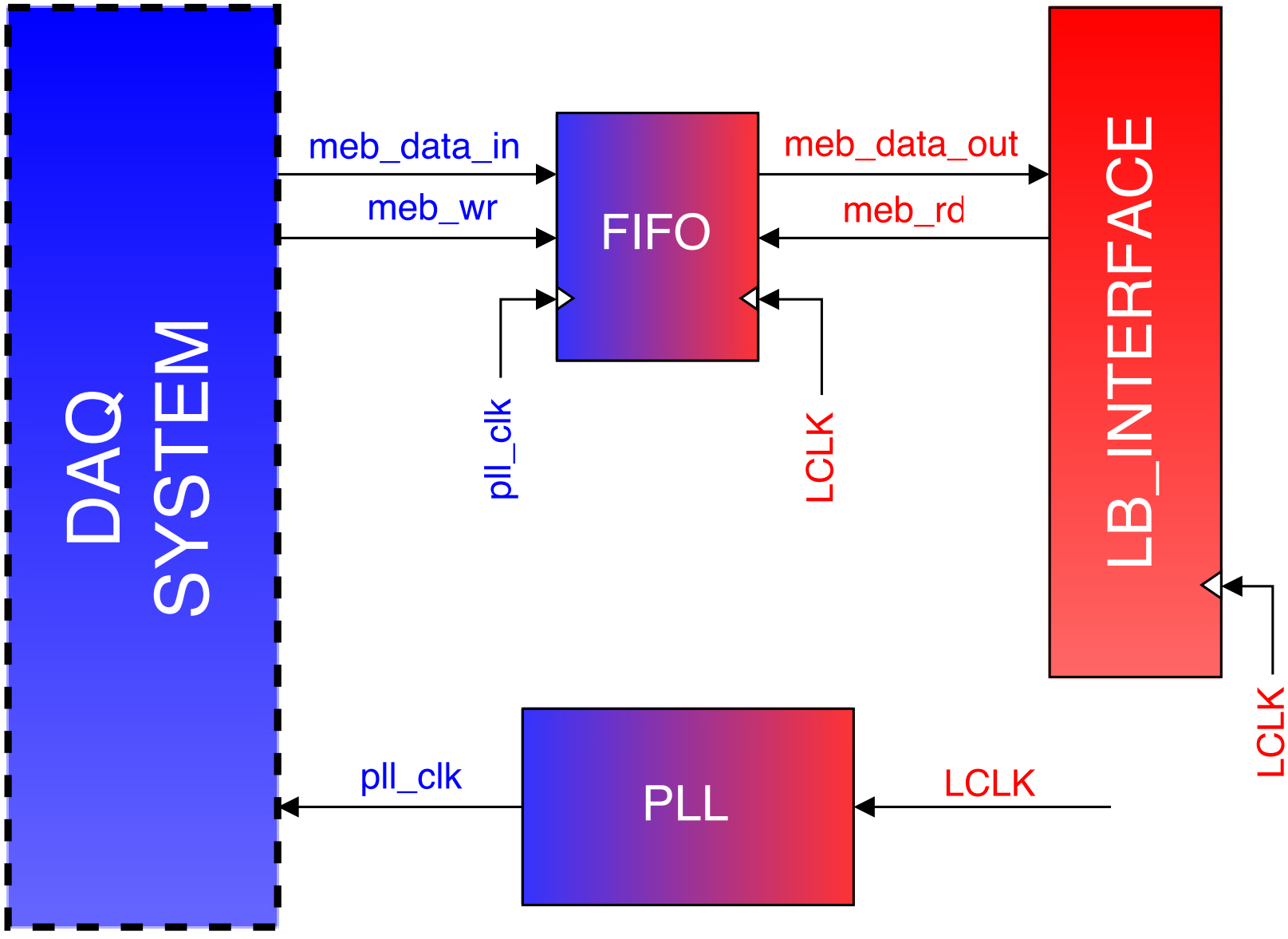




Data storing



Local Bus Interface



FIFO

First-In First-Out memory to store events data and make them available for a BLock Transfer (BLT) Read Access:

- 4096 x 32bit words
- Address = `base + 0x0000`
- Independent Read and Write lines $\longrightarrow$ **reduce dead time**
- Control signals:
  - meb_wrfull
  - meb_rdempty
  - meb_wrused