Upgrade del sistema di trigger e readout per la stazione di test delle camere RPC di ALICE

F. Cossio (Università degli Studi di Torino - INFN Torino)



Roma, 25 Settembre 2015

The ALICE Experiment

ALICE (A Large Ion Collider Experiment) \rightarrow heavy-ion collisions (Pb-Pb)



Resistive Plate Chamber (RPC)

- Gaseous single-gap detector
- Parallel plates made out of bakelite ($\rho \simeq 10^{10} \Omega$ cm)
- Area $\sim 270 \times 70 \text{ cm}^2$
- Gas mixture: 89.7% C₂H₂F₄ 10% i-C₄H₁₀ 0.3% SF₆
- Strips readout by FE discriminators ($V_{th} = 7 \text{ mV}$)





2 Tracking Chambers

- TRK1, TRK2
- 40 strip x (2cm pitch)
- 72 strip y (2cm pitch)
- 112 x 2 channels



3 planes of Scintillators

- Scint1, Scint2, Scint3
- 9 Scintillators each (10x150 cm²)



2 Test Chambers

- TST1, TST2
- 16 strip x
- 32 strip y
- 48 x 2 channels



Efficiency Trigger



▷ global and local efficiency

Efficiency Trigger



Auto-Trigger



- monitoring background noise
- ▷ detecting "hot-spots"

 \triangleright global and local efficiency

Before the Upgrade...





...After the Upgrade

VME





FPGA (Field Programmable Gate Array)



Integrated circuit designed to be programmed by the user after manufacturing.

- Very fast custom logic (digital domain)
 - massively parallel operation
 - faster than microprocessors
- Reprogrammable at any time
 - more flexible than dedicated chipsets
 - easy and fast design

User FPGA

- ALTERA Cyclone I EP1C204F400C6
- Programmable with Altera Quartus II software (VHDL)

- 1. Trigger: generate a signal when a muon crosses the test stand
- 2. Readout: store strips hit-pattern data
- 3. Scaler: count pulses coming from RPC channels



320 input channels

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BLock Transfer: \sim 320 ev/s (7.5 kB/s)

F. Cossio

101° Congresso Nazionale

DAQ Software

C++ / ROOT acquisition program

Setup

- Write Registers (Mask, Delay, n_clock)
- Start, Stop, Reset control

Readout

- Check blt_ready signal
- Block Transfer (BLT)
- Event Building
- Store Data (bin file)
- ▷ Online histograms

TRACKING 1 Hit-Pattern



50000 events





1. HV working point

2. Local Efficiency

• High Statistics run (1000000 events)



High Statistics run (1000000 events) •

- 1. HV working point
- 2. Local Efficiency
- 3. Cluster Size
- 4. Noise Map



- AutoTrigger run (20000 events)
- ⊳ "Hot-Spot"

- New Trigger and Readout System successfully developed, integrated and tested.
- Faster (FIFO+BLT) and easily monitored (online histograms).
- Efficiency-AutoTrigger selection easier, simpler and reliable.
- 3 RPCs tested: one already mounted on the ALICE Muon Spectrometer at CERN.

Backup

QGP in heavy-ion collisions

Quark Gluon Plasma is a state of strongly interacting matter in which quarks and gluons are no more confined into hadrons.



QGP "signatures"

- Heavy Quarkonia: $J/\Psi, \Psi', \Upsilon(1S), \Upsilon(2S), \Upsilon(3S)$
- Open heavy flavours: D and B mesons

Muon Spectrometer

Study the production of heavy quark resonances via their muonic decay.

Absorbers

- Front Absorber
- Beam Shielding
- Iron Wall

Muon Tracking System

5 stations of 2 planes of Cathode Pad Chambers (CPC)

Muon Trigger System

2 stations of 2 planes of Resistive Plate Chambers (RPC)



Trigger System

Setup

- 4 planes of detector arranged in 2 stations of 2 planes each
- Each plane $\sim 5.5 \times 6.5 m^2$, with $\sim 1.2 \times 1.2 m^2$ central hole (beam pipe and shielding)
- 18 RPCs per plane, read on both sides with orthogonal strips
- 21k strips (1, 2, 4 cm pitch) readout by FE discriminators (LVDS output)
- Projective Geometry: different strip pitch and length on each plane



Muon p_t cut to reduce background from light meson decays





Before the Upgrade...





Specifications

- VME 6U board, 1U wide
- I/O Channels: support for NIM, TTL, ECL, and LVDS
- Internal Clock = 40 MHz (default)
- 405 MHz maximum frequency support for PLL (Phase-Locked Loops) synthesis
- User and Bridge FPGAs (Field Programmable Gate Array)

I/O Interface

- \triangleright 64 dedicated differential LVDS, ECL inputs (A, B)
- > 32 dedicated LVDS outputs (C)
- ▷ 2 bidirectional NIM, TTL ports (G)
- \triangleright 3 optional expansion card module slots (D, E, F)



Programming V1495

User FPGA: ALTERA Cyclone I EP1C204F400C6

Programmable with Altera Quartus II software:

- 1. Analysis & Synthesis
- 2. (Simulation)
- 3. Place & Route
- 4. Assembler
- 5. Timing Analysis

VHDL = VHSIC Hardware Description Language



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All logic elements are synchronized with a clock signal allowing them to simultaneously perform their intended function.

input signals width = 20 ns

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Positive-edge-triggered circuit

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$$\triangleright$$
 pll_clk \longrightarrow T = 12.5 ns

• input signals width = 20 ns

Positive-edge-triggered circuit

SLAVEs input stage



Trigger Logic





Data storing



Local Bus Interface



First-In First-Out memory to store events data and make them available for a BLock Transfer (BLT) Read Access:

- 4096 x 32bit words
- Address = base + 0x0000
- Independent Read and Write lines $\longrightarrow reduce \ dead \ time$
- Control signals:
 - meb_wrfull
 - meb_rdempty
 - meb_wrused