HVR - CCPD

Pixel detectors in BCD technology

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Introduction

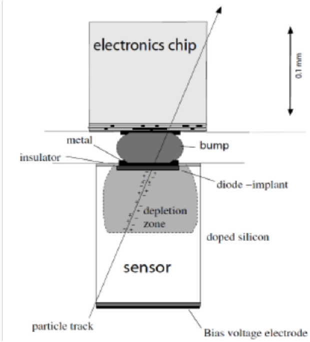
The **HVR-CCPD** (High Voltage and Resistivity - Capacitively Coupled Pixel Detector) INFN project develops innovative pixel detector for **ATLAS** next upgrade in **BCD** (Bipolar-CMOS-DMOS) technology. BCD8sP technology is provided by STMicroelectronics (Agrate Brianza).

Targeting the 2024 High Luminosity LHC upgrade:

- instantaneous luminosity 5×10^{34} cm^{-2}s^{-1} (five times original ATLAS design)
- Radiation hardness up to 1 Grad (10 MGy) for the detectors nearest to the beam line (3 cm)

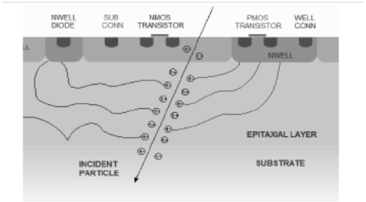
Why BCD technology?

Hybrid pixel sensors



- ✗ **expensive** (Bump-Bonding)
- ✓ charge collection → drift
  - radiation hardness
  - high readout speed

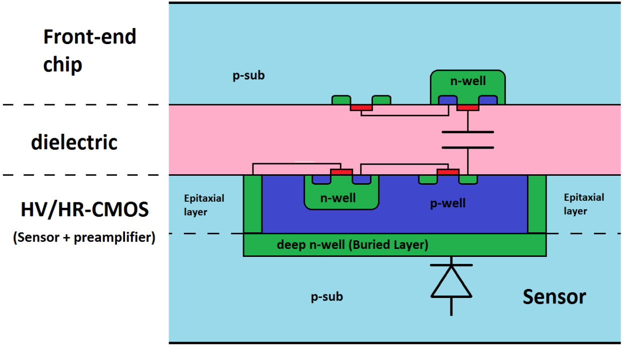
Monolithic pixel sensors



- ✓ effective cost (IC standard technology)
- ✗ **charge collection** → diffusion
  - radiation damage
  - small readout speed

Why BCD technology?

HV-CMOS Hybrid pixel in BCD technology

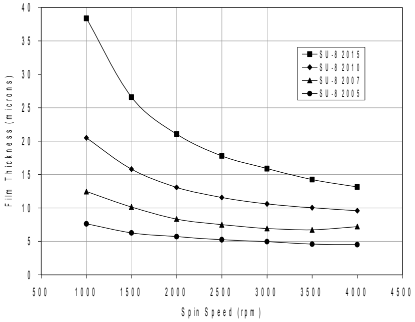


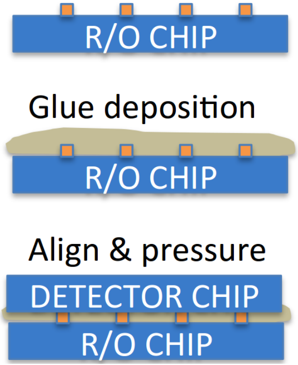
- ✓ cheap (BCD technology + Capacitive Coupling + IC standard technology)
- ✓ **charge collection** → drift

Hybridization at INFN Genova

Capacitative Coupling: cheaper and easier alignment than Resistive Coupling.

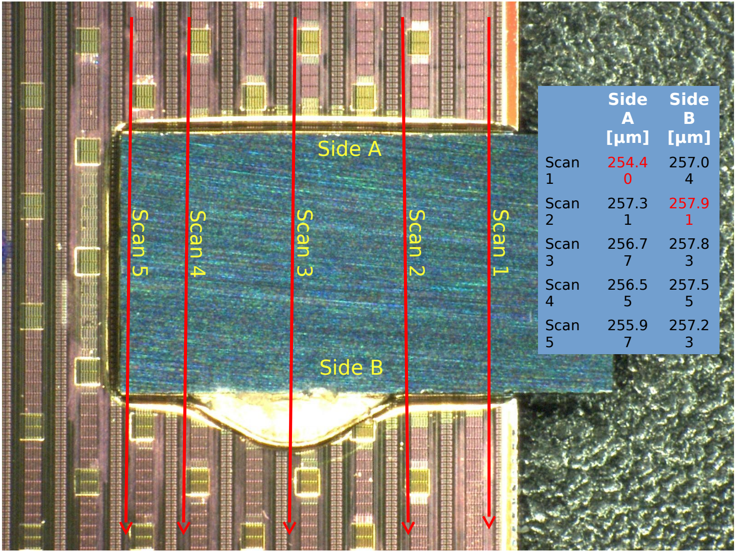
Pillars:
- used to separate uniformly the two wafers
- obtained with photoresist using lithography process





Photoresist thickness depends on the spin speed of the wafer in the deposition process

Hybridization at INFN Genova



	Side A [µm]	Side B [µm]
Scan 1	254.40	257.04
Scan 2	257.31	257.91
Scan 3	256.77	257.83
Scan 4	256.55	257.55
Scan 5	255.97	257.23

Hybridization tests are in progress. (in picture: HV2FE-I4)

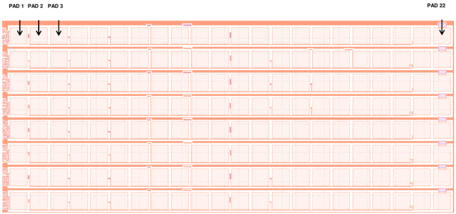
Targets for validation of BCD technology:

- **MOSFET performance does NOT depend on substrate voltage**
- **RADIATION HARDNESS**
  - electronic devices
  - sensor

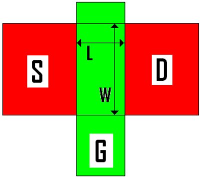
BCD Technology

KC01 is a standard test chip provided by STMicroelectronics.

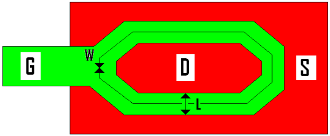
Each row contains MOS transistors with different working voltage (**1.8 V**/5 V), type (NMOS/PMOS), geometry (linear/ELT) and size (W/L=10 μm/10 μm, 10 μm/1 μm, 20 μm/1 μm, 40 μm/1 μm, 100 μm/1 μm)



KC01 is a standard test chip provided by STMicroelectronics



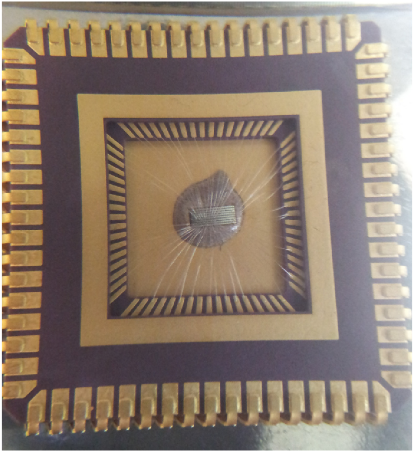
Linear Transistor



Enclosed Layout Transistor (ELT)

Test chip

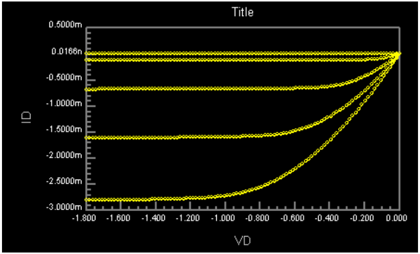
All pads of 1.8 V transistors are bonded on the JLCC68 package



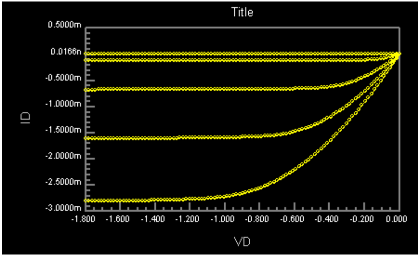
The measurement instrument is a Semiconductor Parameter Analyzer

Pch; ELT; W/L=100 μm/1 μm;
$V_{GS} = -1.8$ V, -1.44 V, -1.08 V, -0.72 V, -0.36 V, 0 V

$V_{sub} =$ **-1.8 V**



$V_{sub} =$ **-25 V**

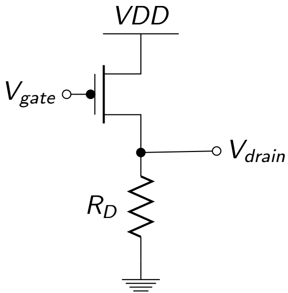


✓**MOSFET performance does NOT depend on substrate voltage**

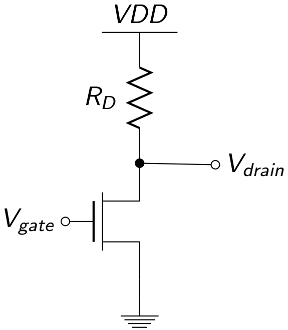
Board in radiation environment

Simplified measurement setup has been used in the radiation hall (oscilloscope + wave generator)

Transistor characterization is made through a NOT-gate circuit



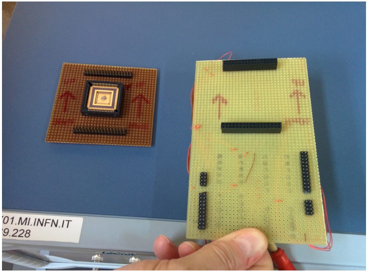
PMOS

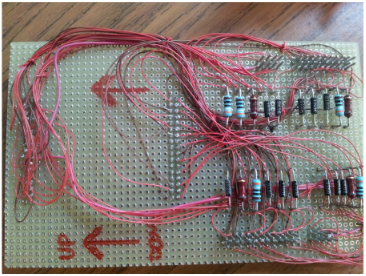


NMOS

During irradiations, all transistors were **biased** and **switched on**.

Test in radiation environment





At **Laboratorio Energia Nucleare Applicata (LENA)** in Pavia:

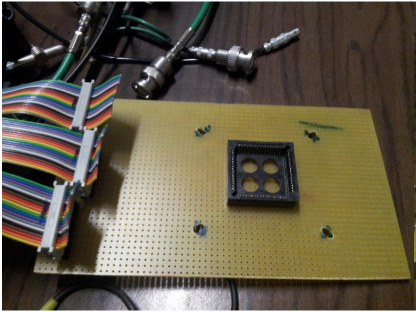
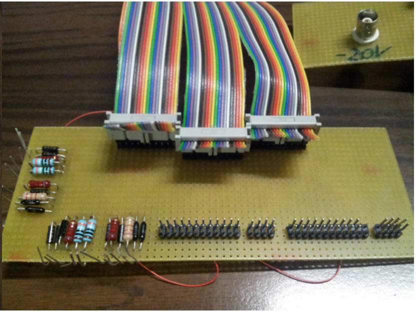
Irradiation with γ-rays (^{60}Co):

- 48 krad
- 128 krad
- 224 krad
- 488 krad
- 861 krad
- 2.0 Mrad
- 2.8 Mrad
- 3.5 Mrad
- 6.2 Mrad

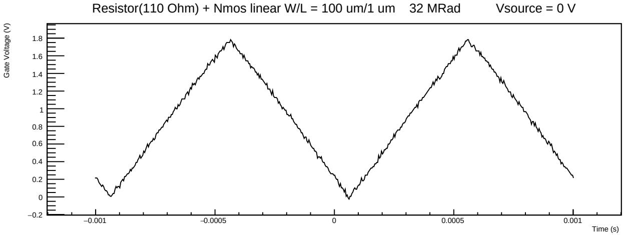
Test in radiation environment

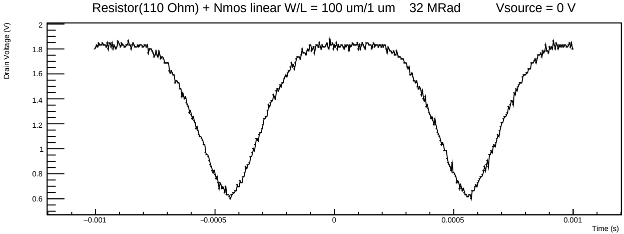
At **Laboratori Nazionali del Sud (LNS)** in Catania:

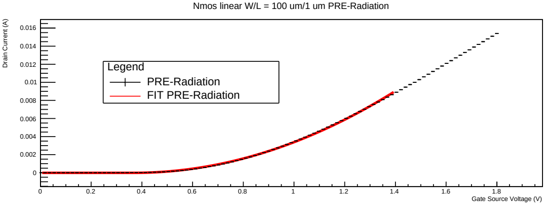
Irradiation with 62 MeV proton beam up to 32 Mrad

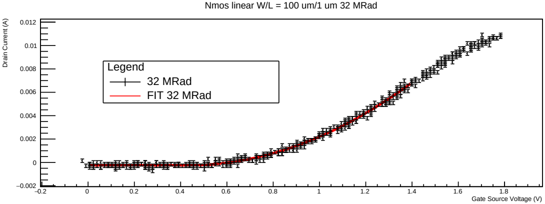



Data Collection



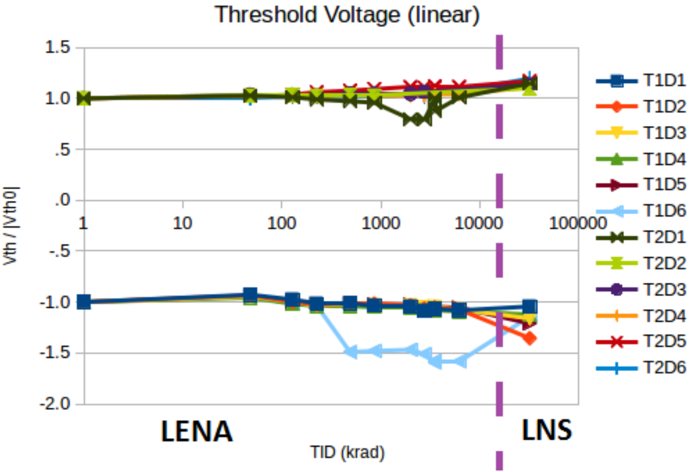






$$I_D = \begin{cases} I_0, & \text{if } \textit{switched off} \\ I_0 + K\left(V_{GS} - V_{th}\right)^2, & \text{if } \textit{switched on in saturation} \end{cases}$$

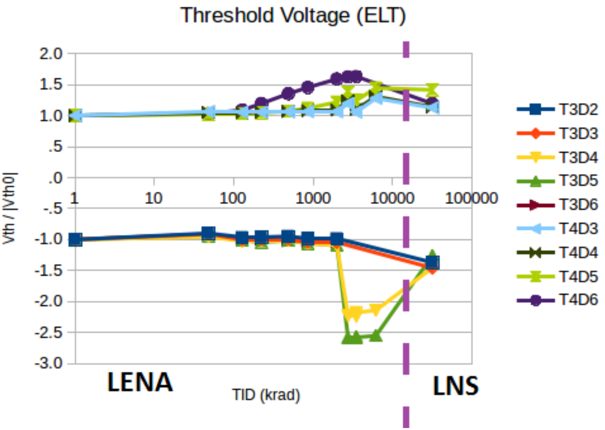
Results



T1: PMOS linear transistor; T2: NMOS linear transistor

D1, ... , D6 : size of transistor

Results



T3: PMOS ELT transistor; T4: NMOS ELT transistor
D1, ... , D6 : size of transistor

During proton beam irradiation, most of ELTs looked like switched off

Conclusions

- Hybridization:
  - ✓ detector and front-end chip separation is uniform at few microns level
  - in progress
- Transistors in standard test chip KC01:
  - ✓ No difference of channel current at different substrate voltages
  - ✓ Linear transistors (both PMOS and NMOS) can be considered radiation hard up to 32 Mrad
  - ✗ During and after irradiation, ELT performance is worse than linear transistors
- Tests of the sensor:
  - devices delivered in July
  - tests in progress

Thank you

Particular thanks to:

- dott. Daniele Dondi (Università degli Studi di Pavia)

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- prof. Daniele Alloni

L.E.N.A.

- dott. Gabriele Chiodini (INFN-Lecce)

- Laboratori Nazionali del Sud
- dott. Marzio de Napoli

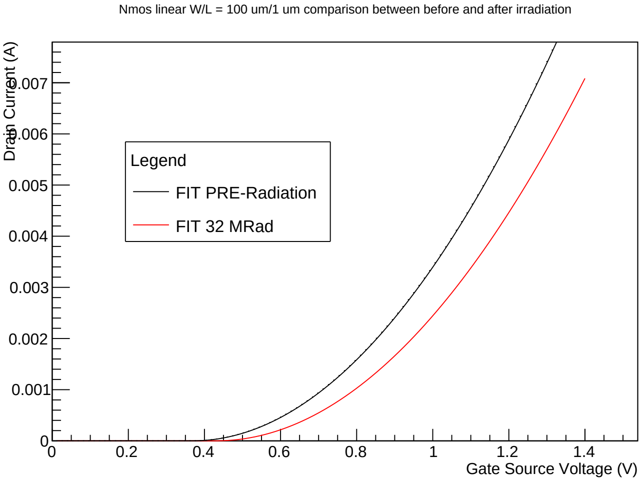
Test chip KC01

		$Teg1 - 1V8CMOS$		
		W_{EL} (μm)	L (μm)	Notes
T1D1	1V8Pch	10	10	NG=2
T1D2	1V8Pch	10	1	NG=2
T1D3	1V8Pch	20	1	NG=2
T1D4	1V8Pch	40	1	NG=2
T1D5	1V8Pch	100	1	NG=2
T1D6	1V8Pch	100	1	NG=20
		$Teg2 - 1V8CMOS$		
		W_{EL} (μm)	L (μm)	Notes
T2D1	1V8Nch	10	10	NG=2
T2D2	1V8Nch	10	1	NG=2
T2D3	1V8Nch	20	1	NG=2
T2D4	1V8Nch	40	1	NG=2
T2D5	1V8Nch	100	1	NG=2
T2D6	1V8Nch	100	1	NG=20

Test chip KC01

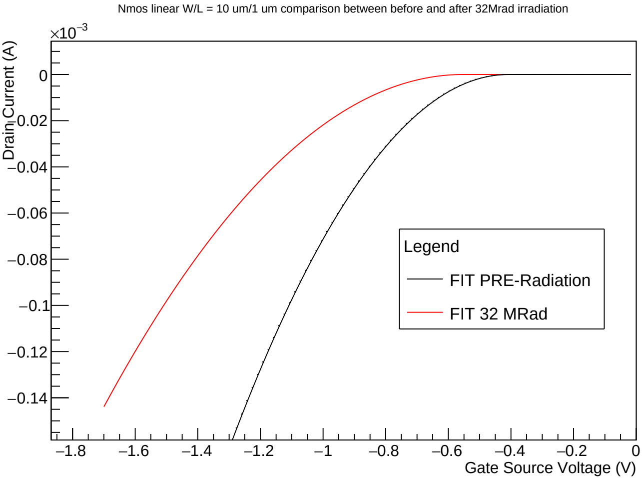
		$Teg3 - 1V8CMOS - Closed$		
		W_{EL} (μm)	L (μm)	Notes
T3D2	1V8Pch	10	1	NG=2
T3D3	1V8Pch	20	1	NG=2
T3D4	1V8Pch	40	1	NG=2
T3D5	1V8Pch	100	1	NG=2
T3D6	1V8Pch	100	1	NG=20
		$Teg4 - 1V8CMOS - Closed$		
		W_{EL} (μm)	L (μm)	Notes
T4D2	1V8Nch	10	1	NG=2
T4D3	1V8Nch	20	1	NG=2
T4D4	1V8Nch	40	1	NG=2
T4D5	1V8Nch	100	1	NG=2
T4D6	1V8Nch	100	1	NG=20

Fit Comparison



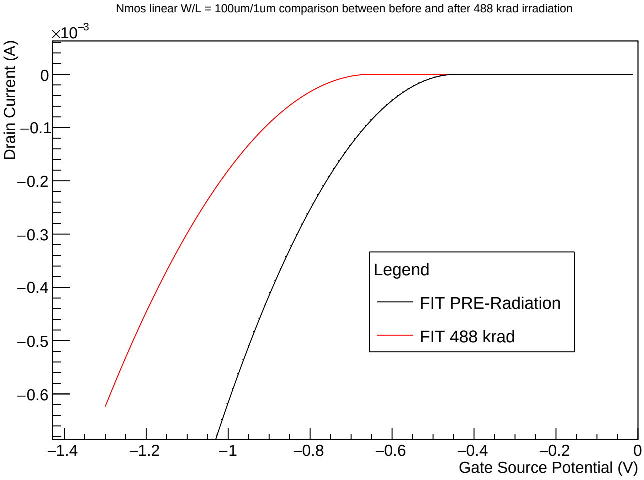
Fit Comparison: first case

T1D2



Fit Comparison: second case

T1D6



Fit Comparison: second case

T3D4