Pixel detectors in BCD technology

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The **HVR-CCPD** (High Voltage and Resistivity - Capacitively Coupled Pixel Detector) INFN project develops innovative pixel detector for **ATLAS** next upgrade in **BCD** (Bipolar-CMOS-DMOS) technology. BCD8sP technology is provided by STMicroelectronics (Agrate Brianza).

**Targeting the 2024 High Luminosity LHC upgrade:**

- instantaneous luminosity $5 \times 10^{34} \text{ cm}^{-2} \text{s}^{-1}$ (five times original ATLAS design)
- Radiation hardness up to 1 Grad (10 MGy) for the detectors nearest to the beam line (3 cm)
Why BCD technology?

**Hybrid pixel sensors**
- **X** expensive (Bump-Bonding)
- **✓** charge collection $\rightarrow$ drift
  - radiation hardness
  - high readout speed

**Monolithic pixel sensors**
- **✓** effective cost (IC standard technology)
- **X** charge collection $\rightarrow$ diffusion
  - radiation damage
  - small readout speed
Why BCD technology?

HV-CMOS Hybrid pixel in BCD technology

- cheap (BCD technology + Capacitive Coupling + IC standard technology)
- charge collection $\rightarrow$ drift
Hybridization at INFN Genova

Capacitative Coupling: cheaper and easier alignment than Resistive Coupling.

Pillars:
- used to separate uniformly the two wafers
- obtained with photoresist using lithography process

Photoresist thickness depends on the spin speed of the wafer in the deposition process.
Hybridization tests are in progress. (in picture: HV2FE-I4)
Targets for validation of BCD technology:

- **MOSFET** performance does NOT depend on substrate voltage

- **RADIATION HARDNESS**
  - electronic devices
  - sensor
KC01 is a standard test chip provided by STMicroelectronics.

Each row contains MOS transistors with different working voltage (1.8 V/5 V), type (NMOS/PMOS), geometry (linear/ELT) and size ($W/L=10 \, \mu m/10 \, \mu m$, $10 \, \mu m/1 \, \mu m$, $20 \, \mu m/1 \, \mu m$, $40 \, \mu m/1 \, \mu m$, $100 \, \mu m/1 \, \mu m$)
All pads of 1.8 V transistors are bonded on the JLCC68 package
No radiation

The measurement instrument is a Semiconductor Parameter Analyzer

Pch; ELT; $W/L=100 \, \mu m/1 \, \mu m$;

$V_{GS} = -1.8 \, V, -1.44 \, V, -1.08 \, V, -0.72 \, V, -0.36 \, V, 0 \, V$

$V_{sub} = -1.8 \, V$  $V_{sub} = -25 \, V$

✅ MOSFET performance does NOT depend on substrate voltage
Simplified measurement setup has been used in the radiation hall (oscilloscope + wave generator)

Transistor characterization is made through a NOT-gate circuit

During irradiations, all transistors were biased and switched on.
Test in radiation environment

At Laboratorio Energia Nucleare Applicata (LENA) in Pavia:

Irradiation with $\gamma$-rays ($^{60}\text{Co}$):

- 48 krad
- 128 krad
- 224 krad
- 488 krad
- 861 krad
- 2.0 Mrad
- 2.8 Mrad
- 3.5 Mrad
- 6.2 Mrad
Test in radiation environment

At Laboratori Nazionali del Sud (LNS) in Catania:

Irradiation with 62 MeV proton beam up to 32 Mrad
Data Collection

Resistor (110 Ohm) + Nmos linear W/L = 100 um/1 um  32 MRad  Vsource = 0 V

Resistor (110 Ohm) + Nmos linear W/L = 100 um/1 um  32 MRad  Vsource = 0 V
\[ I_D = \begin{cases} I_0, & \text{if switched off} \\ I_0 + K (V_{GS} - V_{th})^2, & \text{if switched on in saturation} \end{cases} \]
Results

T1: PMOS linear transistor; T2: NMOS linear transistor
D1, ..., D6: size of transistor
Results

T3: PMOS ELT transistor; T4: NMOS ELT transistor
D1, ..., D6: size of transistor

During proton beam irradiation, most of ELTs looked like switched off
Conclusions

- **Hybridization:**
  - ✔ detector and front-end chip separation is uniform at few microns level
  - in progress

- **Transistors in standard test chip KC01:**
  - ✔ No difference of channel current at different substrate voltages
  - ✔ Linear transistors (both PMOS and NMOS) can be considered radiation hard up to 32 Mrad
  - ❌ During and after irradiation, ELT performance is worse than linear transistors

- **Tests of the sensor:**
  - devices delivered in July
  - tests in progress
Thank you

Particular thanks to:

- dott. Daniele Dondi (Università degli Studi di Pavia)
- Laboratorio Energia Nucleare Applicata
- prof. Daniele Alloni
- dott. Gabriele Chiodini (INFN-Lecce)
- Laboratori Nazionali del Sud
- dott. Marzio de Napoli
### Teg1 – 1V8CMOS

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### Teg4 – 1V8CMOS – Closed

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Nmos linear W/L = 100 um/1 um comparison between before and after irradiation
Fit Comparison: first case

T1D2

NMOS linear W/L = 10 µm/1 µm comparison between before and after 32Mrad irradiation

Legend:
- FIT PRE-Radiation
- FIT 32 MRad
Fit Comparison: second case

T1D6

Nmos linear W/L = 100um/1um comparison between before and after 488 krad irradiation

Legend
- FIT PRE-Radiation
- FIT 488 krad
Fit Comparison: second case

T3D4

Nmos linear W/L = 40um/1um comparison between before and after 2.8 Mrad irradiation

Legend
FIT PRE-Radiation
FIT 2.8 Mrad