Very front-end electronics for the upgrade of the CMS experiment

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Funded by CHIPIX65 / INFN project
The CMS experiment

- Silicon tracker ⇒ Inner part of the CMS detector
  - Composed of pixels and strips layers
  - Pixel detector ⇒ Closest to the beam pipe
The HL_LHC upgrade

- Parameters of the silicon pixel detector of the CMS experiment:

<table>
<thead>
<tr>
<th>PARAMETER or FEATURE</th>
<th>1st generation LHC phase 0</th>
<th>2nd generation LHC Phase 1</th>
<th>3rd generation LHC Phase 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max Particle Flux</td>
<td>~50 MHz/cm²</td>
<td>~200 MHz/cm²</td>
<td>~500 MHz/cm²</td>
</tr>
<tr>
<td>Max Pixel Flux</td>
<td>200 MHz/cm²</td>
<td>600 MHz/cm²</td>
<td>2 GHz/cm²</td>
</tr>
<tr>
<td>Rad. Hardness</td>
<td>1.5 MGy</td>
<td>3.5 MGy</td>
<td>10 MGy</td>
</tr>
<tr>
<td>Pixel Dimension</td>
<td>100x150 um²</td>
<td>100x150 um²</td>
<td>50x50 um²</td>
</tr>
<tr>
<td></td>
<td>400x50 um²</td>
<td>250x50 um²</td>
<td>25x100 um²</td>
</tr>
<tr>
<td>Signal Threshold</td>
<td>2500-3000 e⁻</td>
<td>1500-2000 e⁻</td>
<td>~1000 e⁻</td>
</tr>
<tr>
<td>L1 Trigger Latency</td>
<td>2-3 us</td>
<td>4-6 us</td>
<td>6-20 us</td>
</tr>
<tr>
<td>Power Budget</td>
<td>~0.3 W/cm²</td>
<td>~0.3 W/cm²</td>
<td>&lt;0.4 W/cm²</td>
</tr>
</tbody>
</table>

- RD53, a CMS-ATLAS collaboration, has been developed in order to design the new chip

- INFN contribute: CHIPIX 65 collaboration, a group 5 project approved in 2013 for the 2014-2016 period. 7 INFN sections involved (TO, MI, BA, PD, PI, PV, PG)
Main challenges

- New readout chip required
  - The present one can not survive the extreme Phase 2 conditions

- 65nm technology new for HEP experiment
  - Low power and radiation hard

- Very high particle flux (2 GHz/cm²)

- Maintaining or improving the detector performance
  - New pixel size (50x50 μm² or 25x100 μm²)

- Low power architecture
  - Required in order to maintain the material budget as low as possible
  - Around 10 μW per pixel
TORINO:
Synchronous Analog Chain

- **PREAMPLIFIER**
  - One stage CSA with Krummenacher feedback
- **Synchronous DISCRIMINATOR**
  - (AC coupled to CSA)
  - offset compensated diff.amplif. + latch;
  - **FAST Time-over-Threshold**
    - Local oscillator strobing Latch (to 800MHz)
- **Calibration circuit**
  - digital signal + DC calibration level

**Performance SUMMARY**
- Compact: ~26um x 40 um
- Low power: < 5.5 uW (with ToT logic)
- Low noise: ENC=100e @C_{det}=100 fF
- Leakage compensation: up to 50nA/pixel
- Fast Charge measurement:
  - 30 ke- in <300ns (or 800ns)
  - up to 7-8bit (125-250e/ADC) - no ext clock
- NO Threshold-Trimming:
  - autozeroing made by hardware
• CSA + Disc + Calibration circuit -> 26x40 um²

• In addition for tests:
  ‣ Different capacitances to simulate the detector
  ‣ Analog buffer in order to see the preamp analog output
Torino work 2014-May2015

Integration CHIPIX_VFE_1 mini@sic
64 pixels matrix

Real chip bonded to
PCB for testing

Integration CHIPIX_VFE_2 mini@sic
Second version - 64 pixels matrix

Design PCB

Measurements

1-Oct-2014

20-Jan-2015

20-May-2015

New version

Design : VFE-TO.v1, VFE-To.v2, JTAG
Peaking time

Analog signal (oscilloscope)

- $C_{\text{input}} = 50 \text{ fF} \Rightarrow T_{\text{peak}} \text{ around 25 ns}$
- At the schematic level the value of $T_{\text{peak}}@ 50 \text{ fF}$ is around 18 ns
- Layout improved in the second version to reduce the peaking time
Voltage gain

Gain linearity for one pixel

Gain distribution of the 64 pixels ($Q_{in} = 6k^-$)

Amplitude dispersion below 2.2% RMS

Excellent gain uniformity

$\chi^2$/ndf 2.033/8
P0 13.59 ± 4.53
P1 0.86 ± 0.04

10ke$^-$
Noise measured

- Linear trend of the Equivalent Noise Charge vs input capacitance as expected
- Noise increases with the feedback current (ballistic deficit)
- Threshold = 1000 e- ⇒
  Around 7σ of the noise
Comparator results

Input signal 10 ke⁻  Threshold ≃ 1000 e⁻

Time duration of HIT multiple of 25 ns (clock period)
Comparator results

Input signal 10 ke\(^{-}\) Threshold \(\approx\) 1000 e\(^{-}\)

- Oscillator @ 100 MHz
- Time duration of the ToT output compatible with HIT in binary mode
- In the present version, oscillation speed can be tuned up to 500 MHz, but set-up bandwidth is limited to about 100 MHz
ToT linearity

ToT linearity

<table>
<thead>
<tr>
<th>$\chi^2 / \text{ndf}$</th>
<th>9.947 / 9</th>
</tr>
</thead>
<tbody>
<tr>
<td>$p_0$</td>
<td>$87.38 \pm 2.826$</td>
</tr>
<tr>
<td>$p_1$</td>
<td>$21.94 \pm 0.1491$</td>
</tr>
</tbody>
</table>

ToT is linear up to (at least) 40 ke$^{-}$. 

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Conclusions and future plans

• First version of a synchronous front-end with offset compensation designed and tested

• Idea of “self-oscillating” comparator for fast ToT measurement works

• Good ToT linearity in a wide range of input signals

• Improved version submitted in May 2015

• Testing on the second version on the chip started this month
BACKUP
Pixel matrix with analog output

- 8x8 pixel matrix
  - 1/4 of the Mini@sic submitted in October and received in the end of January
- Readout of CSA output using analog buffering
- Readout of discriminator output using a digital buffer
- 4 pixel (2x2 region) are readout at the same time
Pixel matrix with analog output

Picture of the chip wire-bonded to the test board
Objectives

- **Preamp:**
  - Krummenacher feedback to compensate leakage currents up to 50 nA
  - Fast charge measurement

- **Synchronous Comparator:**
  - Eliminate time walk
  - "Hardware" Offset compensation using capacitors

- **Different speed for ToT measurement:**
  - FAST: ToT of 90 ns for Qin = 10 ke- ==> OK for 2 GHz/cm²
  - SLOW: ToT of 300 ns for Qin = 10 ke- ==> OK for 0.5 GHz/cm² (~0.5% ineff.)
  - Choice depends on layer, sensor used and particle flux
Power consumption

- Static current around 3.5 uA
  - Preamplifier -> 2.5 uA
  - Discriminator -> 1 uA

- Dynamic current (latch) around 0.8 uA

- The average total current is around 4.3 uA per pixel

- Considering VDD = 1.2 V the total power consumption is around 5.2 uW
  - It corresponds to around 0.2 W/cm² considering a 50x50 µm² pixel
  - OK ~ 50% of the 0.4 W/cm² required

- This configuration has been used for the measurements showed in this presentation
VFE layout - v2 - 2x2 region
Measurements on First Prototype

Analog-Out Q=10ke-, ToT=90ns
Measurement with Very-Fast ToT

ToT linear up to >40ke
measurement with Standard-ToT

Fast ToT: oscillator counting ToT; threshold @1ke-
100 MHz (limited by analog readout and set-up)

ENC~100e⁻ for $C_{\text{det}}$~130fF
for Standard ToT
VFE layout - v2

40 um

26 um
Noise \( \triangleq \text{Cin} = 130 \text{ fF} \)

- ENC ~ 167 e\(^{-}\) @ Ifeed = 40 nA (fast), Cinput = 130 fF
- ENC ~ 102 e\(^{-}\) @ Ifeed = 10 nA (slow), Cinput = 130 fF

- Measurement performed with the clock activated
Noise @ Cin = 50 fF

- ENC ~ 108 e^- @ Ifeed = 40 nA (fast), Cinput = 50 fF
- ENC ~ 83 e^- @ Ifeed = 10 nA (slow), Cinput = 50 fF

- Measurement performed with the clock activated
Offset compensation

It could be better

We have understood the problems
  - Too high gain fluctuations due to mismatch
  - Underestimation of the latch dynamic offset

Solved in version 2

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CSA schematic

Cascode with current splitting and source follower
Synchronous Discriminator with offset compensation

No more need of threshold trimming
• Why?
  ▸ AC coupling between CSA and comparator and offset compensation technique
Latch
Krummenacher

Cascode with current splitting and source follower
• Preamp
  ‣ One stage Charge Sensitive Amplifier
  ‣ Krummenacher feedback to compensate leakage currents up to 50 nA
  ‣ Selectable feedback capacitance (2.5, 4, 6.5 fF)
Hit Logic

**Fast ToT**: comparator turned into local oscillator using an asynchronous logic feedback loop