Very front-end electronics for the upgrade of the CMS experiment

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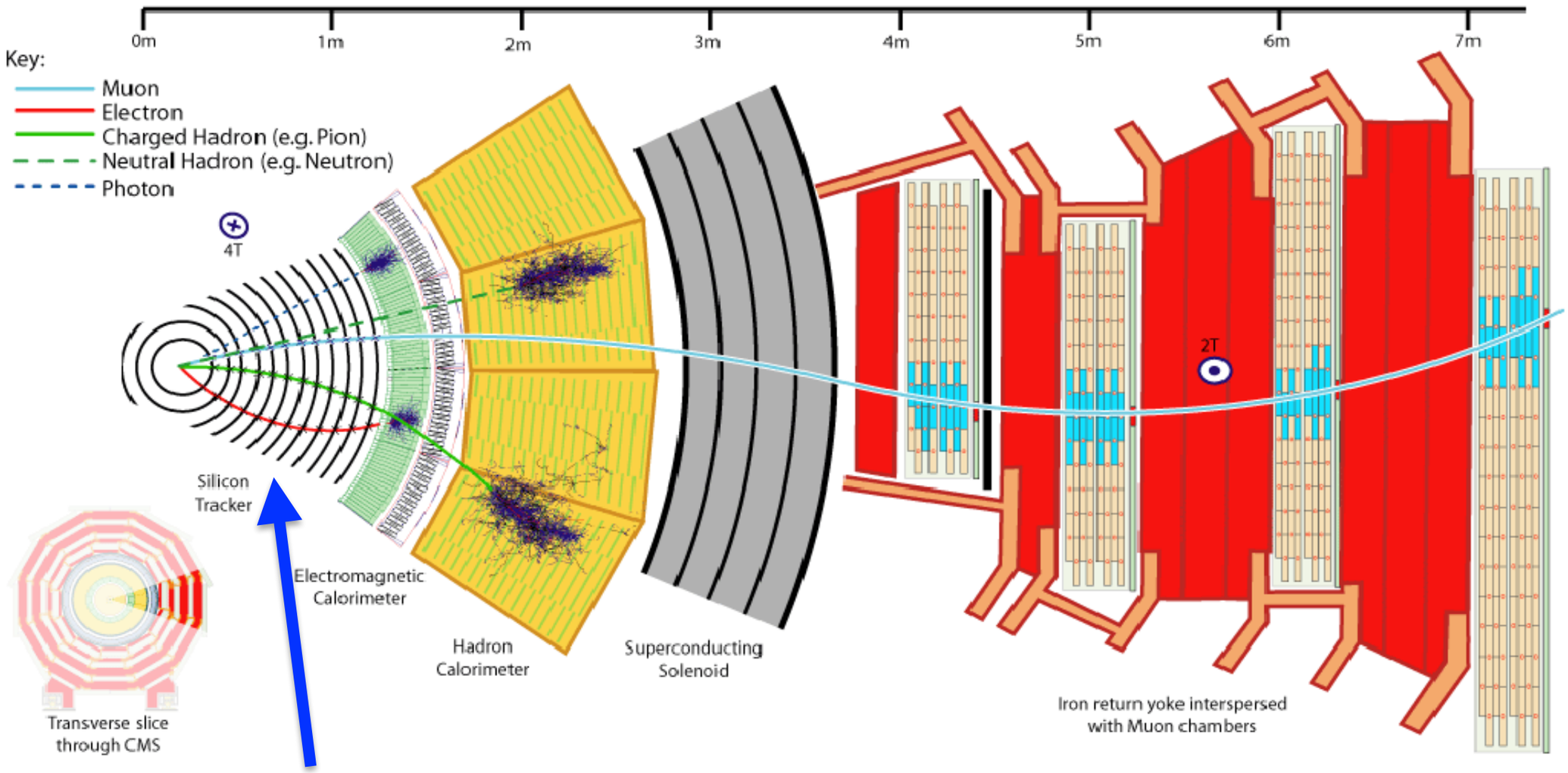
Funded by CHIPIX65 / INFN project

The CMS experiment



- Silicon tracker ⇒ Inner part of the CMS detector
  - Composed of pixels and strips layers
  - Pixel detector ⇒ Closest to the beam pipe

The HL_LHC upgrade

- Parameters of the silicon pixel detector of the CMS experiment:

PARAMETER or FEATURE	1st generation LHC phase 0	2nd generation LHC Phase 1	3rd generation LHC Phase 2
Max Particle Flux	~50 MHz/cm^2	~200 MHz/cm^2	~500 MHz/cm^2
Max Pixel Flux	200 MHz/cm^2	600 MHz/cm^2	2 GHz/cm^2
Rad. Hardness	1.5 MGy	3.5 MGy	10 MGy
Pixel Dimension	100x150 um^2 400x50 um^2	100x150 um^2 250x50 um^2	50x50 um^2 25x100 um^2
Signal Threshold	2500-3000 e$^-$	1500-2000 e$^-$	~1000 e$^-$
L1 Trigger Latency	2-3 us	4-6 us	6-20 us
Power Budget	~0.3 W/cm^2	~0.3 W/cm^2	<0.4 W/cm^2
Electronics technology node	250nm CMOS	250nm CMOS (CMS) 130nm CMOS (ATLAS)	65nm CMOS

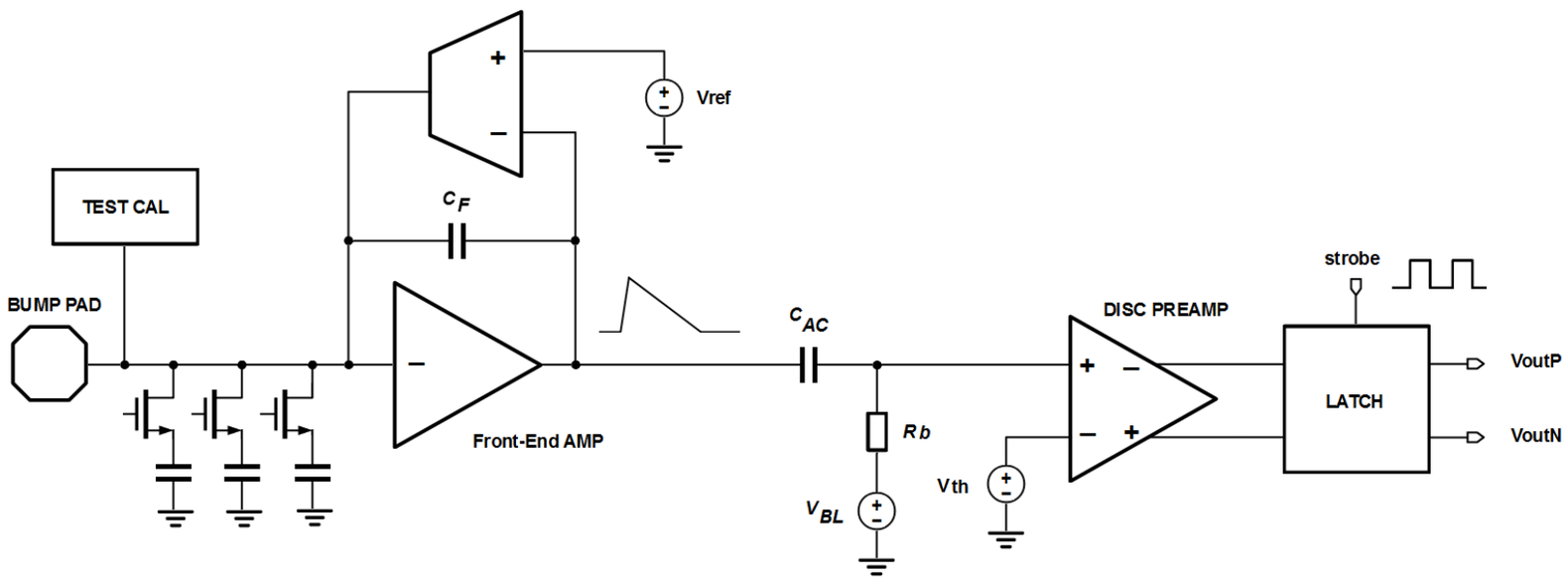
- RD53, a CMS-ATLAS collaboration, has been developed in order to design the new chip

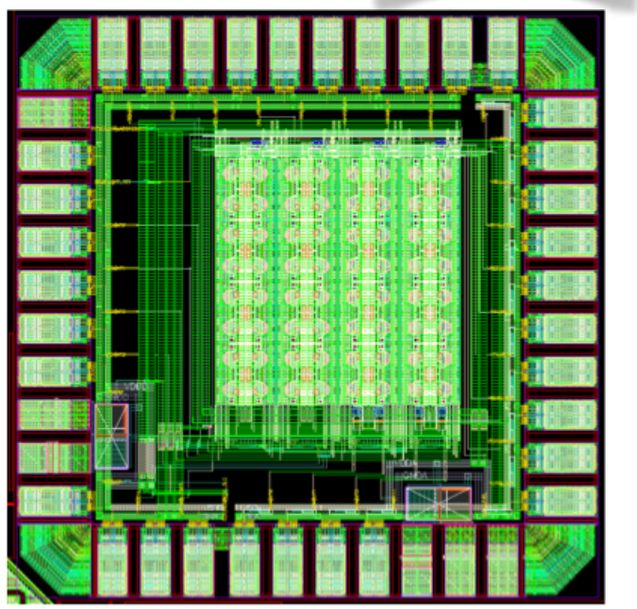
- INFN contribute: CHIPIX 65 collaboration, a group 5 project approved in 2013 for the 2014-2016 period. 7 INFN sections involved (TO, MI, BA, PD, PI, PV, PG)

Main challenges

- **New readout chip required**
  - The present one can not survive the extreme Phase 2 conditions
- 65nm technology new for HEP experiment
  - Low power and radiation hard
- Very **high particle flux** (2 GHz/cm^2)
- Maintaining or improving the detector performance
  - **New pixel size** (50x50 um^2 or 25x100 um^2)
- **Low power architecture**
  - Required in order to maintain the material budget as low as possible
  - Around 10 uW per pixel

TORINO : Synchronous Analog Chain





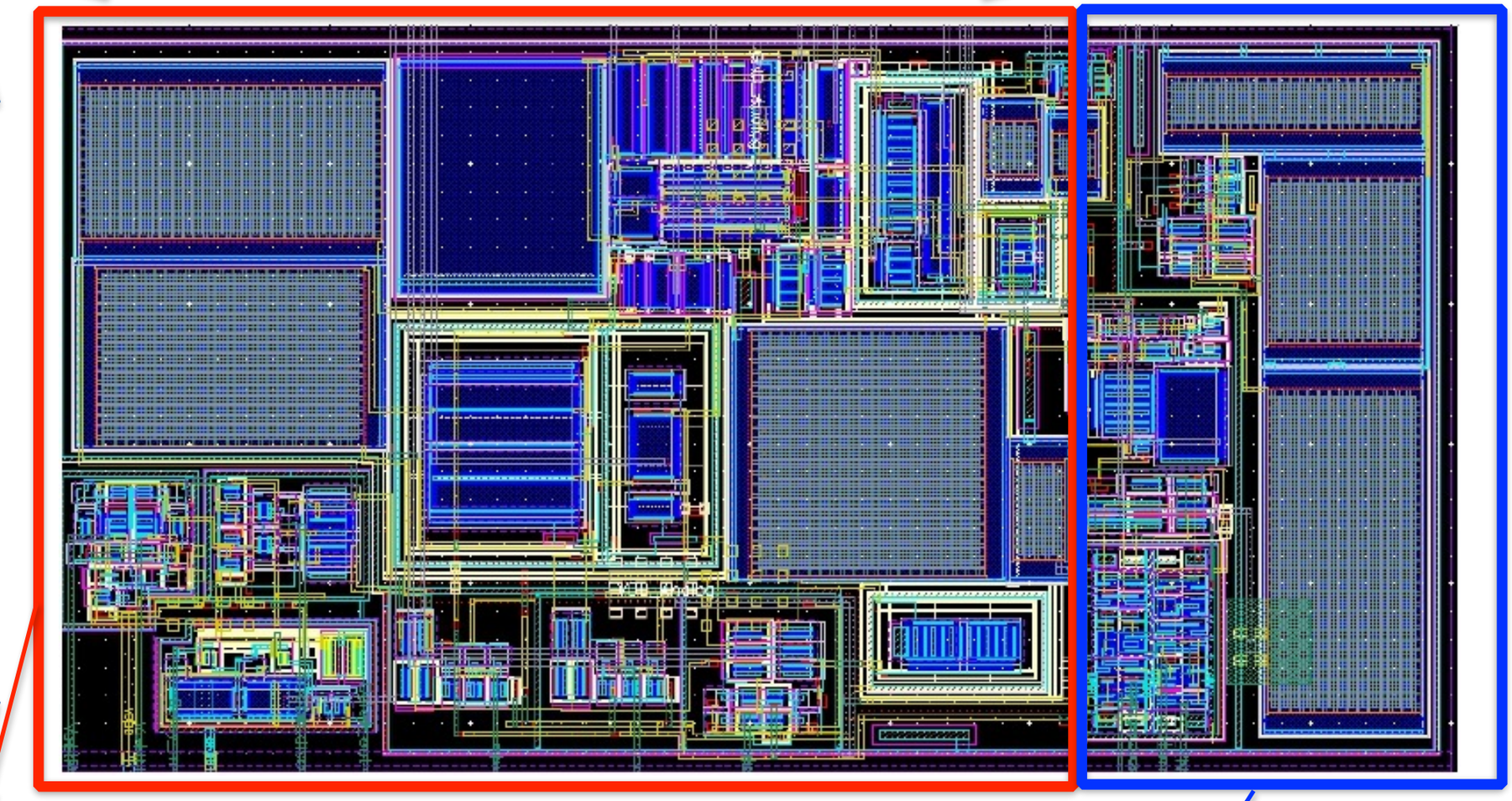
8x8 pixel matrix submitted and tested
Analog readout of CSA and Discriminator (via buffers)

- **PREAMPLIFIER**
  - One stage CSA with Krummenacher feedback
- **Synchronous DISCRIMINATOR**
  - (AC coupled to CSA)
  - offset compensated diff.amplif. + latch;
  - **FAST Time-over-Threshold**
    - Local oscillator strobing Latch (to 800MHz)
- **Calibration circuit**
  - digital signal + DC calibration level

Performance SUMMARY

- Compact: ~26um x 40 um
- Low power: < 5.5 uW (with ToT logic)
- Low noise: ENC=100e^- @C_{det}=100 fF
- Leakage compensation: up to 50nA/pixel
- Fast Charge measurement:
  - 30 ke^- in <300ns (or 800ns)
  - up to 7-8bit (125-250e^-/ADC) - no ext clock
- NO Threshold-Trimming:
  - autozeroing made by hardware

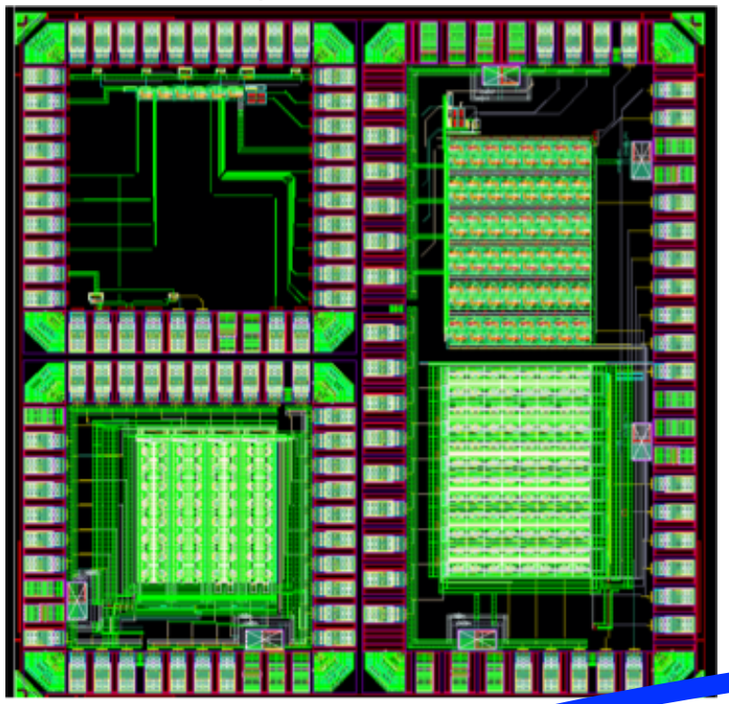
VFE_1 Layout



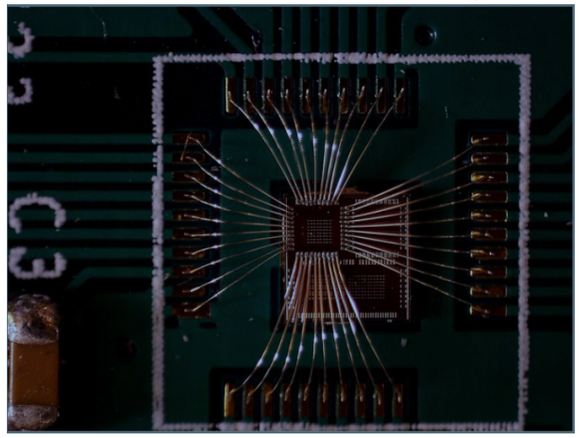
- CSA + Disc + Calibration circuit -> 26x40 um^2
- In addition for tests:
  - Different capacitances to simulate the detector
  - Analog buffer in order to see the preamp analog output

Torino work 2014-May2015

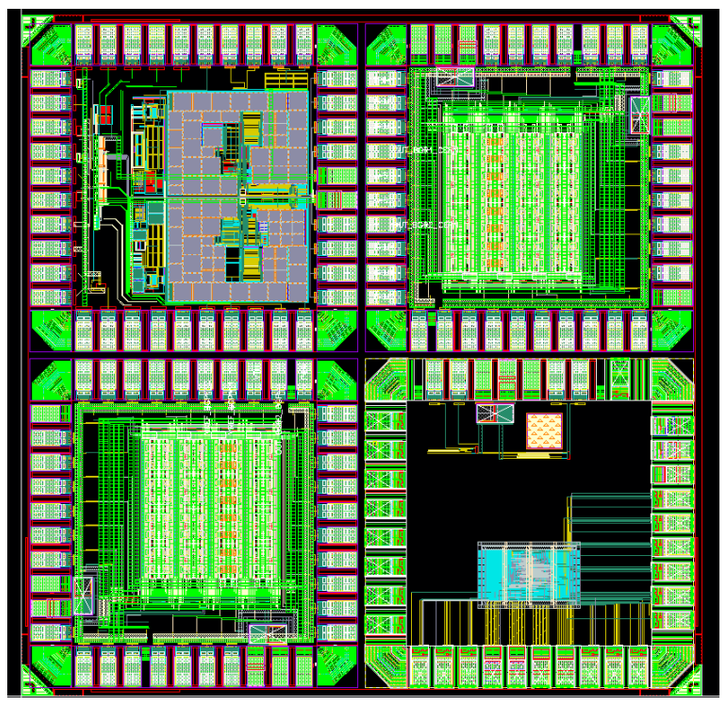
Integration CHIPIX_VFE_1 mini@sic
64 pixels matrix

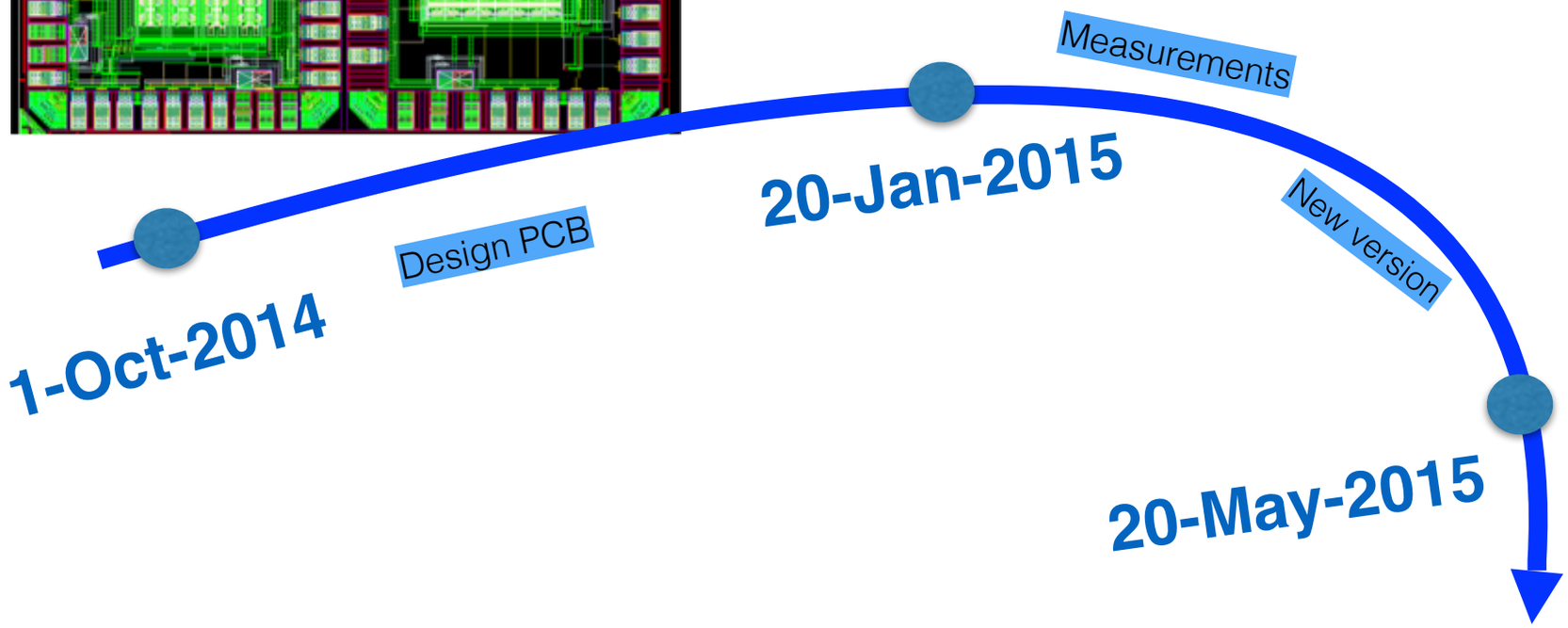


Real chip bonded to
PCB for testing



Integration CHIPIX_VFE_2 mini@sic
Second version - 64 pixels matrix

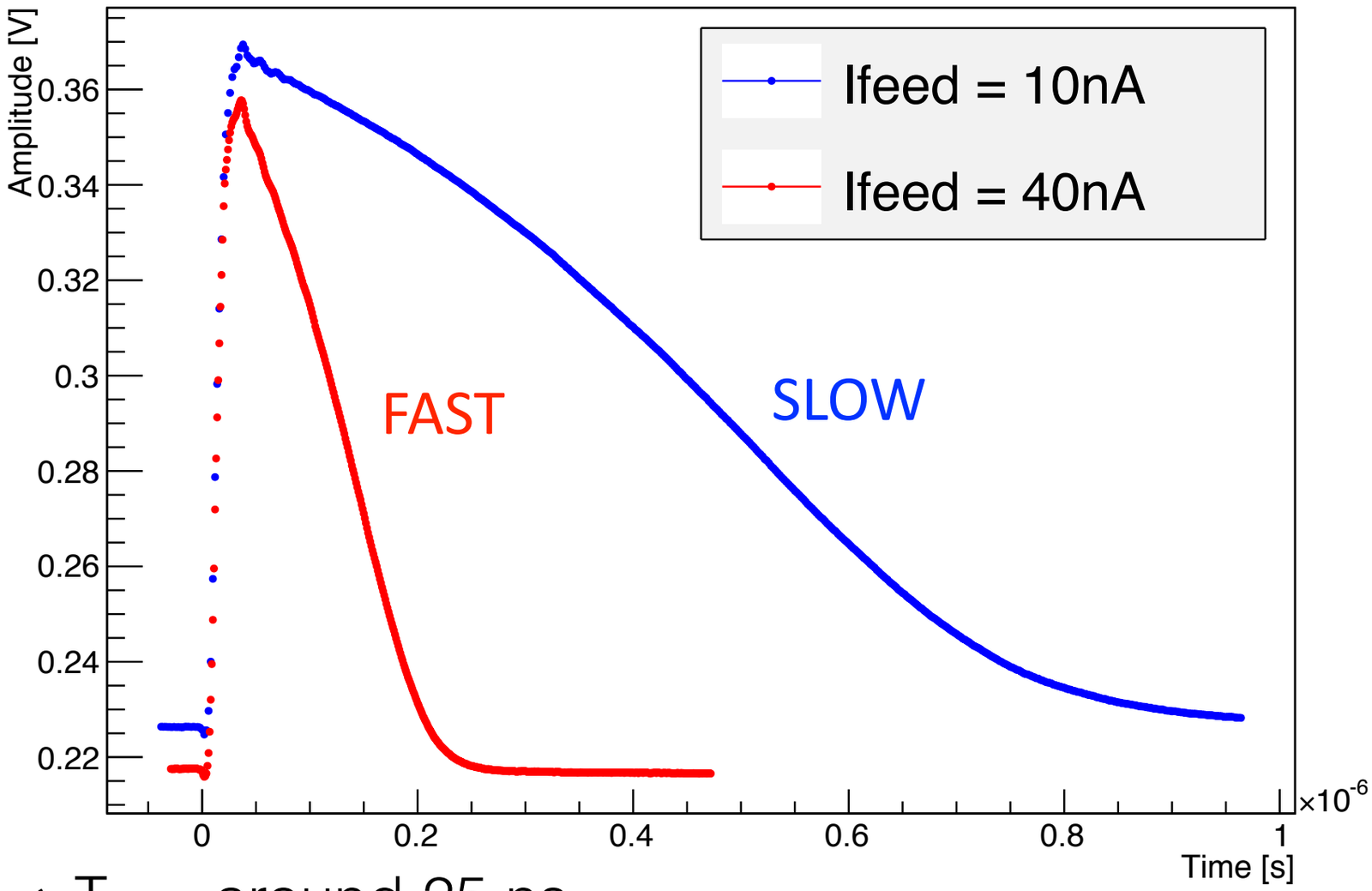




Design : VFE-TO.v1, VFE-To.v2, JTAG

Peaking time

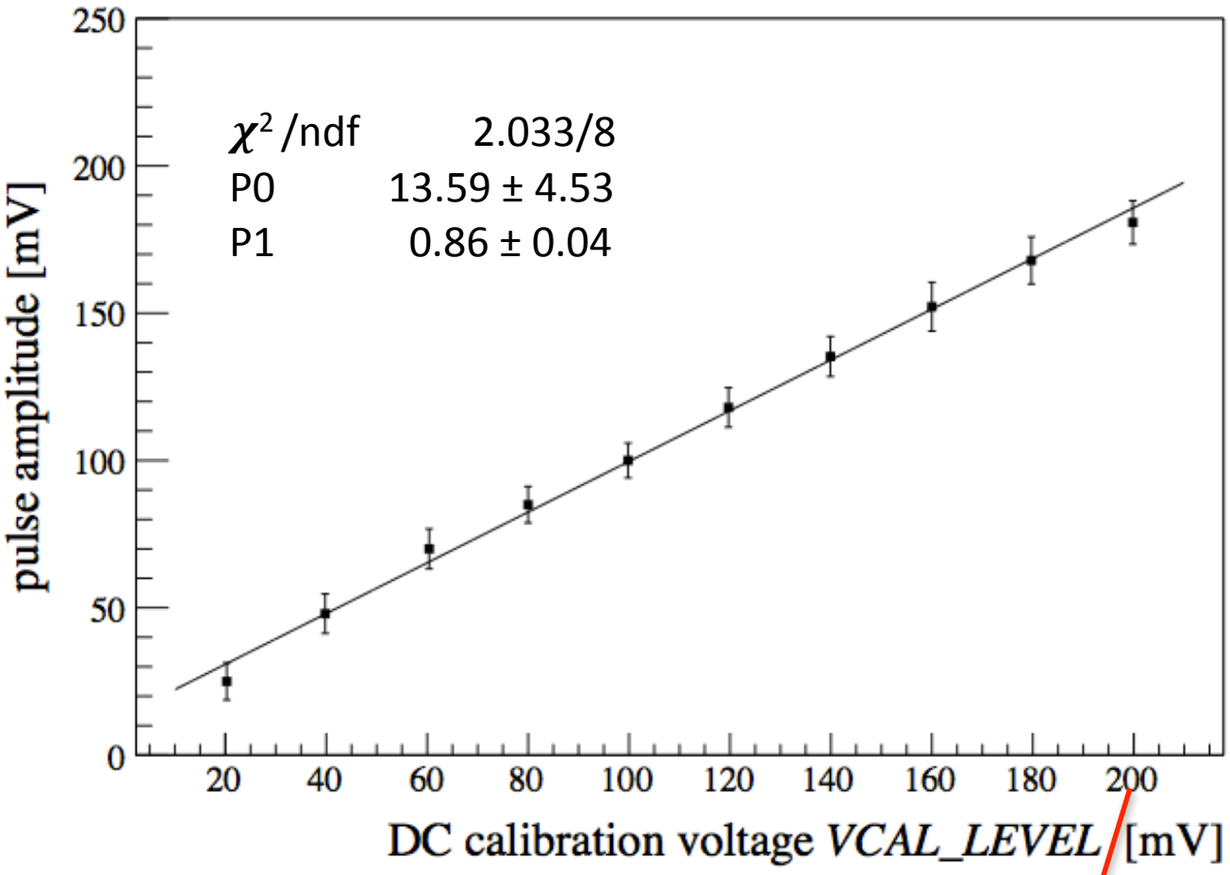
Analog signal (oscilloscope)



- C_{input} = 50 fF ⇒ T_{peak} around 25 ns
- At the schematic level the value of T_{peak} @ 50 fF is around 18 ns
- Layout improved in the second version to reduce the peaking time

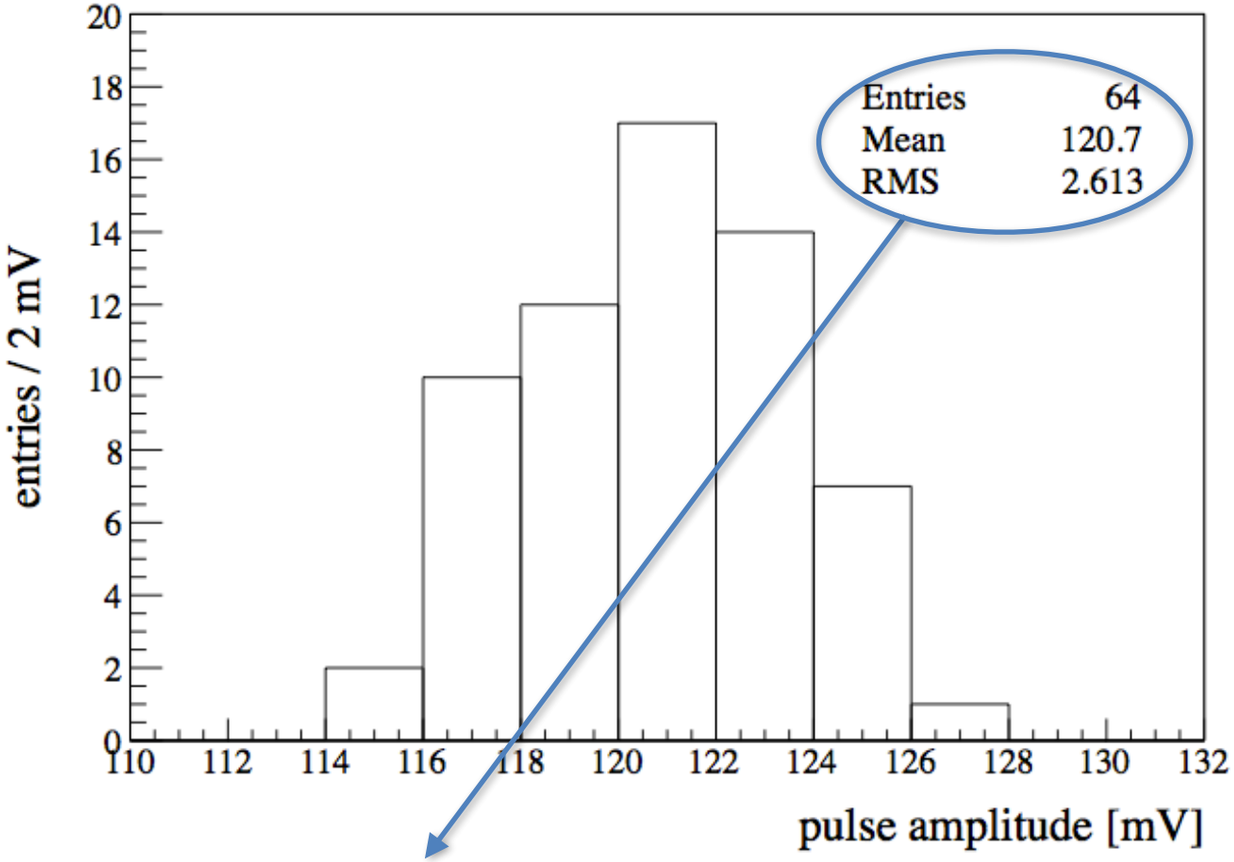
Voltage gain

Gain linearity for one pixel



10ke$^-$

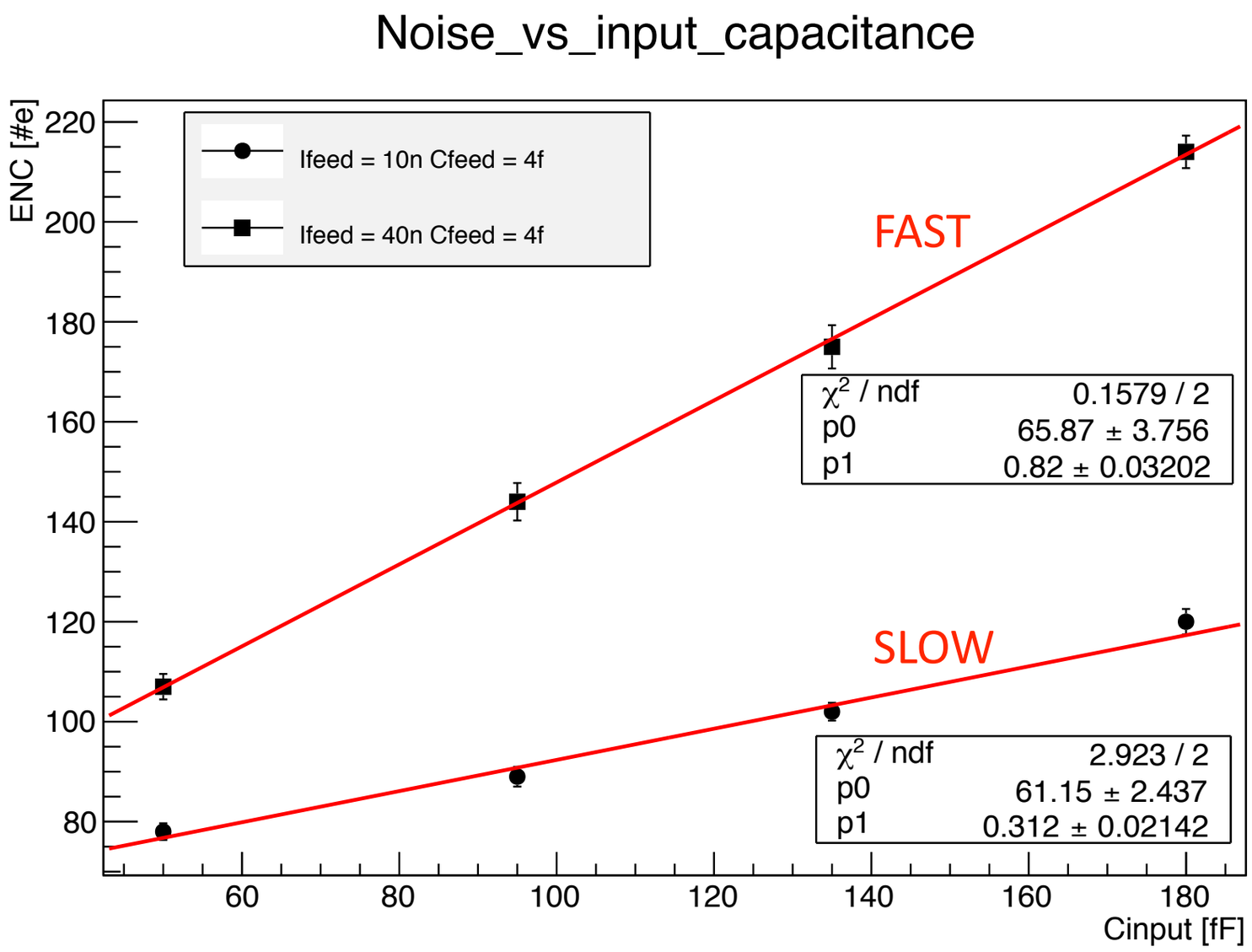
Gain distribution of the 64 pixels (Q_{in} = 6ke$^-$)



Amplitude dispersion below 2.2% RMS

Excellent gain uniformity

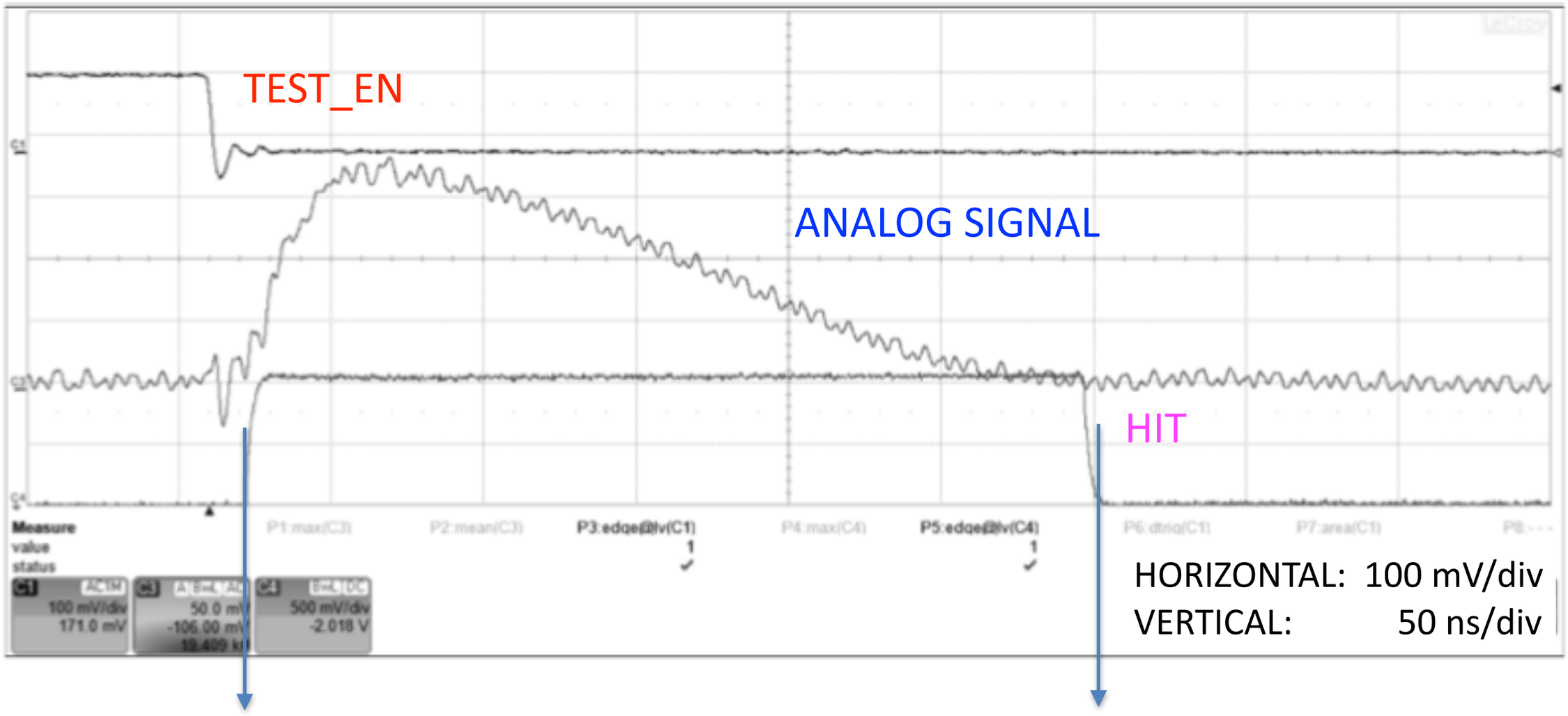
Noise measured



- Linear trend of the Equivalent Noise Charge vs input capacitance as expected
- Noise increases with the feedback current (ballistic deficit)
- Threshold = 1000 e- ⇒ Around 7σ of the noise

Comparator results

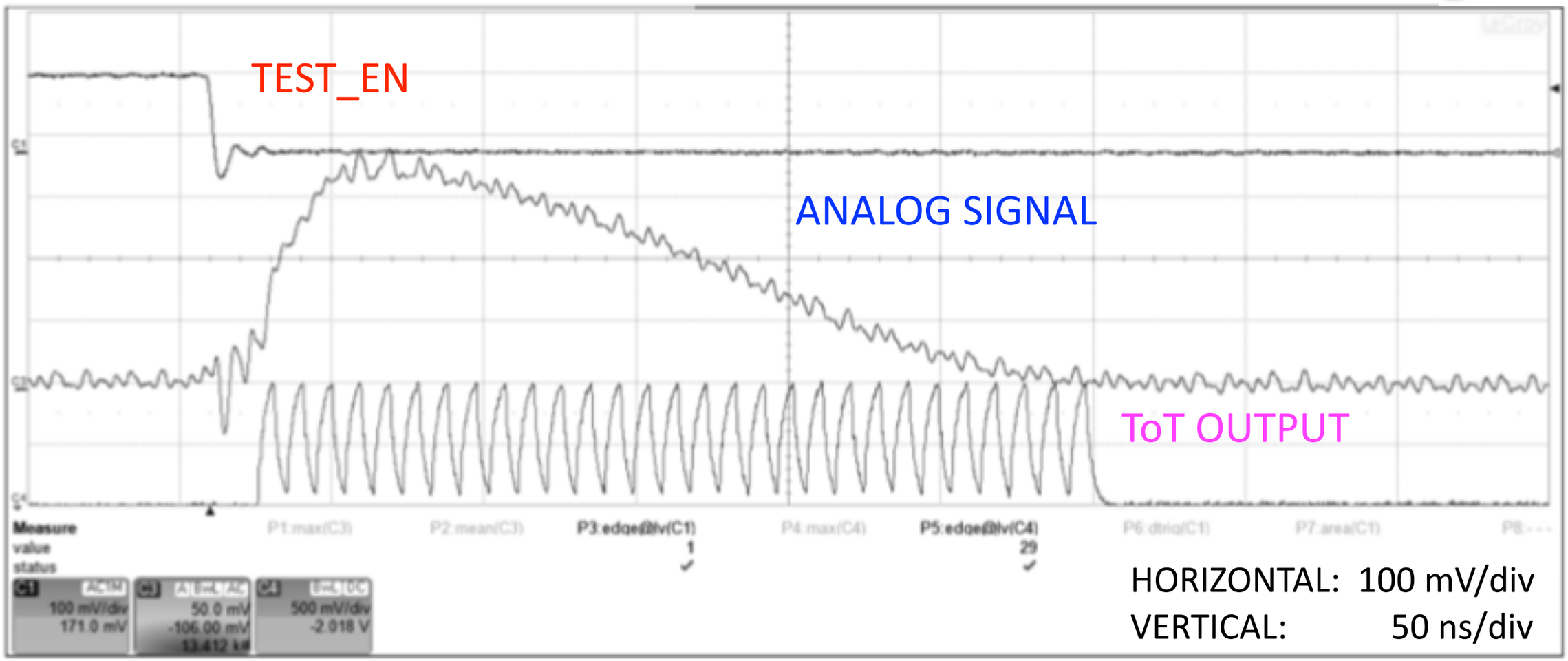
Input signal 10 ke$^-$ Threshold ≈ 1000 e$^-$



Time duration of HIT multiple of 25 ns (clock period)

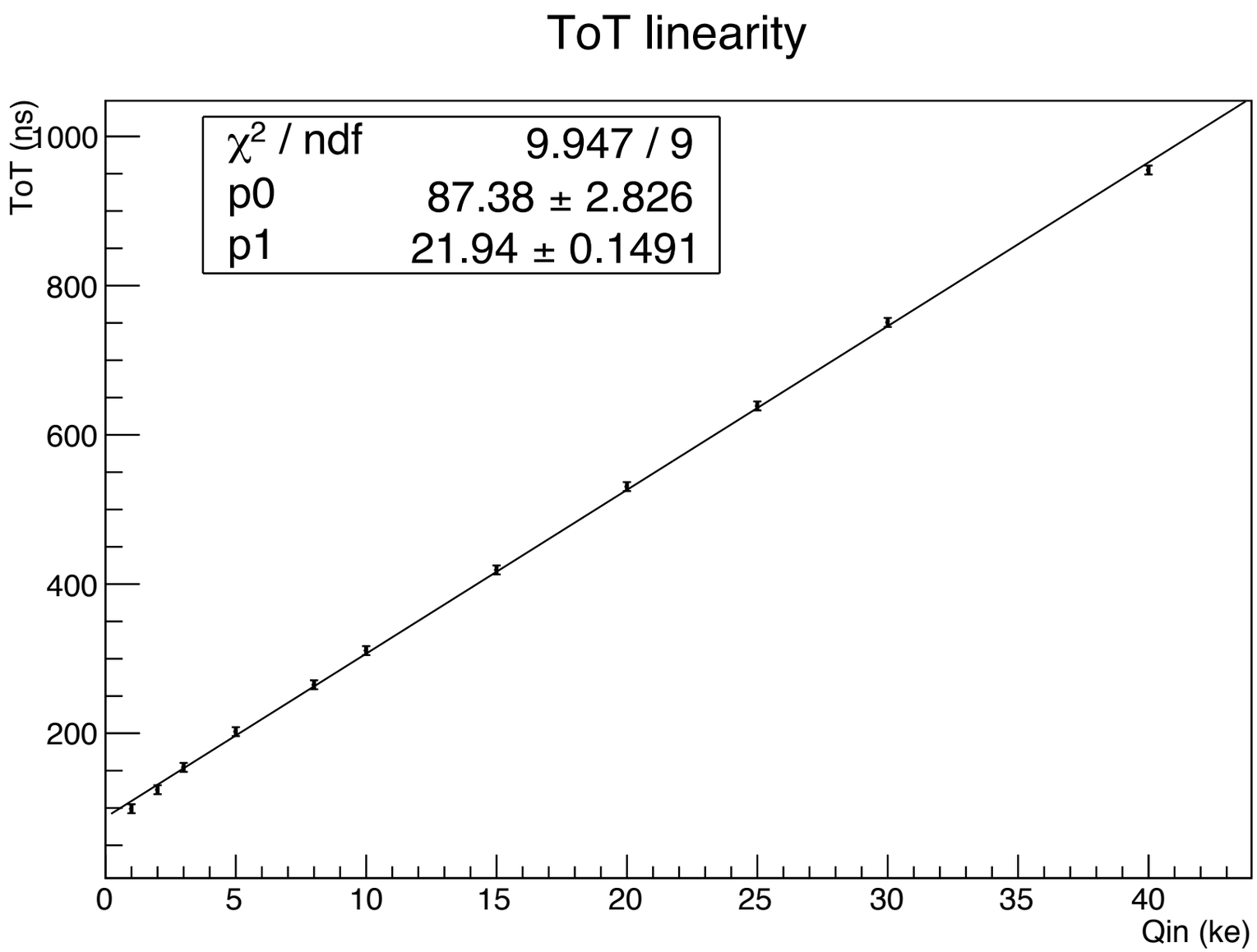
Comparator results

Input signal 10 ke$^-$ Threshold ≈ 1000 e$^-$



- Oscillator @ 100 MHz
- Time duration of the ToT output compatible with HIT in binary mode
- In the present version, oscillation speed can be tuned up to 500 MHz, but set-up bandwidth is limited to about 100 MHz

ToT linearity



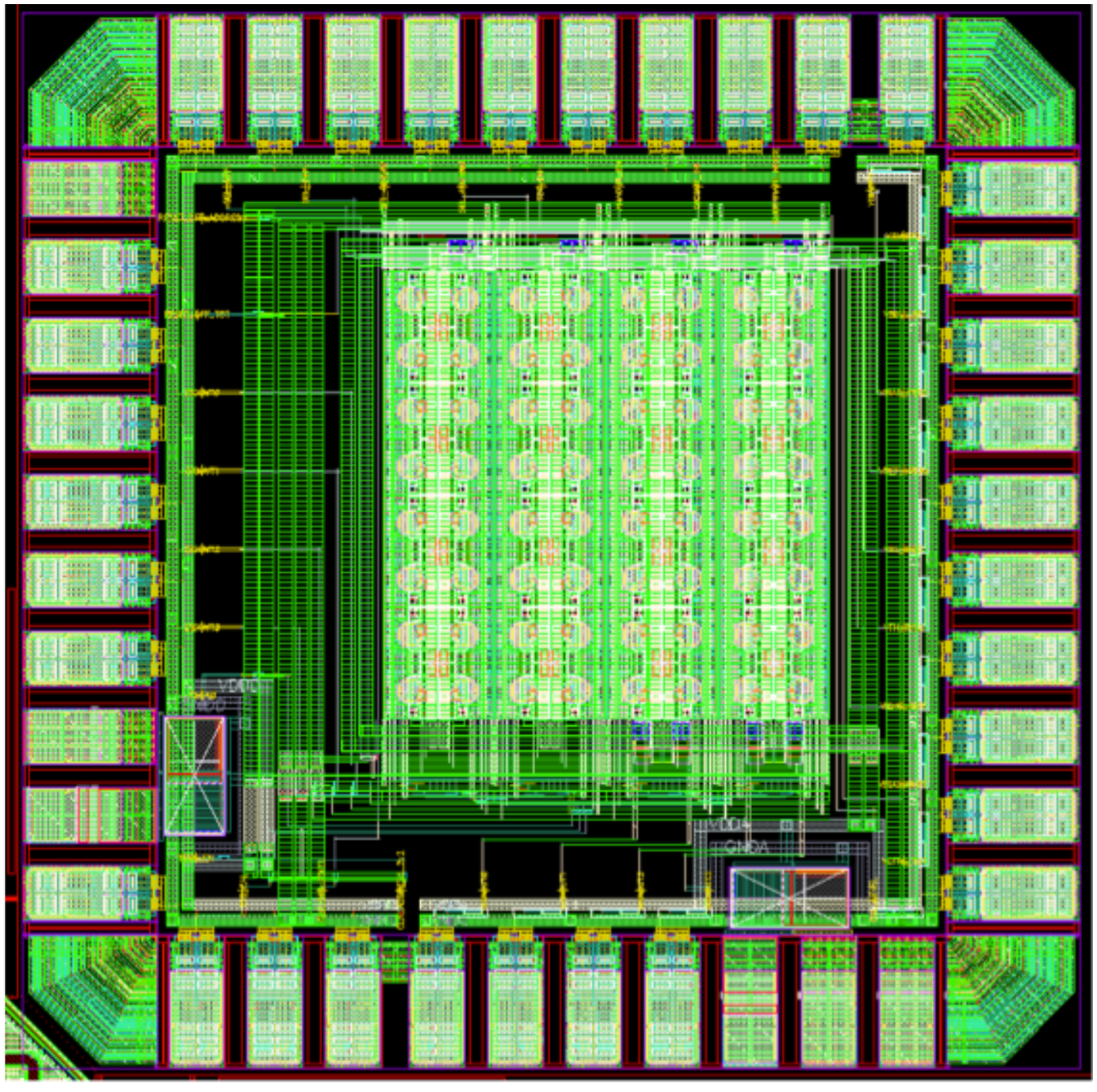
ToT is linear up to (at least) 40 ke$^-$

Conclusions and future plans

- First version of a synchronous front-end with offset compensation designed and tested
- Idea of “self-oscillating” comparator for fast ToT measurement works
- Good ToT linearity in a wide range of input signals
- Improved version submitted in May 2015
- Testing on the second version on the chip started this month

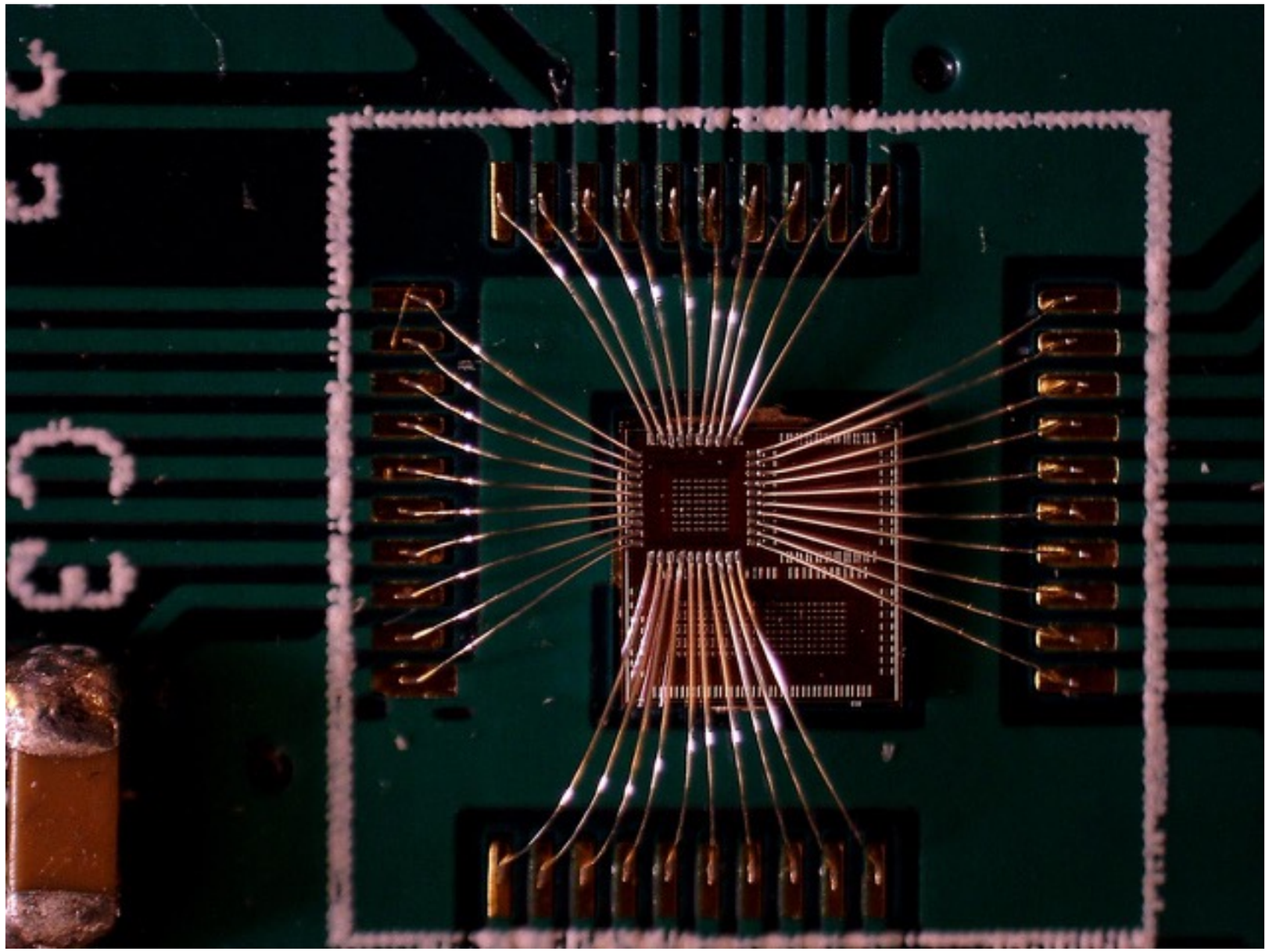
BACKUP

Pixel matrix with analog output



- 8x8 pixel matrix
  - 1/4 of the Mini@sic submitted in October and received in the end of January
- Readout of CSA output using analog buffering
- Readout of discriminator output using a digital buffer
- 4 pixel (2x2 region) are readout at the same time

Pixel matrix with analog output



Picture of the chip wire-bonded to the test board

Objectives

- Preamp:
  - Krummenacher feedback to compensate leakage currents up to 50 nA
  - Fast charge measurement

- Synchronous Comparator:
  - Eliminate time walk
  - “Hardware” Offset compensation using capacitors

- Different speed for ToT measurement:
  - FAST: ToT of 90 ns for Qin = 10 ke^- ==> OK for 2 GHz/cm^2
  - SLOW: ToT of 300 ns for Qin = 10 ke^- ==> OK for 0.5 GHz/cm^2 (~0.5% ineff.)
  - Choice depends on layer, sensor used and particle flux

Power consumption

- Static current around 3.5 uA
  - Preamplifier -> 2.5 uA
  - Discriminator -> 1 uA

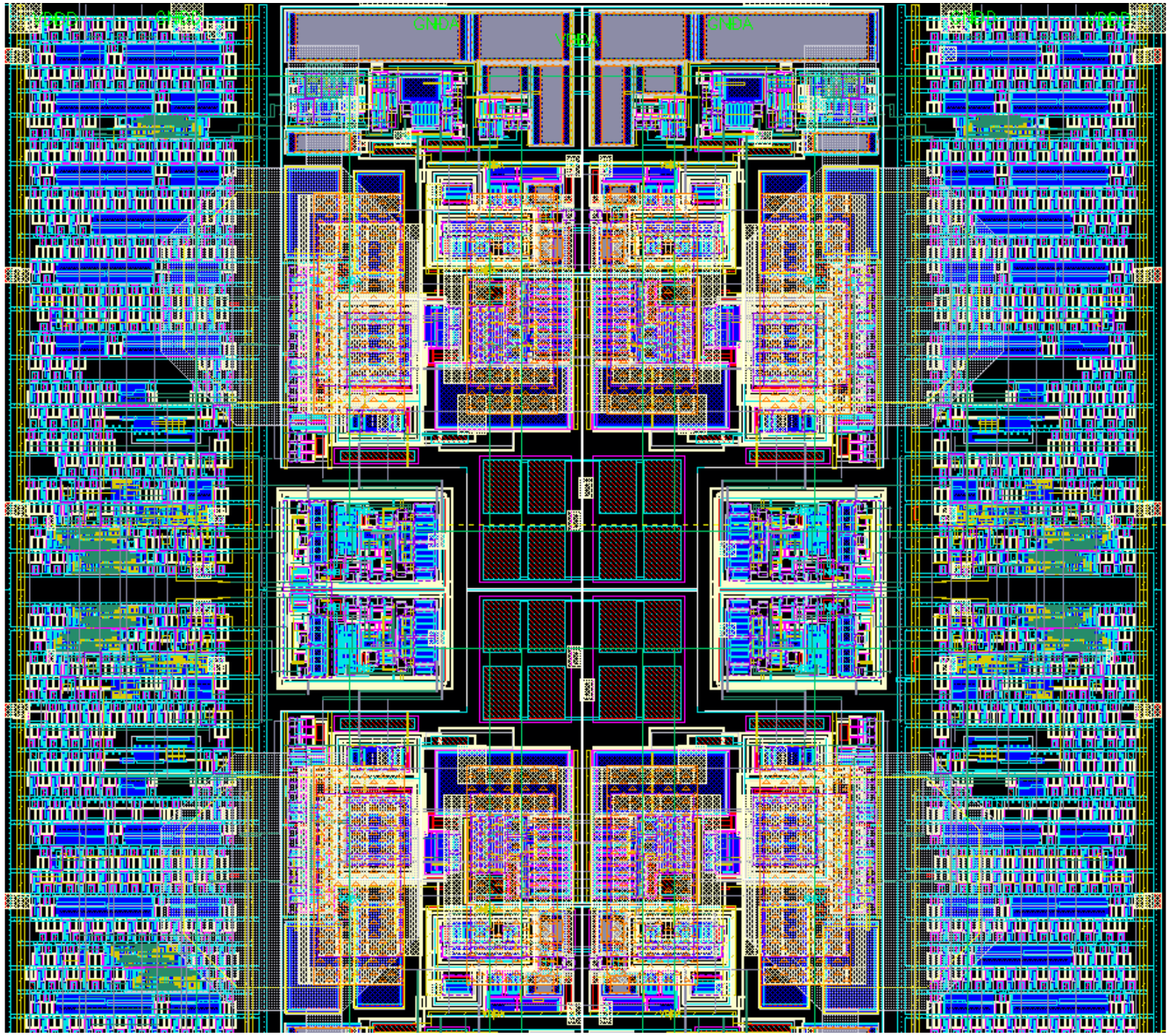
- Dynamic current (latch) around 0.8 uA

- The average total current is around 4.3 uA per pixel

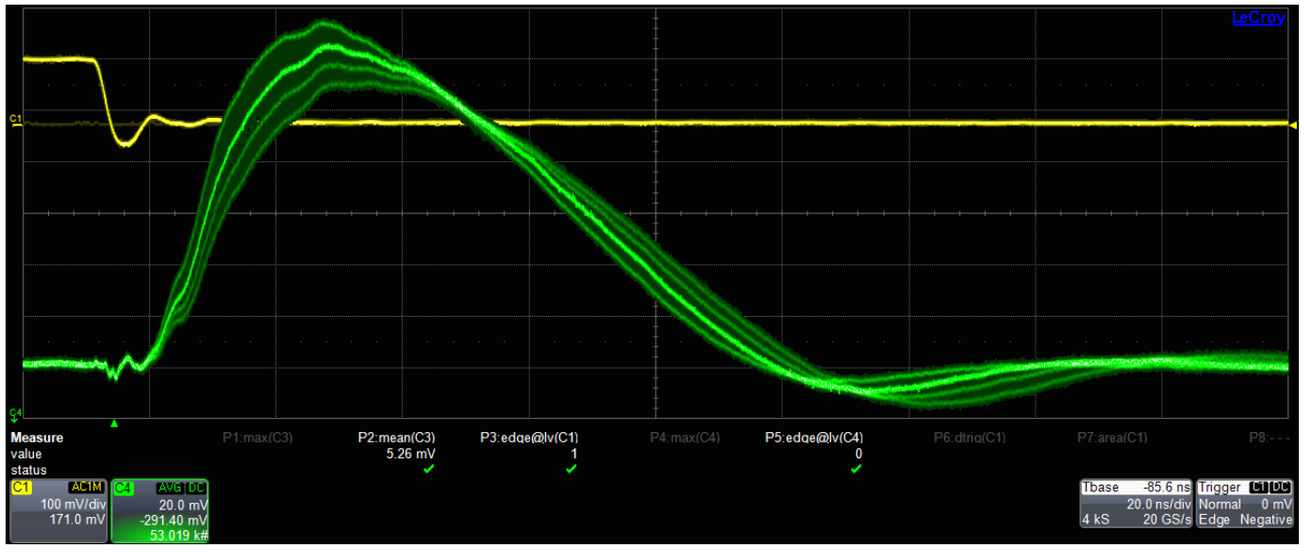
- Considering VDD = 1.2 V the total power consumption is around 5.2 uW
  - It corresponds to around 0.2 W/cm^2 considering a 50x50 um^2 pixel
  - OK ~ 50% of the 0.4 W/cm^2 required

- This configuration has been used for the measurements showed in this presentation

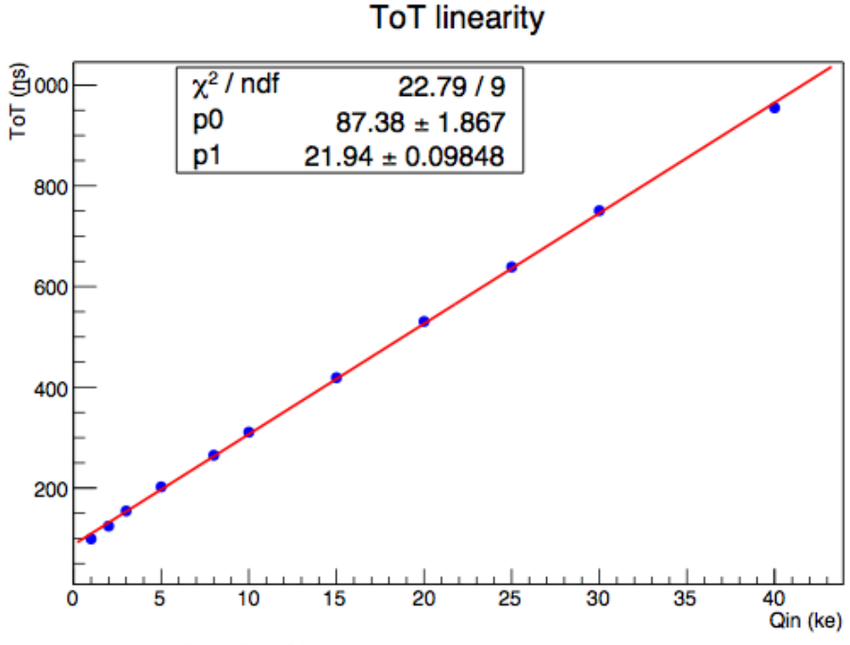
VFE layout - v2 - 2x2 region



Measurements on First Prototype

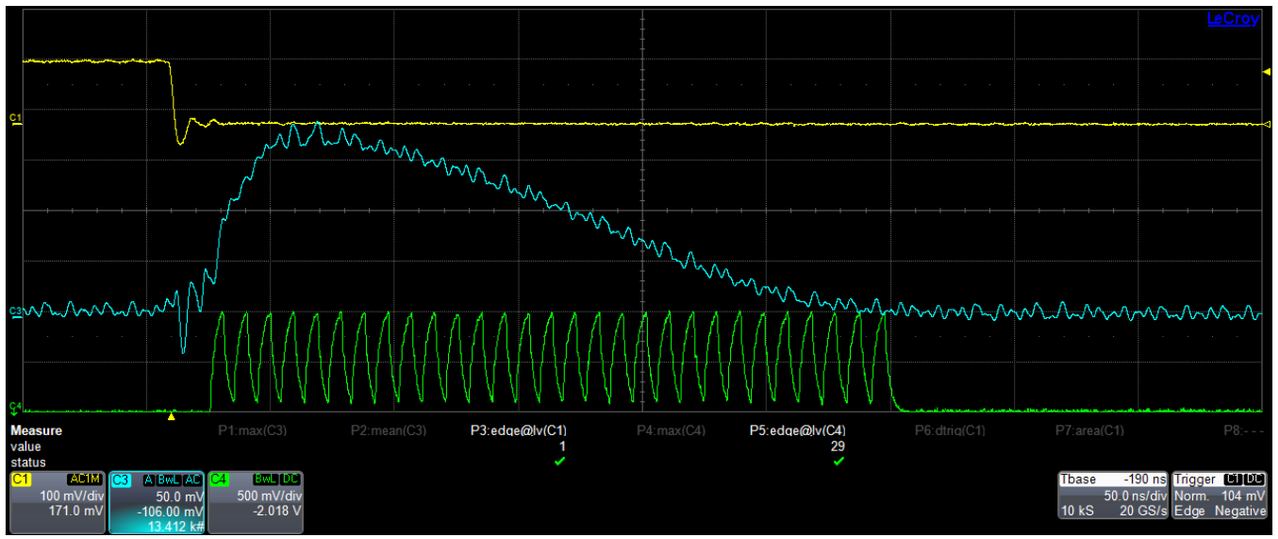


Analog-Out Q=10ke-, ToT=90ns

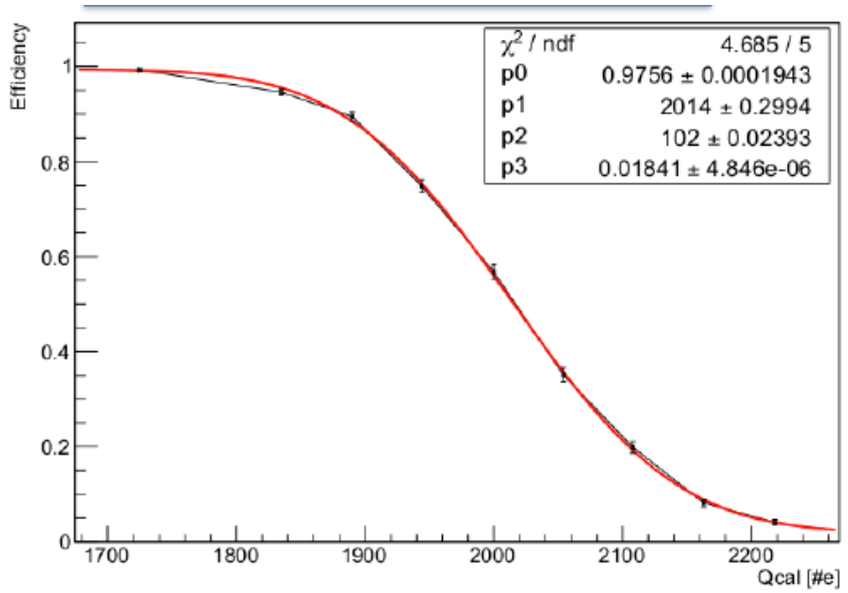


ToT linear up to >40ke

Measurement with Very-Fast ToT

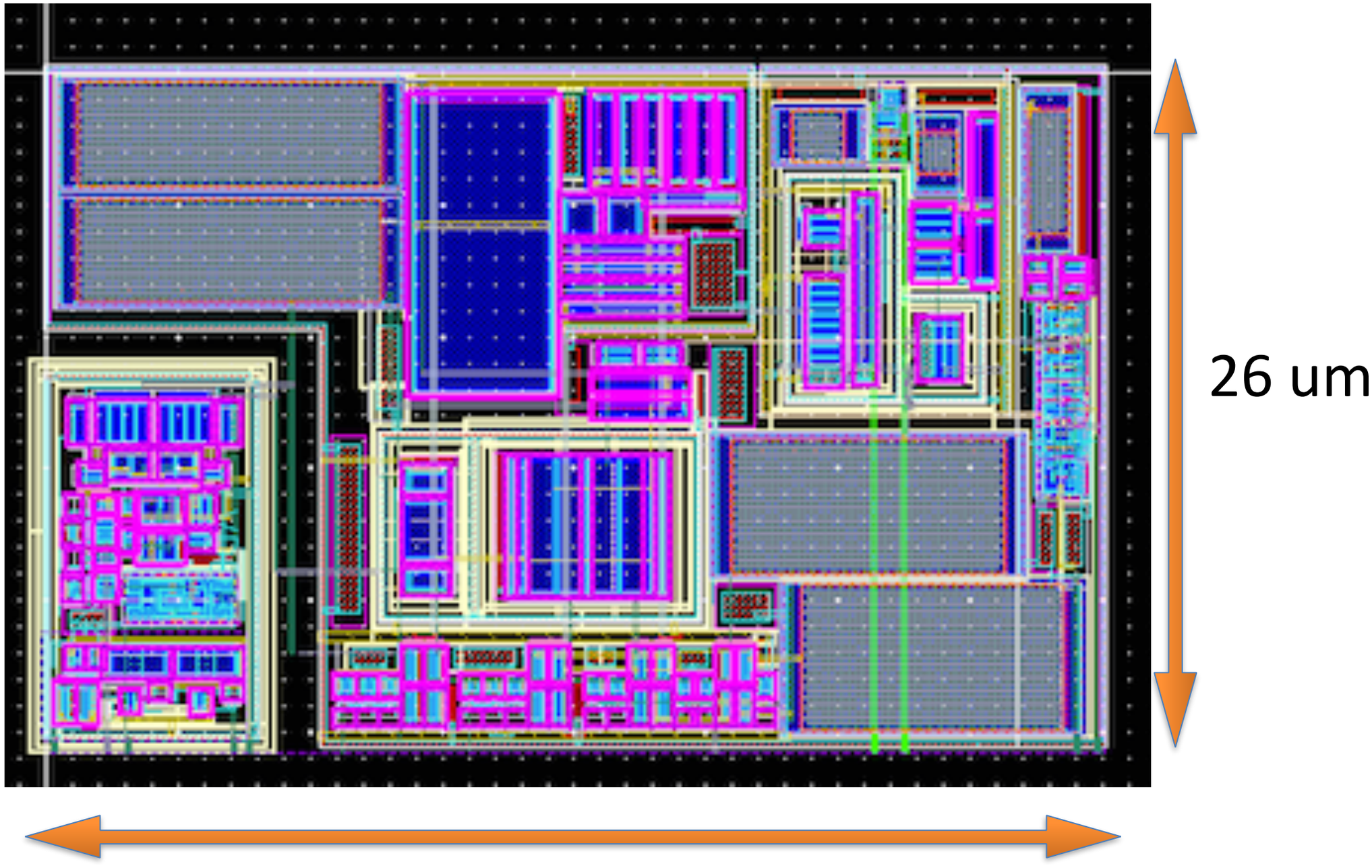


Fast ToT: oscillator counting ToT ; threshold @1ke-
100 MHz (limited by analog readout and set-up)



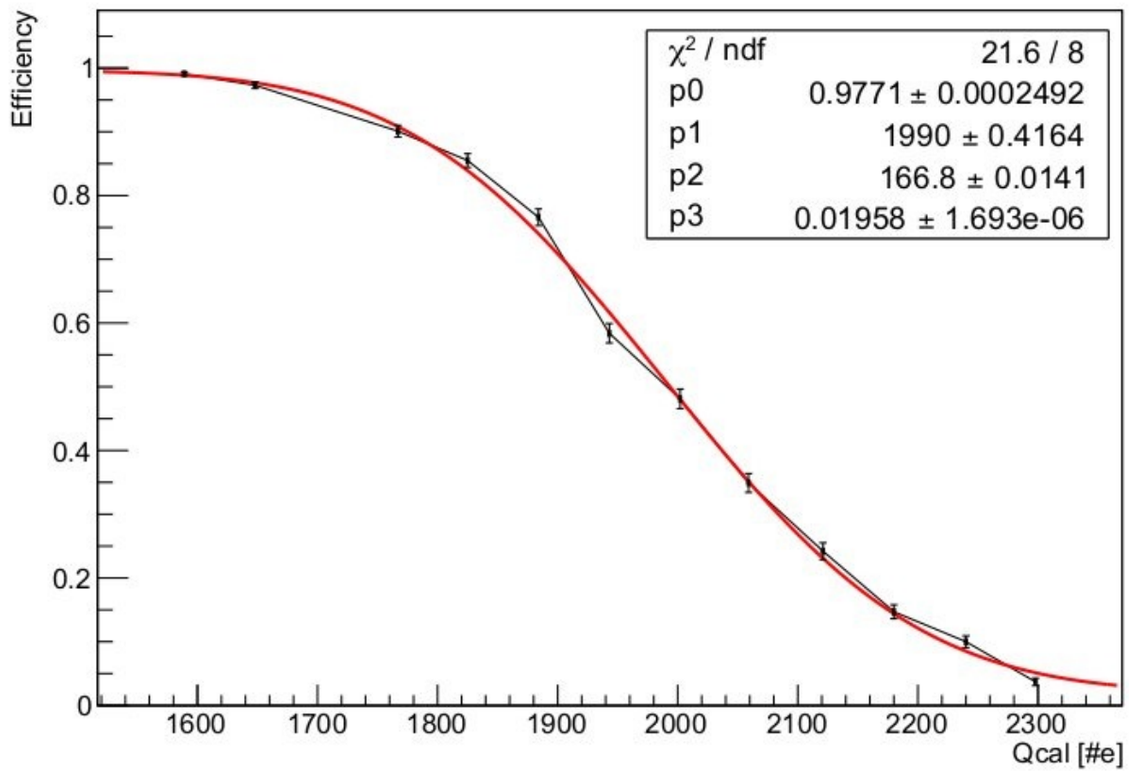
ENC~100e$^-$ for C_{det}~130fF
for Standard ToT

VFE layout - v2

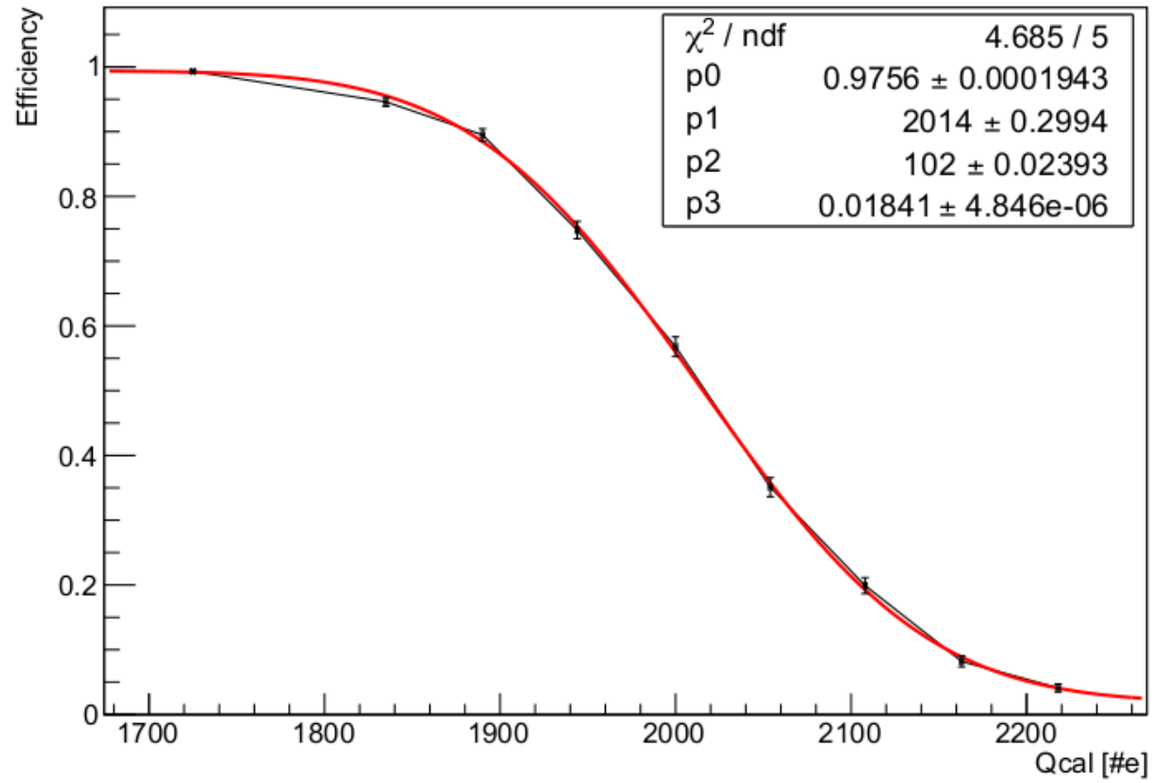


Noise @ Cin = 130 fF

Ifeed = 40 nA (FAST ToT) Cinput = 130 fF



Ifeed = 10 nA (SLOW ToT) Cinput = 130 fF

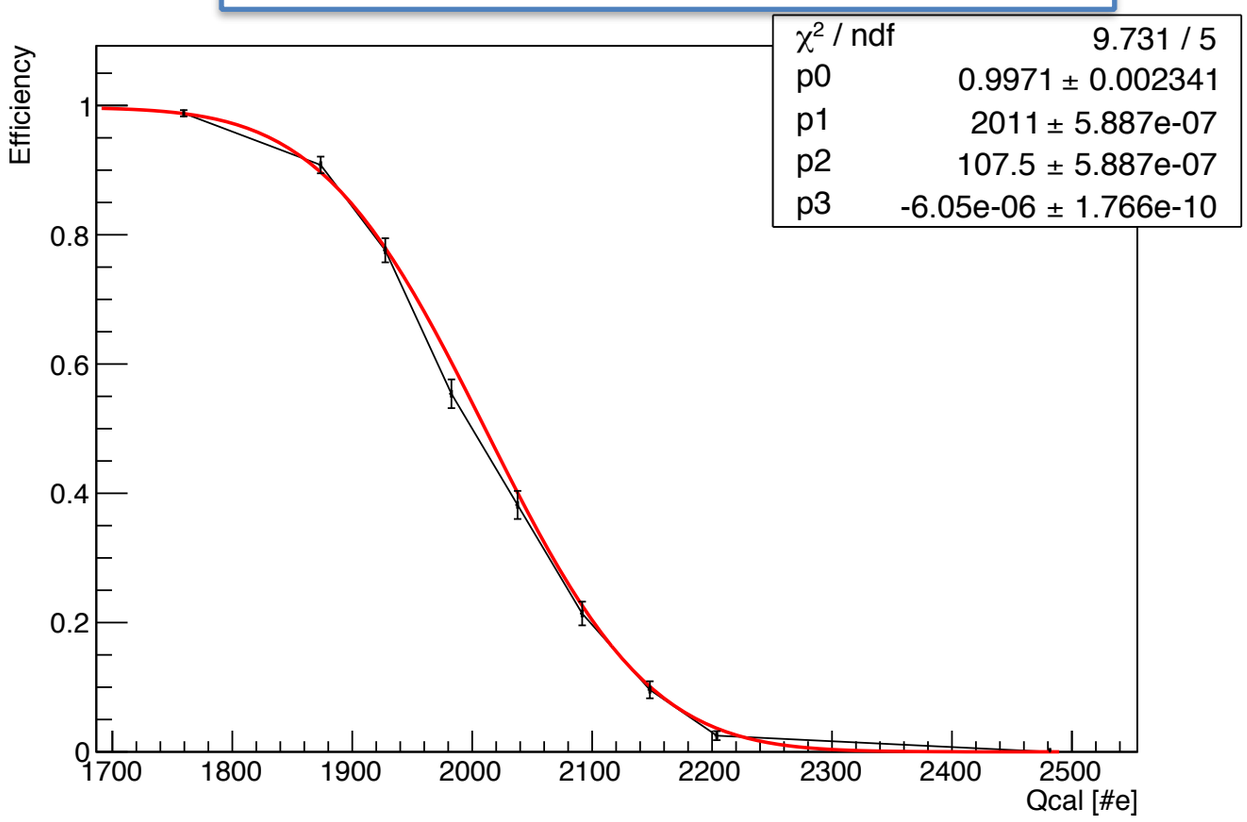


- ENC ~ 167 e^- @ Ifeed = 40 nA (fast), Cinput = 130 fF
- ENC ~ 102 e- @ Ifeed = 10 nA (slow), Cinput = 130 fF

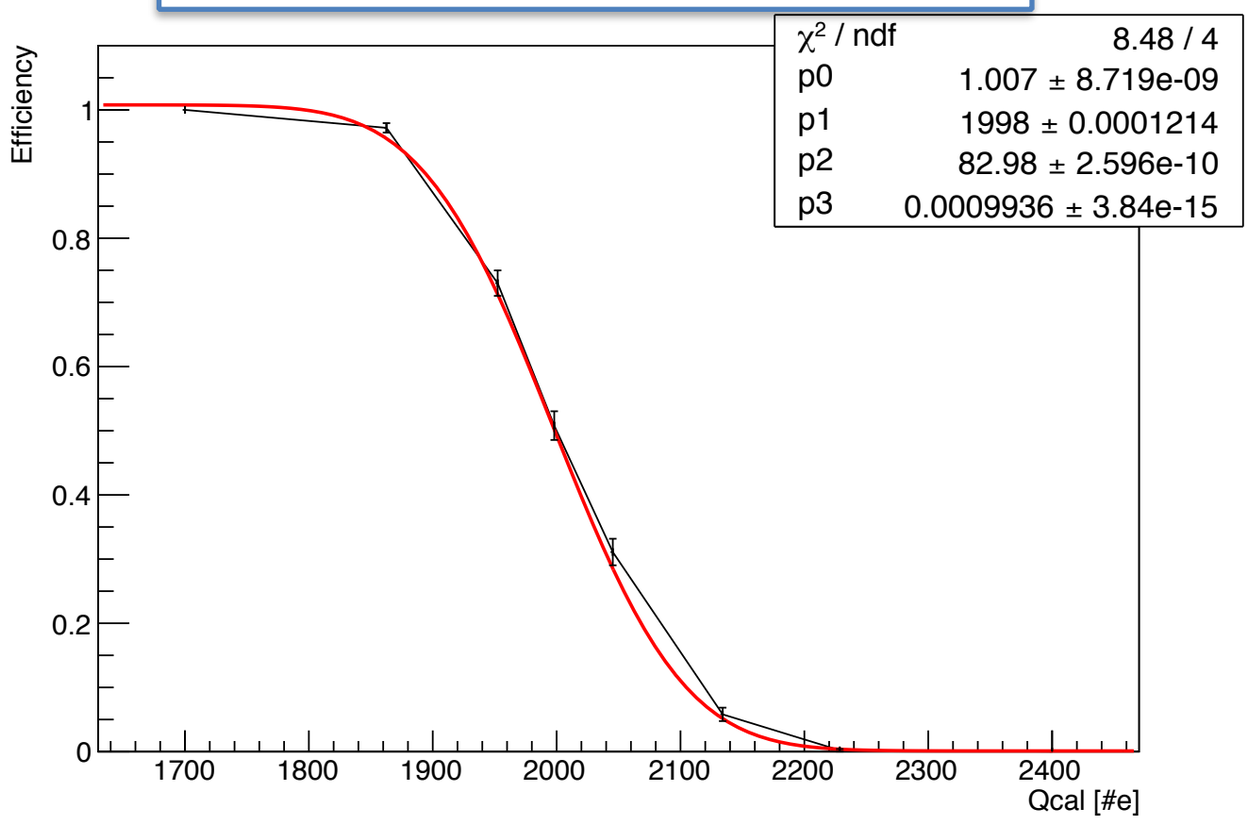
- Measurement performed with the clock activated

Noise @ Cin = 50 fF

Ifeed = 40 nA (FAST ToT) Cinput = 50 fF



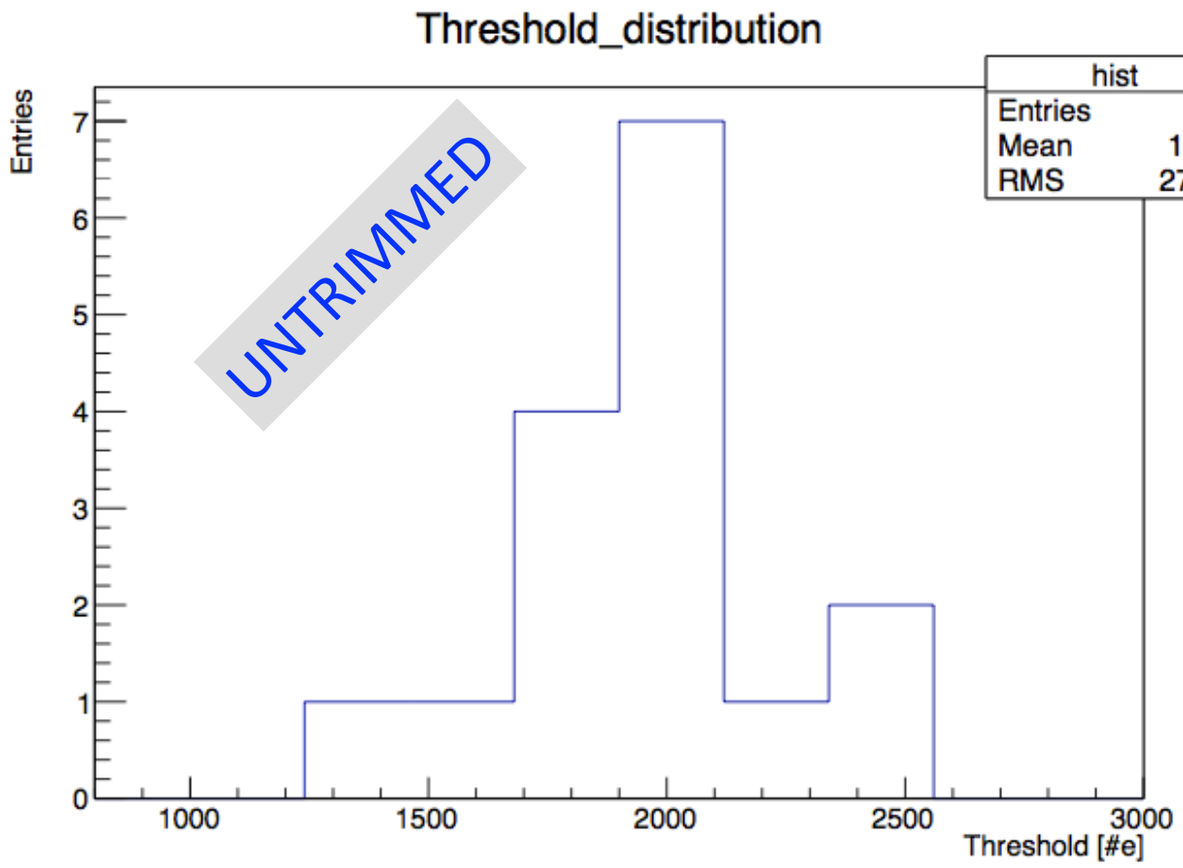
Ifeed = 10 nA (FAST ToT) Cinput = 50 fF

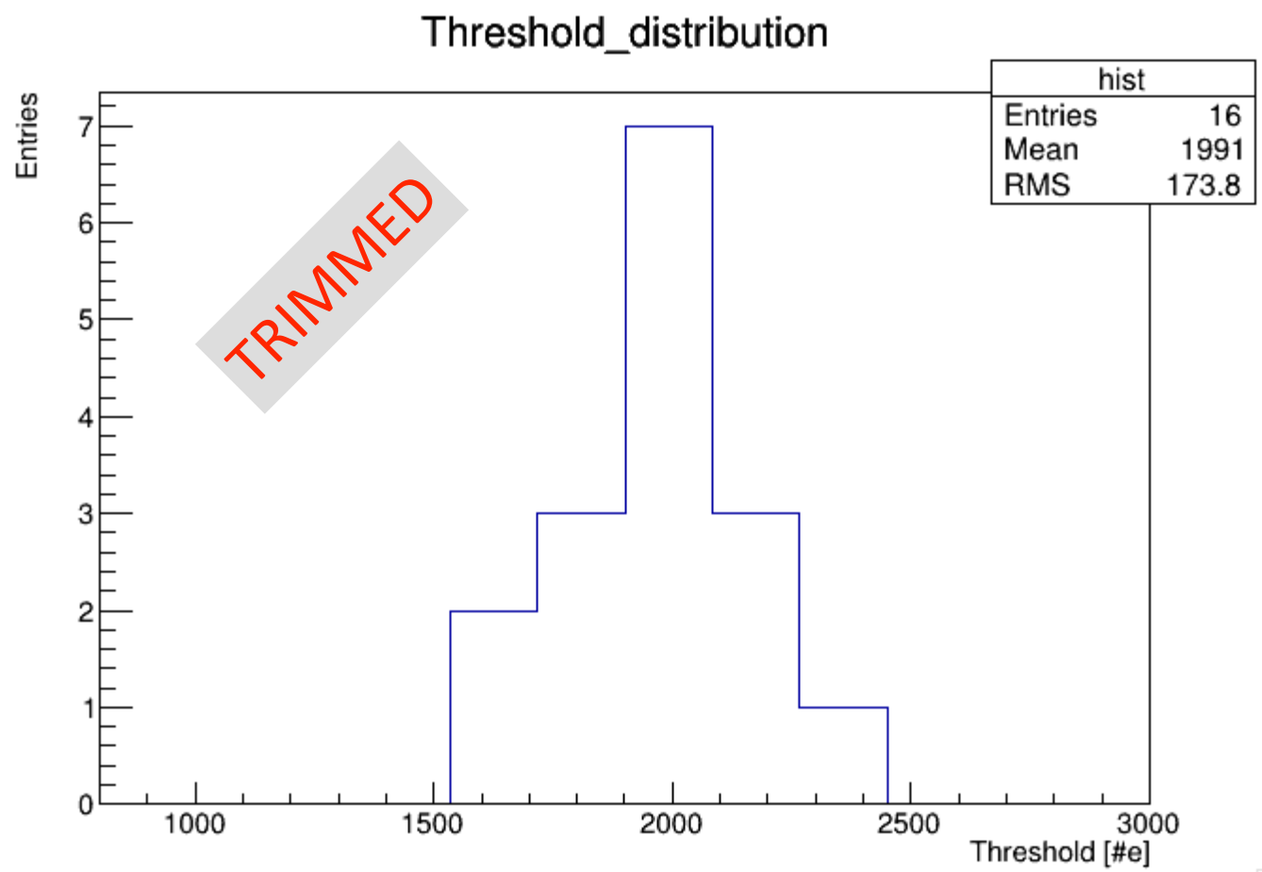


- ENC ~ 108 e^- @ Ifeed = 40 nA (fast), Cinput = 50 fF
- ENC ~ 83 e- @ Ifeed = 10 nA (slow), Cinput = 50 fF

- Measurement performed with the clock activated

Offset compensation





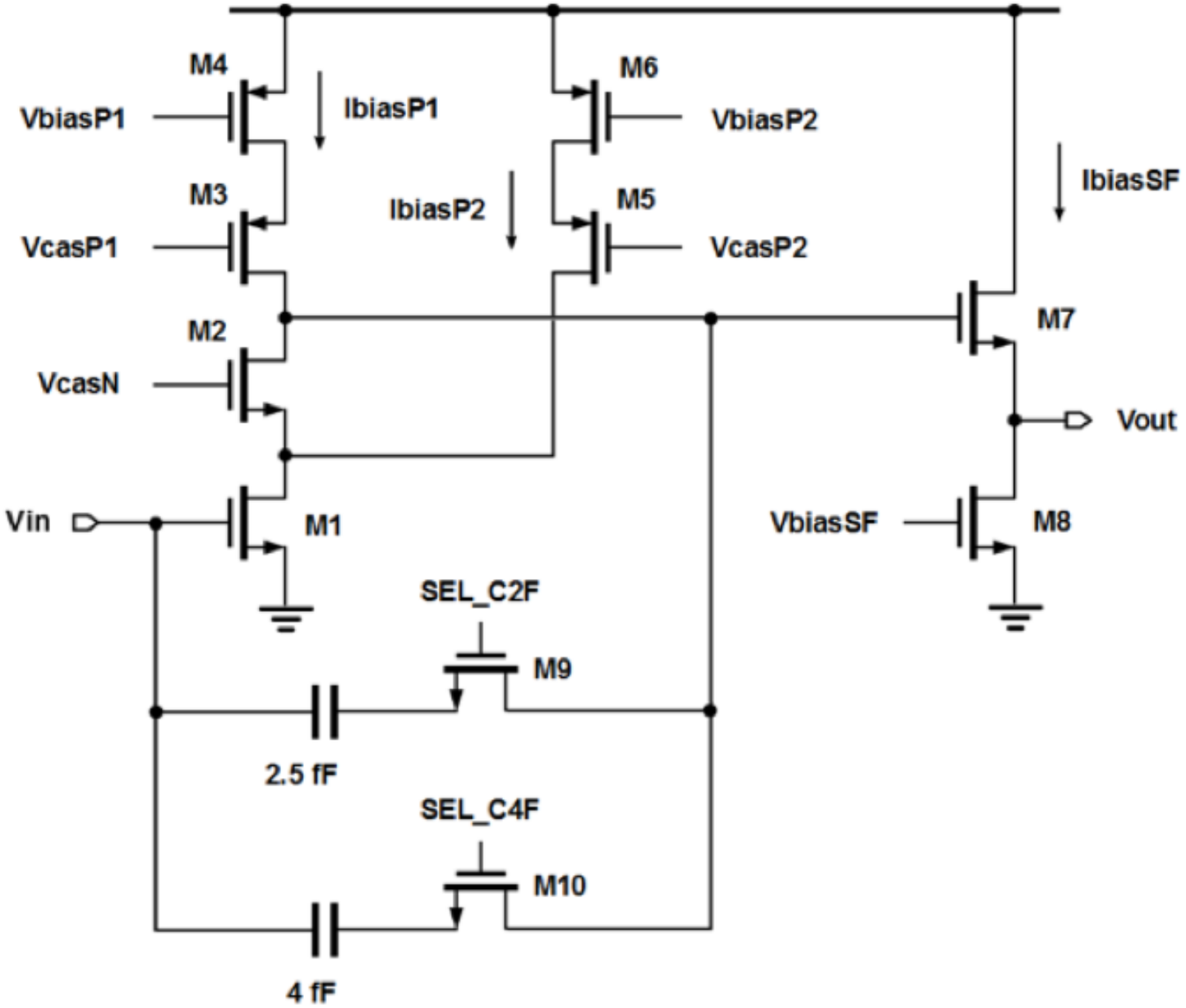
☹ It could be better

☺ We have understood the problems

- Too high gain fluctuations due to mismatch
- Underestimation of the latch dynamic offset

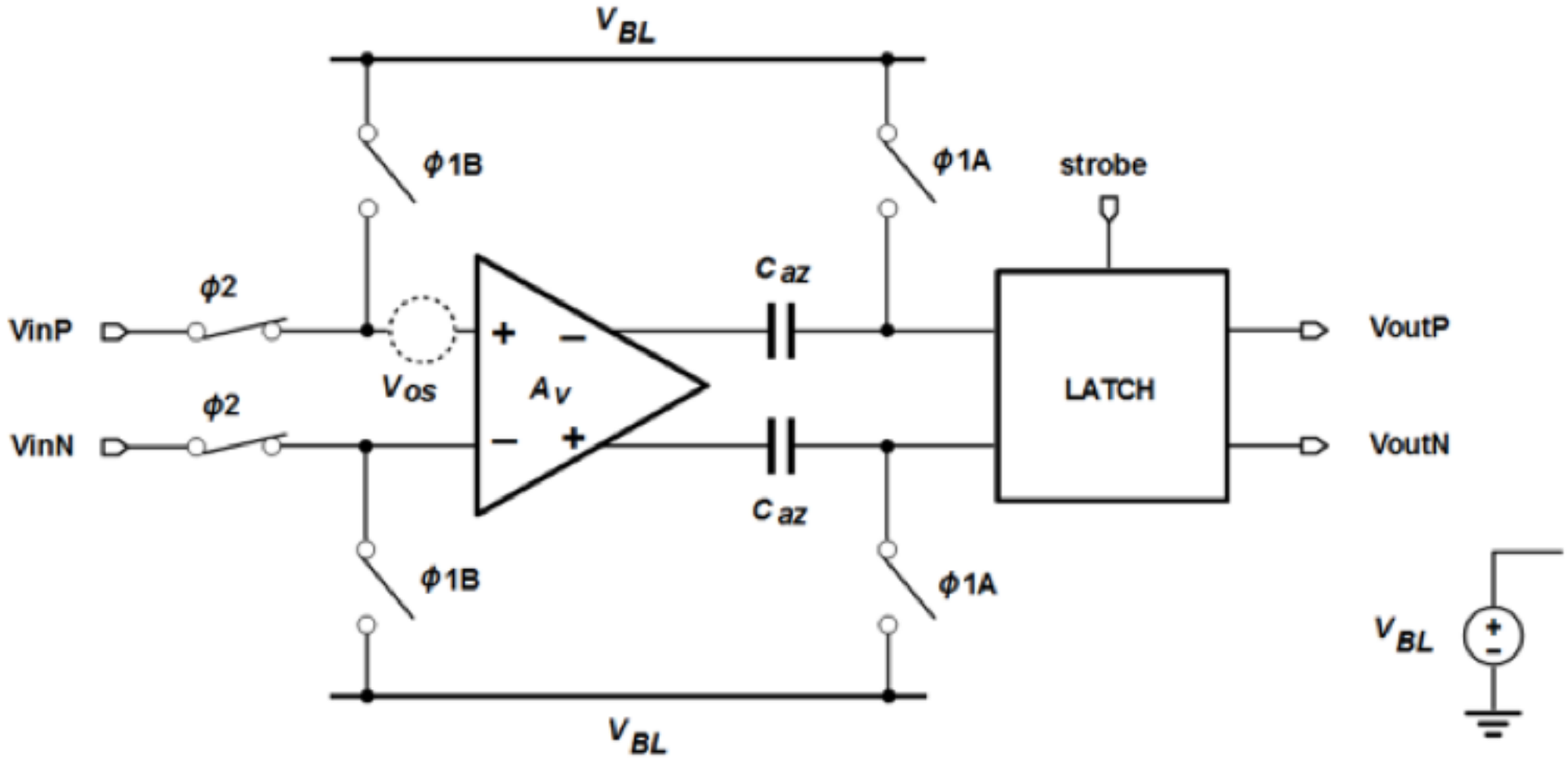
⇨ **Solved in version 2**

CSA schematic



Cascode with current splitting and source follower

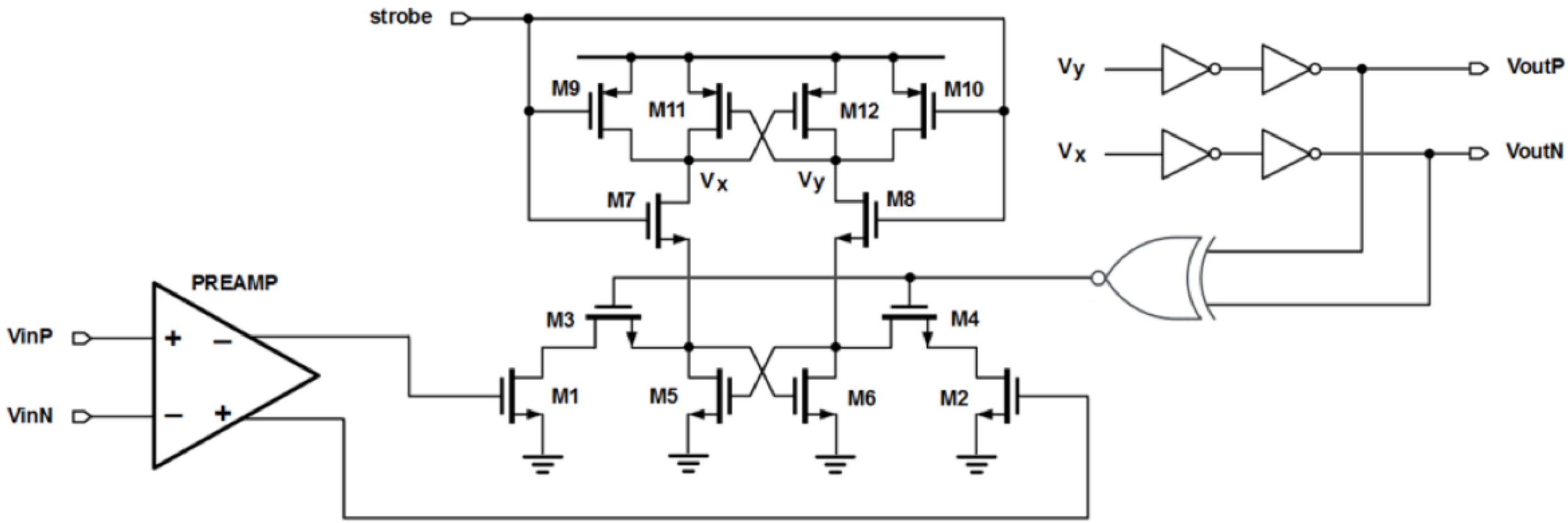
Synchronous Discriminator with offset compensation



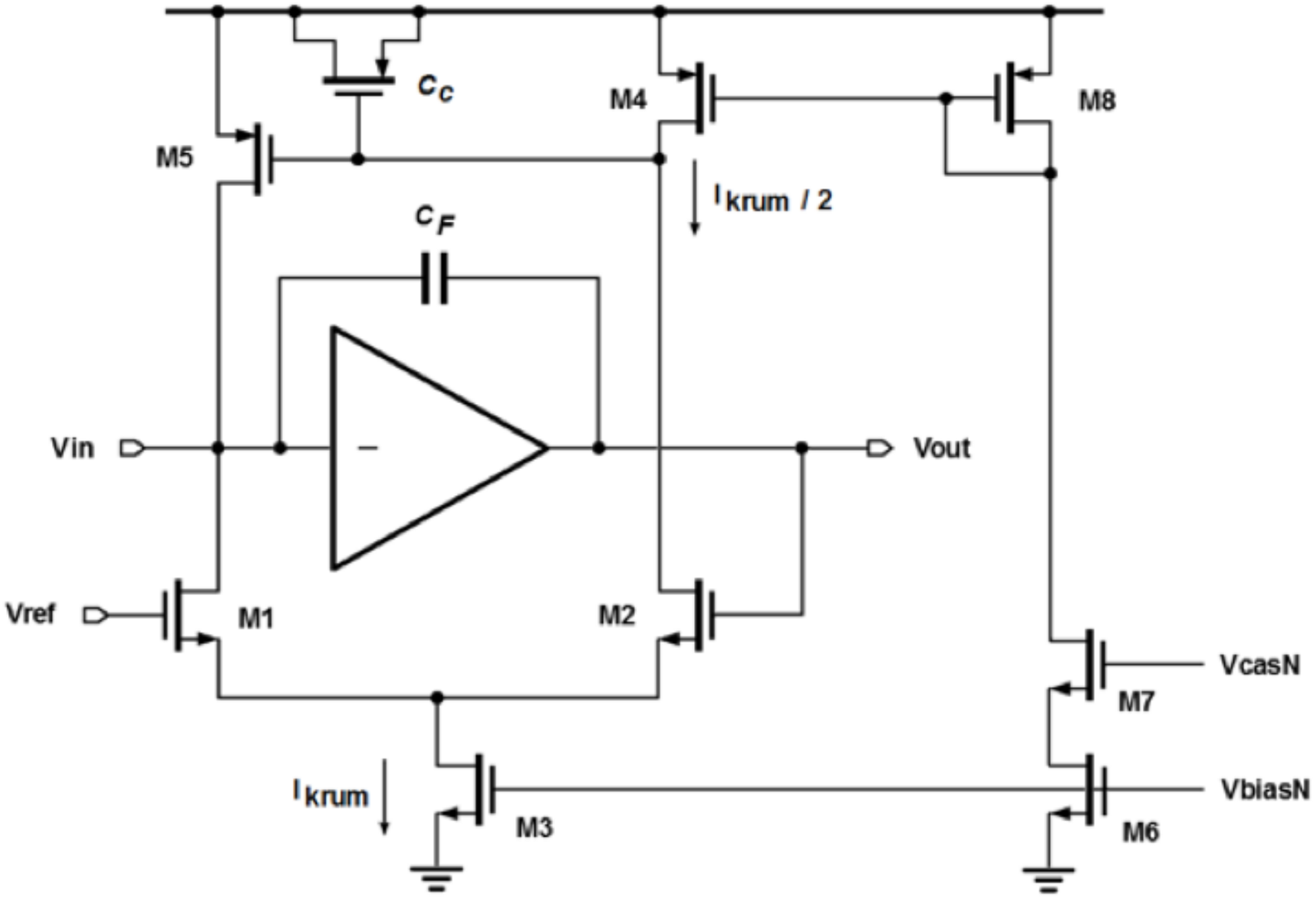
No more need of threshold trimming

- Why?
  - AC coupling between CSA and comparator and offset compensation technique

Latch

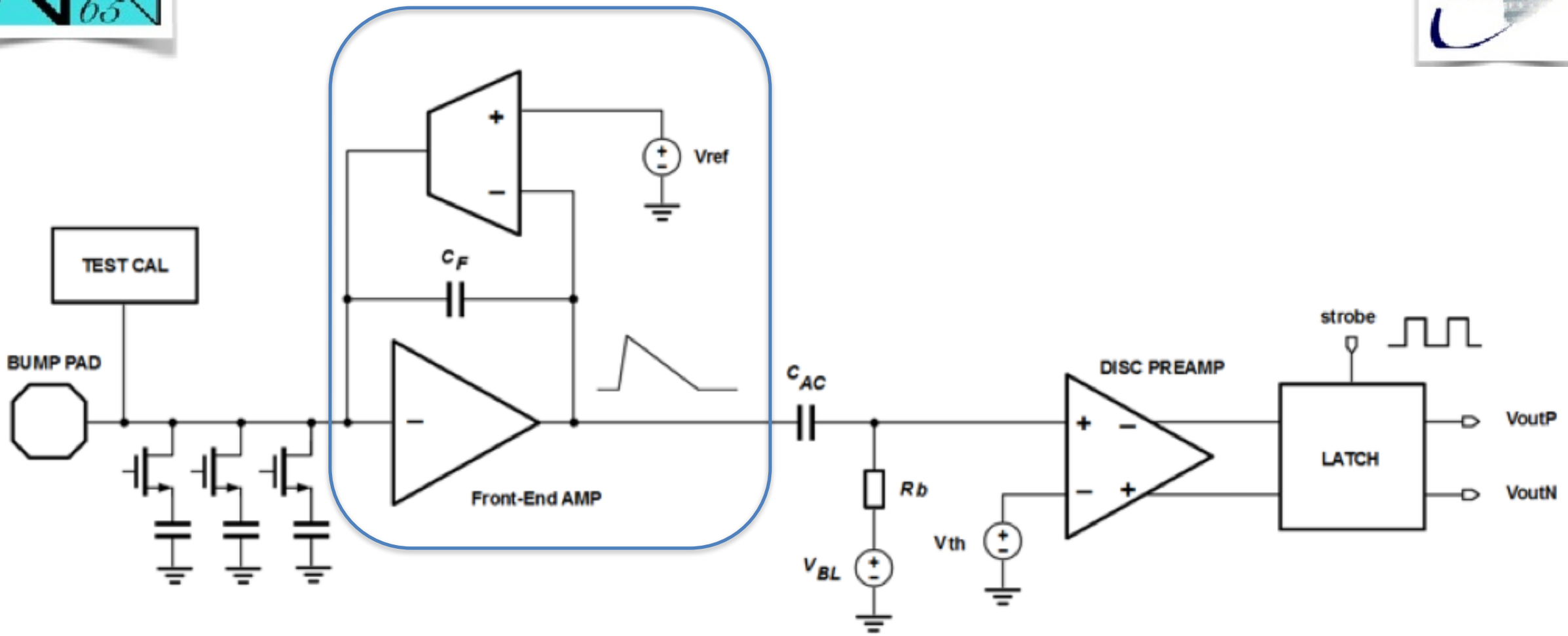

strobe
M9
M11
M12
M10
Vx
Vy
M7
M8
Vy
Vx
VoutP
VoutN
PREAMP
VinP
VinN
M3
M4
M1
M5
M6
M2

Krummenacher



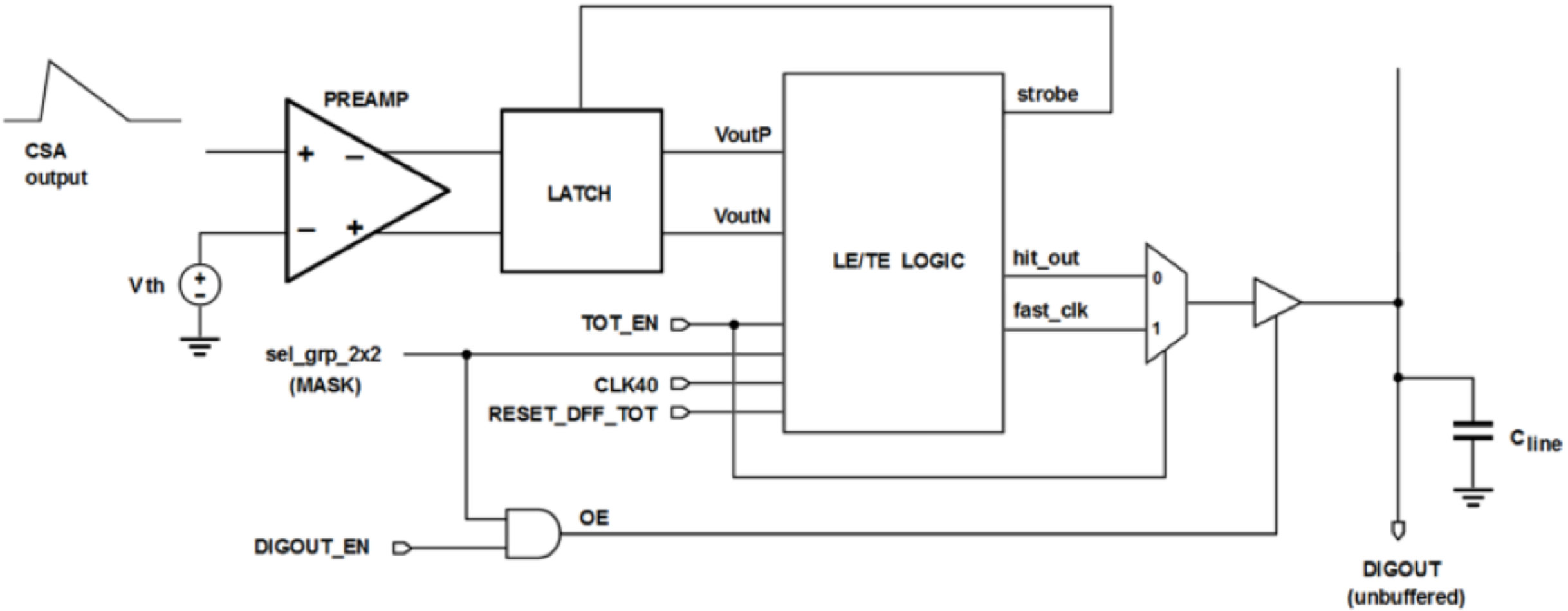
Cascode with current splitting and source follower

Preamp



- Preamp
  - One stage Charge Sensitive Amplifier
  - Krummenacher feedback to compensate leakage currents up to 50 nA
  - Selectable feedback capacitance (2.5,4,6.5 fF)

Hit Logic



Fast ToT: comparator turned into local oscillator using an asynchronous logic feedback loop