INFN Istituto Nazionale di Fisica Nucleare

ALICE

# Il nuovo tracciatore a pixel monolitici di silicio dell'esperimento ALICE a LHC del CERN

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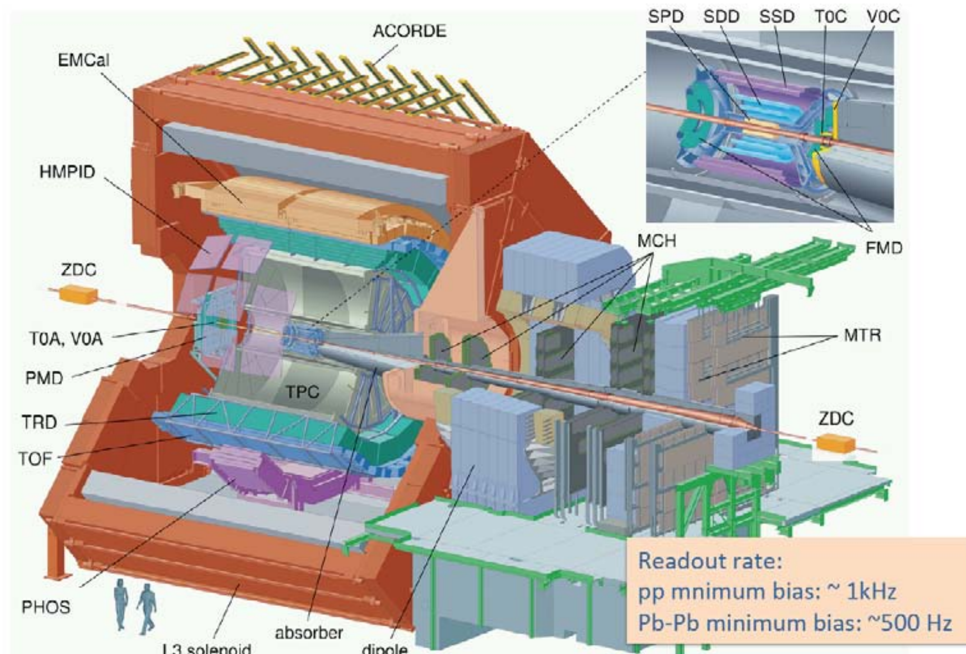
*INFN e Università di Bari*
*per la collaborazione ALICE Italia*

## OUTLINE

- ❖ Strategie dell’upgrade di ALICE
- ❖ Perché l’upgrade dell’ attuale Inner Tracking System
- ❖ Layout del nuovo rivelatore e i suoi principali componenti
- ❖ Conclusioni

# Strategie dell'upgrade di ALICE

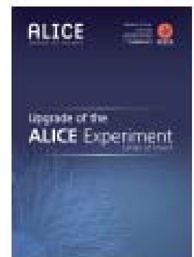



**Target dell'upgrade di ALICE** (previsto durante 2° Long Shutdown 2018/19):

1. Upgrade dei rivelatori, sistemi di readout e sistemi online
   per aumentare frequenze readout fino a **50 kHz** per interazioni Pb-Pb (luminosità superiore a $7 \times 10^{27}$ $cm^{-2}s^{-1}$) e aggiornamento sistemi on-line per processare eventi Pb-Pb con trigger minimum bias

2. Migliore risoluzione sui vertici, soprattutto a basso $p_T$

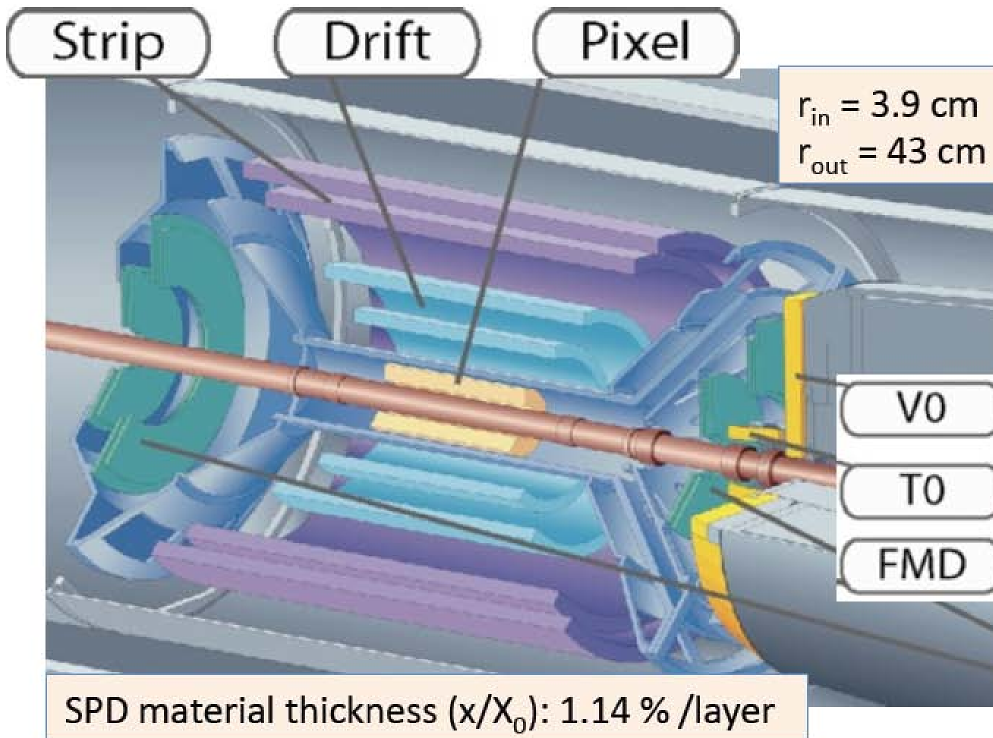
2. Maggior efficienza nel tracciamento

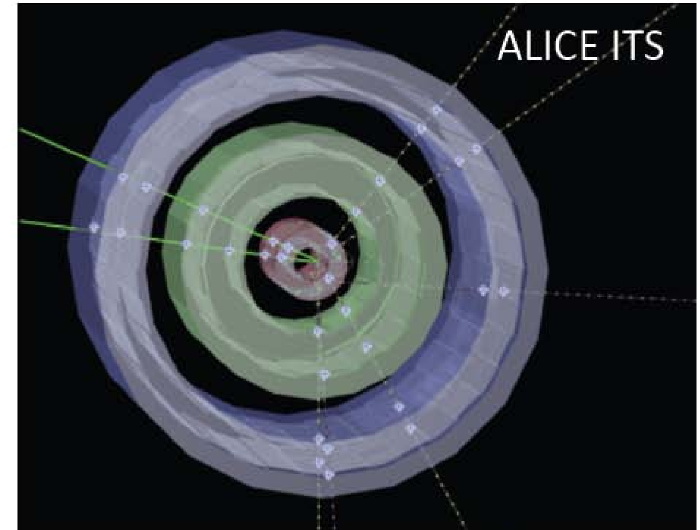


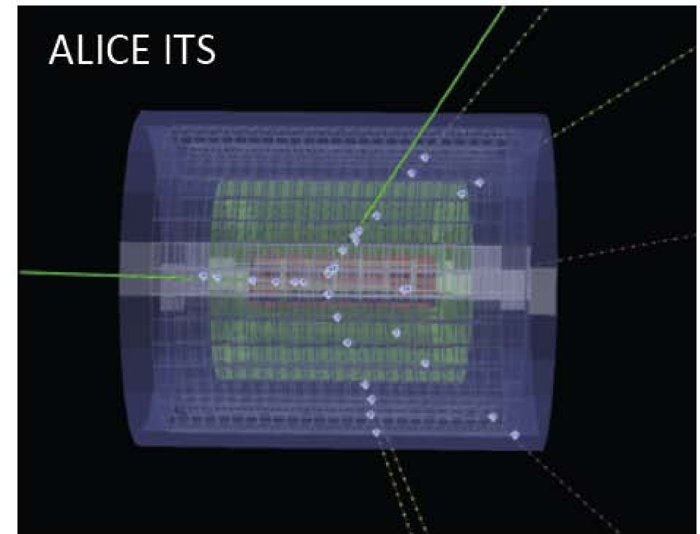

ALICE upgrade LoI
September 2012

Addendum
September 2013

# L'attuale rivelatore di ALICE: Inner tracking System




Current ITS

6 concentric barrels, 3 different technologies

- 2 layers of silicon pixel (SPD)
- 2 layers of silicon drift (SDD)
- 2 layers of silicon strips (SSD)

# Perché l'upgrade dell' attuale ITS

1. **Migliorare la risoluzione spaziale di un fattore ≈ 3**

- Avvicinare il più possibile lo strato più interno del rivelatore al IP (39 mm ➡ 22 mm)
- riduzione di un fattore ≈ 4 su material budget strati più interni(≈ 1.14 % ➡ 0.3 % )
-ridurre dimensione del singolo pixel (da 50×425 $\mu m^2$ a 30×30 $\mu m^2$)

2. **Migliorare efficienza tracciamento e risoluzione sui bassi valori di pT**

- una più fitta granularità: uno strato di rivelatori in più e una ridotta dimensione del pixel
-una globale riduzione del "material-budget/layer"

3. **Readout veloce**

-readout Pb-Pb ad almeno 50 kHz, e p-p ≈ 400 kHz

4. **Inserzione/rimozione veloce per manutenzione.**

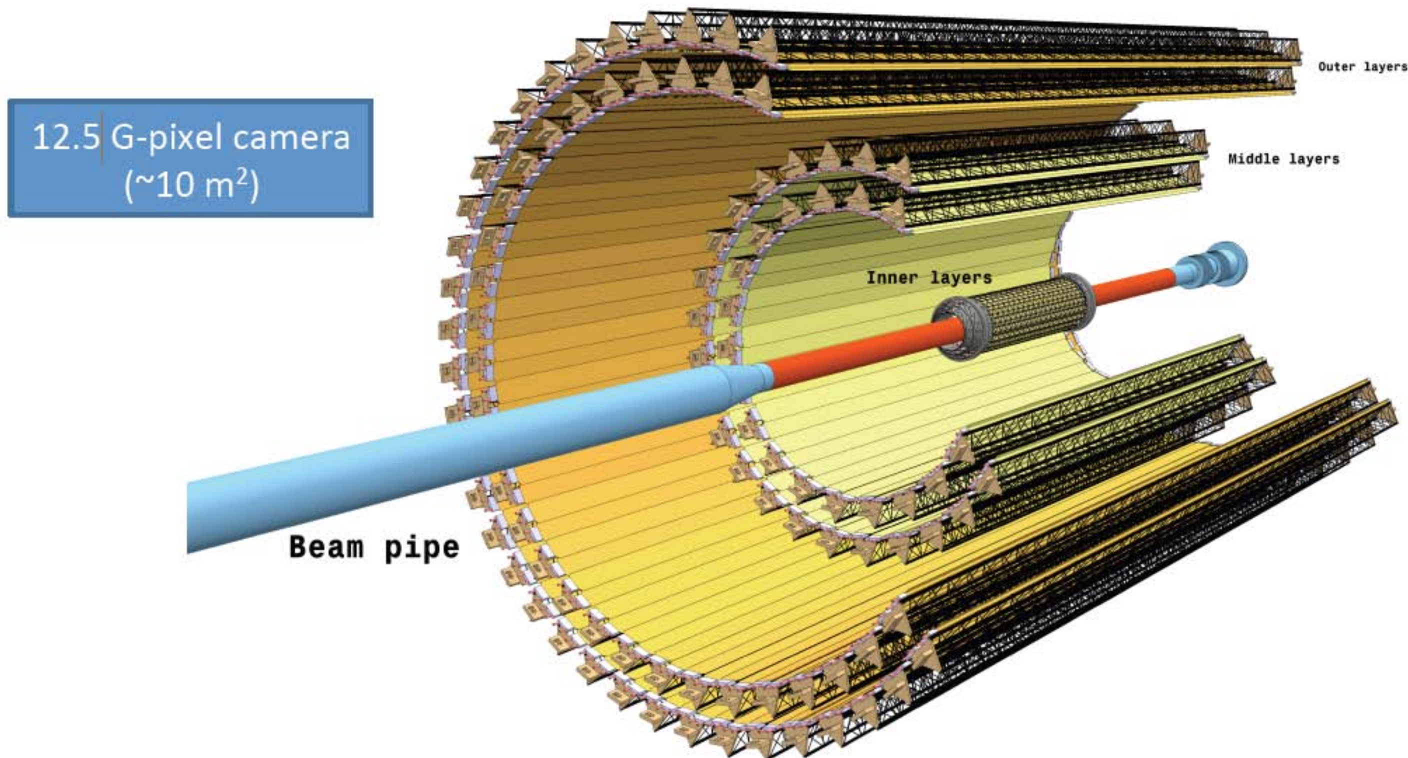
- Possibilità di sostituire moduli del detector non funzionanti durante lo shutdown annuale

**Installazione del detector durante LHCC LS2 (2018-2019)**

*CERN-LHCC-2013-24*

*J. Phys. G (41) 087002*

# Layout del nuovo rivelatore e i suoi principali componenti




7-layer barrel geometry based on MAPS

r coverage: 23 – 400 mm

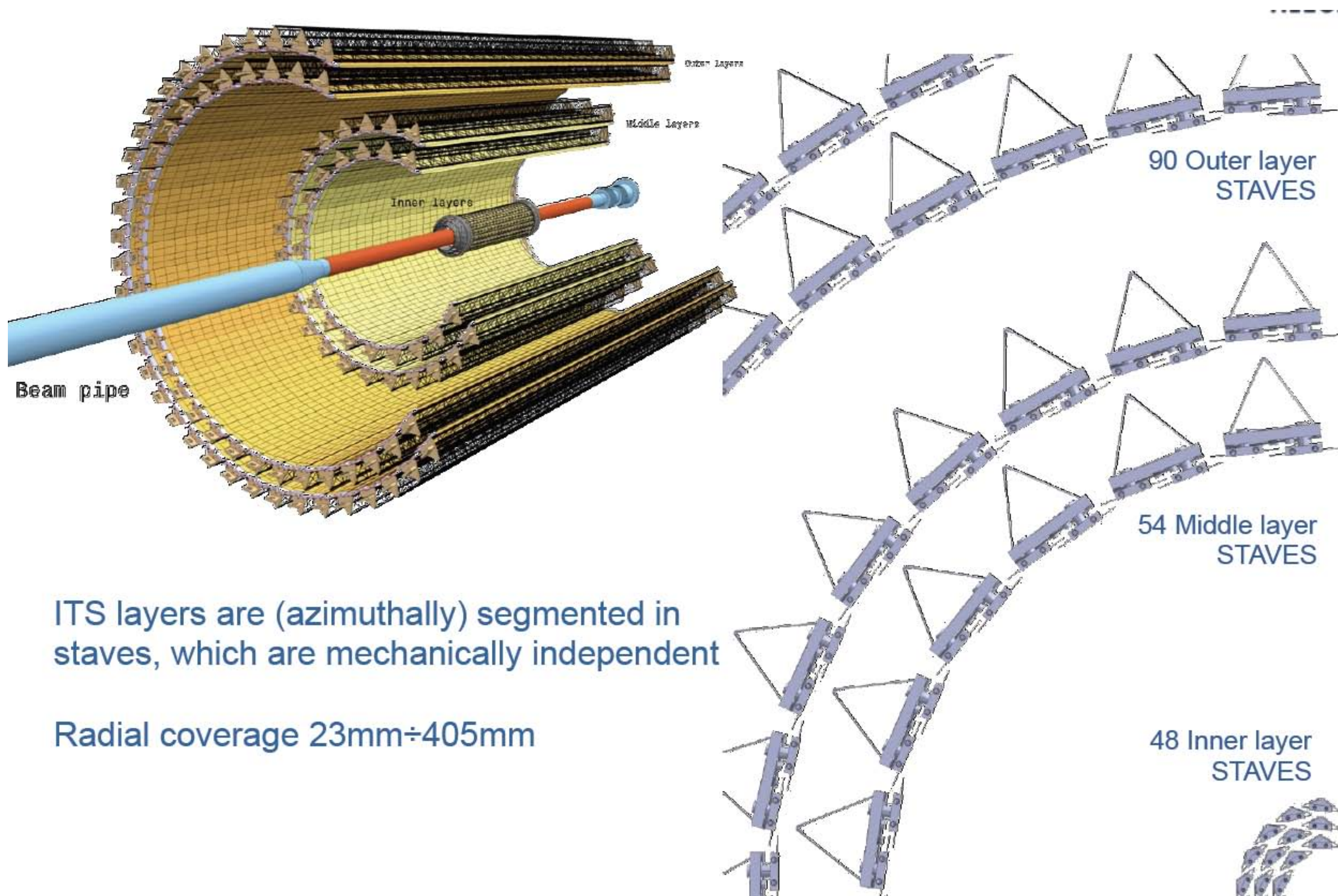
$\eta$ coverage: $|\eta| \leq 1.22$
for tracks from 90% most luminous region

**3** Inner Barrel layers (**IB**)

**4** Outer Barrel layers (**OB**)

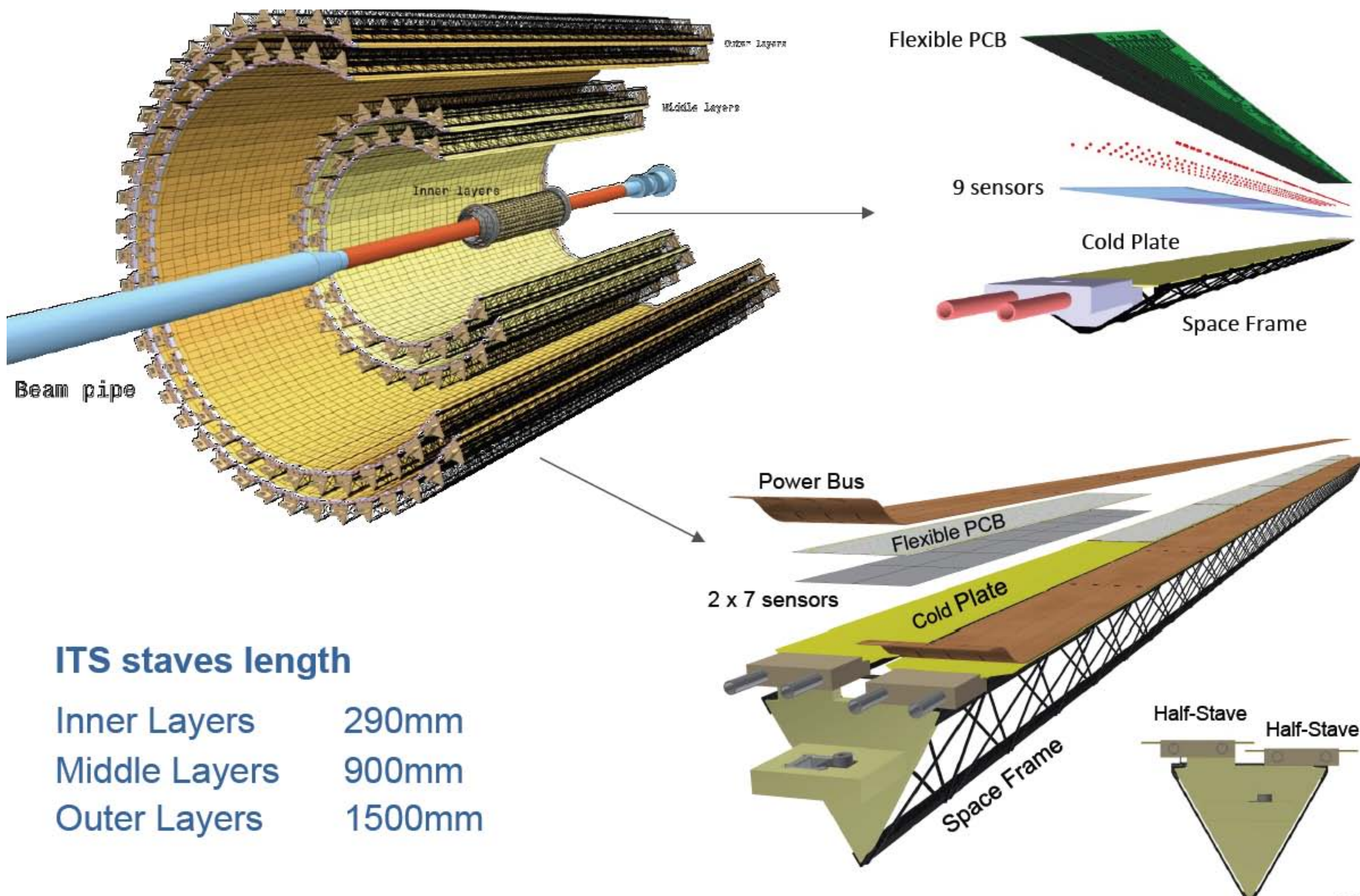
Material /layer : 0.3% $X_0$ (IB), 1% $X_0$ (OB)

# Layout del nuovo rivelatore e i suoi principali componenti



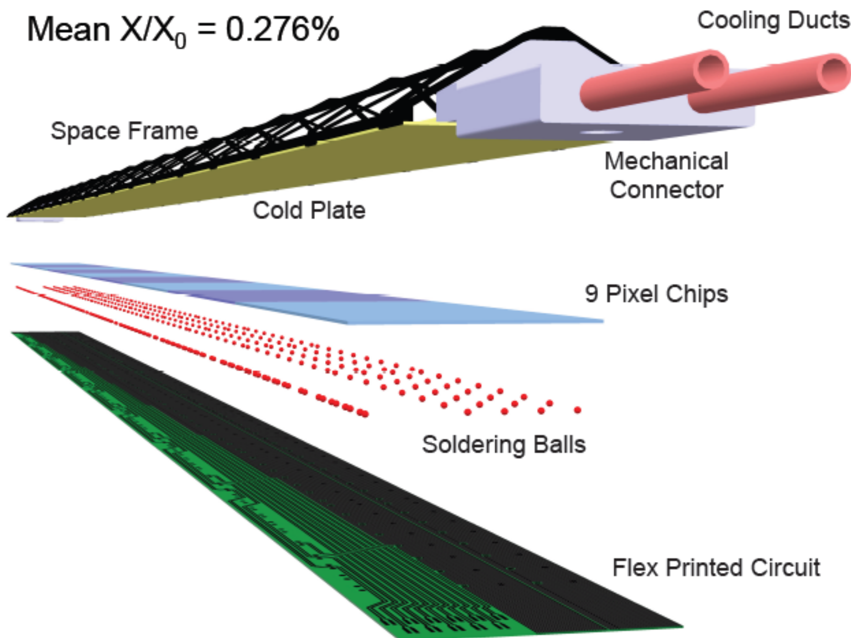
# Layout del nuovo rivelatore e i suoi principali componenti

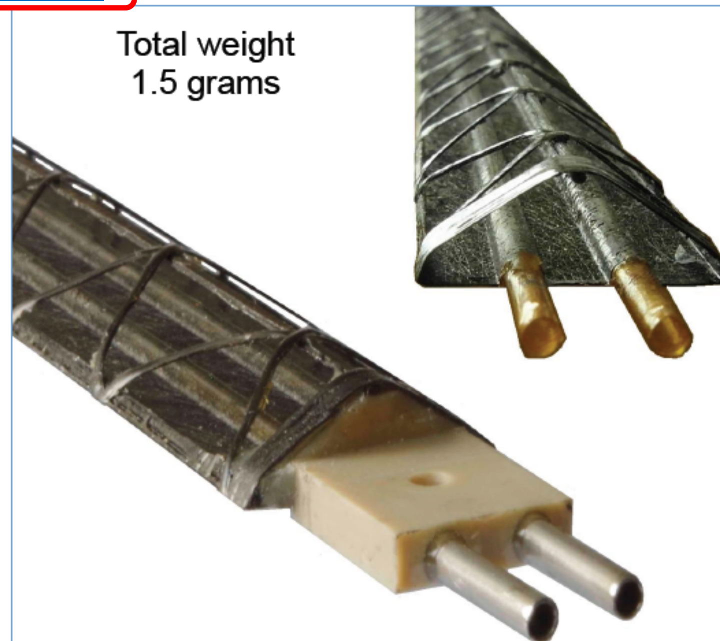
## STAVES



# Layout del nuovo rivelatore e i suoi principali componenti

## INNER BARREL STAVE




<Radius> (mm): 23,31,39

Nr. of staves: 12, 16, 20

Nr. of chips/layer: 108, 144, 180

Power density: < 100 mW/cm$^2$

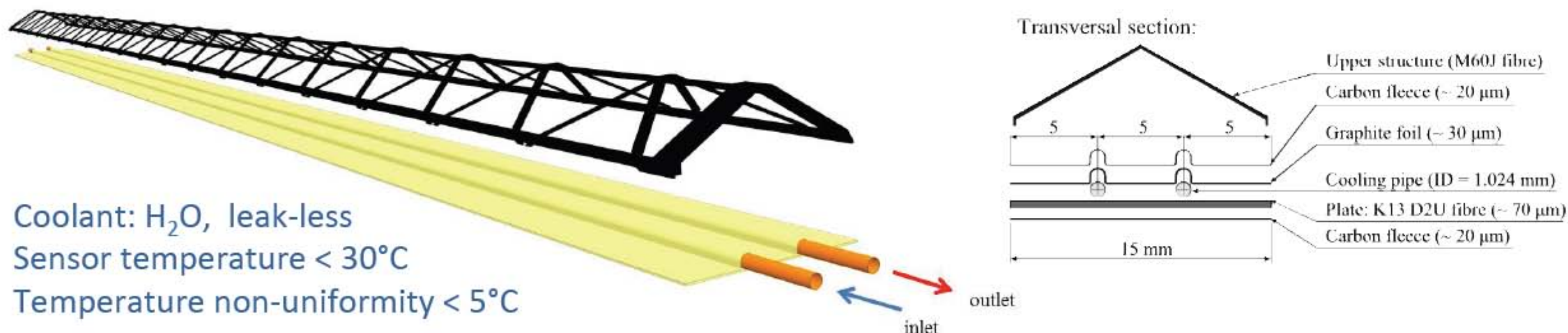
Length in z (mm): 290

Nr. of chips/stave: 9

Material thickness: ~ 0.3% $X_0$

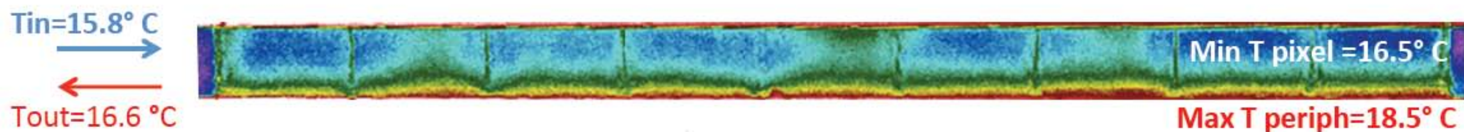
Throughput (@100kHz): < 80 Mb/s × cm$^{-2}$

# Layout del nuovo rivelatore e i suoi principali componenti




Coolant: $H_2O$, leak-less
Sensor temperature < 30°C
Temperature non-uniformity < 5°C

290mm length, 1.5gram weight




Tin=15.8° C

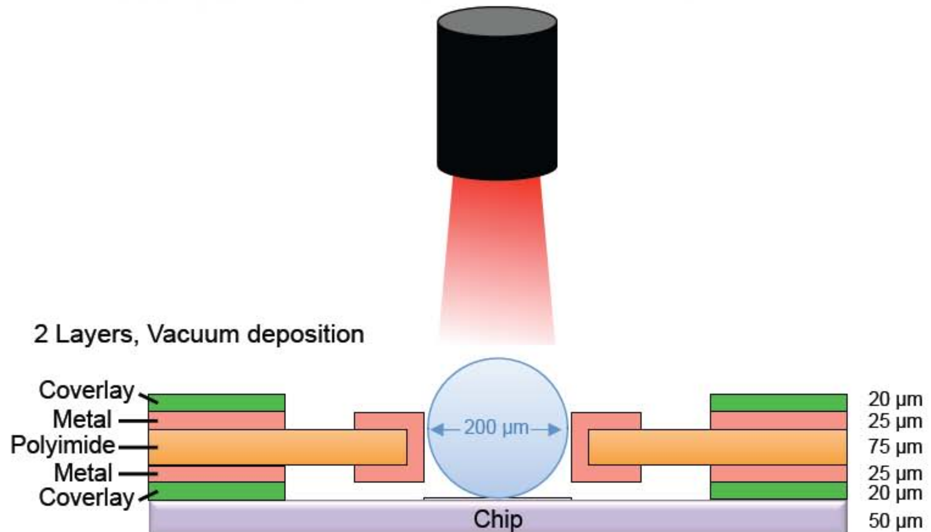
Tout=16.6 °C

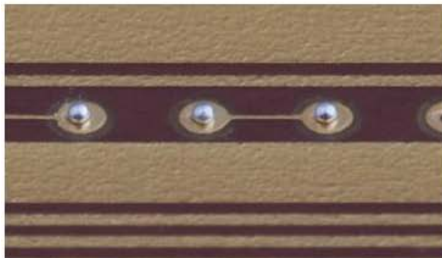
Max T periph=18.5° C

# Layout del nuovo rivelatore e i suoi principali componenti

## INTERCONNECTION

Laser soldering: Interconnection of Pixel chip on flexible printed circuit



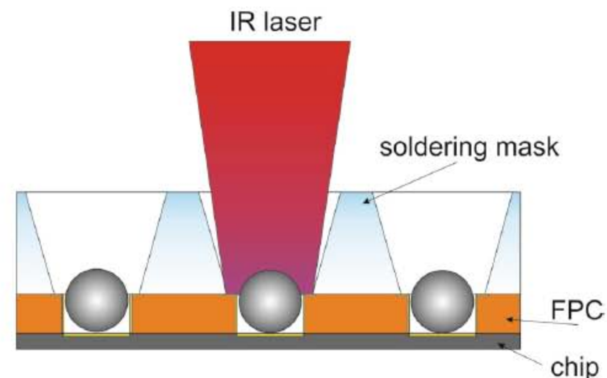



# Layout del nuovo rivelatore e i suoi principali componenti



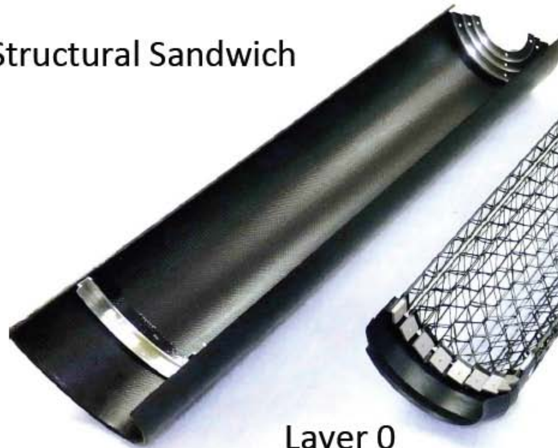
## Laser Soldering

- Flux-less soldering of 200 μm diameter Sn/Ag(96.5/3.5) balls (227 °C melting T) in vacuum ( $\leq 10^{-1}$ mbar)
- IR diode laser, 976 nm, 25 W, 50 mm focal length, 250 μm beam spot size
- Laser power modulated by pyrometer, programmable T profile ensures precise limitation of heating
- Soldering mask (in Macor® or Rubalit ®) used to press FPC on chip and guide soldering balls inside FPC vias
- Solder provides electrical and mechanical connection → no glue

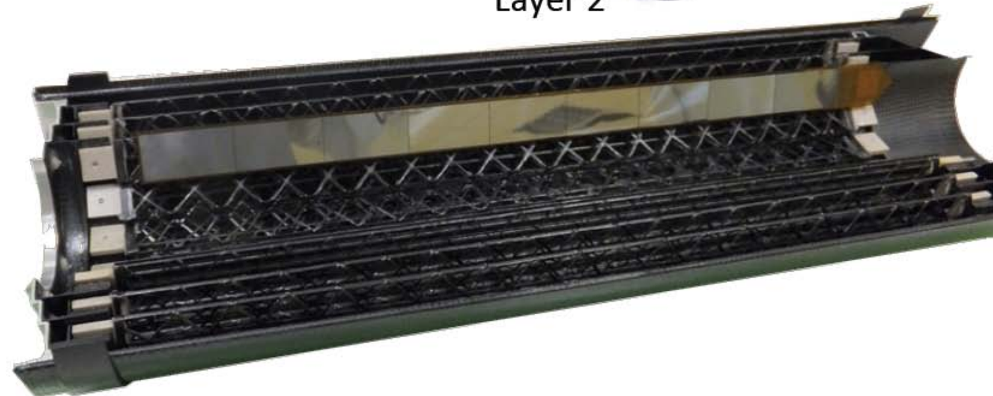


# Layout del nuovo rivelatore e i suoi principali componenti

## INNER BARREL - FULL SCALE PRORTOTYPE

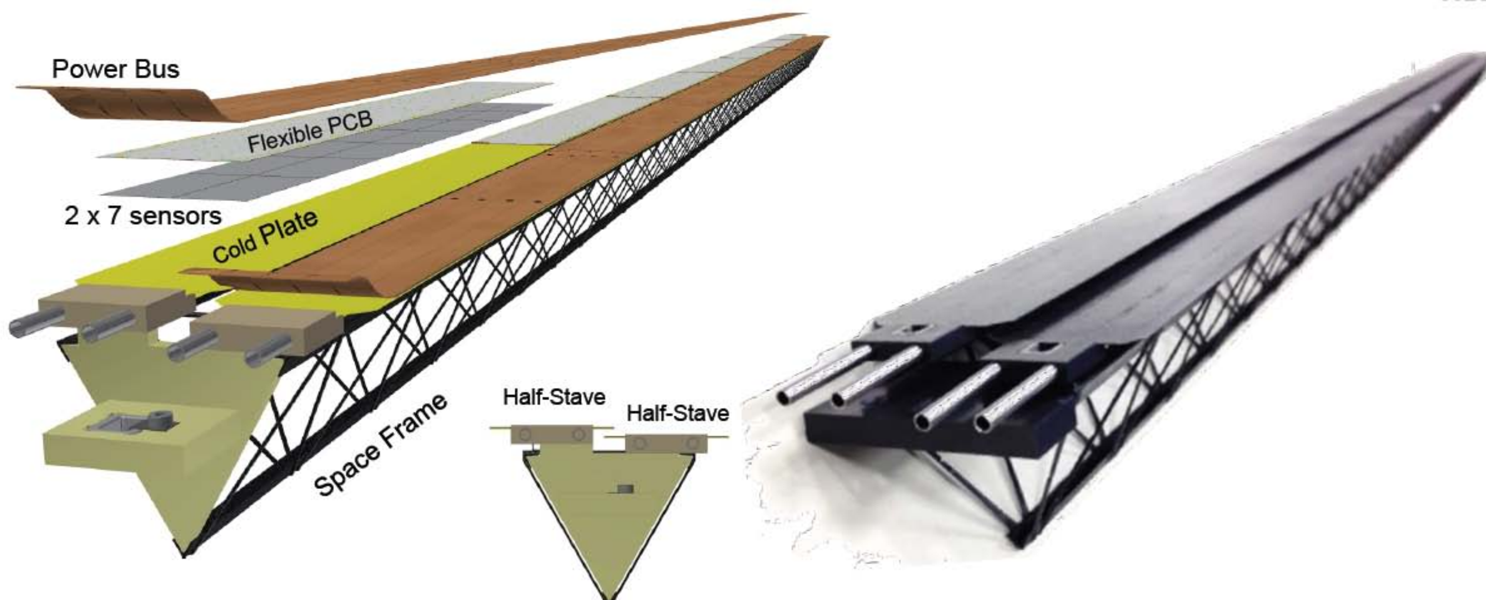


**Prototype**



# Layout del nuovo rivelatore e i suoi principali componenti

## OUTER BARREL




Outer Barrel (OB)

<radius> (mm): 194, 247, 353, 405

Nr. staves: 24, 30, 42, 48

Nr. Chips/layer: 6048 (ML), 17740(OL)

Power density < 100 mW / cm$^2$

Length (mm): 900 (ML), 1500 (OL)

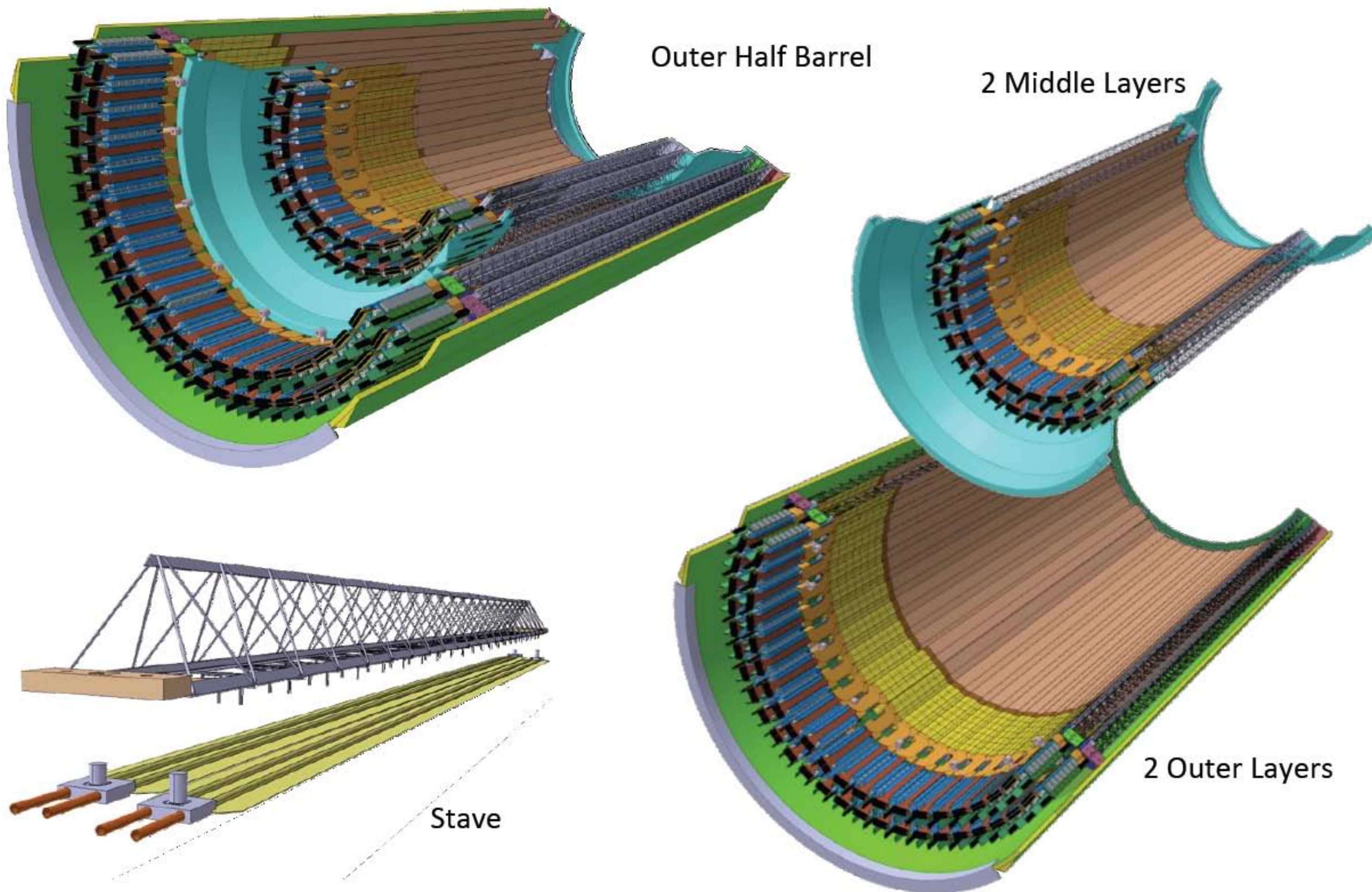
Nr. modules/stave: 4 (ML), 7 (OL)

Material thickness: ~ 1% $X_0$

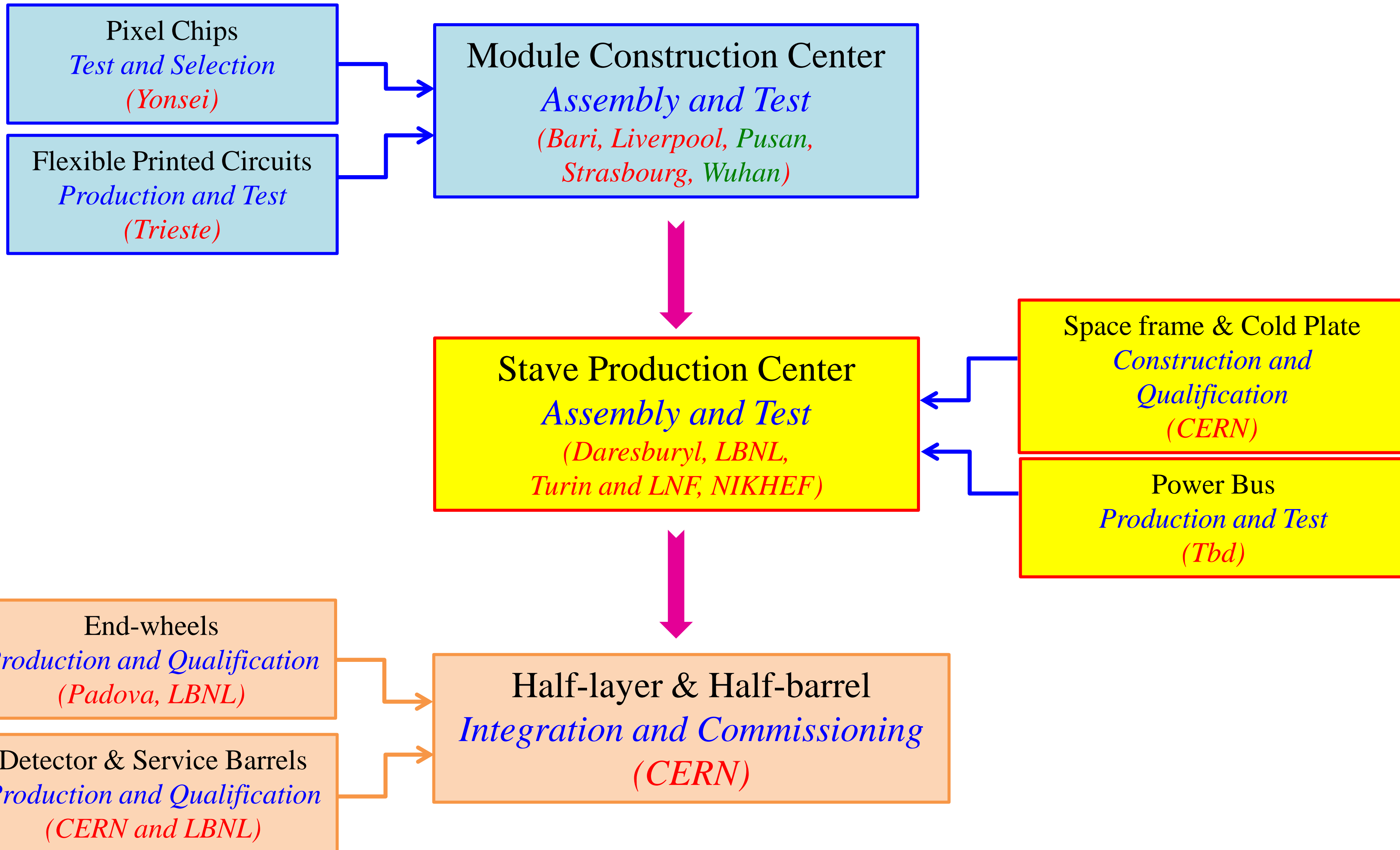
Throughput (@100kHz): < 3Mb/s × cm$^{-2}$

# Layout del nuovo rivelatore e i suoi principali componenti

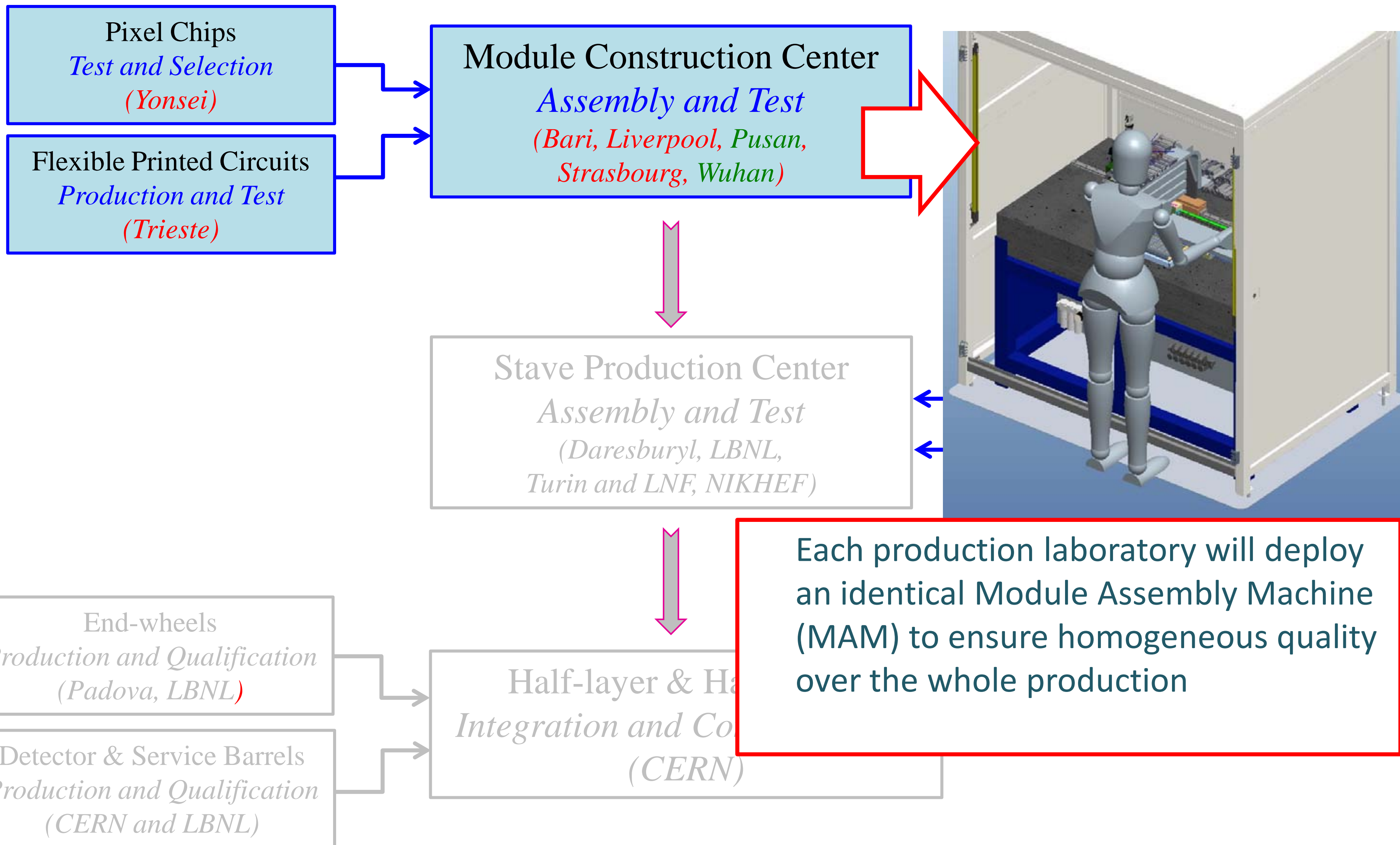
## OUTER DETECTOR BARREL



# OB Construction flow-diagram



# OB Construction flow-diagram



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# Conclusioni

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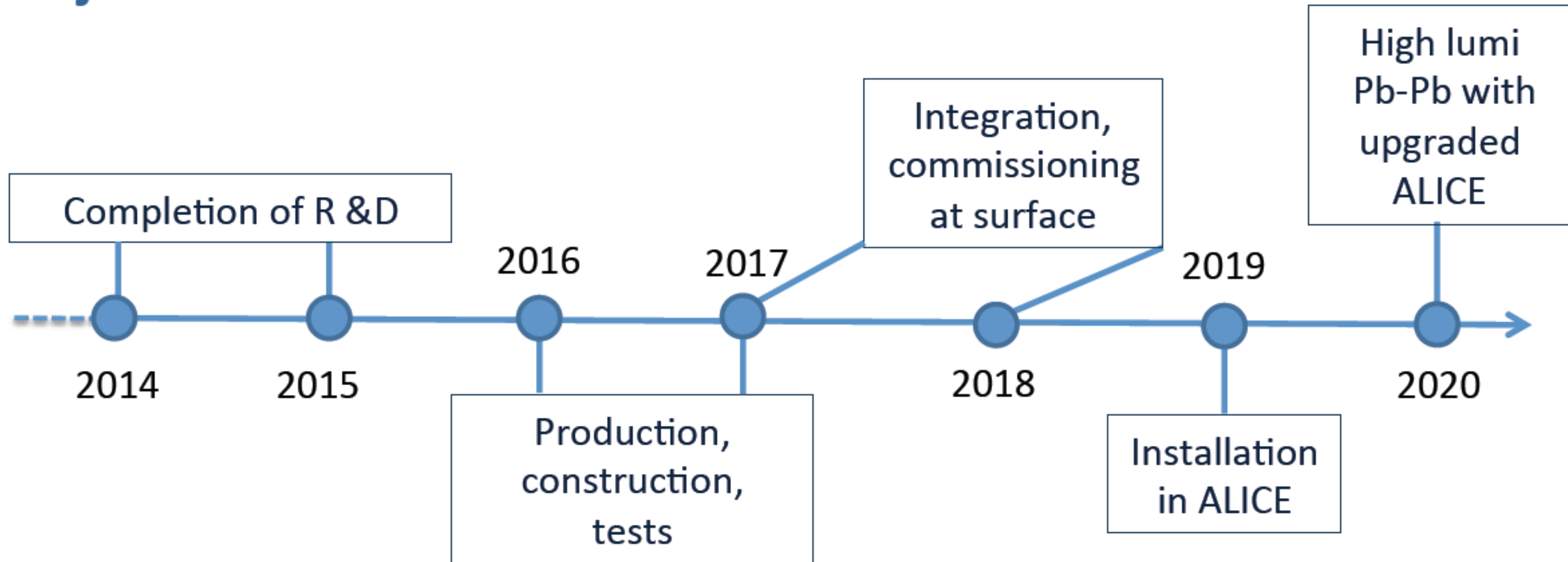
## Project Timeline and Collaboration

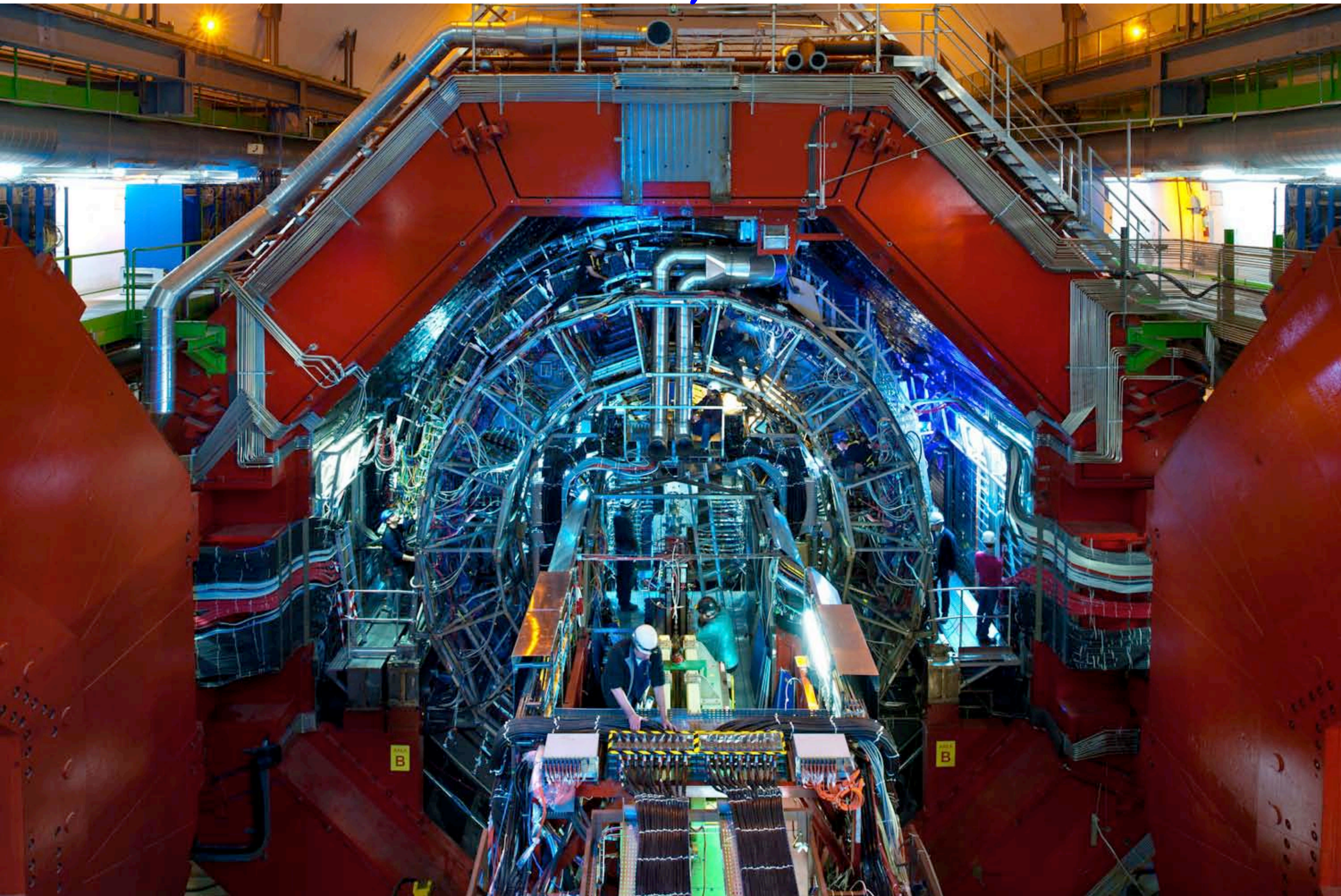



ALICE ITS Collaboration

CERN, China (Wuhan), Check Republic (Prague), France (Grenoble, Strasbourg),
Italy (Aless., Bari, Cagliari, Catania, Frascati, Padova, Roma, Trieste, Torino),
Indonesia (LIPI), Korea (Pusan, Inha, Yonsei), Netherlands (Nikhef, Utrecht),
Pakistan (CIIT-Islamabad), Russia (St. Petersburg), Slovakia (Kosice),
Thailand (Suranaree, SLRI, TMEC), UK (Daresbury, Liverpool, RAL), Ukraine (Kharkov),
USA (Austin, Berkeley)

Institute = participated in current ITS

# Thank you !



# SPARES

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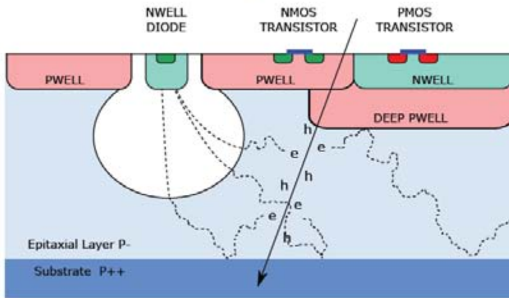
## Chip – technology choice

CMOS Pixel Sensor using TowerJazz 0.18μm CMOS Imaging Process




**Tower Jazz 0.18 μm CMOS**

- feature size 180 nm
- metal layers 6

➔ Suited for high-density, low-power

- Gate oxide 3nm

➔ Circuit rad-tolerant

- High-resistivity (> 1kΩ cm) p-type epitaxial layer (20μm - 40μm thick) on p-type substrate
- Small n-well diode (2-3 μm diameter), ~100 times smaller than pixel => low capacitance
- Application of (moderate) reverse bias voltage to substrate can be used to increase depletion zone around NWELL collection diode
- Quadruple well process: deep PWELL shields NWELL of PMOS transistors, allowing for full CMOS circuitry within active area

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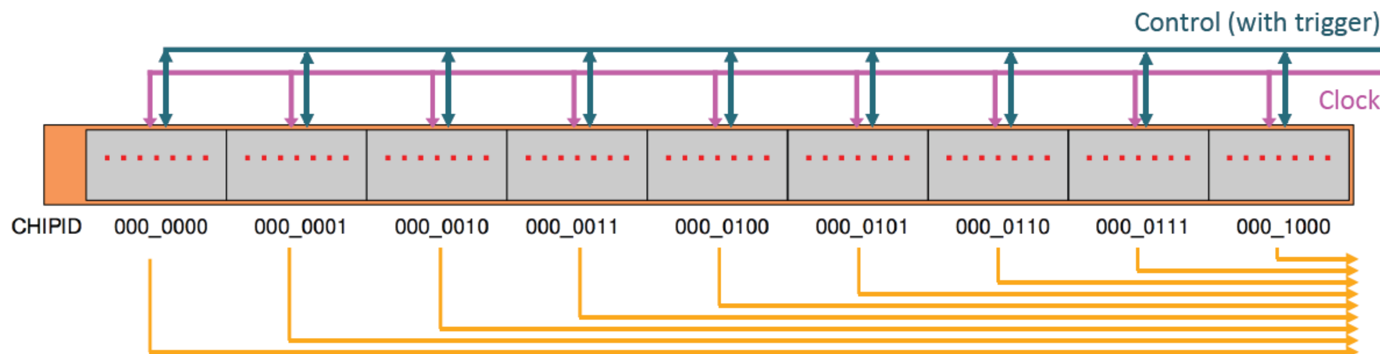
## PIXEL Chip – General Requirements

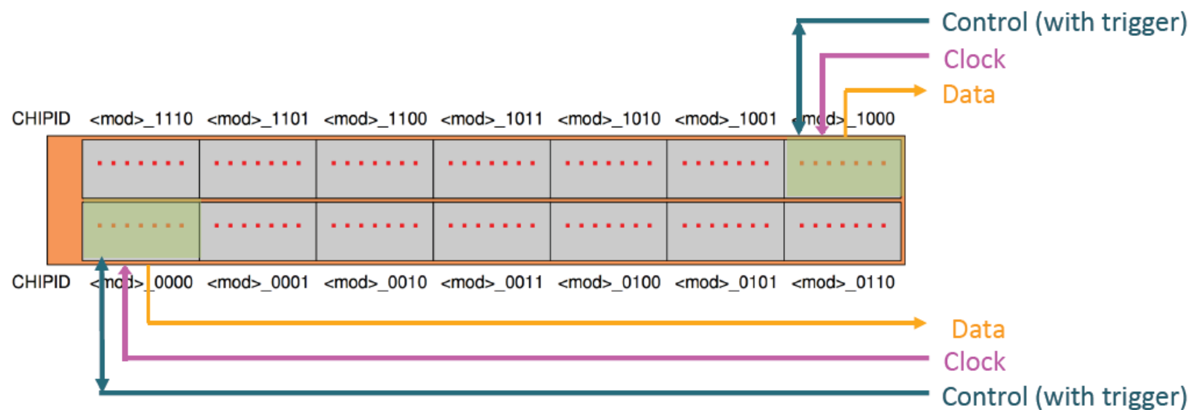
| Parameter | Inner Barrel | Outer Barrel |
|---|---|---|
| Silicon thickness | 50 μm | |
| Spatial resolution | 5 μm | 10 μm |
| chip dimensions | 15 mm x 30 mm | |
| Power density | < 300 mW/cm² | < 100 mW/cm² |
| Event time resolution | < 30 μs | |
| Detection efficiency | > 99% | |
| Fake hit rate | < $10^{-5}$ per readout frame | |
| TID radiation hardness (*) | 2700 krad | 100 krad |
| NIEL radiation hardness (*) | $1.7\times10^{13}$ 1MeV $n_{eq}$ /cm² | $10^{12}$ 1MeV $n_{eq}$ / cm² |

# Readout – Inner and Middle/Outer Layers connections

**Inner layers stave**, 9 independent sensors (each read/drives its own data lines)

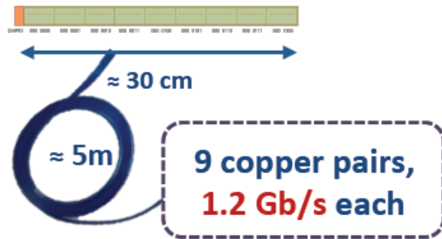


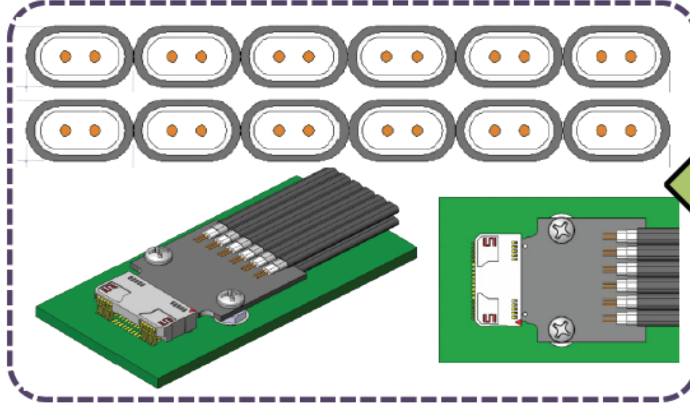

**Mid/Outer layers module**: 2 symmetric group of 1 master and 6 slave chips. Only the master accesses the data/control lines toward/from the outer world.

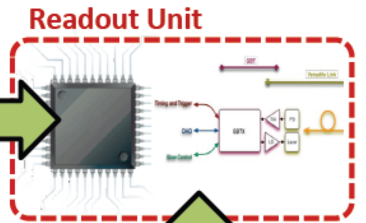


# Readout – copper links and available bandwidth

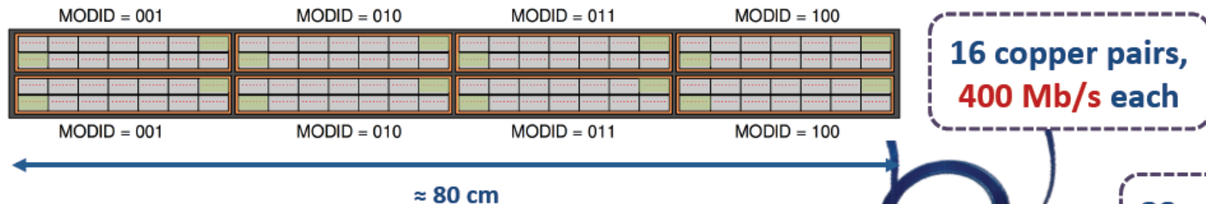
**Inner layers** (0, 1, 2) staves:
9 masters for each stave

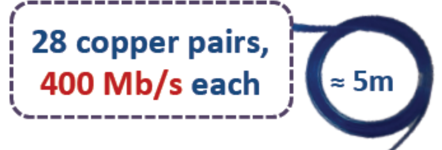


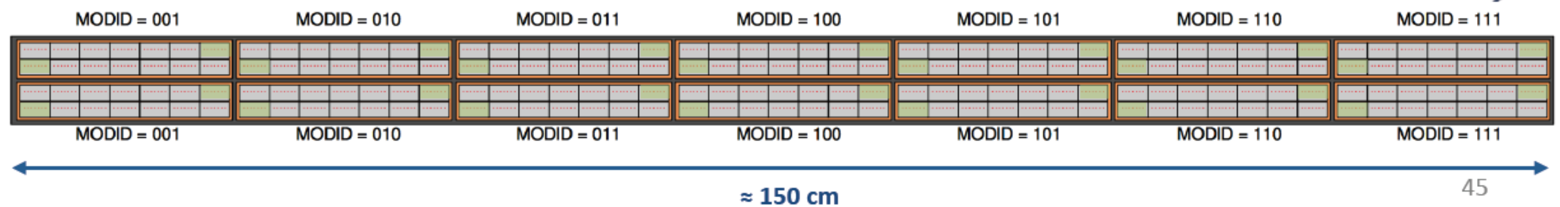



**Mid layers** (3, 4) staves: 8 modules per stave, 2 master each




**Outer layers** (5, 6) staves: 14 modules per stave, 2 master each



# Readout – copper links and available bandwidth

WORK IN PROGRESS

**Inner Layers**

9 links @ 1.2 Gb/s
1 Clock links
1 Control link
12 pairs Twinax copper assembly

OR

**Mid & Outer Layers**

8/14 links @ .4 Gb/s
2 Clock links
2 Control link
2 × 12 pairs Twinax copper assemblies

8/14 links @ .4 Gb/s
2 Clock links
2 Control link
2 × 12 pairs Twinax copper assemblies

**Readout Unit**

2 × 16 channel FPGA per half stave (only one used for inner layers)

VTRx: edge-connector, GBLD, I2C, Laser Diode, TOSA, PIN + GBTIA, ROSA, PCB
VTRx: edge-connector, GBLD, I2C, Laser Diode, TOSA, PIN + GBTIA, ROSA, PCB
VTTx: edge-connector, GBLD, I2C, Laser Diode, TOSA, GBLD, Laser Diode, TOSA, PCB

50-150m

TRx: Data @ 3.2 Gb/s, Control
TRx: Data @ 3.2 Gb/s, Trigger
DRx12: Data @ 3.2 Gb/s, Data @ 3.2 Gb/s

**Common Readout Unit (Counting Room)**

Not mandatory for "baseline" (Pb-Pb @ 50 kHz) operations.

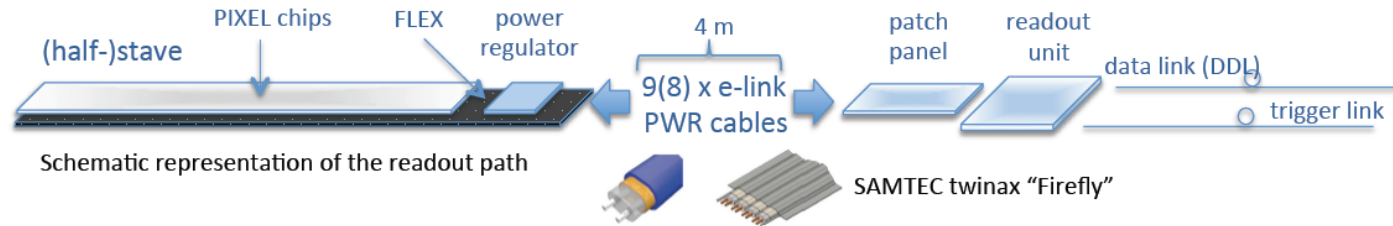
Control

**Power Unit**

Independent to control system

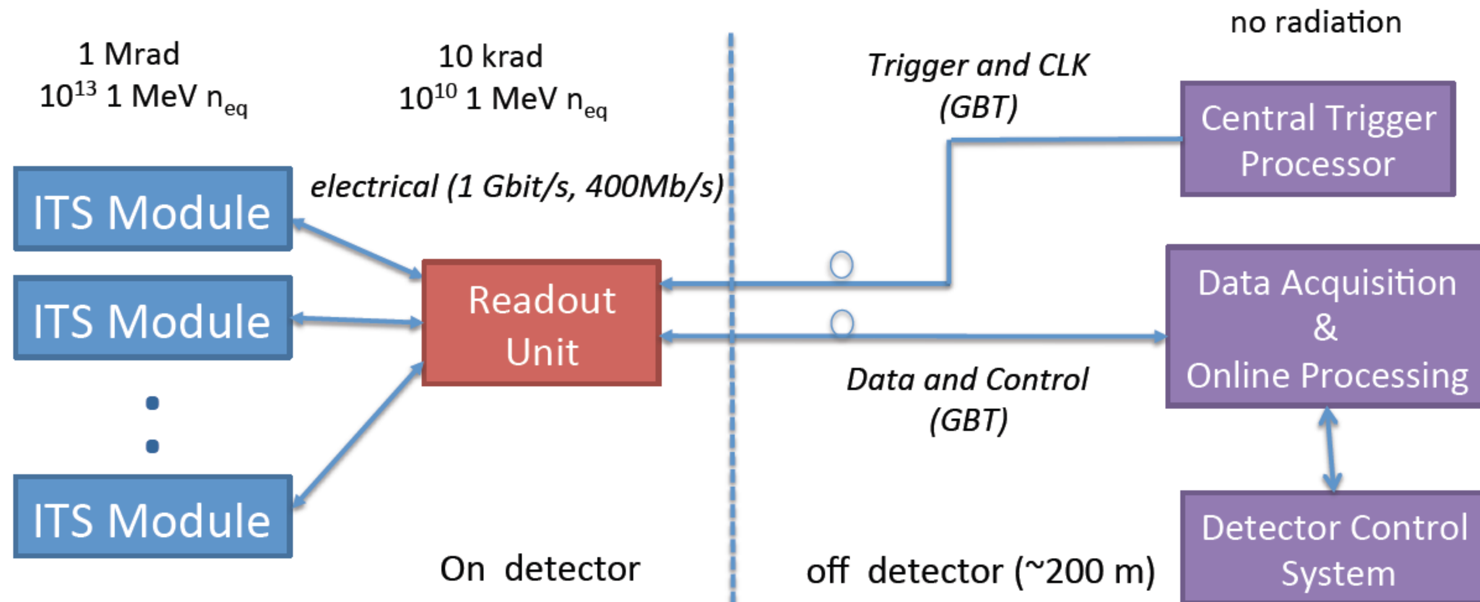
Cables from power supply

# Readout – general scheme and data throughput



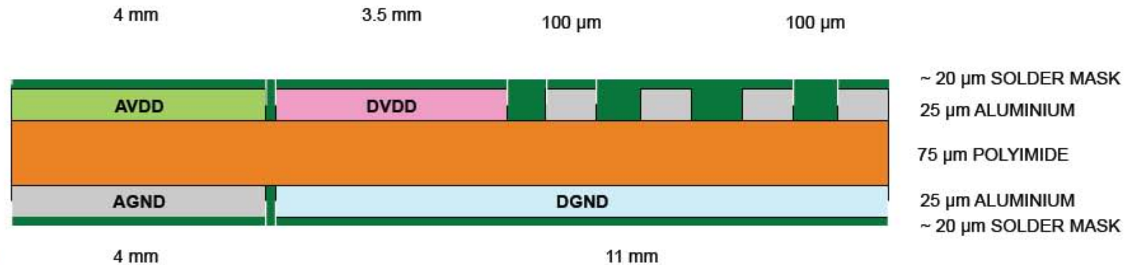

Data throughput 324 Gbit/s
1008 electrical links

(184 DAQ optical links + n Trigger links )



# FPC main characteristics

## Flexible Printed Circuit




- 2 layouts:
  - IB: 1x9 chips, Al
  - OB: 2x7 chips, Cu
- Metallised vias of 220 mm diameter
- Two openings of 1x1 and 1x0.4 $mm^2$, respectively, to “see” chip targets