ASIC Test spec doc

Version 4.0
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Author:

1 Revision status summary table

Revision status summary				
Revision	**Requestor**	**Date mm/dd/yy**	**Pages updated**	**Description**
1.0				

2 Customer details

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3 General ASIC information

- Technology : 65nm LP
- Foundry : TSMC
- Power supply IO cells : 2.5 Volts
- Power supply core cells : 1 and 1,2 Volts
- Analog power supply : Volts
- Min voltage level I/O : 0.25 Volts
- Max voltage level I/O : 2.25 Volts
- Clock frequency : 100 Mhz
- If PLL used

1. Frequency : Input 60-125 Mhz
   : Output 600 - 2500 Mhz (internally)
2. Power supply PLL : 2.5 Volts

- Total number of pins : 529

1. Number of digital VDD pads : 111
2. Number of digital VSS pads : 356
3. Number of analog VDDA pads : 28
4. Number of analog VSSA pads : 0
5. Number of Digital Input pads : 28 => 6 Single Ended, 11 Differential LVDS 2.5V
6. Number of Digital Output pads : 6 => 4 Single Ended, 1 Differential LVDS 2.5V
7. Number of Digital tri-state pads : 0
8. Number of Digital Bidir pads : 0
9. Number of Analog Input pads : 0
10. Number of Analog Output pads : 0
11. Number of Analog Bidir pads : 0

4 Hardware development

4.1 Hardware checklist

- Digital circuit Yes
- Mixed signal circuit No
- PLL available Yes

- Drive capability of ASIC outputs (Capac load of the tester pin >= 66pF)

  Buffers needed at load board to drive the tester No

4.2 Packaging information

Package type	Package name	Text on lid
Plastic	FBGA 23x23	
Ceramic		

4.3 Probe card

- Probe card required Yes/No

Wafer size	
# dies/wafer	

	X-dim (µm)	Y-dim (µm)
Circuit		
Circuit + scribe		
Bond pad openings		

4.4 Pin description table.

Refer to Netlist.xls.

- AMCHIP06PINOUT_Netlist20141211.xlsx: list of signal names versus package pins.
- AAA11586-0.pdf : Package drawing.

4.5 Power supply connections

A list of all the power supply connections & voltage levels of the ASIC must be specified in following tables:

Power supply	Pin number of package	Voltage level (Volts)		
		Min	Nom	Max
VDDcore		0.9	1	1.1
VDDIO		2.25	2.5	2.75
VDDfc		0.9	1	1.1
VDDH		2.25	2.5	2.75
VDDSERDES		1.08	1.2	1.32

Power supply PLL's	Pin number of package	Voltage level (Volts)		
		Min	Nom	Max
PLL1				

Power supply analog blocks	Pin number of package	Voltage level (Volts)		
		Min	Nom	Max
VDDA		1.08	1.2	1..32
VDDA_LVDS		2.25	2.5	2.75
VDD_BGREF		2.25	2.5	2.75

- Only test @ nominal supply voltage to be performed.
- The digital core has …… power domains.
    - Core VSS, VDD
    - The IO ring
    - The PLL has 2 power domains
    - The analog power and the digital power, etc….

4.6 Pad type characteristics

The name of each Input/Output/Bidir pad used in the circuit must be filled out in the following tables.

These tables describe the minimum and maximum value of the Input current and Output current of the cells used.

4.6.1 Input cells

Cell name	Type	Remarks	Input Trigger Voltage (V)	
			Min [ViL]	Max [ViH]

Cell name	Type	Remarks	Input Trigger Voltage (V)		
			Min [ViL]	Hysteresis	Max [ViH]

4.6.2 *Output cells*

Cell name	Type	Remarks	Ouput current (mA)		
			Min [IoL] Min-Max	Nom [I]	Max [IoH] Min-Max

4.6.3 *Bidir cells*

Cell name	Type	Remarks	Input voltage (V)	Output Current (mA)			
			Min [ViL]	Max [ViH]	Min [IoL]	Nom [I]	Max [IoH]

4.6.4 *I/O pad measurements*

- Input current measurement

- All the bidir pads must be forced into input mode. A vector set will drive all the inputs to “0” and “1” respectively and measure the amount of leakage current consumed by each input/bidir pad.
- High-impedance measurement
- Output voltage measurement
- All the bidir pads must be forced into output mode. A vector set will drive all the outputs to “0” and “1” respectively and measure the output voltage levels of each output/bidir pad.

5 Software development

5.1 Test pattern format

- WGL format

Pattern file name	Number of test patterns	Size of file	Version number

- VCD format

Pattern file name	Number of test patterns	Size of file	Version number

- BIST test

Pattern file name	Number of test patterns	Size of file	Version number

- IDDQ test

Pattern file name	Number of test patterns	Size of file	Version number

6 ASIC characterization

- Variation of VDD
- Variation of freq
- Variation of temperature between upper and lower corners

1. Specify lower temperature corner
2. Specify high temperature corner

7 ESD & LU tests

- ESD test
  - 3 devices @ 2 kV
  - 3 devices @ 3 kV
  - 3 devices @ 4 kV

- LU test
  - 4 devices @ 125 °C, 100mA
  - 4 devices @ 85 °C, 100mA

8 Technical description

Application description.

8.1 Block diagram

Include picture of block diagram.

8.2 Description of the different blocks

The ASIC consists of the following IP blocks:

9 Test pattern description

This chapter describes the different test modes: relevant IO, pin timing, scripts and test patterns.

9.1 BIST

Description of the BIST test patterns.

9.1.1 Asic IO

Below the function of the pins for the BIST test is listed.

ASIC IO for BIST test			
BIST controller pins	**I/O**	**Description**	**Pad name**

9.1.2 List of memories tested

In total …. memory instances are present in the Asic, tested in …. groups.

9.1.2.1 Memory 1

…………….

9.1.2.2 Memory 2

Etc…..

9.1.3 Pin Timing

The table below list the pin timing of the relevant pins for this test. The BIST test does not test the memories at speed.

Test cycle	…. ns			
Type	**Pad name**	**ASSERT time (ns)**	**DEASSERT time (ns)**	**Strobe time (ns)**
Clock 1				

The diagram below shows the pin timing of the relevant pins for this test.

9.1.4 Patterns

The pattern file sets up the BIST test and contains ….. cycles:

- Nr of patterns:
- Cycle 1 : initialize all inputs + reset
- Cycle 2 : Define test mode
- Cycle 3-20:
- Cycle 21: Start of actual BIST test.
- Rest of cycles :

The Table below shows number of expected cycles needed to perform the BIST tests for the different groups.

Group	Nr of Cycles

9.1.5 *Files*

The test patterns are generated.

File name	Contents

9.2 Scan

The ASIC is tested by Scan ATPG Test Vectors. There are … scan chains inside the ASIC.

The test coverage of the ASIC is more than …% with …. patterns.

The internal chains contain ….. FF each.

9.2.1 *ASIC IO*

Below the function of the ASIC pins for the BIST test are listed.

SCAN CONTROL			
ASIC pins	**I/O**	**Description**	**Pad name**

9.2.2 *Pin Timing*

The table below list the pin timing of the relevant pins for this test.

Test cycle	….. ns			
Type	**Pad name**	**ASSERT**	**DEASSERT**	**Strobe**

		time (ns)	time (ns)	time (ns)
Clock				

The diagram below shows the pin timing of the relevant pins for this test.

9.2.3 Description of the pattern generation

The patterns have been automatically generated in wgl format using the Synopsys tetramax tool. The test coverage reaches ….% for about …. patterns. The following applies:

- Bidirectional pads are considered as outputs, i.e. the tester never asserts them.
- All patterns are of the same type (basic_scan patterns), no fast sequential patterns have been generated, etc…..

9.3 PLL

For more information about the PLL, refer to the datasheet:………...pdf

9.3.1 Asic IO

Below the function of the ASIC pins for the PLL test are listed

ASIC IO for PLL test			
Connected to PLL pin	**I/O**	**Description**	**Pad name**

9.3.2 Pin Timing

The table below list the pin timing of the relevant pins for this test.

Test cycle	…. ns			
Type	**Pad name**	**ASSERT time (ns)**	**DEASSERT time (ns)**	**Output observe window (ns)**

9.3.3 Files

The test patterns are generated in

File name	Contents

9.3.4 Patterns

Application note …….appnote.pdf describes production test of the PLL as follows:

TestMethod	Expected result (Parts verified)
Lock:	

PLL lock output:

- Lock Test :
- Lock-reset Test :

PLL clock output:

- The output frequency

The IDDQ test is to be executed using ………

10 Operating conditions for mixed signal devices

10.1 Description of the test conditions (optional)

Signal name	Parameter	Min	Nom	Max	Unit	Note

10.2 Initialization of the ASIC

Signal name	Description of signal	type	Value

10.3 Test modes of the device

Signal name	Description of signal	type

Etc….