One year working for WP6

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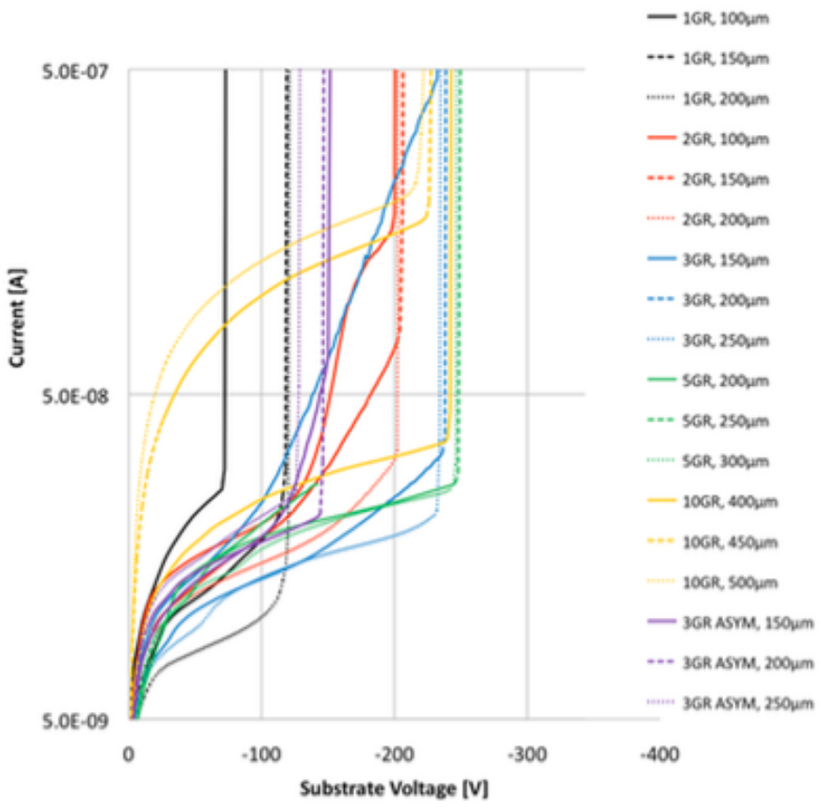
IAPP and WP6

- During my recruitment at LPNHE in Paris i have been working on the IAPP FP7-PEOPLE-2012-IAPP FTK project.
- In particular i worked for WP6 which is “Silicon Detector R&D”.
- Inside this WP at LPNHE we have followed different tasks:
  1. Development and testing of Silicon Detectors R&D for Phase-II.
  2. Development of new Front End electronics in 65nm technology.
- Both tasks are essential in providing a solid link between our project and the R&D community of both sensor and electronics in view of the high luminosity upgrade of the LHC (~2020).
- In addition it provides a solid link between our community and CAEN that will provide the power supply system.

Detector

- During 2014 the LPNHE Paris group has continued its developing of silicon sensors for pixel detectors (200 um down 100 um) in n-in-p bulk technology.
- This technology was chosen in order to improve radiation hardness of the devices and to reduce fabrication costs maintaining, or even improving, present detector performances.
- Through simulations of the proposed devices was performed at LPNHE and the first measurement results (of devices produced at FBK) showed a very good agreement between expected results and measured values.
- I personally contributed to the measurements and the picture shows the characterisation of the devices in terms of current which show a breakdown voltage steadily over 100V after irradiation.



Electronics

- Another area of R&D was the study and definition of new Front End electronic devices to be able to read out these new detectors.
- These new FE chips will be fabricated in 65nm technology and will provide a new generation of readout chips able to cope with extremely high hit rates (up to 2-3GHz/cm^2) and radiation tolerance (~ 10MGy).
- In order to be able to handle such high rates a novel architecture of the Pixel chip has to be developed together with a new Input Output channel definition.
- I personally worked on the simulation, development and definition of the IO protocols and the overall readout architecture.
- Input will be provided with both clock and data encoded on a single differential line running at 160 MHz. A custom protocol was defined in order to fulfil the Single Event Upset required robustness and all clock decoding/alignment features.
- The output lines will provide a 5Gbit/s output data rate.