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Energy vs time performances of HPC applications on Tegra K1

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Energy efficiency is lately becoming of paramount importance in the HPC field and high-end processors are quickly evolving towards more advanced power-saving and power-monitoring technologies. On the other hand, low-power processors, designed for the mobile market, are gaining interest in the HPC area thanks to their increasing computing capabilities, in conjunction with their competitive pricing and low power consumption. In this work we explore energy and computational performances of a Tegra K1 mobile processor, in the context of HPC, using a Lattice Boltzmann application as a benchmark. Current drawing of the board is monitored with custom hardware for different CPU, GPU and memory clocks.

Presenter: CALORE, Enrico (FE)

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