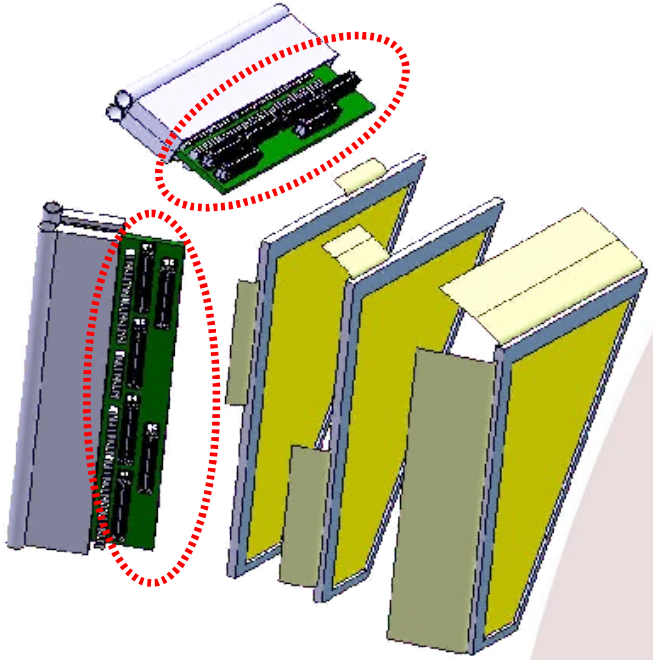
Front End Electronics

Thursday 26th March 2015



© P. Rosier

Abstract:

. iPACI status

. Architecture study Option 1

. A word about Option 2

Unité mixte de recherche

CNRS-IN2P3
Université Paris-Sud

91406 Orsay cedex
Tél. : +33 1 69 15 73 40
Fax : +33 1 69 15 64 70
http://ipnweb.in2p3.fr

Jean-Jacques DORMARD

GHT Meeting

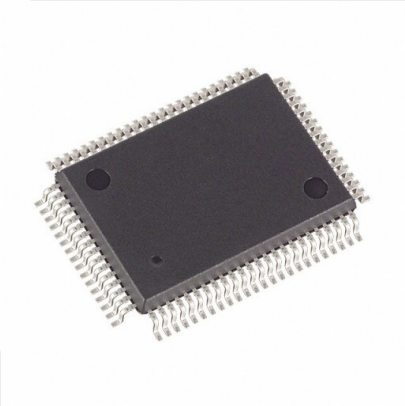
iPACI

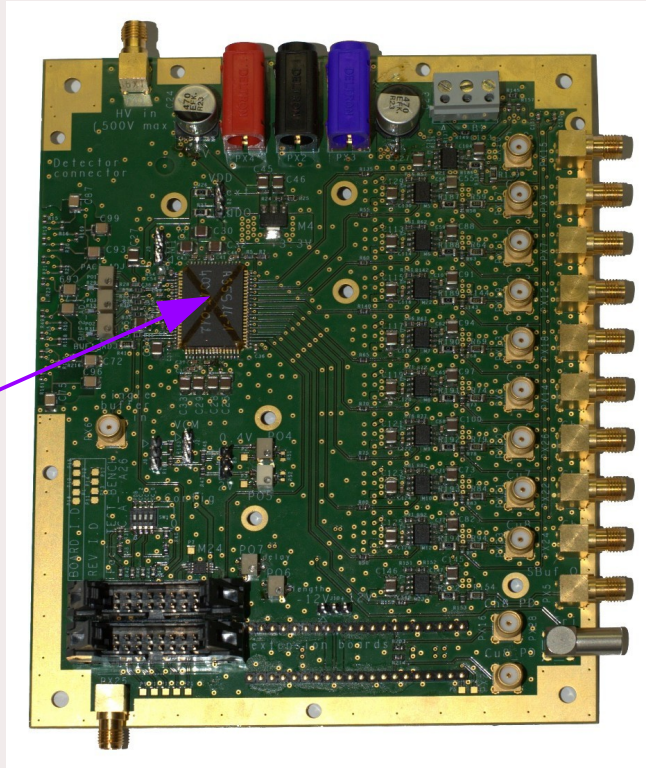
IPACI : 9-channel integrated *Charge* and *Current* output preamplifier

Status:
- ASIC and Testbench available, test starting soon

To do next:
- ASIC qualification via test input
- Coupling with a detector (June/15)
- Possibly ASIC redesign

- Design slow shaper





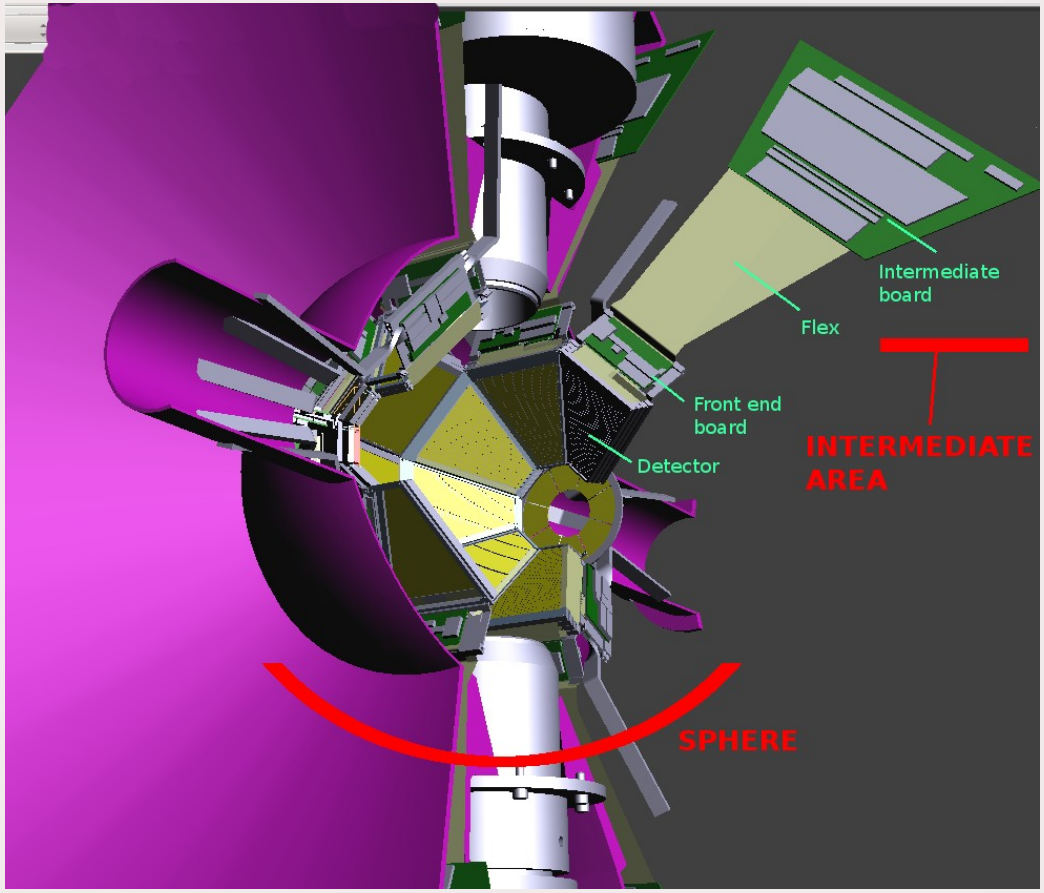
9 **Charge** and **Current** preamps

Architecture study - Purpose

Purpose of study:
Propose architectural options for GASPARD electronics and derive:
- Functionality
- Performance
- Area requirements
- Consumption involved
- Planning & cost

Check feasibility vs Mechanics and Physics

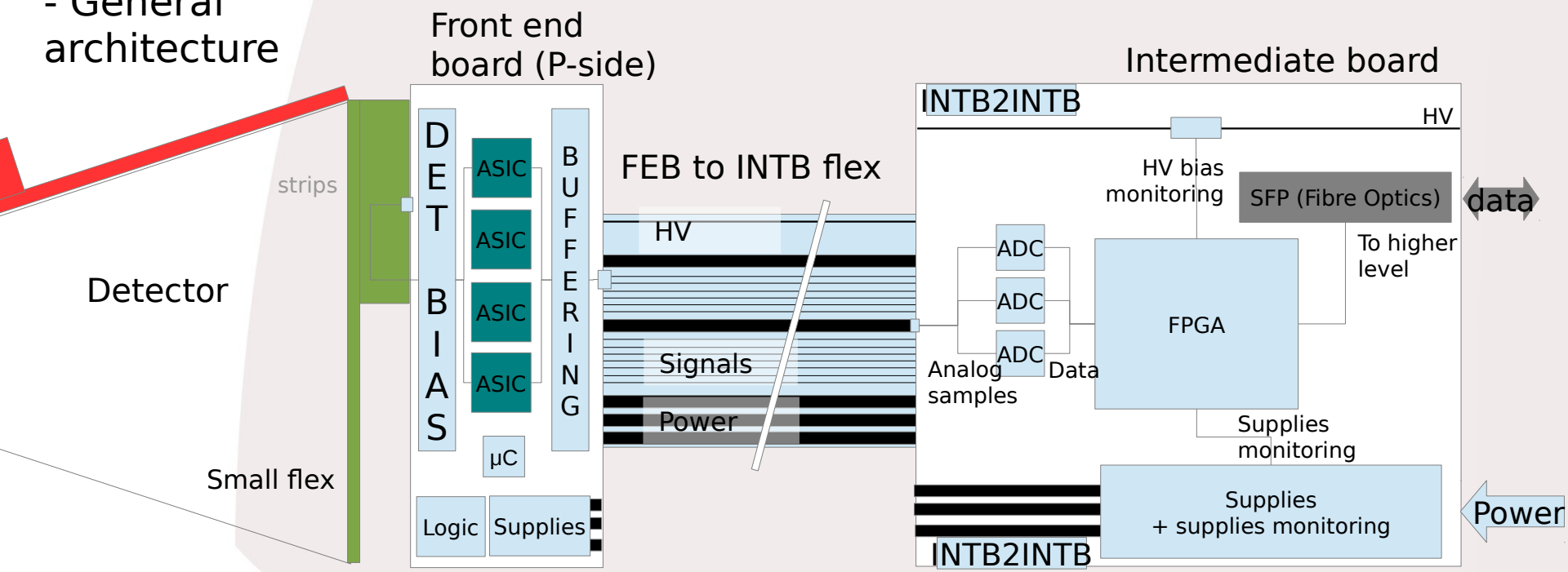
Mechanics:
- Geometries are ~ frozen
- FEB area is very small
- INTB is large but distant
- Power dissipation should not be an issue



Architecture study – Option 1 architecture

Option 1 document

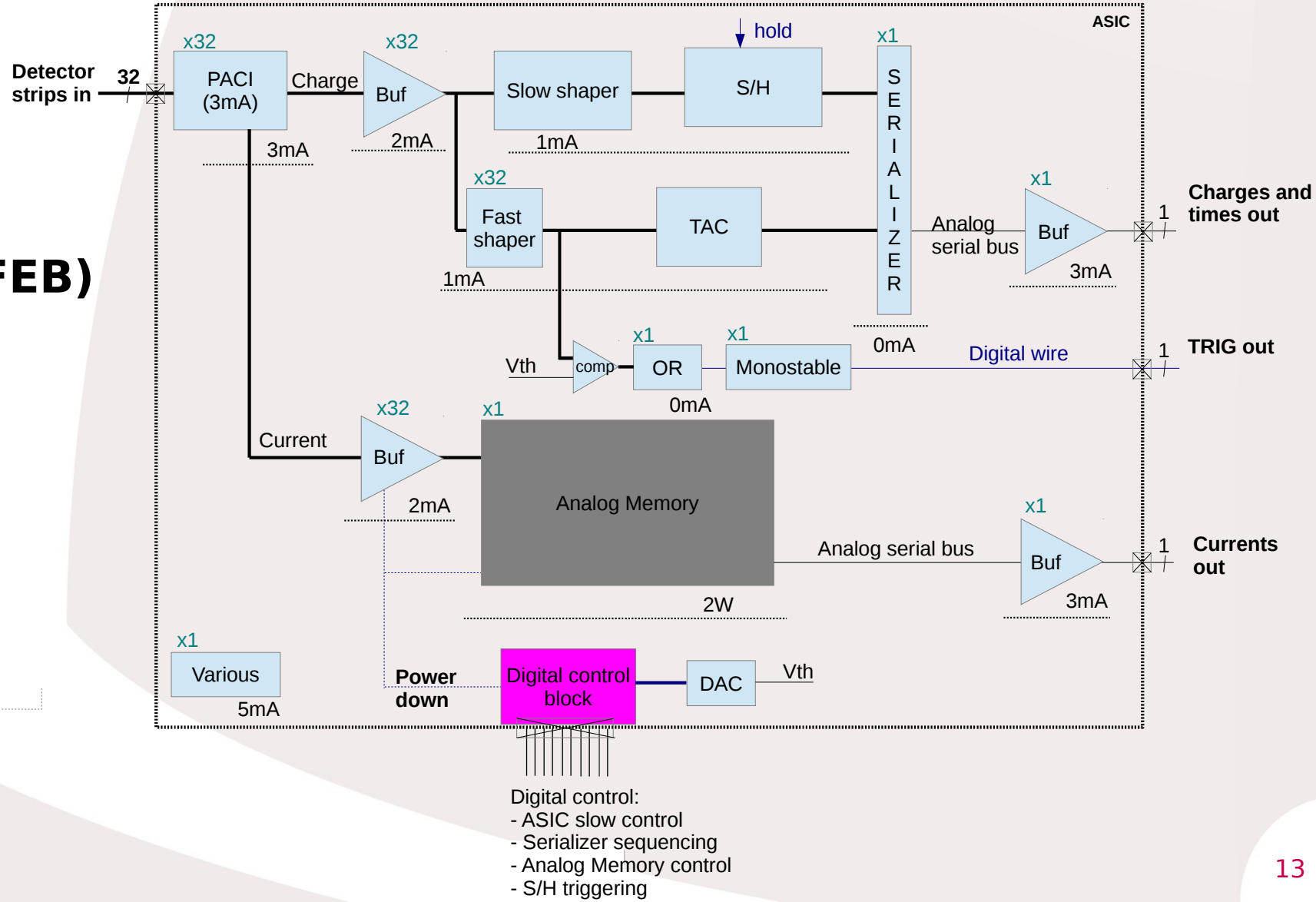
- General architecture



- Other boards

Architecture study – Option 1 architecture

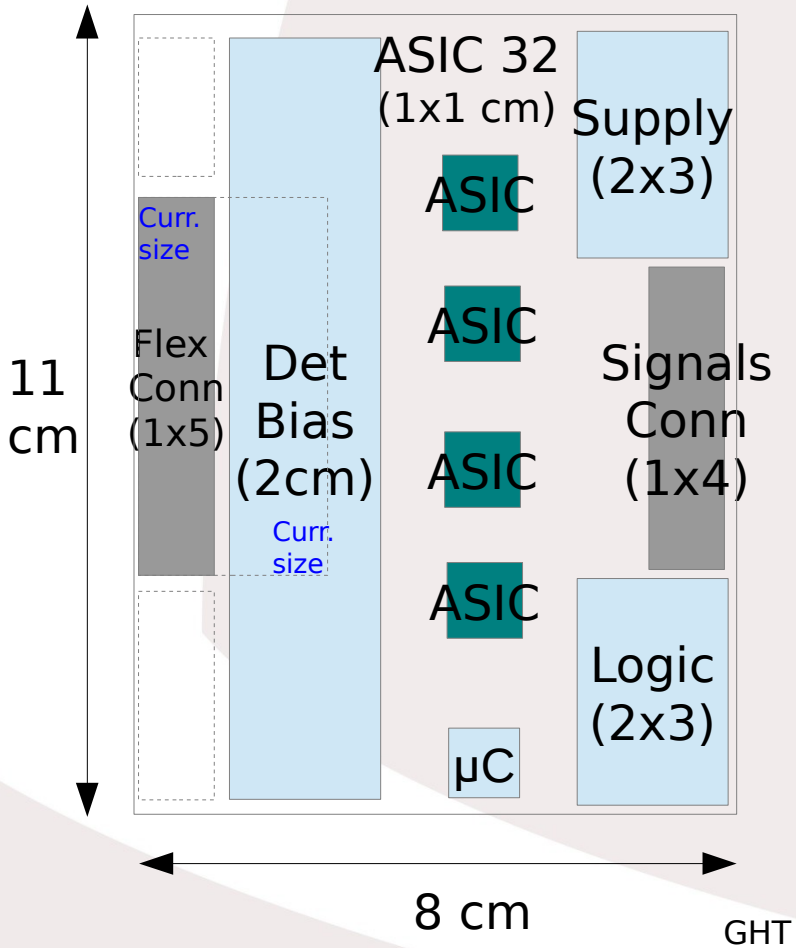
ASIC (on FEB)



Digital control:
- ASIC slow control
- Serializer sequencing
- Analog Memory control
- S/H triggering

Architecture study – Option 1 area

FEB:



Area estimation:

Graphical method - very basic

FEB : 8cm x 11 cm
INTB : 9cm x 12cm
(rough estimations !)

Tips to reduce the area on the FEB:

- Use two sides of one PCB
- Use thinner connectors
- Detector bias..

.. need your input!

Architecture study – Option 1 consumption

Power dissipation estimation. Want to quote consumption:
- On the *sphere*
- On the *intermediates*
- On the *forward detectors only*, *layer 1 only*, ..

Requires:
- ASIC consumption vs options (Blocks on/off, ..)
- Boards consumption vs options (Features on/off, # detectors attached ..)
- Information about GASPARD construction (2/3 layers, PSA on/off, ..)

-> Python script that loops through a subset or all of the detectors and adds up consumptions.

Result (sphere): 640W

Layer	**1**	**2**	**3**
Forward detectors conso (W)	184	27	27
SQ conso (W)	161	24	
Backward detectors conso (W)	184	27	
Forward annulars detectors conso (W)			
Backward annulars detectors conso (W)			

Rough estimations !

Result (intermediates): 550W

Architecture study – Option 1

Conclusion:

- First draft of GASPARD electronics, option 1. Needs reviewing, more work and ideas
  - Define actual parts
  - Refine sizes and consumptions
  - Derive performance
  - Propose planning

- Set up collaboration on design

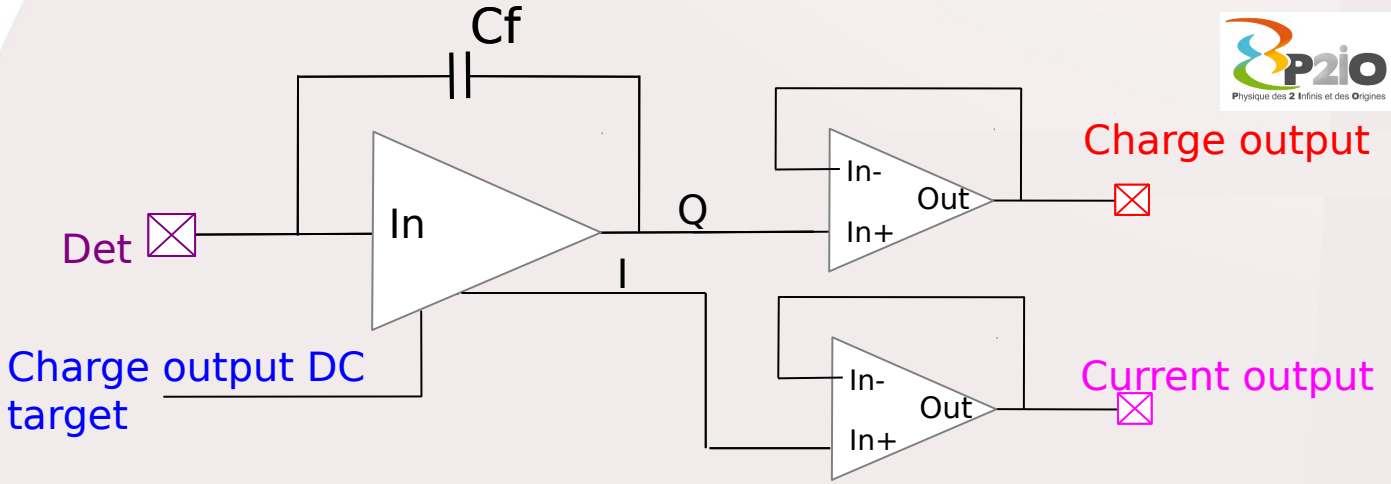
- And/or start again with **option 2**!!
  (Option 1 heavily dependant on Analog Memory)

Questions ?

Thank you for your feedback at:

Emmanuel Rauly <rauly@ipno.in2p3.fr>
Jean-Jacques Dormard <dormard@ipno.in2p3.fr>

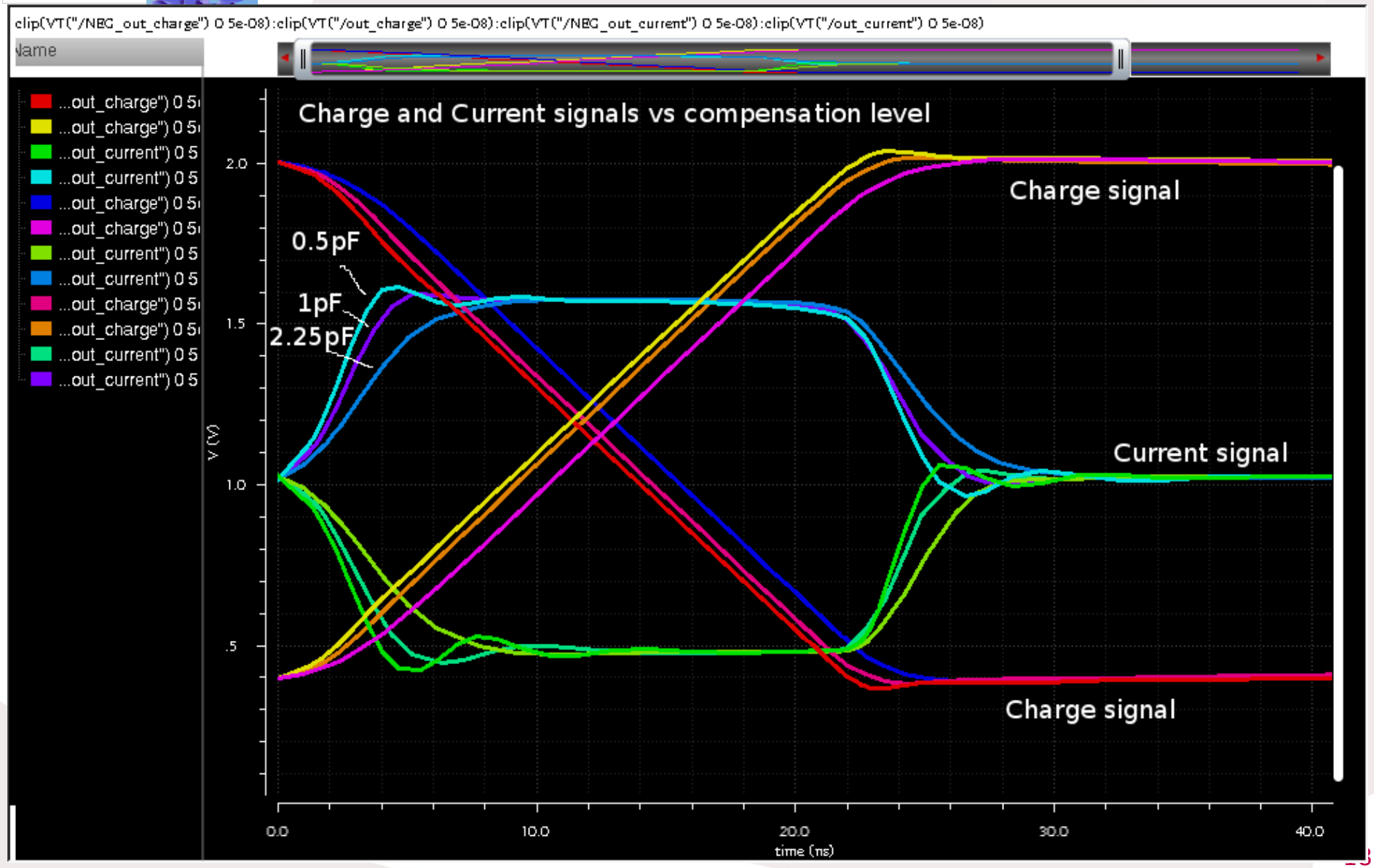
1-Channel performance (simulated!)



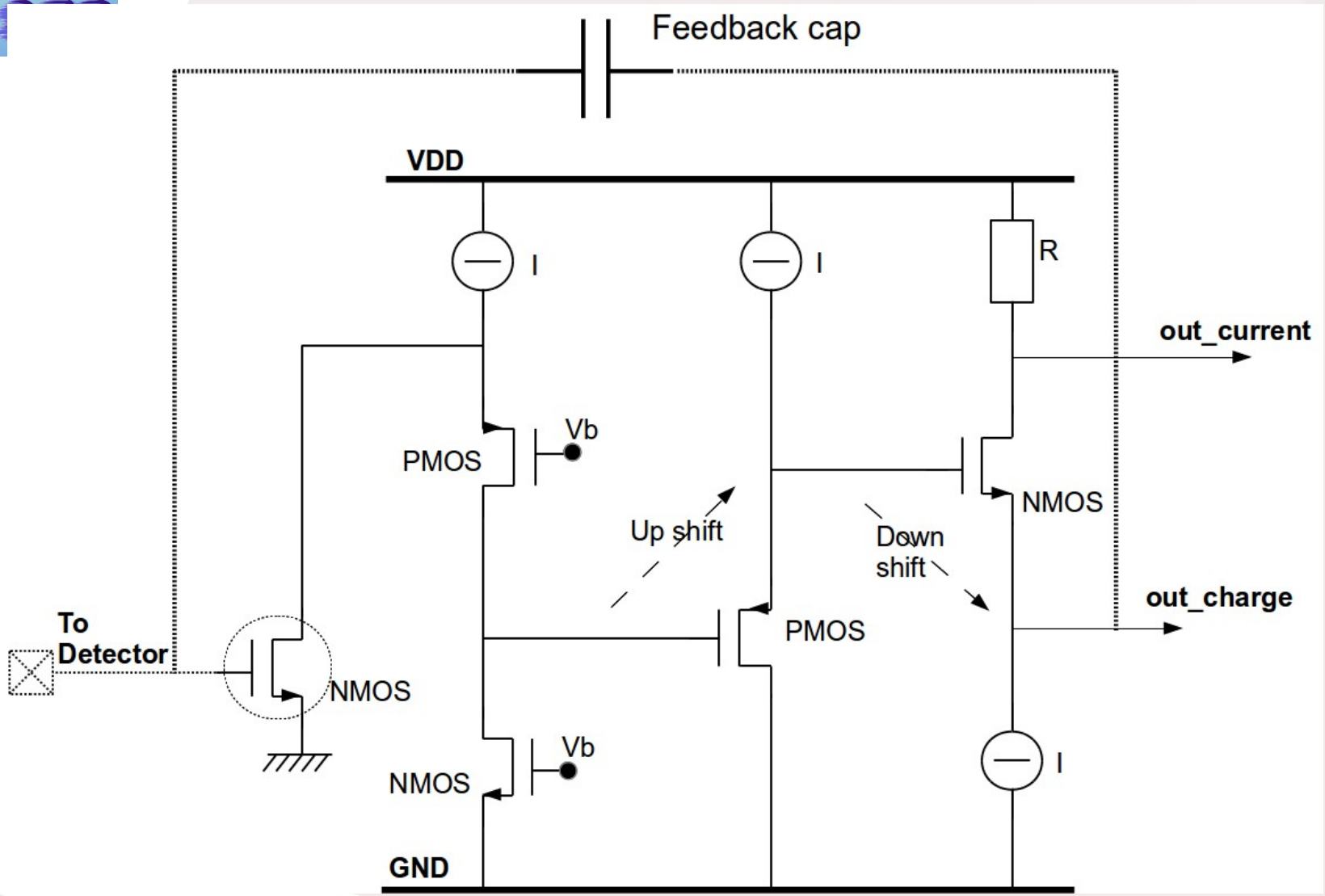
	Charge Output
Energy max (Si)	50 MeV
Charge signal swing (50MeV)	1.6V single ended
Charge gain	32mV/MeV
Equivalent noise charge (Input-refered, FWHM)	7 keV 830 e- Si
Charge resolution	12.8 bits ENOB
Charge non-linearity	< 2%
Charge output recovery time	100µs
	Current Output
Current gain	7kΩ
Current signal swing	1.5V single ended
Current signal BW	[4MHz .. 120MHz]

	System data
Technology	AMS 0.35µm BICMOS
Supply	3.3V
Detector's input capacitance	Compatible with [10pF .. 40pF] range
Compensation cap	Digitally tunneable within [0.5pF .. 2.25pF], step 0.25pF
Current consumption	12mA (40mW) / Channel
Size	220 x 100µm (PACI block) + 130 x 70µm (Buffer ch) + 130 x 70µm (Buffer cu)

Charge and current transient outputs

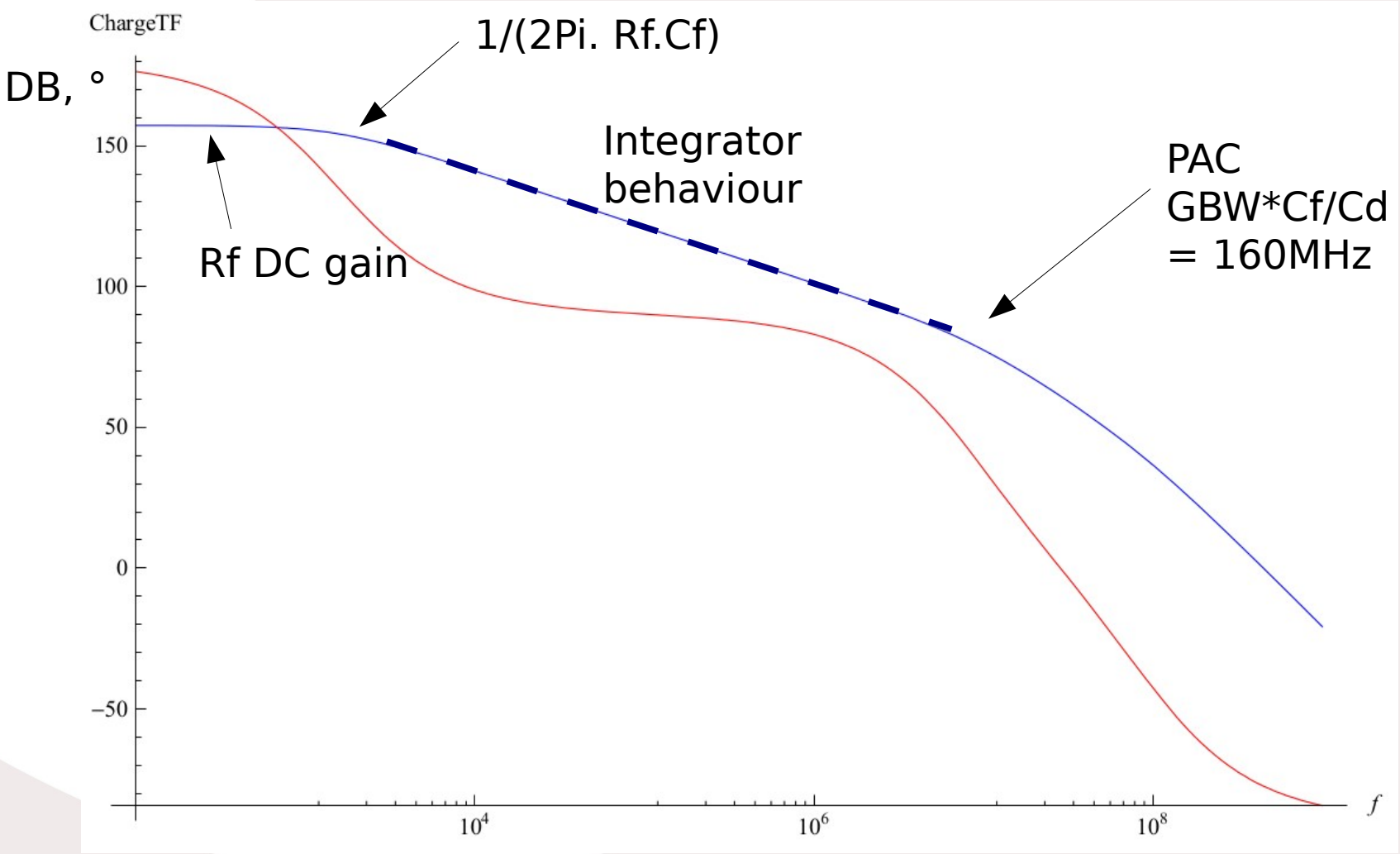


PACI schematic



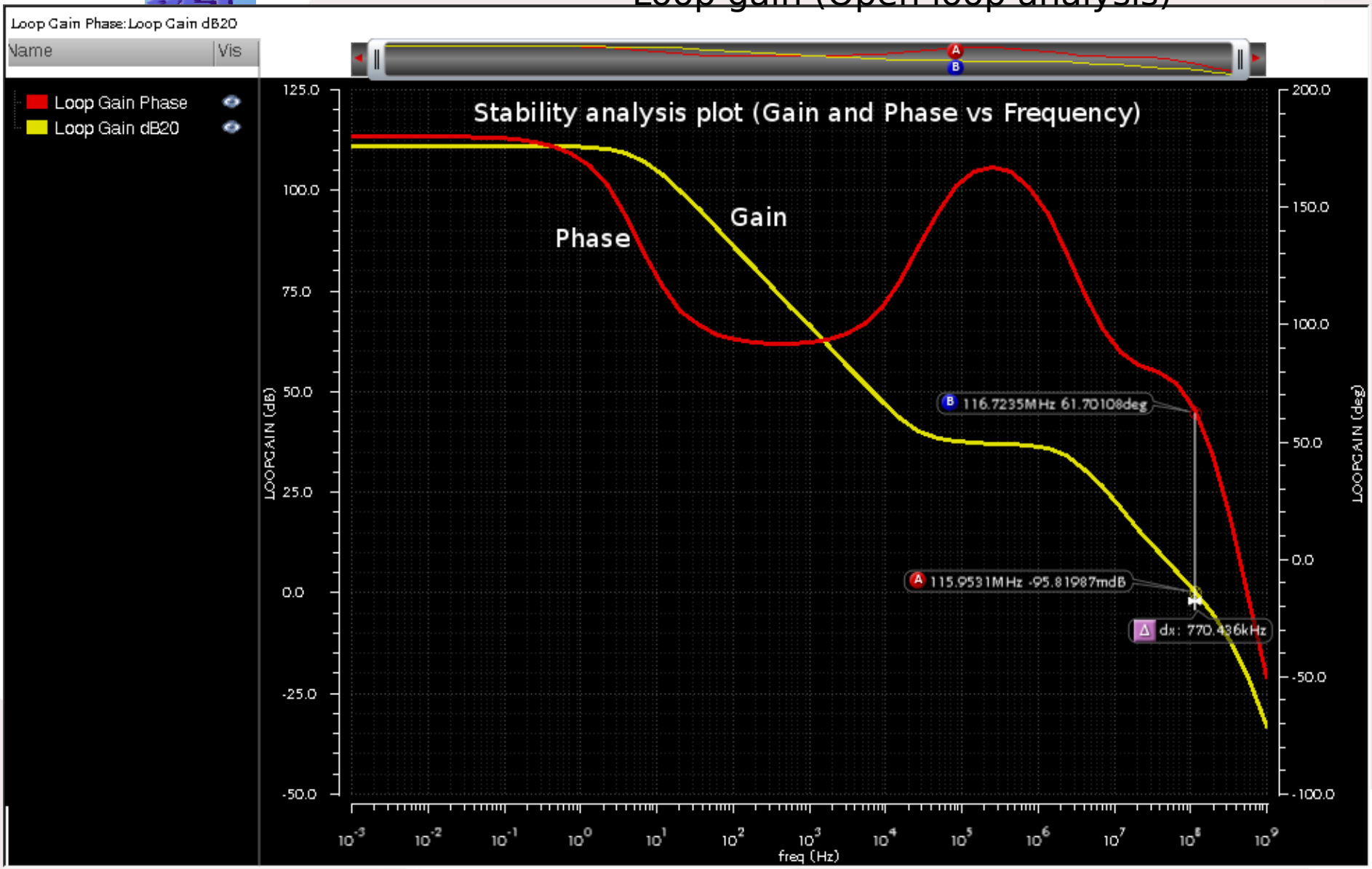
PAC modeling

Transfer Function
(Charge output / Detector current)

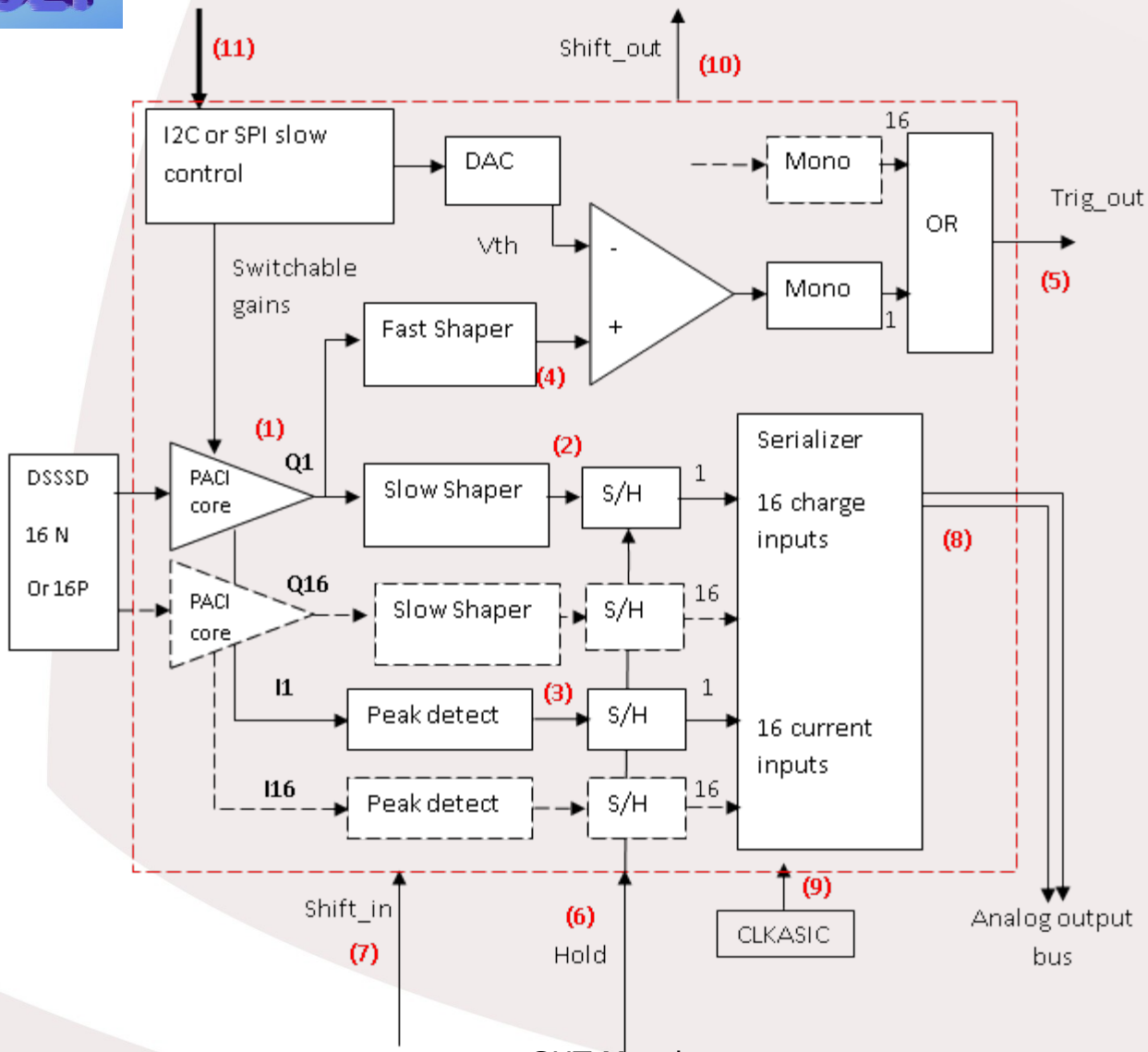


PAC stability

Loop gain (Open loop analysis)



PACI -possible- final version, analog option



PACI -possible- final version, digital option