Synchonisation and Trigger

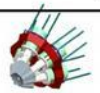
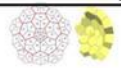
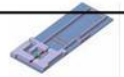
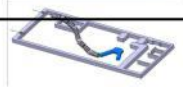
- Instrumentation and Coordination Committee

- The MUTANT system

- The GTS system

Synchonisation and Trigger

Instrumentation and Coordination Committee
Electronics Working Group members

SPIRAL2 detector projects	
ACTAR 	Gilles Wittwer wittwer@ganil.fr
AGATA 	Michel TRIPON tripon@ganil.fr
DESIR 	
EXOGAM2 	Abderrhaman BOUJRAD boujrad@ganil.fr
FAZIA 	Frank Salomon d'Orsay salomon@ipno.in2p3.fr , Maurizio Bini de Florence bini@fi.infn.it
GASPARD 	Didier BAUMEL beaumel@ipno.in2p3.fr
NEDA 	Vicente Gonzalez Millan. vicente.gonzalez@uv.es
NFS 	Stefano Panebianco stefano.panebianco@cea.fr
PARIS 	Adam CZERMAK adam.czermak@ifj.edu.pl
S3 	Nabil Karkour Nabil.Karkour@csnsm.in2p3.fr

ICCEWG overview

- MOTIVATIONS:

To find out and to develop synergies in hardware, firmware and embedded software fields for the instrumentation of the SPIRAL2 future detectors

- MEETINGS:

9 meetings since 2009

3 meetings about trigger and synchronization systems: CENTRUM, TDR, BUTIS, MUTANT, GTS

- ICCEWG technical report and recommendations (January 2012)

1. **ICCEWG advises the designers to incorporate the MFM data format.**

2. **ICCEWG recommends the GTS and the MUTANT systems** which will be deployed at GANIL for coupling detector instrumentations.

3. **Designers can implement interfaces to the GTS or MUTANT system**, from the simple trigger less system (clock and synchronization) to the full system with all the trigger facilities.

Synchonisation and Trigger

MUTANT

On behalf of G.F.GRINYER and G. WITTWER

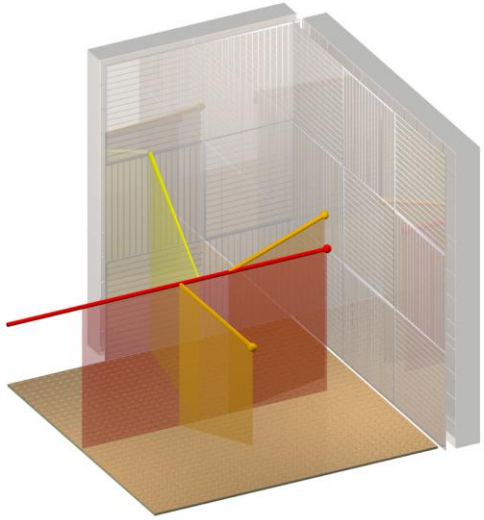
-This Synchronization and Trigger system has been developed in the framework of GET instrumentation
- GET electronics instruments the ACTAR TPC detector

ACTAR TPC detector

Demonstrator :
- **2048 channels**

In-beam test @ GANIL
Campaign @ IPN Orsay in 2015

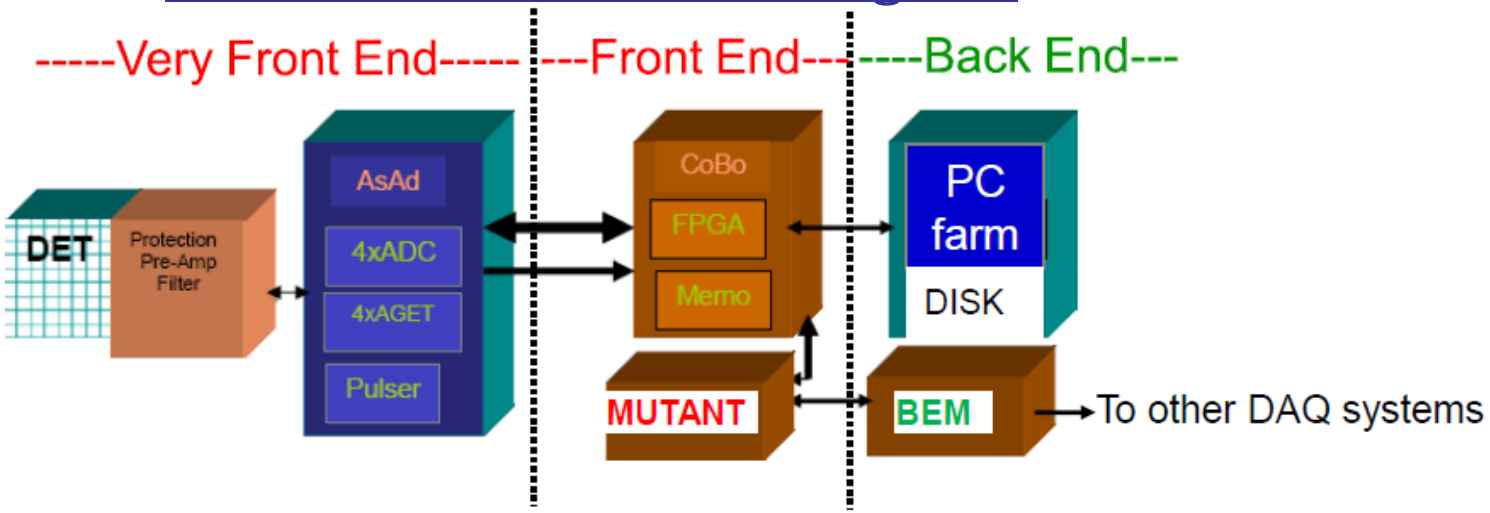
Final Detector
- **16384 channels in 2016**



Synchonisation and Trigger

MUTANT

GET electronics block diagram



AGET: Asic for GET – 64 analog channels - 512 cells/channel **IRFU**

ASAD: ASic and Analog to Digital converter - 4 AGET + 4 ch. ADC **CENBG**

COBO: COncentration BOard – 4 ASAD - 1024 digital channels **NSCL/MSU**

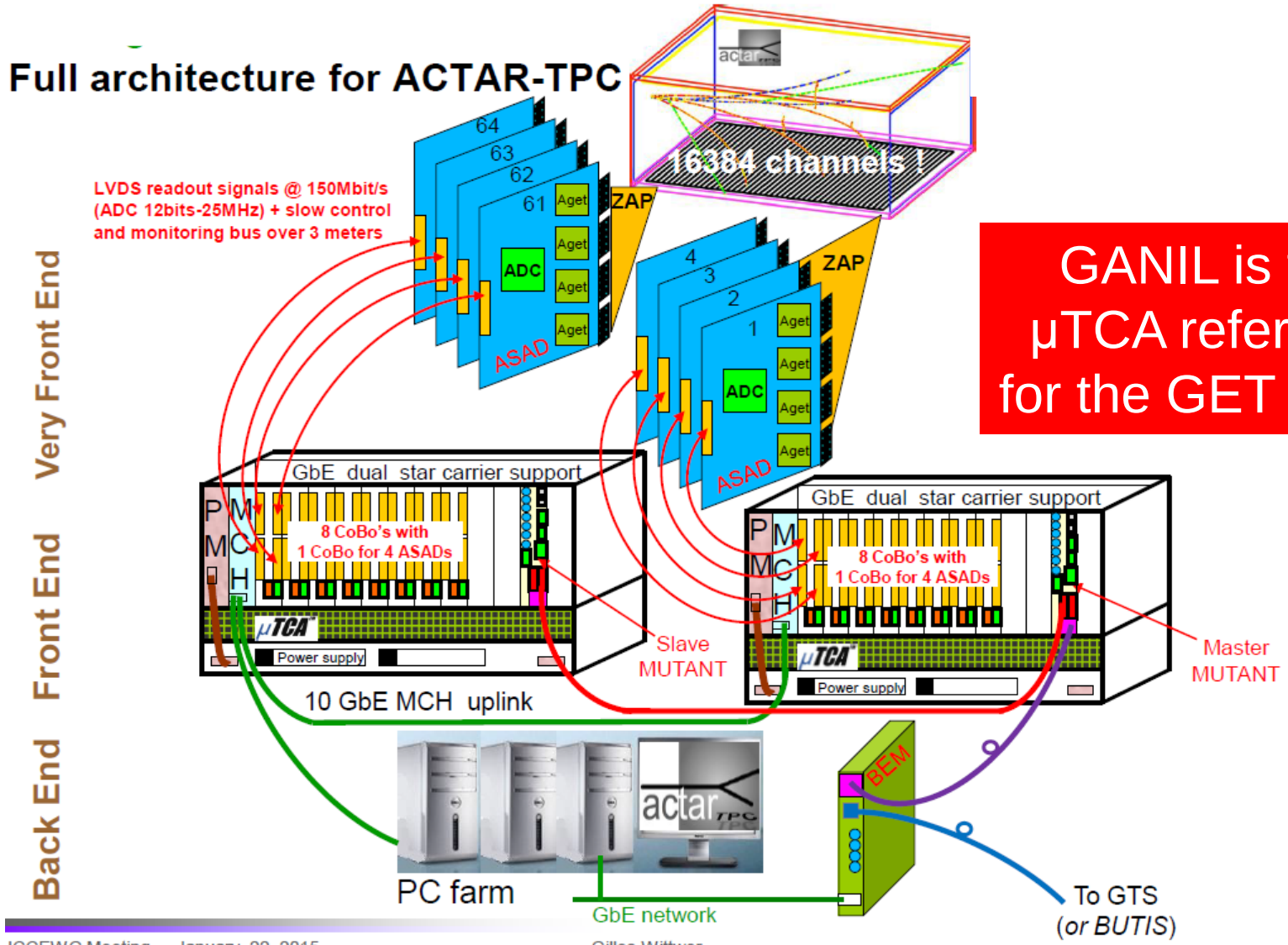
MUTANT: MUtiplicity, Trigger ANd Time (3 trigger levels)

BEM: Back End Module (coupling, remote inspections, …)

collaboration based on an "ANR" grant for the French labs (2009-2014)

Synchonisation and Trigger

ASAD, COBO and MUTANT integration



GANIL is the µTCA reference for the GET project

Synchonisation and Trigger

ASAD

MUTANT , COBO

MUTANT functionalities

Among the main tasks of MUTanT

Distribution of a 100 MHz clock (GMC) to every CoBo of each crate, phase aligned (skew< 1ns - TDC) ⇨ µTCA-CLK1

Distribution of a synchronous start/stop sampling (phase aligned) (WSCA)⇨ µTCA-CLK2

Exchanging data in parallel with the CoBo @ 800 Mbit/s (TX/RX) with its own shelf and **slave shelves**

Building the whole TPC Digital multiplicity:
- Master MUTANT + **slave MUTANT**
- Each MUTANT with the CoBo boards every 40 ns

3 Trigger levels:
- -LØ= External Trigger
- -L1 = Multiplicity Trigger
- -L2 = Hit Pattern Trigger

Time stamp:
- 48 bits / 10 ns
- CDT/autonomous mode
- 32 bit event number (CDT)
- local/**remote (via BEM)**

actar TPC

is the good example to validate all these aspects!

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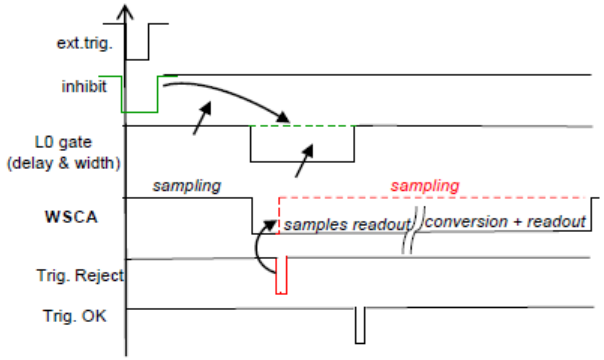
Synchonisation and Trigger

MUTANT

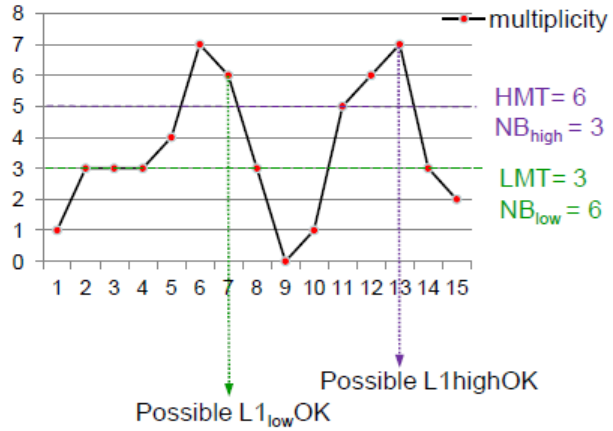
Trigger modes for level 0 and 1

L0: external trigger attached to a programmable gate & delay
with reject and inhibit options



L1: Time over multiplicity threshold with:

- 2 sets of Multiplicity Threshold/Number of Buckets
  (HighMT/NB_{high} and LowMT/NB_{low})
- Logical combination of $L1_{low}OK$ and $L1_{high}OK$ for the final L1 OK:
  L1OK = $L1_{low}OK$
  L1OK = $L1_{high}OK$
  L1OK = $L1_{low}OK$ or $L1_{high}OK$
  L1OK = $L1_{low}OK$ and $L1_{high}OK$
- 2 proton decay mode with 2 successive L1 cycles
  L1 OK for implantation followed or not by a L1 OK for decay
  (with timeout and Half Event Readout option)

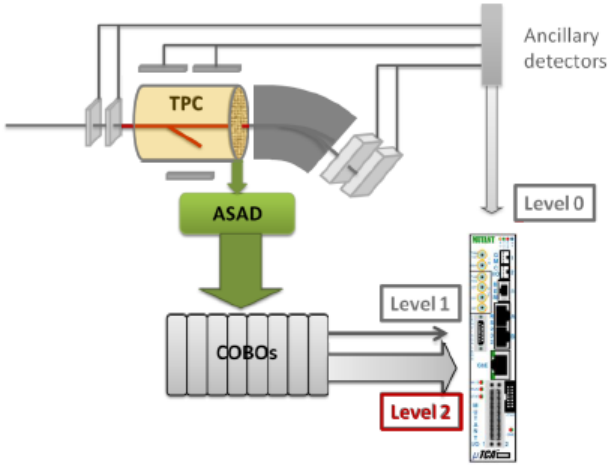


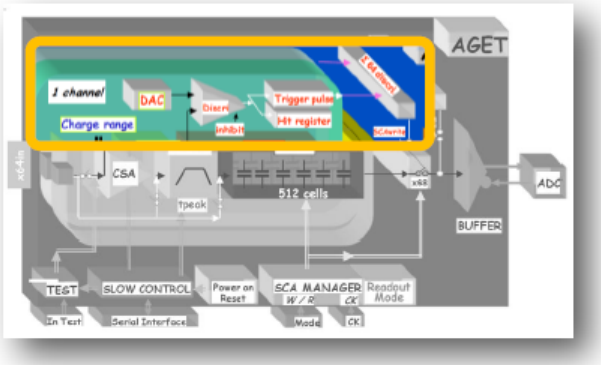
L0/L1: Coincidence of L1 OK with L0 gate triggered externally
or L1 OK starts L0 gate (with delay and width) waiting
for an external validation.

Synchonisation and Trigger

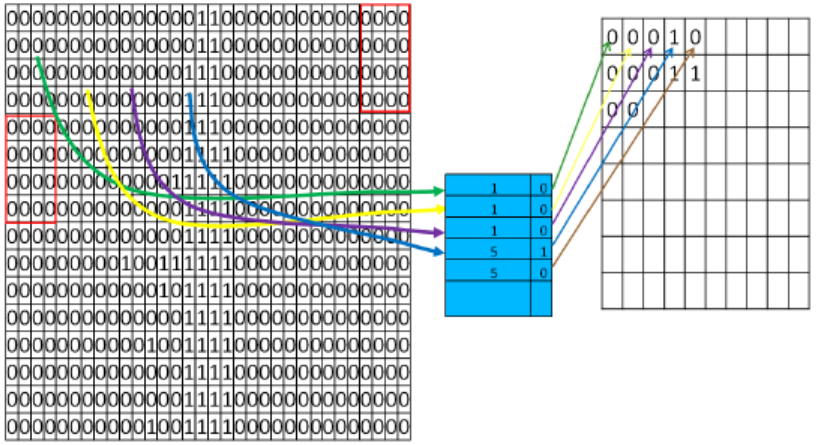
MUTANT

Trigger modes for level 2





- Global hit pattern from all pads
- Comparison: possibilities of using “macropads” with thresholds
  4 × 4, 8 × 8, 16 × 16
- Mask pattern option
- Decision and readout



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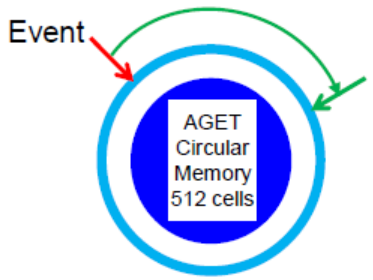
Synchonisation and Trigger

MUTANT

MUTANT- CoBos data exchanges
main time values

AGET: Sampling Frequency = 1-100 MHz
Trigger roundtrip: 512 x 10 ns = 5.12 µs
to 512 x 1µs = 512 µs

Full memory

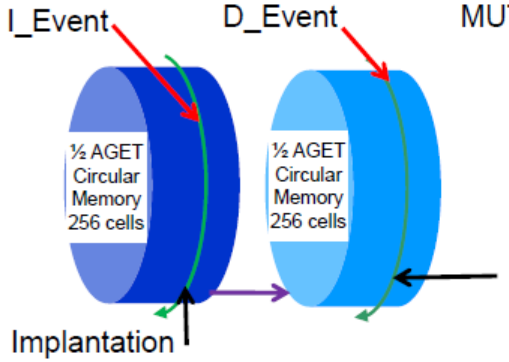


MUTANT Programmable Delay & Gates are 16 bits wide
Attached to GMC (10 ns)

CoBo to MUTANT : L1: new multiplicity value @ 25 MHz max
nothing to do @ MUTANT level for lower frequency
L2: 1.3µs to receive the TPC hit pattern (one shelf)
12.8 µs for added shelves

MUTANT trigger "OK" to CoBo "STOP": -LØ : 30 ns/655 µs max
- L1 : 80 ns /655 µs max
- L2 : depends on the algorithm !

2 x half-memories (2p decay)



MUTANT information's to CoBo: - L2 mask pattern: 1.3 µs
- Time stamp + Event Number: 120 ns
- Time stamp only: 80 ns

Decay Trigger (L1B) or
Time-out (programmable)

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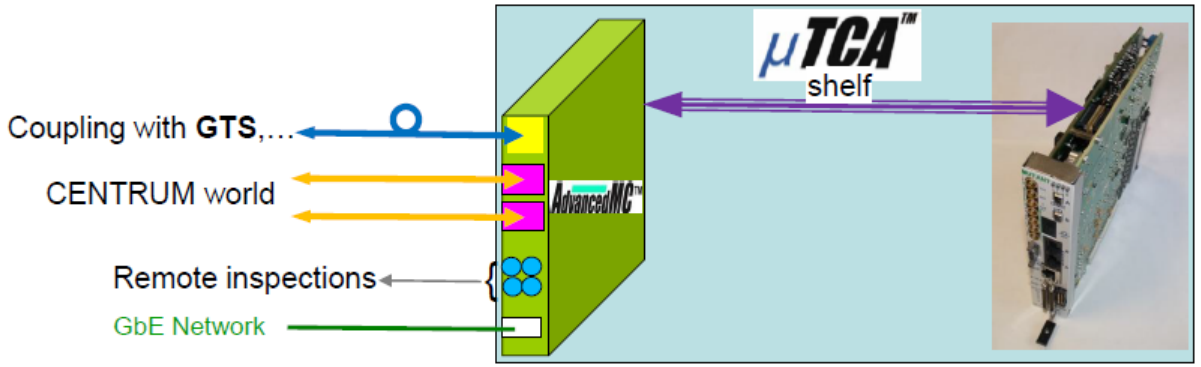
Synchonisation and Trigger

MUTANT

3-Coupling:

About Back End Module (BEM) design

ACTAR-TPC with MUTANT: **Ready today for coupling @ GANIL with CENTRUM interface !**
But tomorrow with SPIRAL2 instrumentations, or when ACTAR-TPC will move to other laboratories ?



Goal: Be able to synchronize ACTAR-TPC DAQ (Clock & Time stamp) by an external system or using the ACTAR-TPC DAQ as reference if ancillary detectors are added to the TPC

Work to do: Writing specifications in mid 2015, and starting design after summer 2015

Synchonisation and Trigger

MUTANT

Scheduled

- µTCA configuration validation (CoBos + MUTANT) early 2015
- MUTANT mass production during 2015 (2 batches)

First users through the world
(with new TPC, Si detectors,…)

(Caen, Saclay Bordeaux)
(Michigan, Texas)
(Catania)
(Riken, JPARC)
(Daejeon)

Planned

Global Trigger and Synchronisation system

Foreword:

❖ The **GTS** has been chosen by GANIL for the **instrumentation of the EXOGAM** detector

❖The GTS has been retrieved from the instrumentation of **AGATA**, the European Ge Advanced GAmma Tracking Array detector.

❖The GTS was designed by the **INFN Padova laboratory.**

***GTS components*:**

❖**Tree topology**

❖ Hardware: **GTS V3 custom mezzanines, COTS Xpress Gen2V5 Trigger Processor, Optical** links**, Local Ethernet** network

❖ Firmware: GTS V3 set up as either **ROOT,** either **FANIN-FANOUT,** either **LEAF**

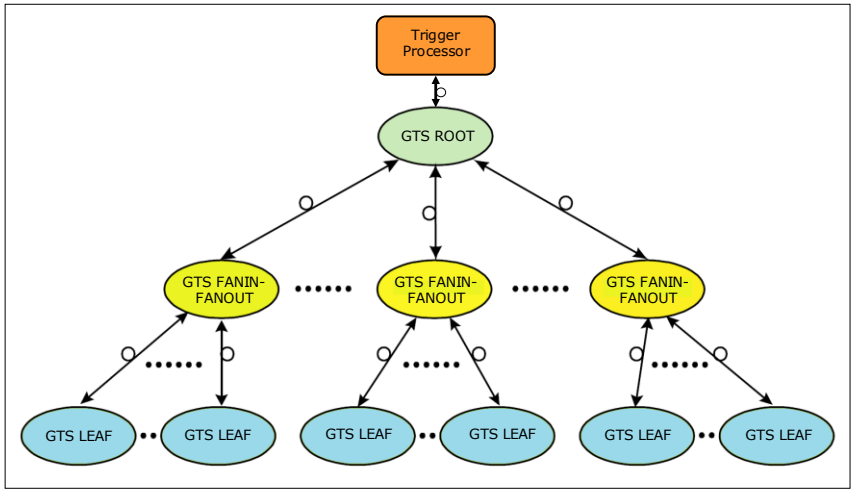
❖Software: Embedded software in **VxWorks environment, GTS command server**

GTS functions:

❖Synchronization and trigger signals are issued from **optically broadcasted messages** between the digitizers (attached to the GTS LEAVES) and the Trigger Processor. In these messages at **2 Gb/s** speed, the **GTS**:

1. **drives the recovered 100 MHz common clock**
2. **sources the time stamp** (48 bits, 10ns resolution)
3. **broadcasts trigger decisions**

XpressGen2V5 Trigger Processor



GTS V3 mezzanine

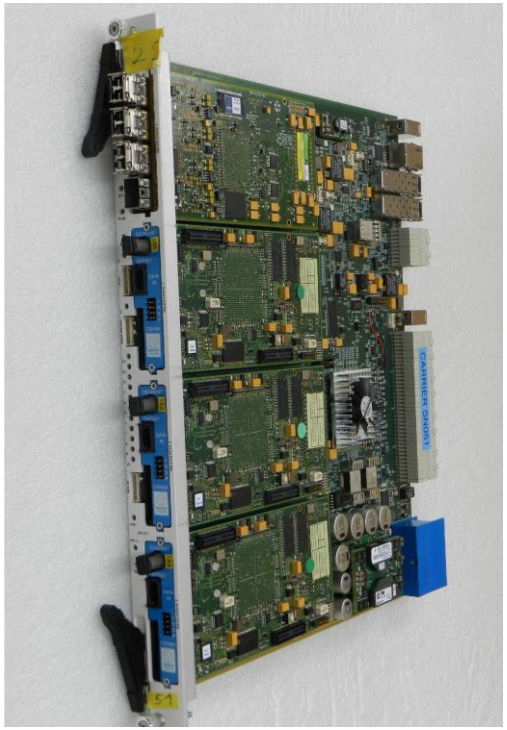
Synchonisation and Trigger

Global Trigger and Synchronisation system

GTS V3 housed in carriers

GTS V3 on VME board

4 GTS V3 housed
in 2/12 NIM module



1 GTS V3 housed
In ATCA processing card

Synchonisation and Trigger

Global Trigger and Synchronisation system

Coupling ancillary detector to the GTS

Ethernet link to GST mezzanine

connectors to TDR

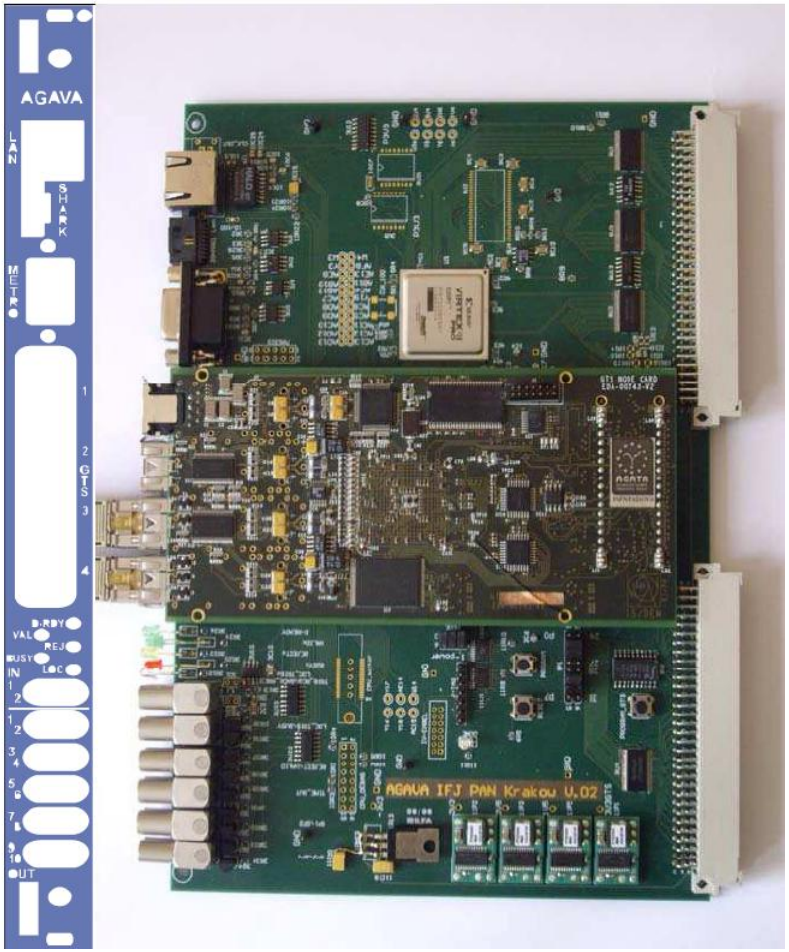
GTS optical clock lines

control LEDs:
DATA-ready, Val.,
Rej., busy, Loc_Trig.

Input signals:
back pressure, Trig. request

fixed inspection lines:
- Loc_trig., Rej., Val.
- busy, timeout

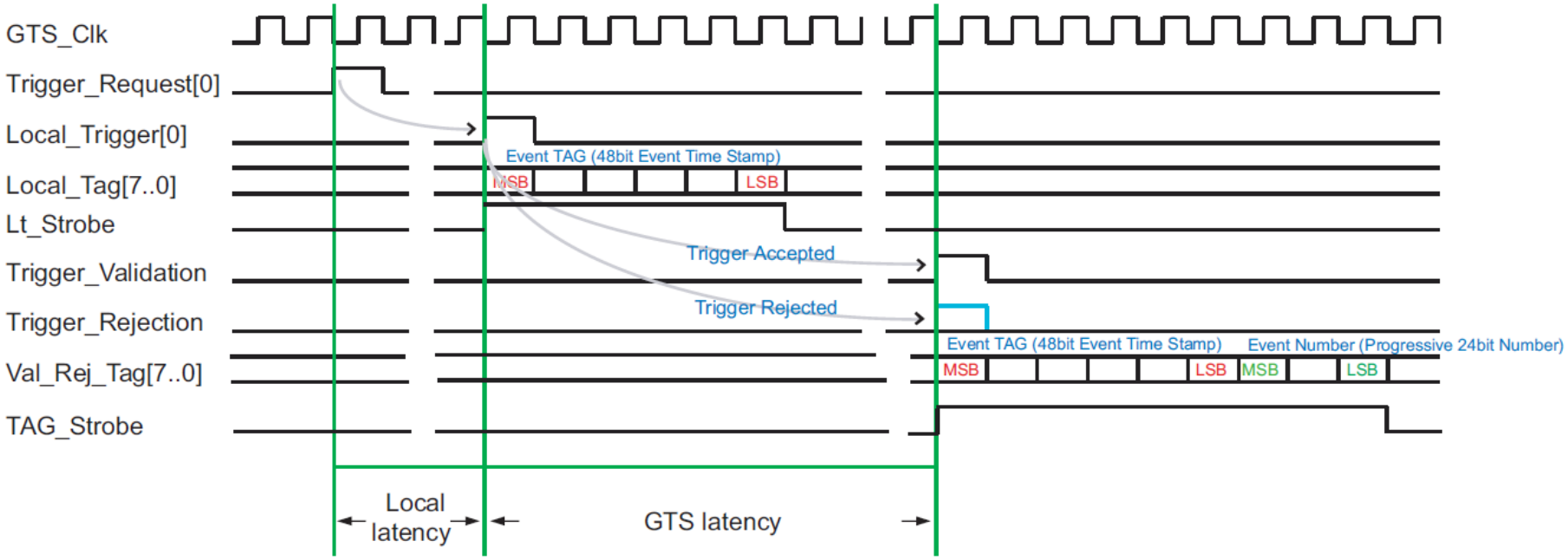
programmable inspection lines



AGAVA and GTS V3 mezzanine

Global Trigger and Synchronisation system

Current GTS cycle

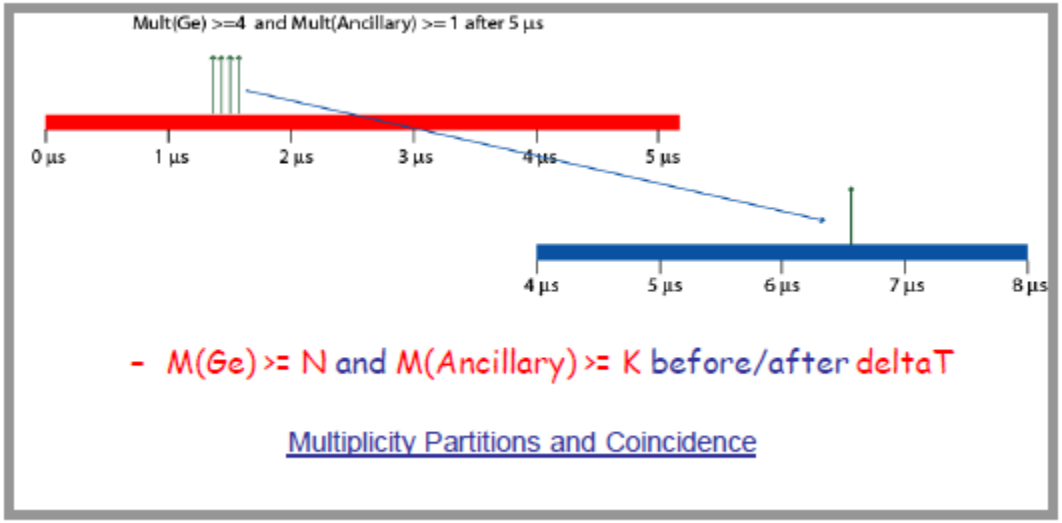


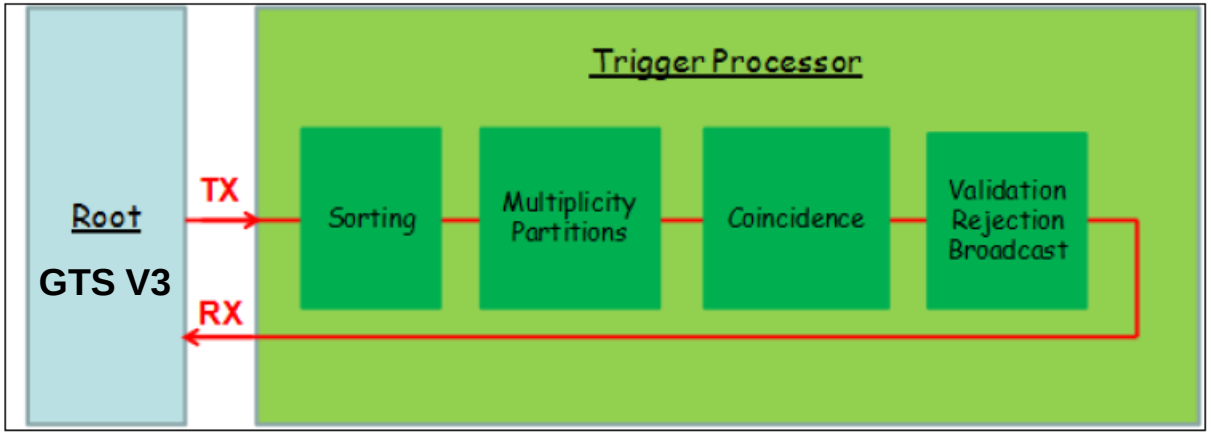
GTS clock period = 10ns; Local Latency = 10ns; GTS latency > 10µs

Synchonisation and Trigger

Global Trigger and Synchronisation system

Current GTS Trigger Processor





Trigger Processor sketch (simplified)

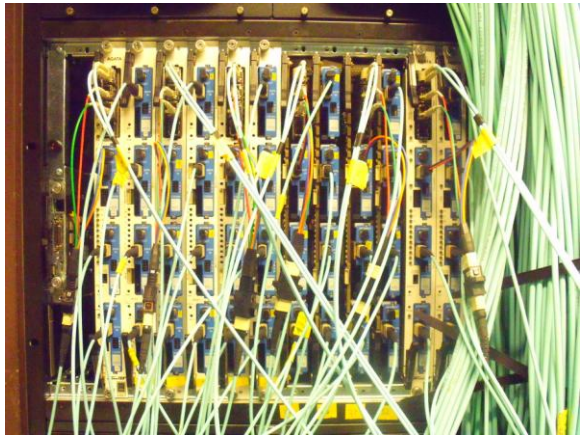
XpressGen2V5 Trigger Processor

Trigger Processor VHDL code
is implemented in the
Virtex 5 FX200
of the XpressGen2V5 PCI board

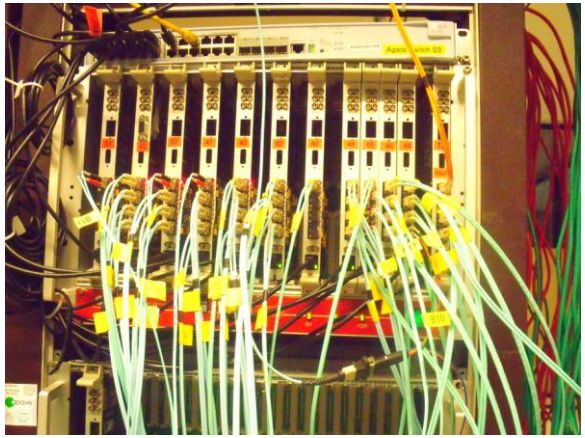
Synchonisation and Trigger

Global Trigger and Synchronisation system

AGATA GTS tree



GTS V3 mezzanines housed in ATCA cards LEAF



GTS V3 mezzanines housed in VME carriers FIFOs and ROOT

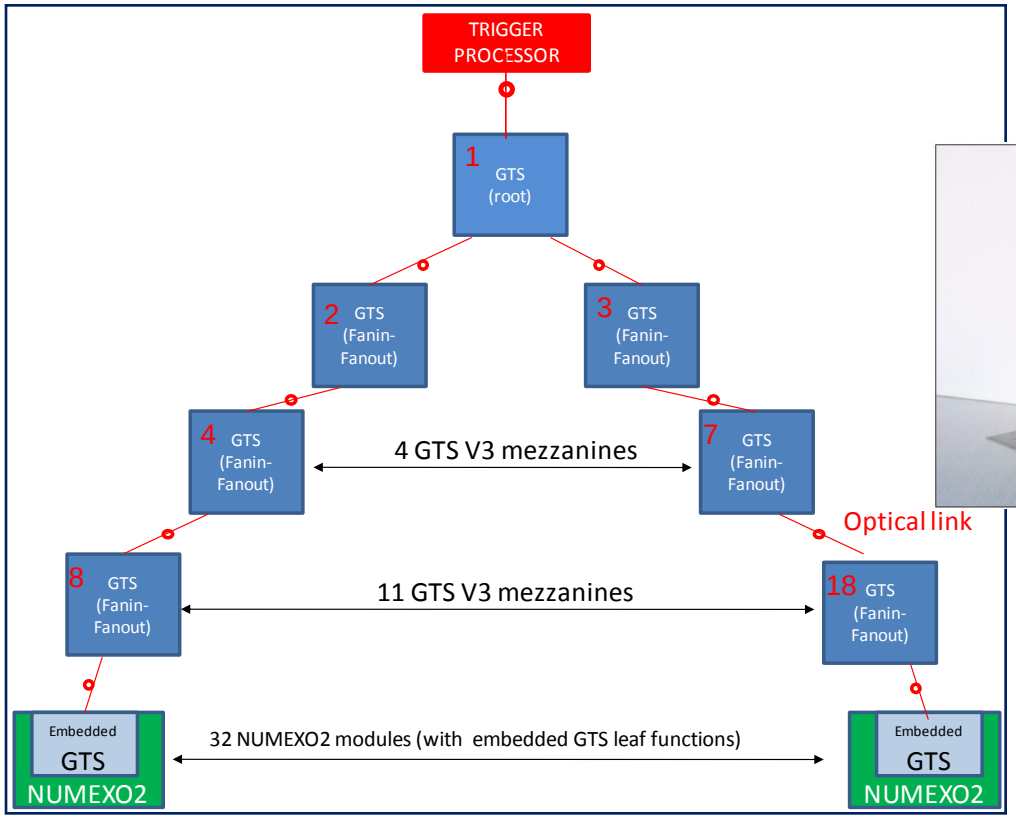
AGATA demonstrator: 25 Ge Crystals
25 core Ge channels => GTS tree features 38 GTS V3 mezzanines:
(25 GTS V3 leaves, 12 FIFOs, 1 ROOT)

AGATA full setup : 180 Ge Crystals
180 core Ge channels => GTS tree features 271 GTS V3 mezzanines:
(180 GTS V3 leaves, 90 FIFOs, 1 ROOT)

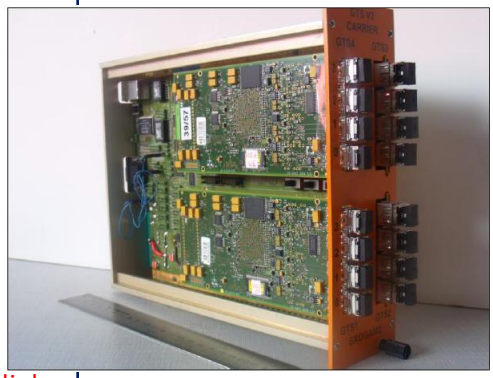
Global Trigger and Synchronisation system

EXOGAM GTS tree (full setup)

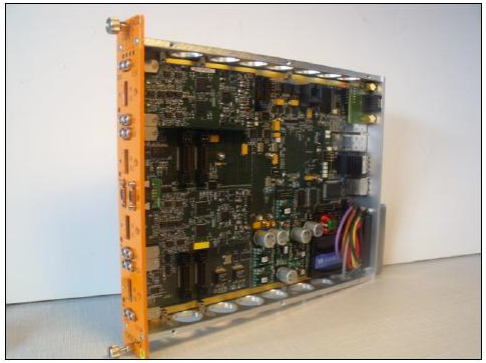
- 32 GTS leaves embedded in 32 NUMEXO2 digitizer
- 18 GTSV3 FanIn-FanOut
- 1 GTS V3 root
- 1 GTS Trigger Processor (under development)



GTS V3



NUMEXO2



Global Trigger and Synchronisation system

Drawbacks of the current GTS

1) **One Trigger Request** (detector channel discriminator) **per optical link** to the GTS tree
   => EXOGAM2 requirements : 2 TR per optical link

2) **Number of GTS V3 cards in the GTS tree < 255**.
   => Number of GTS leaves in the current GTS tree < 170

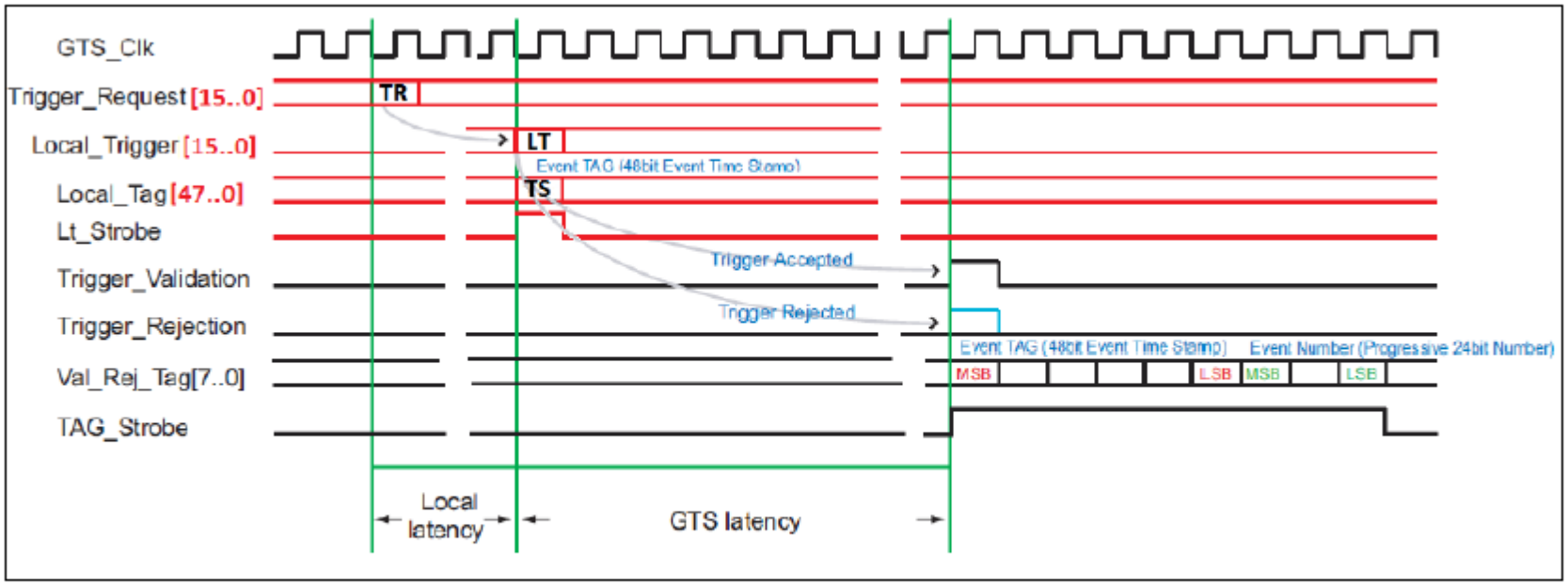
3) **Total number of TR** (detector channel label) **< 255**
   => EXOGAM2 requirements: 64 TR
   => NEDA requirements : > 300 TR

4) **Total number of TR handled by the current trigger processor < 40 TR**
   => EXOGAM2 requirements: 64 TR

Global Trigger and Synchronisation system

GTS upgrade
Point 1 : 16 TR per GTS leaf connection to the tree

=> GTS leaf firmware, implemented 16 TR per leaf, was successfully NUMEXO2 digitizer leaf



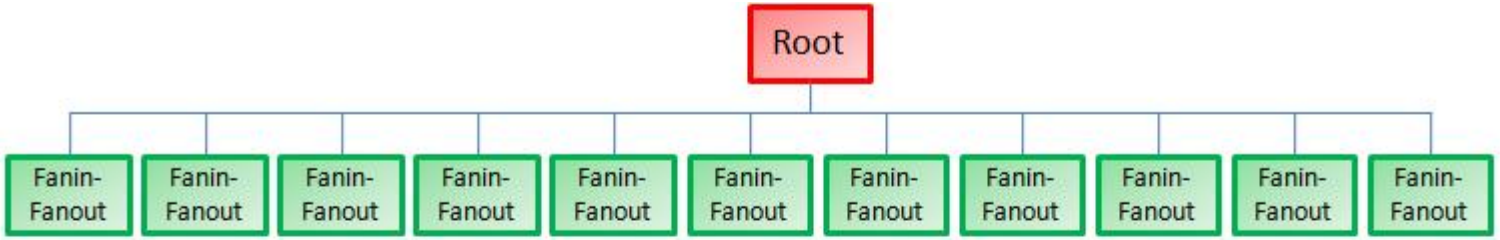
NUMEXO2 GTS cycle

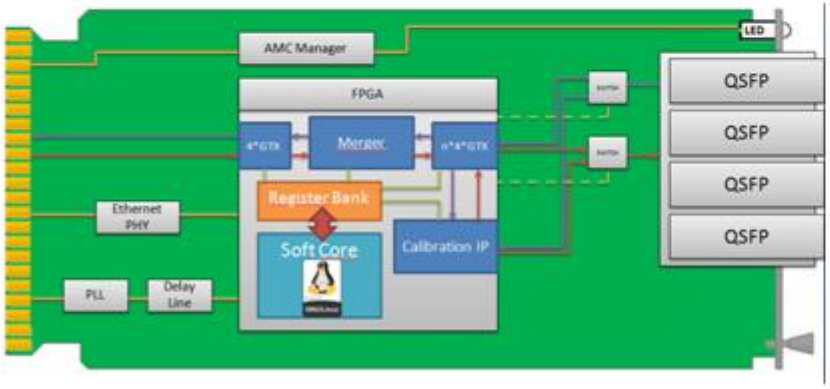
Synchonisation and Trigger

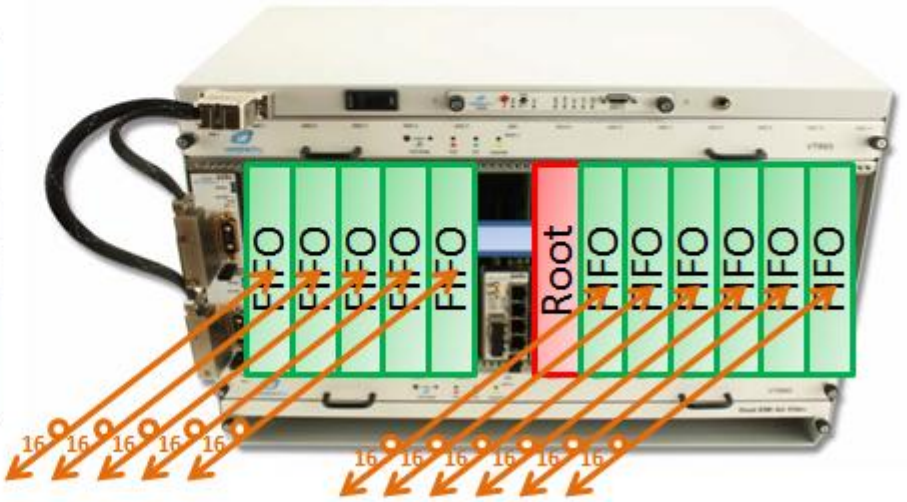
Global Trigger and Synchronisation system

GTS upgrade
Points 2 and 3 : more than 255 TR in the GTS tree

=> GANIL proposal for a GTS tree migration towards the µTCA



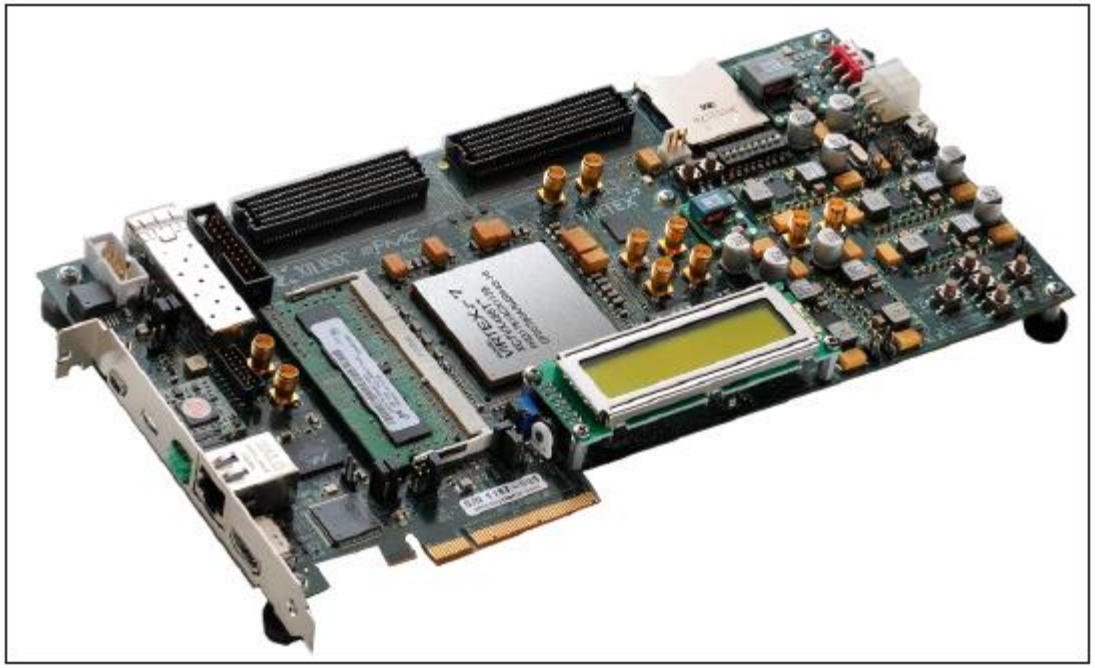




Global Trigger and Synchronisation system

GTS upgrade
Point 4 : more than 40 TR handled by the Trigger Processor

⇒ Firmware development ongoing in Virtex 7
⇒ TP hardware = Xilinx VC707 housed in custom box



Xilinx VC707 development kit