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Design of full custom Data Transmission Unit and M-LVDS transceiver for the Monolithic Active Pixel Sensor chip for the upgrade of the ALICE Inner Tracking System.

In this work we will present the Data Transmission Unit (DTU) and the M-LVDS transceiver designed for the periphery of the ALICE Inner Tracking System (ITS) front-end chip. Actually, in view of the LHC upgrade, even the inner tracker of ALICE has to be upgraded. The ITS upgrade is one of the major project of the upgrade of the ALICE apparatus planned for 2019-2020. In particular, in order to increase granularity, the ITS will be equipped with 7 layers of monolithic active pixel sensors which will cover 10 m2 with 12.5 Gpixels. In order to deal with the increase of the data volume, the DTU sends data out of the chip at the targeting speeds of 1.2 Gb/s and 400 Mb/s. This serial link consists of a 600 MHz clock multiplier PLL, a serializer which works in Double Data Rate and a pseudo-LVDS driver with pre-emphasis. The PLL has a multiplication factor of 15 that is necessary to obtain a 600 MHz and 200 MHz clock from the 40 MHz input clock. The faster clock is sent to the serializer which provides data output at 600 Mb/s and 200 Mb/s respectively. The pseudo-LVDS driver works at 1.2 Gb/s or 400 Mb/s and it has to drive a full 5.3m or 6.5m differential line. In this respect the pre-emphasis was mandatory to overcome the RC limitations imposed by the line.

The M-LVDS transceiver is used to distribute the 40 MHz clock and for chip-to-chip communication. This unit consists of a tristate LVDS based driver and a LVDS receiver where the former allows for a half-duplex topology in which only one driver can transmit while every receiver in the line is receiving. Even if the driver works at 40 MHz (80 Mb/s), it has to drive a 6.5m differential line at which multiple transceivers are connected. For this reason the driver strength of the M-LVDS driver has to be greater then the one of a LVDS driver.

Those two full custom blocks were designed in the 0.18 um CMOS technology chosen for the R&D of the ITS front-end chip.

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