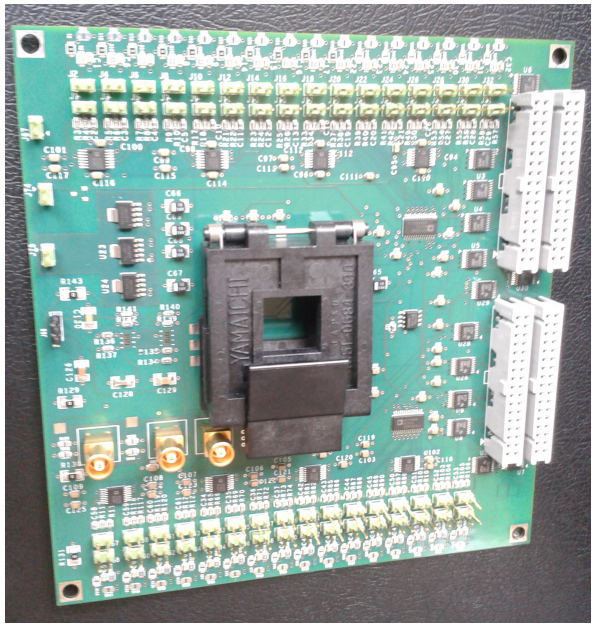
Profiler test electronics: preliminary tests of the evaluation board

Matteo Cecchetti, Giuseppe Battistoni,
Mauro Citterio, Alessandro Andreani,
Adalberto Sciubba

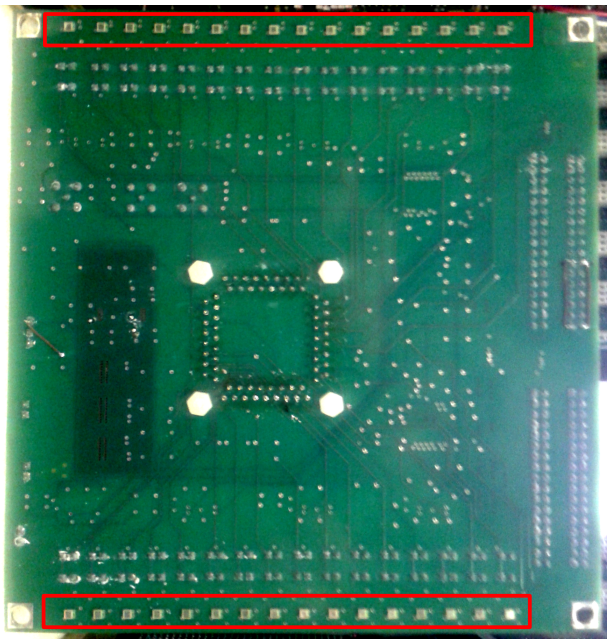
INSIDE Meeting – 18th December 2014, Roma

INFN
Istituto Nazionale
di Fisica Nucleare
SEZIONE DI MILANO

- The evaluation board has been fully assembled
- The board testing has begun during the first week of November
- A preliminary version of the V1495 firmware has been developed

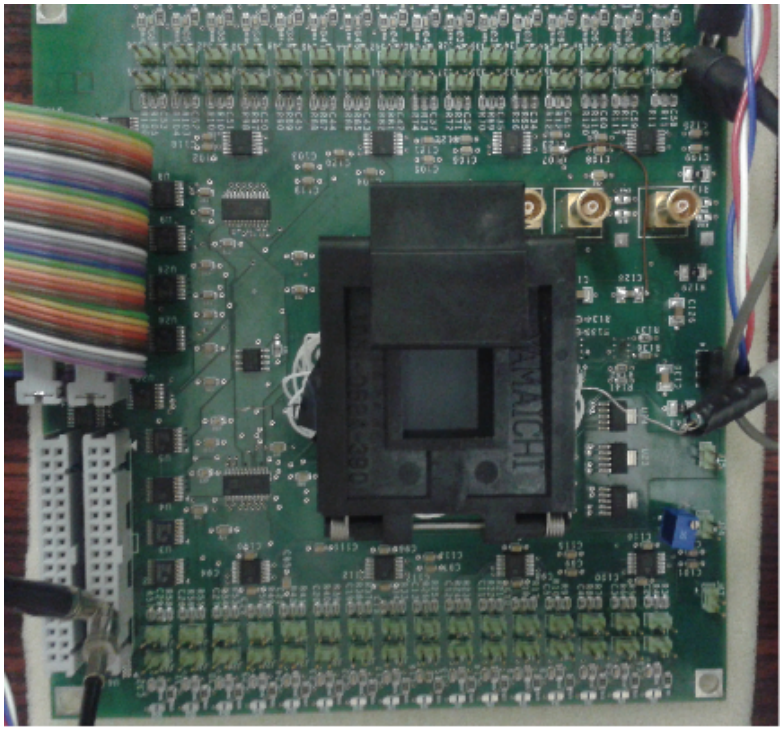


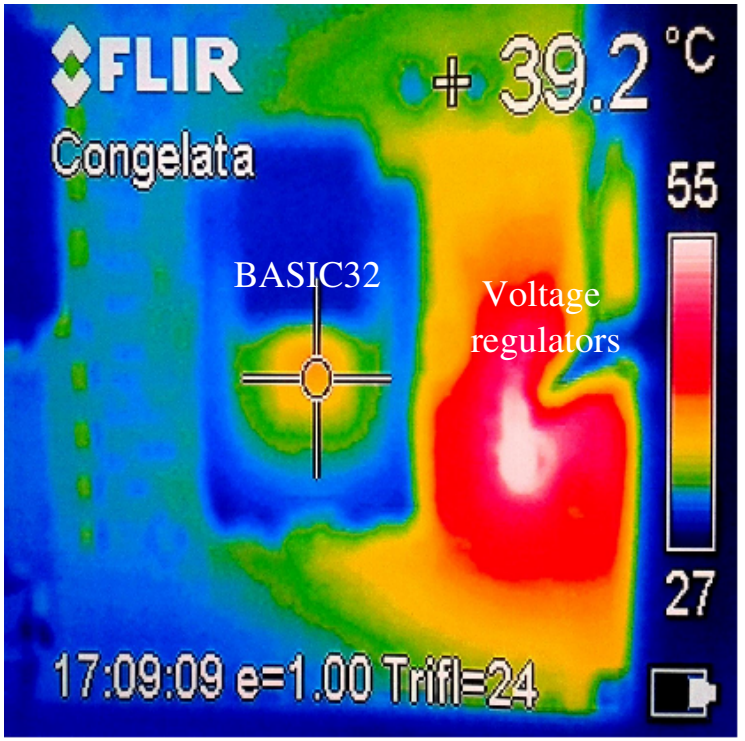
SiPMs



Current absorption and thermal test

- The current absorbed by the evaluation board is approximately 200mA when the BASIC32 is inserted, 100mA otherwise.
- Thermal test few minutes after turning on the board

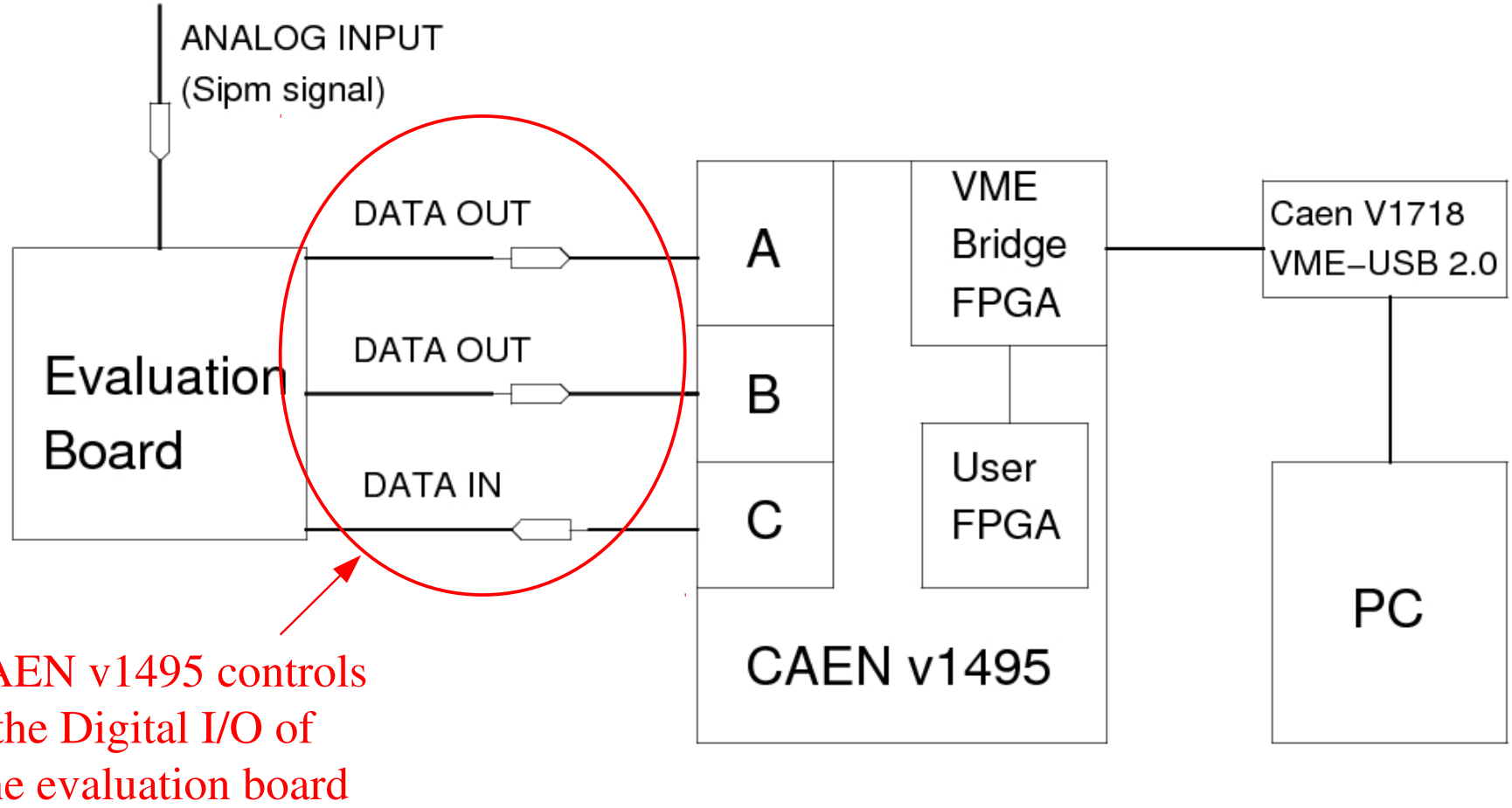




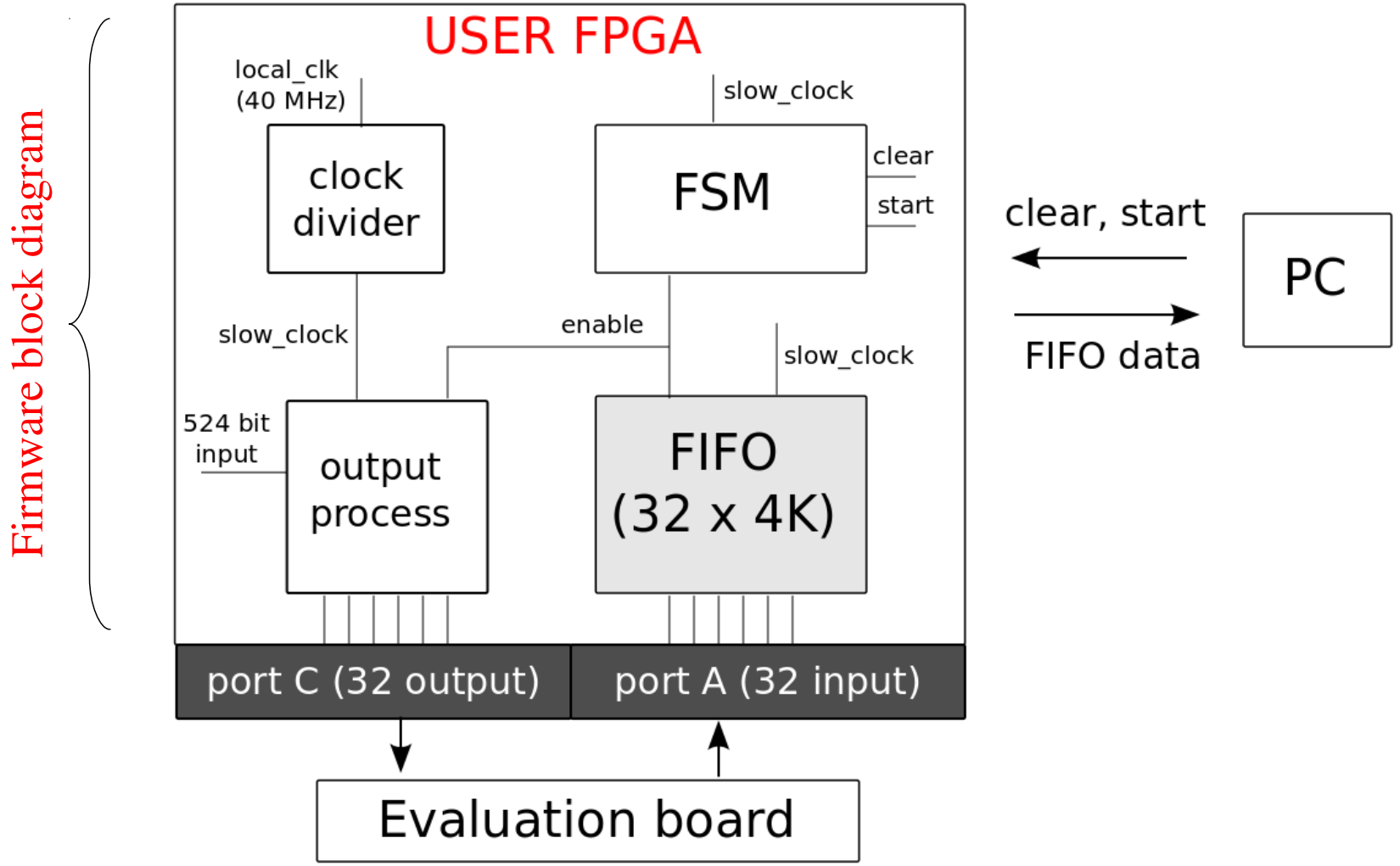
BASIC32 ~ 39°C

Voltage regulators ~ 55°C

- In order to test the evaluation board we need a system able to control the input signals of the board and to store the digital output.

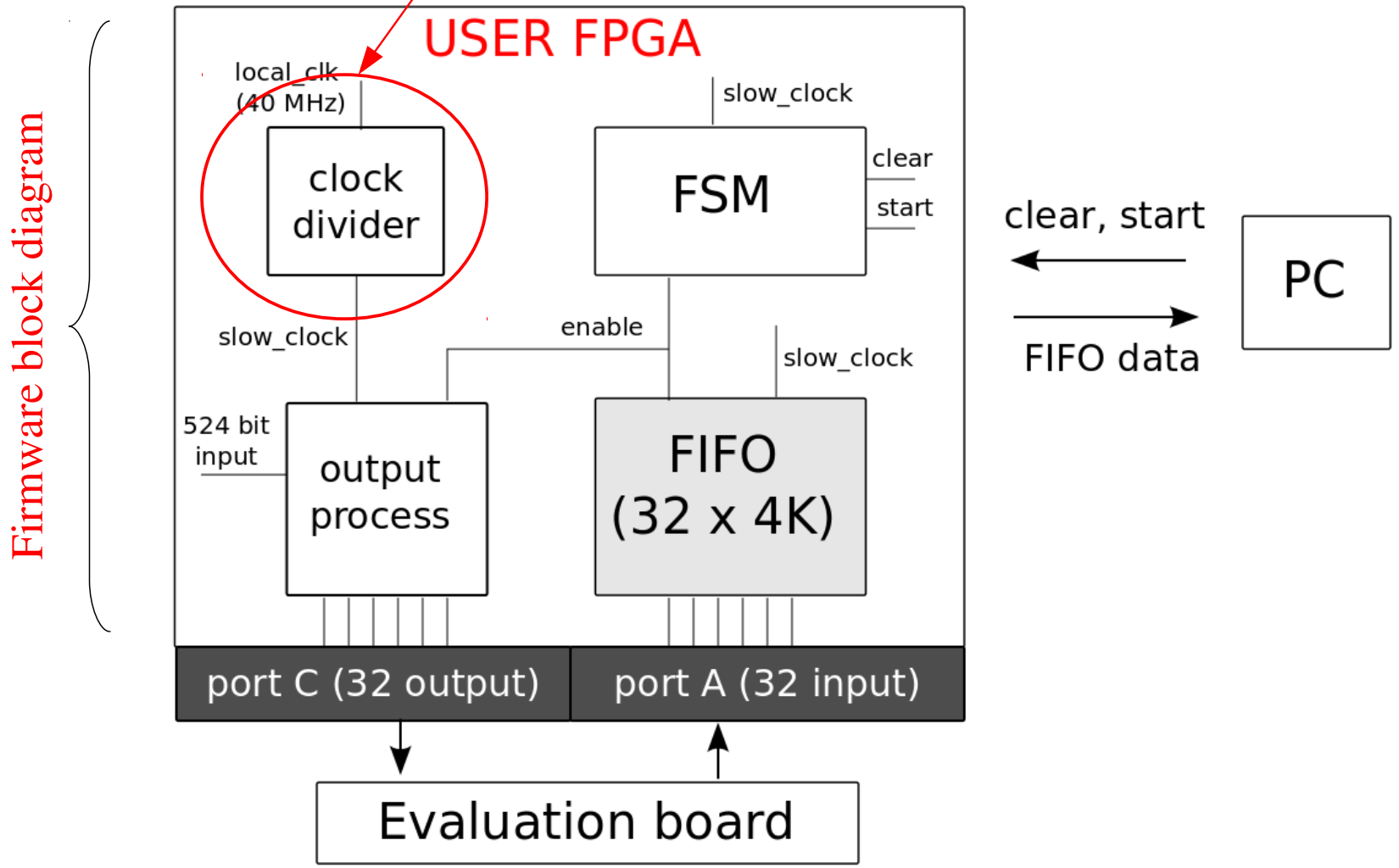


- A first version of the firmware has been developed starting from a CAEN demo.



- A first version of the firmware has been developed starting from a CAEN demo.

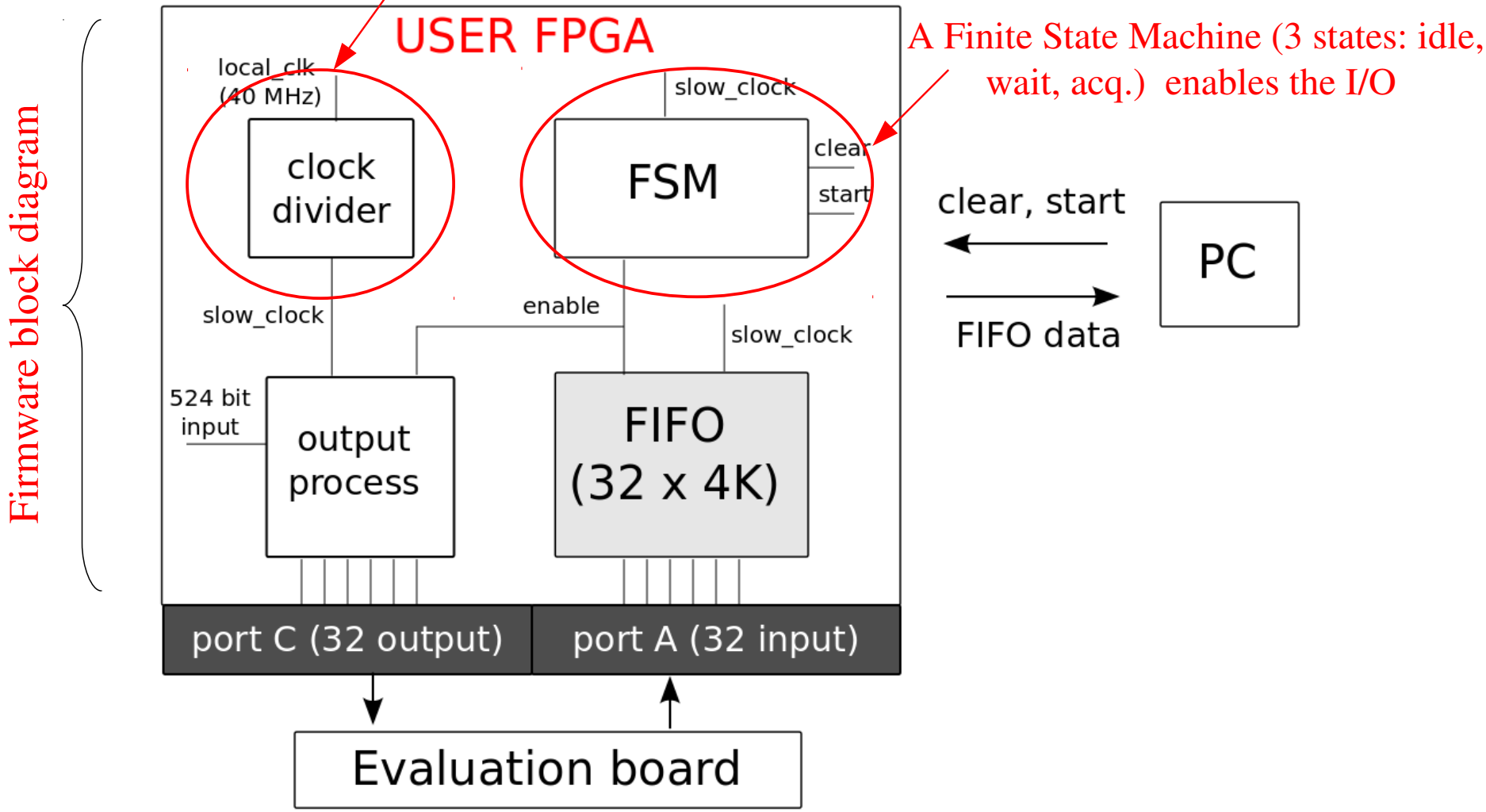
A clock divider produces a slower clock (e.g. 1 MHz) starting from the local clock (40 MHz)



- A first version of the firmware has been developed starting from a CAEN demo.

A clock divider produces a slower clock (e.g. 1 MHz) starting from the local clock (40 MHz)

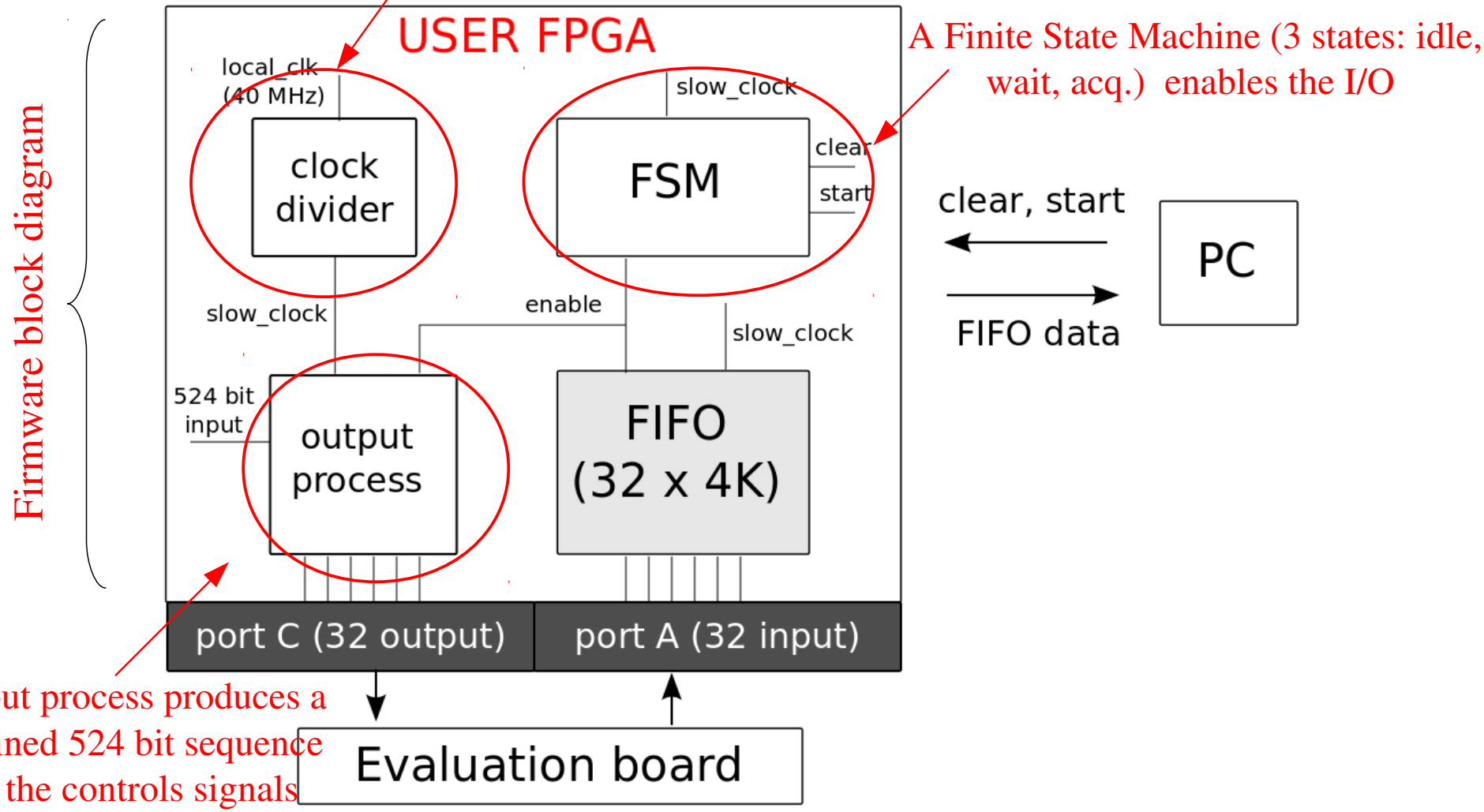
A Finite State Machine (3 states: idle, wait, acq.) enables the I/O



- A first version of the firmware has been developed starting from a CAEN demo.

A clock divider produces a slower clock (e.g. 1 MHz) starting from the local clock (40 MHz)

A Finite State Machine (3 states: idle, wait, acq.) enables the I/O

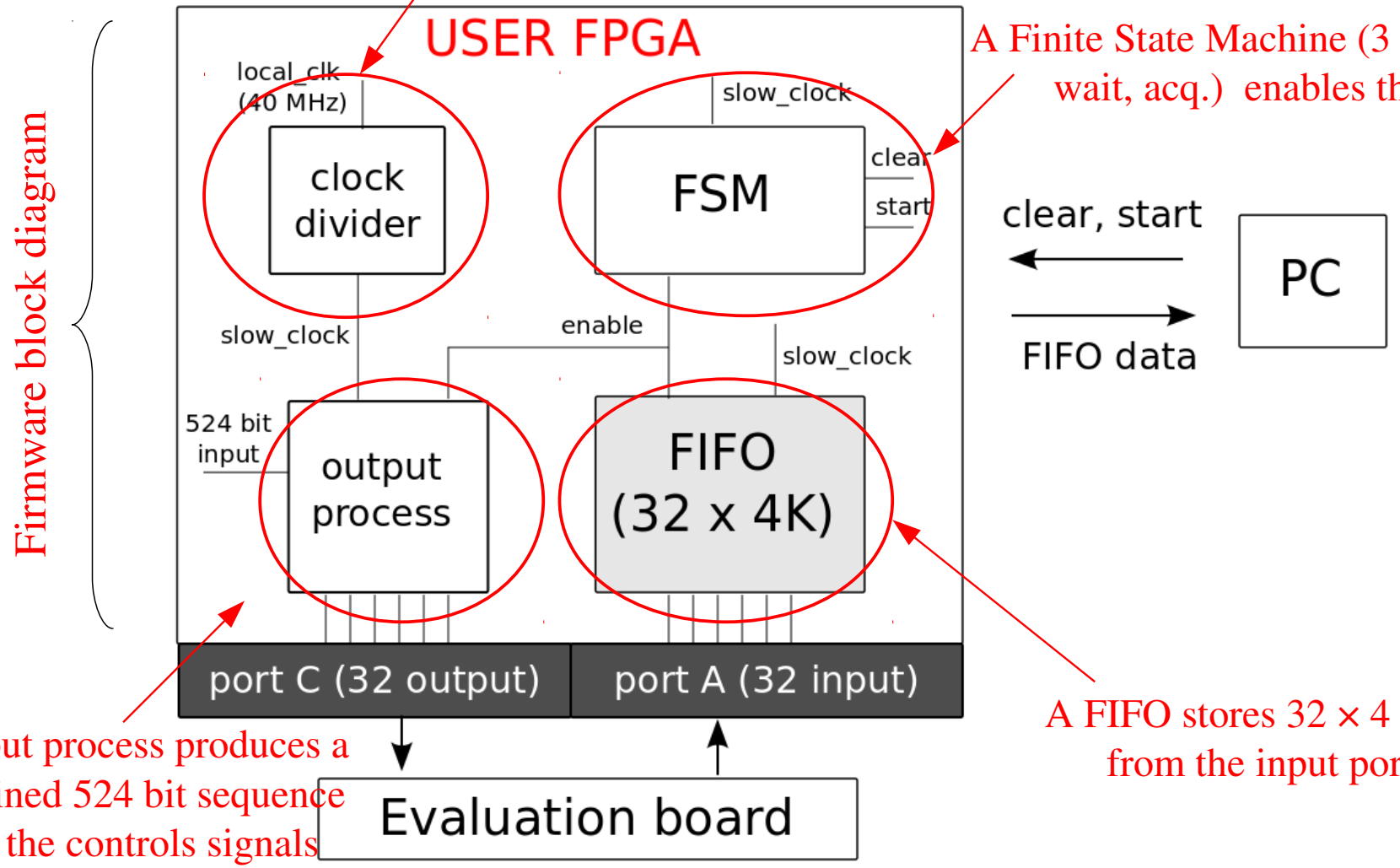


The output process produces a user-defined 524 bit sequence and all the controls signals

- A first version of the firmware has been developed starting from a CAEN demo.

A clock divider produces a slower clock (e.g. 1 MHz) starting from the local clock (40 MHz)

A Finite State Machine (3 states: idle, wait, acq.) enables the I/O



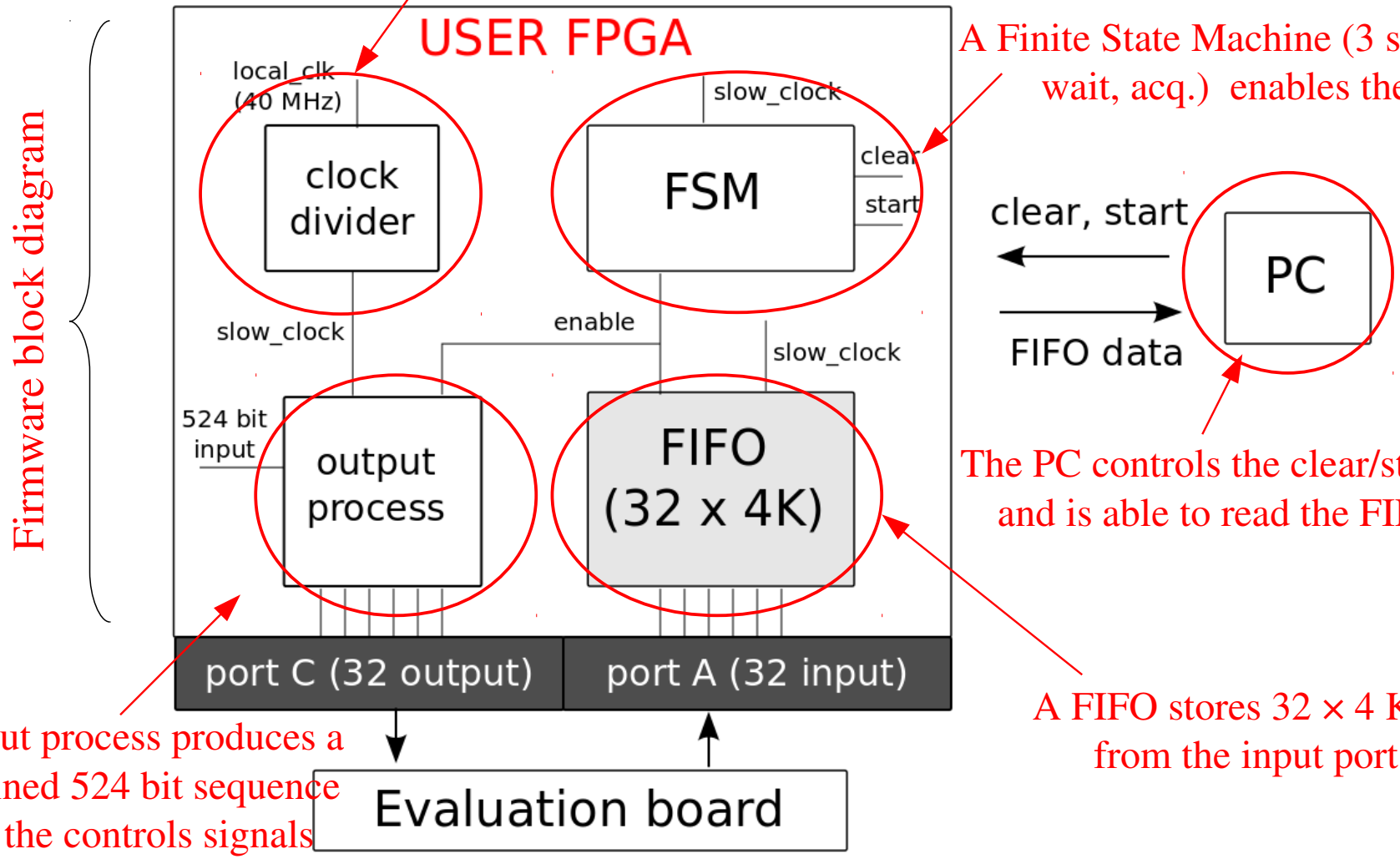
The output process produces a user-defined 524 bit sequence and all the controls signals

A FIFO stores 32 × 4 K BIT from the input port A

- A first version of the firmware has been developed starting from a CAEN demo.

A clock divider produces a slower clock (e.g. 1 MHz) starting from the local clock (40 MHz)

A Finite State Machine (3 states: idle, wait, acq.) enables the I/O



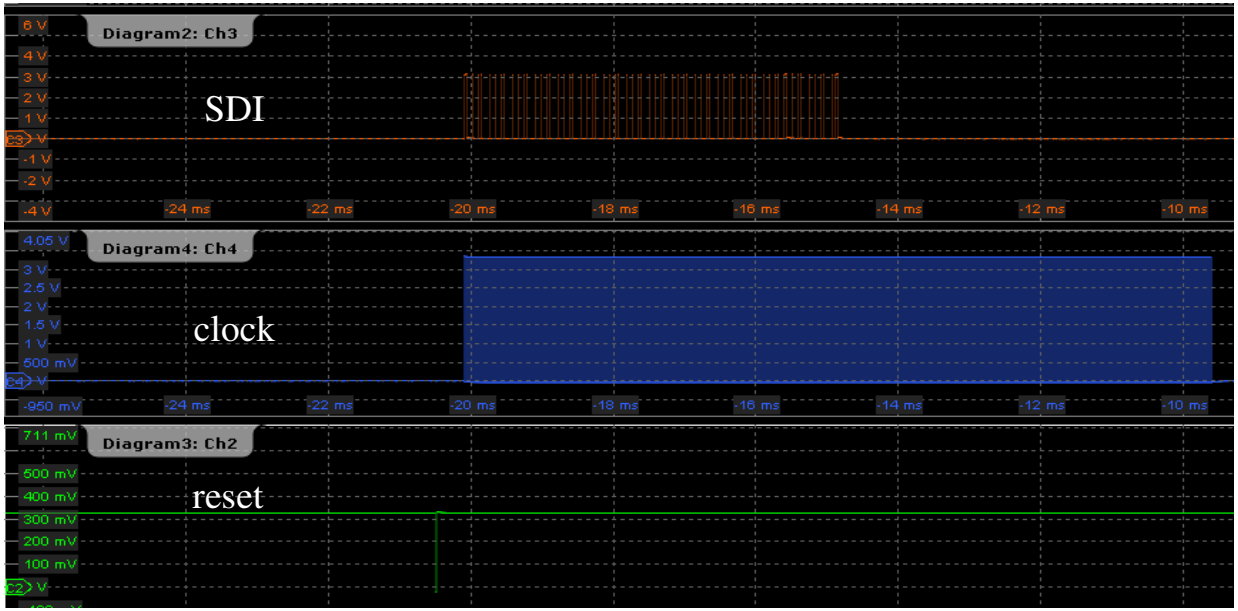
The PC controls the clear/start signals and is able to read the FIFO data

The output process produces a user-defined 524 bit sequence and all the controls signals

A FIFO stores 32 × 4 K BIT from the input port A

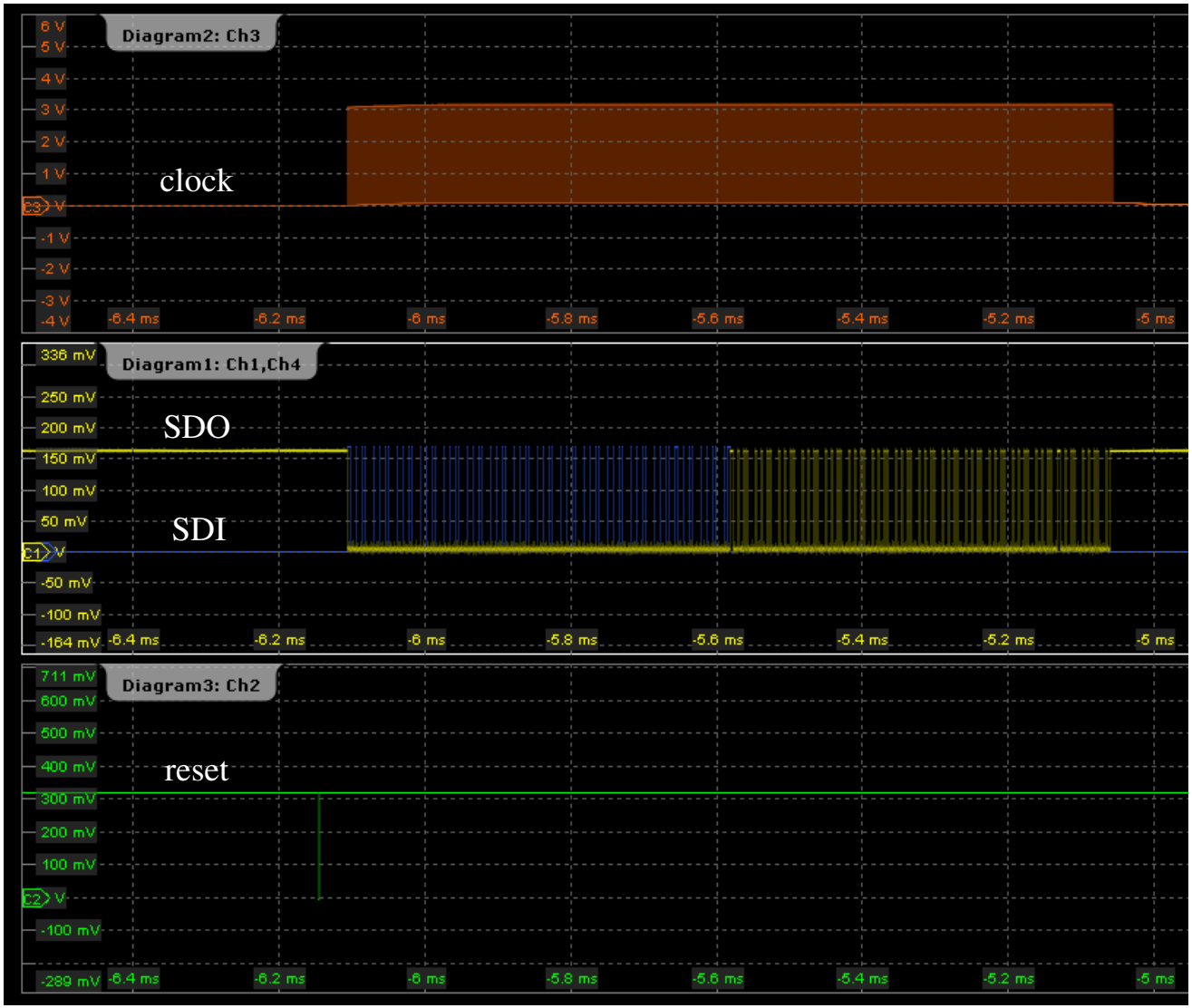
- During the first test, the serial data input (SDI) of the BASIC32 is driven with a 524 bits sequence and 1048 clock cycles.

FPGA output

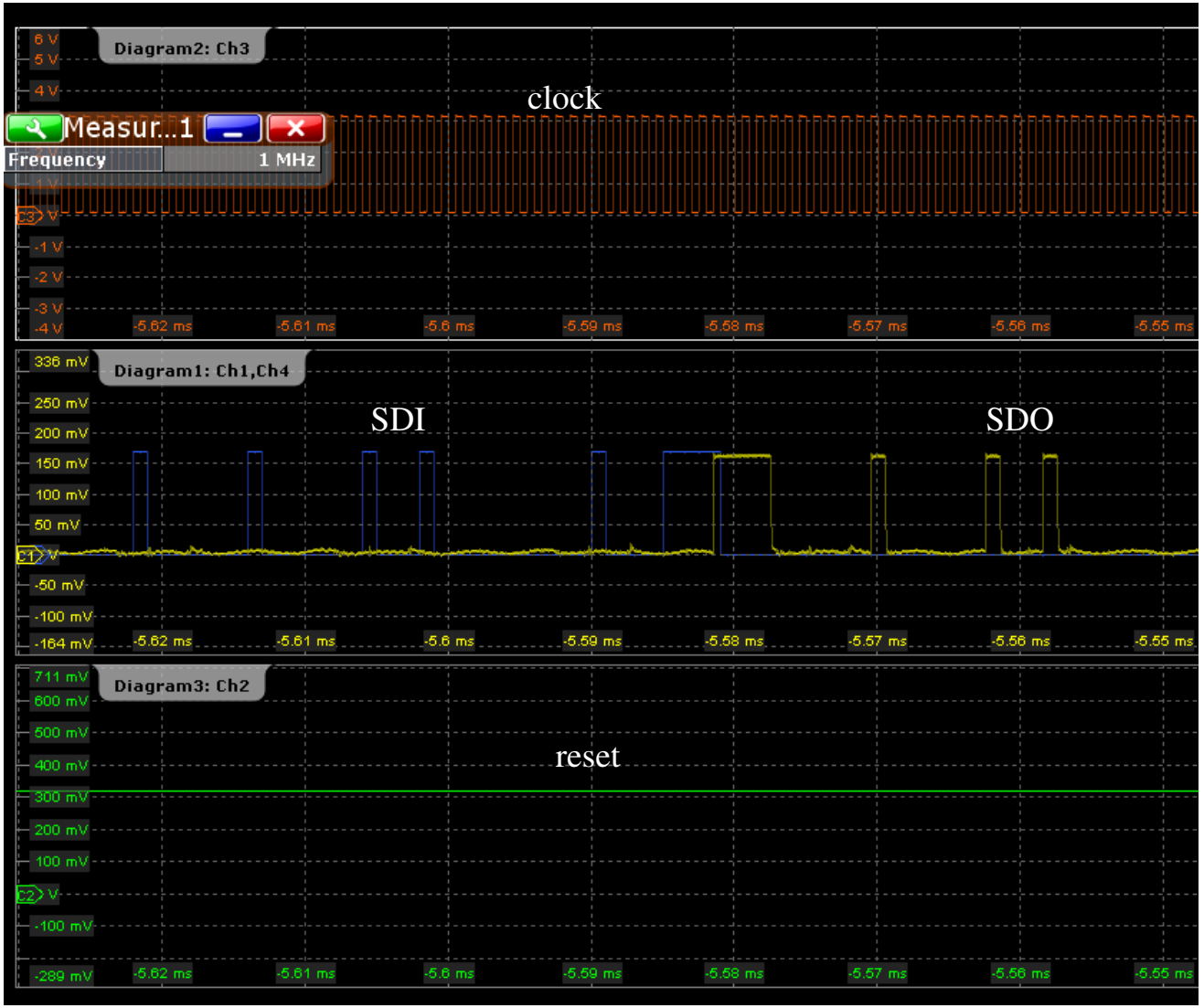


- **Expected behaviour**: in this configuration, the BASIC32 acts as a shift register; during the first 524 clock cycles the input sequence is stored inside the register; at the 524th clock edge the input data begin to flow through the serial data output (SDO)

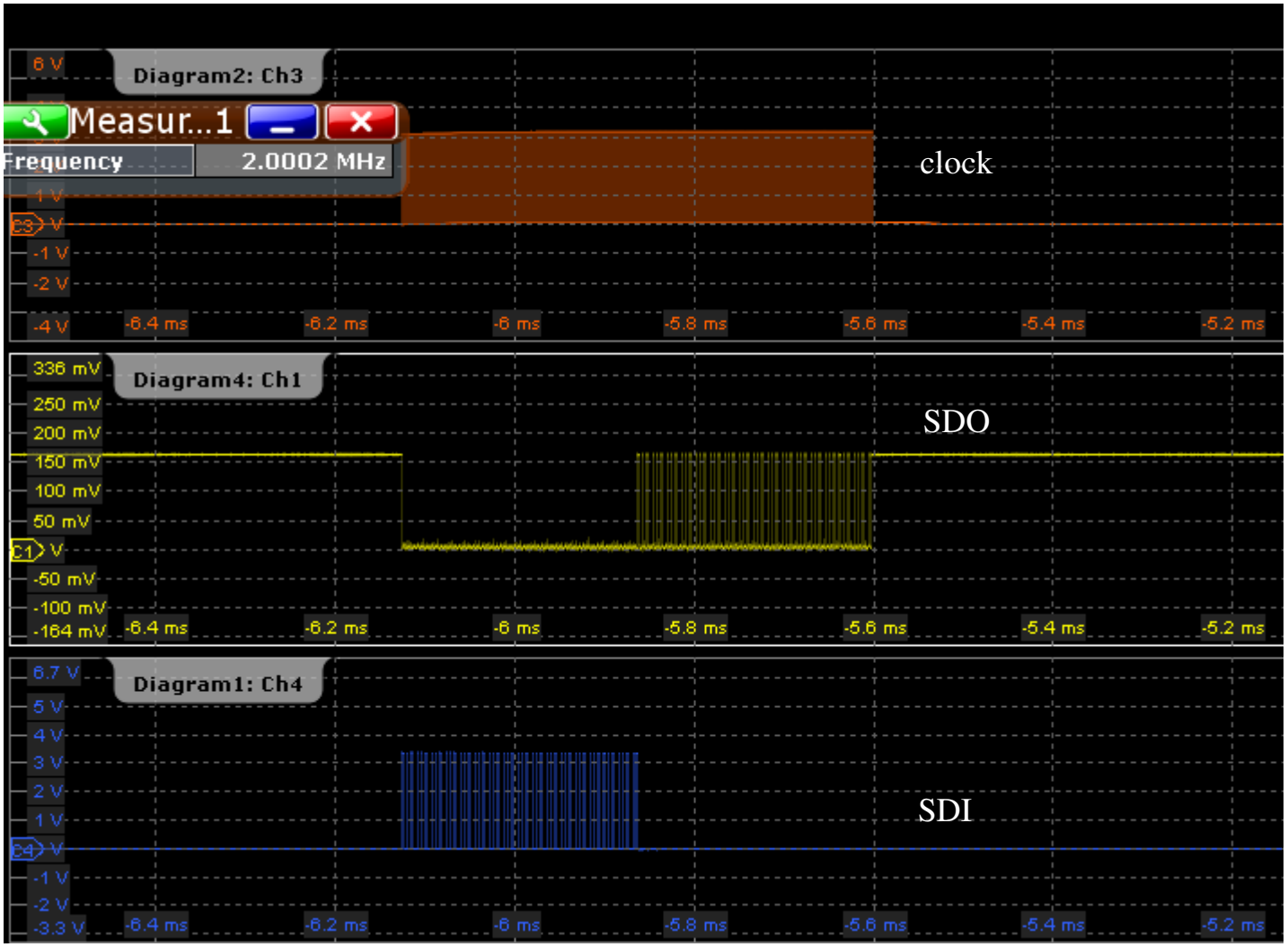
- Serial I/O test at 1 MHz



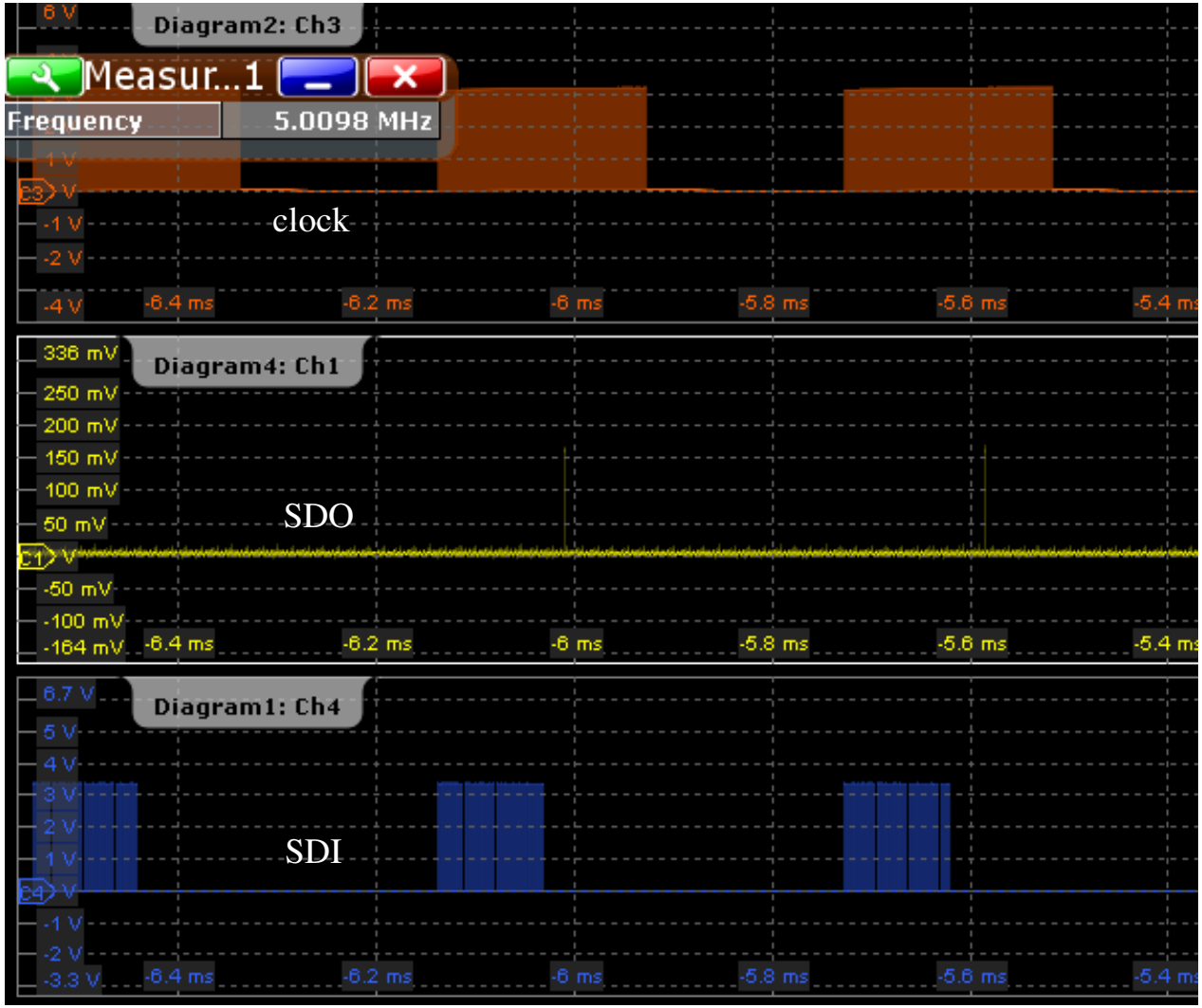
- Serial I/O test at 1 MHz



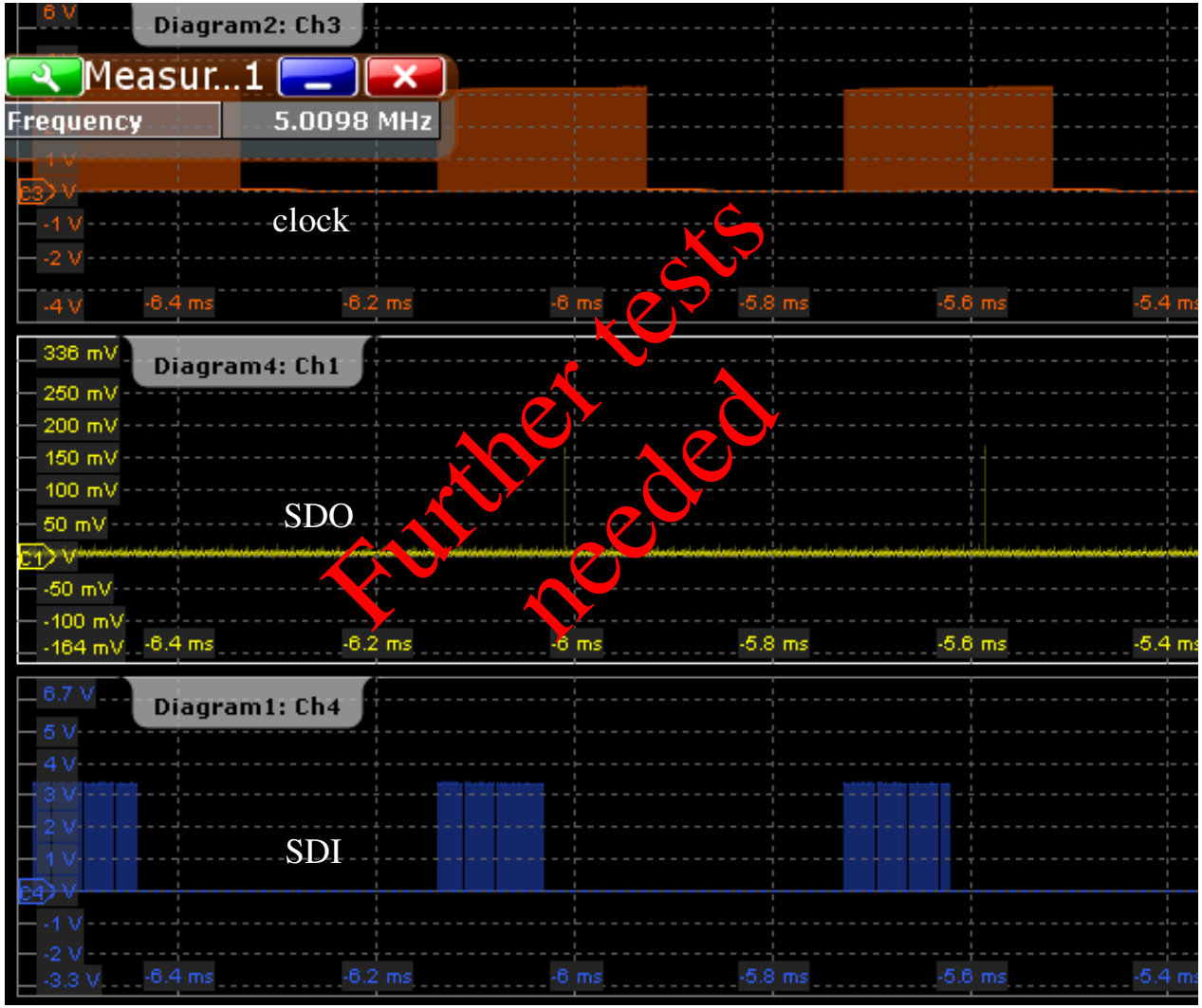
- Serial I/O test at 2 MHz



- Serial I/O test at 5 MHz: the system seems not working

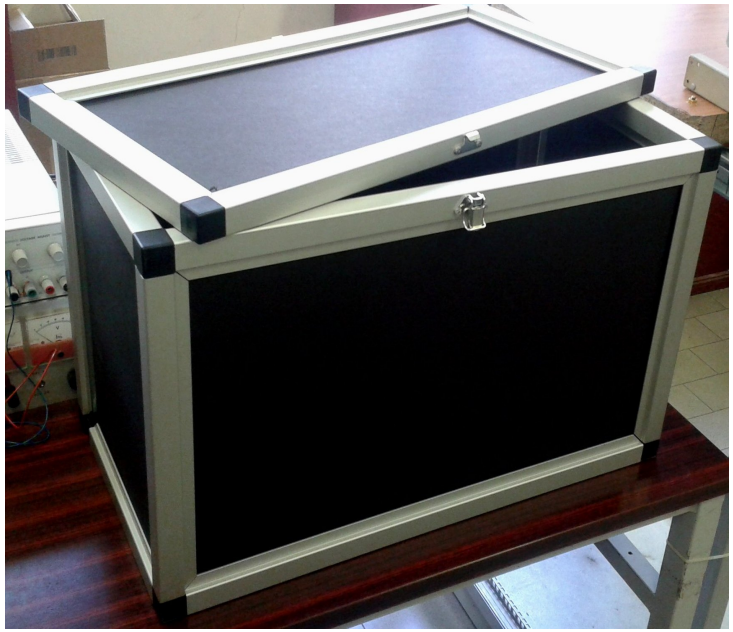


- Serial I/O test at 5 MHz: the system seems not working



Next steps

- Serial digital I/O test at high frequency (> 2MHz)
- Charge injection test on the BASIC32 analog input channels
- SiPM input test within the Light Tight Enclosure (Newport LTE-12)



Thanks for your attention!