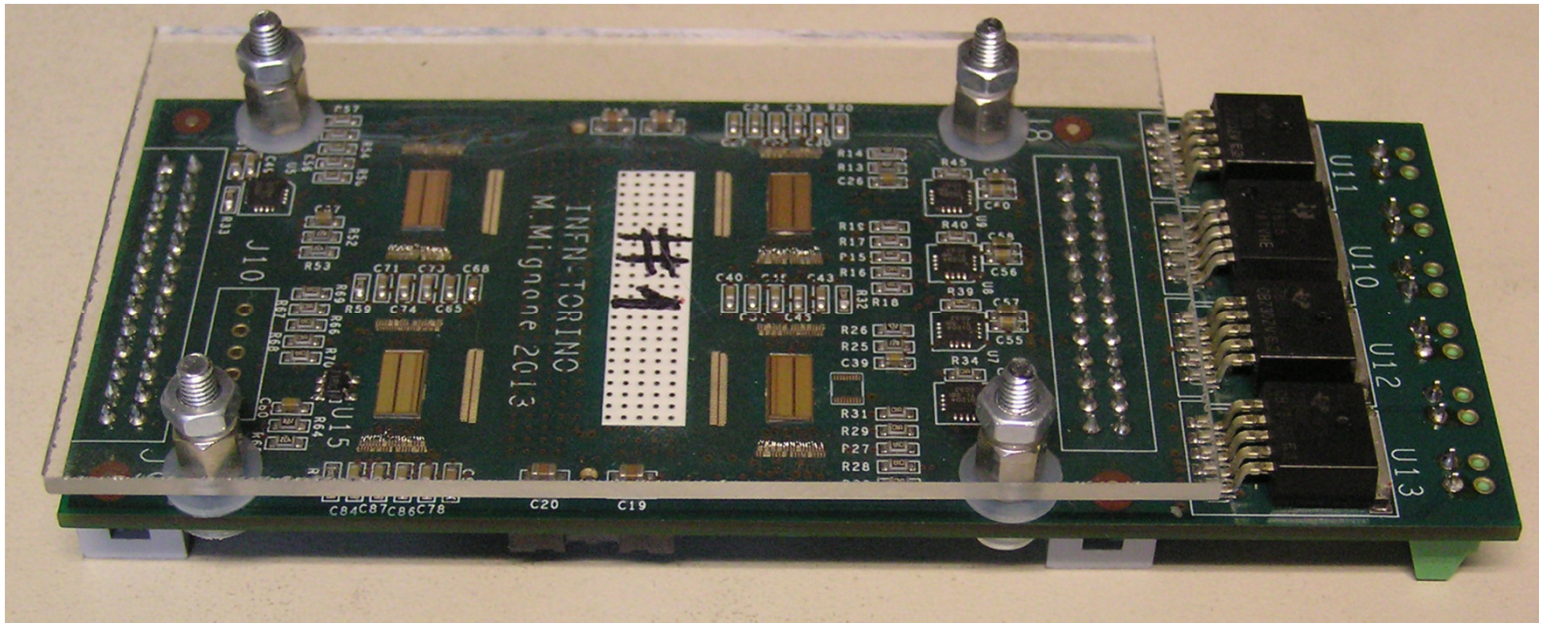
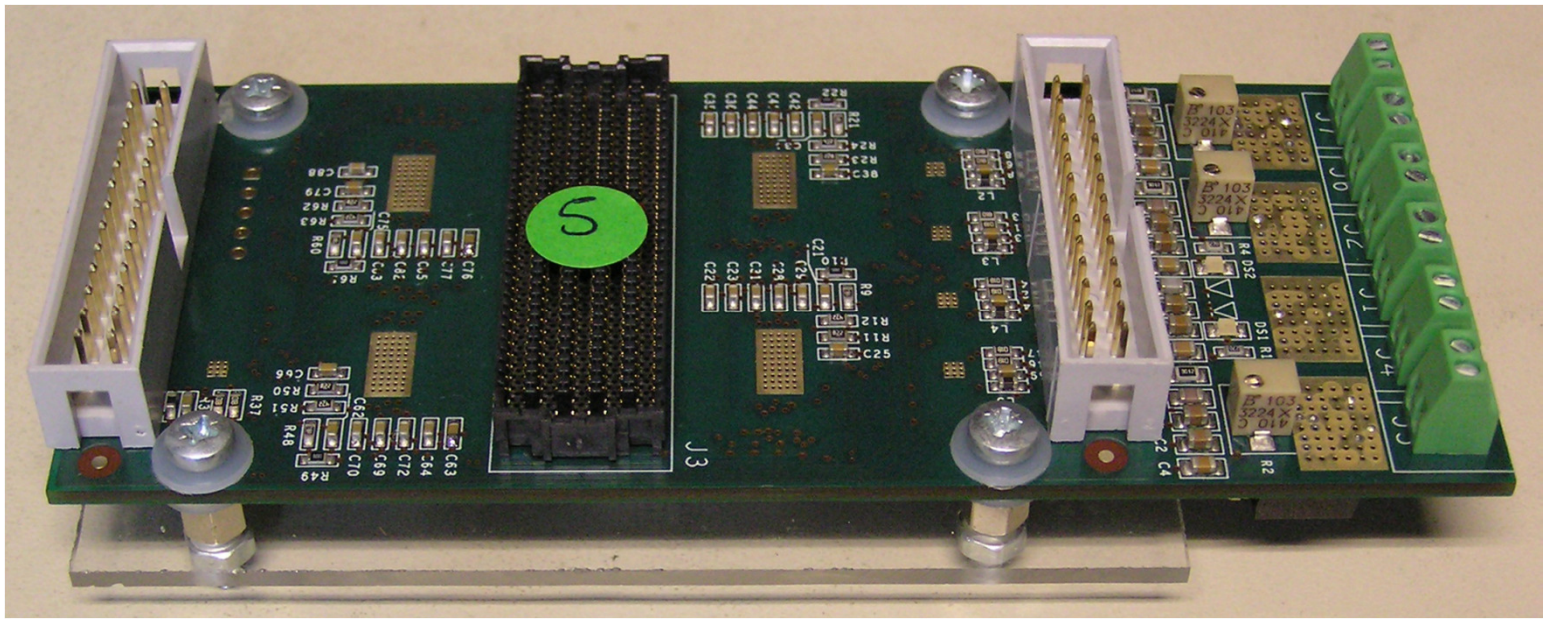
Summary of Torino FE electronics hardware contribution 2014

- Production and test of first 3 Tofpet FE boards
  - Boards run hot, 70+°C in still air (too high), ~ 50°C with forced air cooling
  - Changed side of digital connectors to allow easier substitution of chips
  - Final boards will also have power connectors mounted on opposite side wrt photos
- Firmware for test of single FE board with ML605 (Virtex 6)
- Firmware of SP605 (Spartan 6) proposed as Tx board
  - Very different programming experience, many limitations in clock distribution to work around
  - Discovered that Spartan 6 I/O termination only works with common ground
  - Not safe choice for final system -> go back to ML605 with 2FE / FPGA
  - Cost increase limited by reduction in signal distribution hardware, also more compact
  - ML605 has SFP connector so conceptually could run two Gb Ethernet links if required
- Expansion of ML605 firmware to handle 2 FE boards (8 chips)
  - Consequent changes to software for calibration and acquisition
  - Fine time calculation in hardware complete but not tested or transmitted yet
- Supervision of probe card design
  - Defined original probe station test with Nahema and Manuel
- Long and detailed study of calibration sequence necessary to combat significant process sensitivity
  - Large number of inter-dependent parameters, 8 chips, long parameter vs parameter measurements
  - Discovered calibration issues new for Lisbon group
  - Final calibration sequence substantially different to original

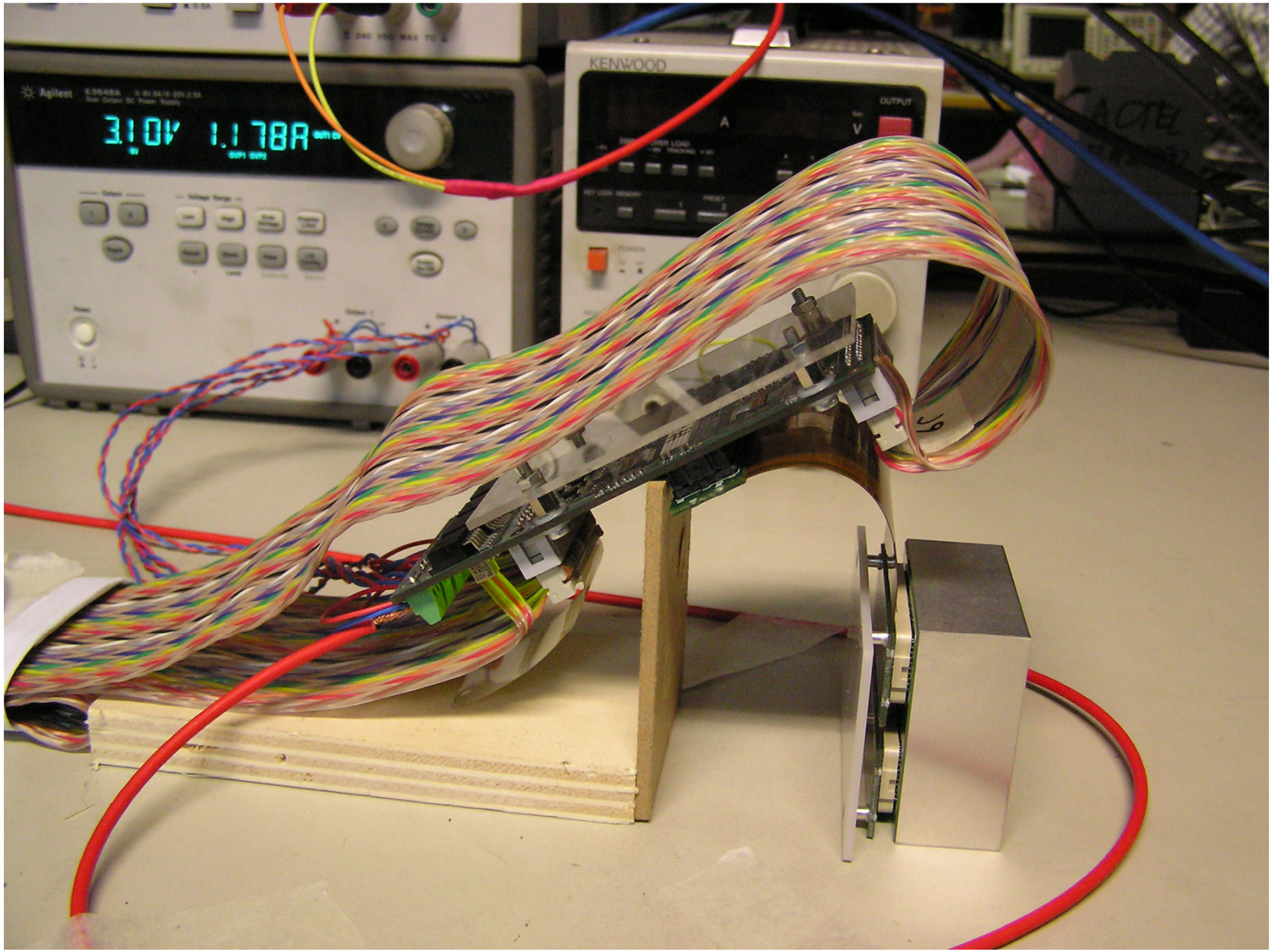
- Test executive software providing fully programmable sequence of measurements and analysis for chip testing and calibration with propagation of chip-dependent values
  - Functional test: 4 measurements, ~ 7 minutes / chip
  - Full calibration: 8 measurements, ~ 16 minutes / chip
- Study of FE boards with first detector modules using LYSO background
  - Electrical performance nominal
  - Discovered that combination of lower level signals with shaping enabled can lead to a condition in which the time is measured from the energy channel -> poor CTR due to time-walk
  - LYSO background alone generates ~ 1 GByte / hour from two modules
  - Added frame-level coincidence logic, ~ factor 8 reduction in data written to disk
- Measurement of CTR with weak Na22 source
  - Good CTR even with shaping on (not measured with shaping off, modules returned to Pisa)
  - Channel map provided by Hamamatsu is clearly either wrong or misinterpreted
- (unfortunately) Adapted test executive for probe station tests
  - Functional test significantly changed from that defined with Manuel at the beginning
  - Nahema's program well-structured and works fine but too hard-wired to adjust in a short time
- Study of Tofpet calibration temperature sensitivity
  - Generally not too sensitive, +/- 5 °C Ok
  - Expected: TAC drift very sensitive to temperature, CTR should be visibly better at 20 °C
  - Unexpected(?): TOT sigma factor 2-3 higher at 20°C compared to 50°C

FE board

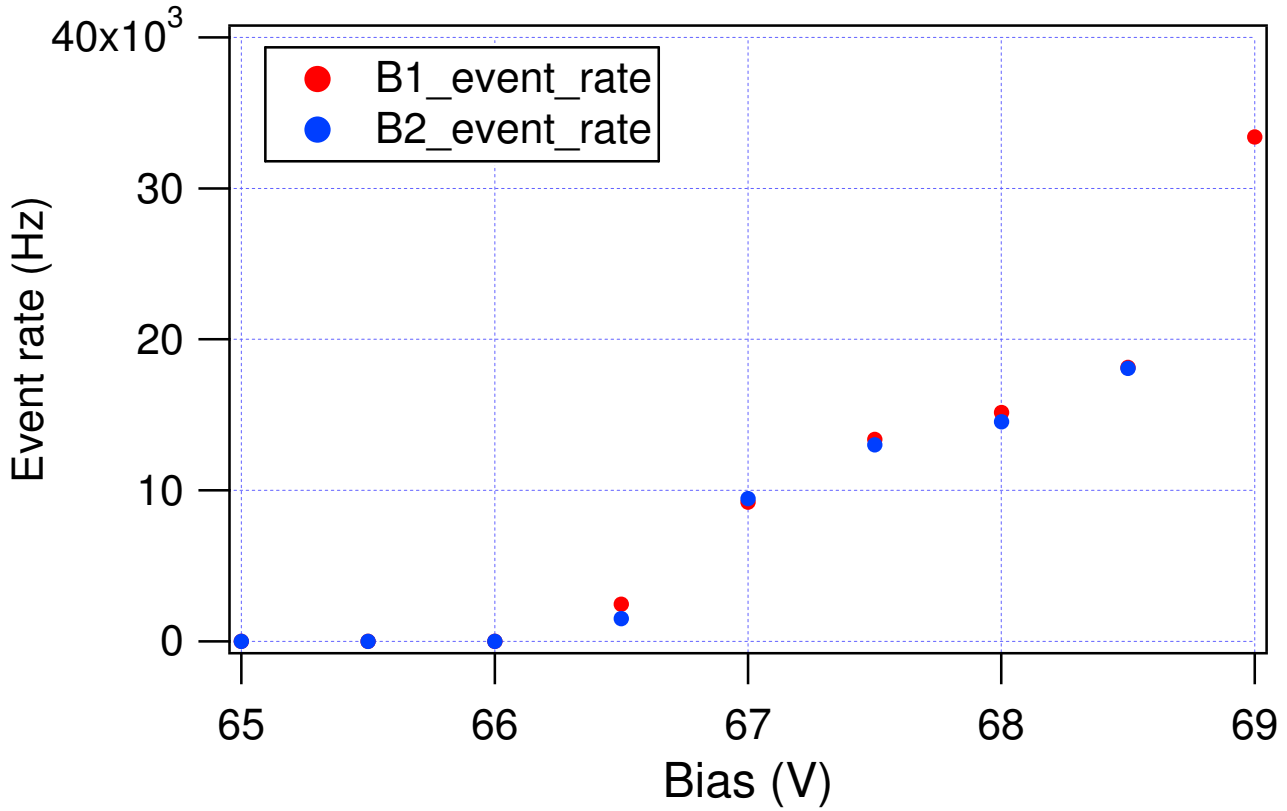




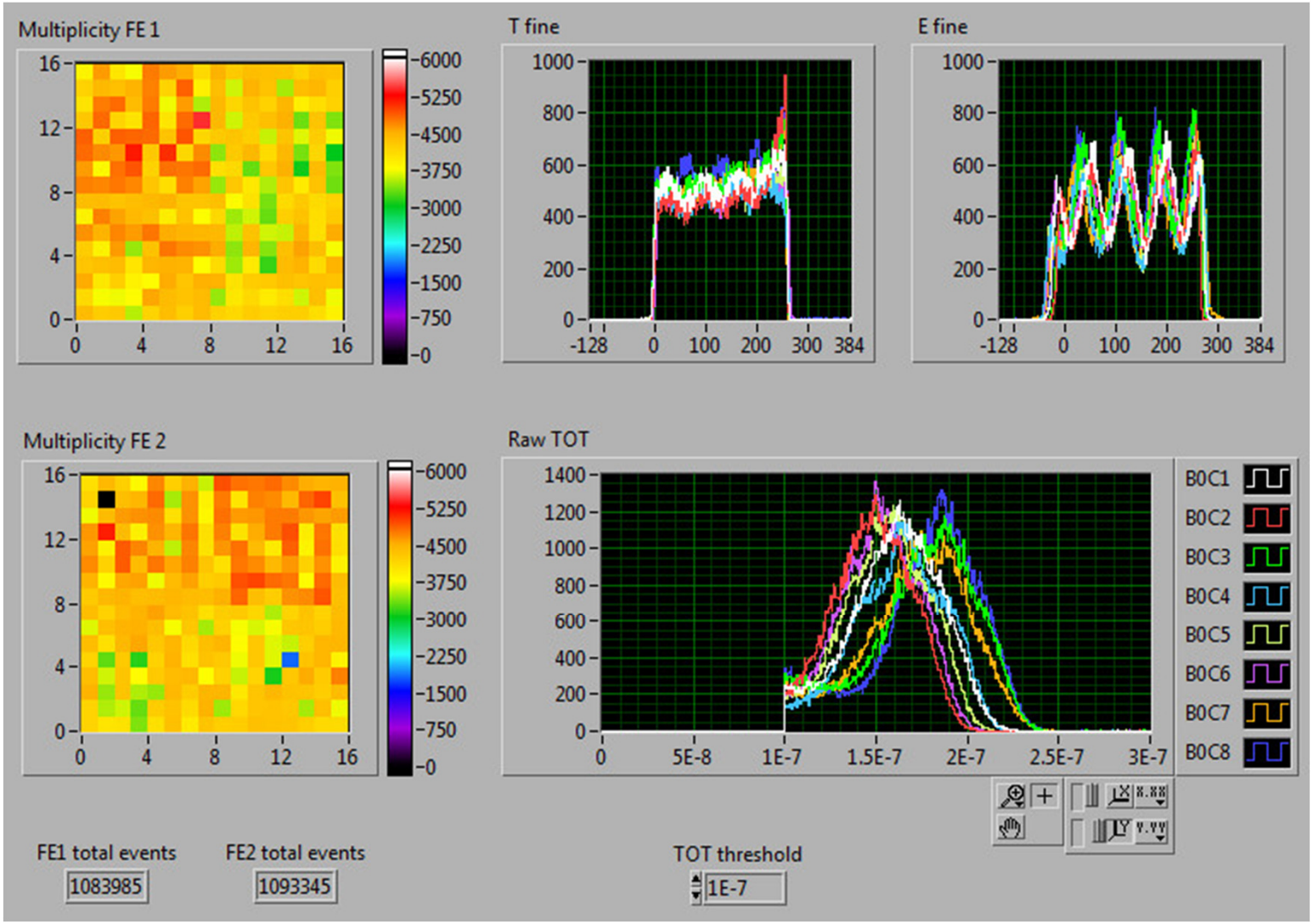
FE board + module



Background event rate vs SiPM bias



LYSO background acquisition uniformity



Torino FE electronics hardware 2015

- Production of remaining Tofpet FE boards (?)
  - Tested and ready ~ 3 months after orders confirmed
- Firmware for Tx board data transmission including fine time calculation
  - Not yet on critical path
- Firmware for Rx board Ethernet interface
  - Not yet on critical path
- Procurement of Tx boards and signal distribution boards
  - Verify costs
- Definition of Tx board boxes, connectors etc
  - Decide on separate clock and reset distribution box
- Assembly of PET detector
  - Medical-certified cables procurement problem