# Large Area Coverage of a TPC Endcap with GridPix Detectors

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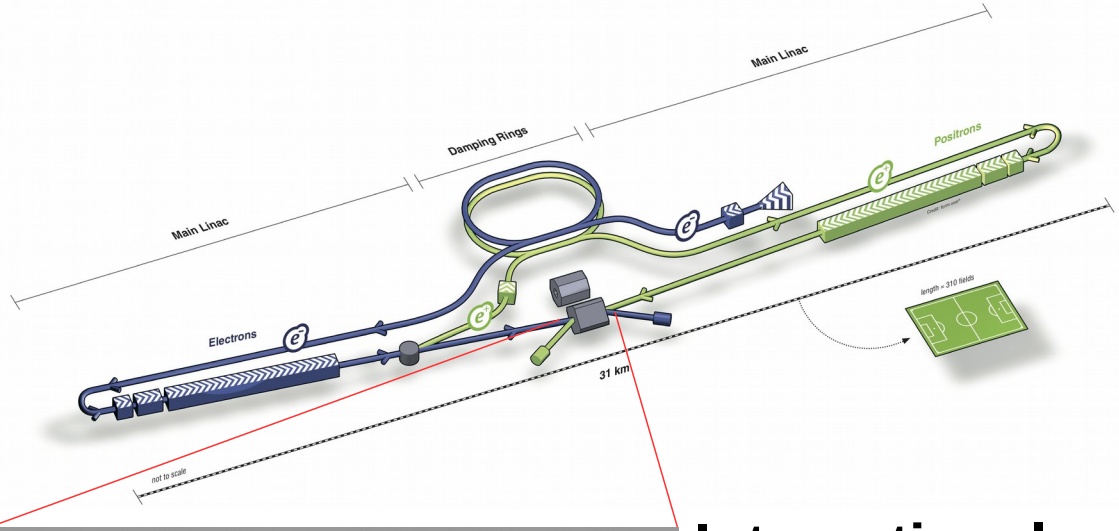
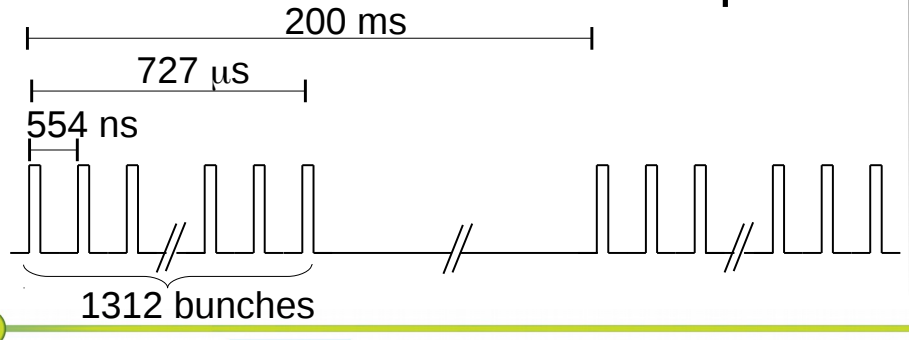
MPGD 2015
Trieste, 12.-15.10.2015

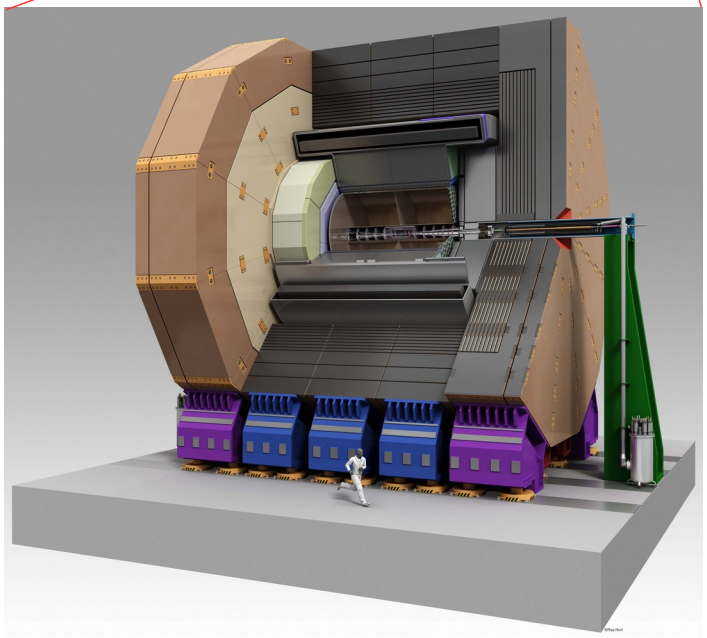
# International Linear Collider

International Linear Collider (ILC) /
Compact Linear Collider (CLIC)
are both linear $e^+e^-$ colliders with:
$\sqrt{s}$ = 500 GeV – 1TeV /
1TeV – 3TeV
Overall length of 30 km / 50 km




<u>Bunch structure (example ILC):</u>
Damping takes 0.2 s, once all the particles are damped, extraction and collision start. But when the damping ring is Empty, it takes again 0.2 s for next bunch train to be damped.

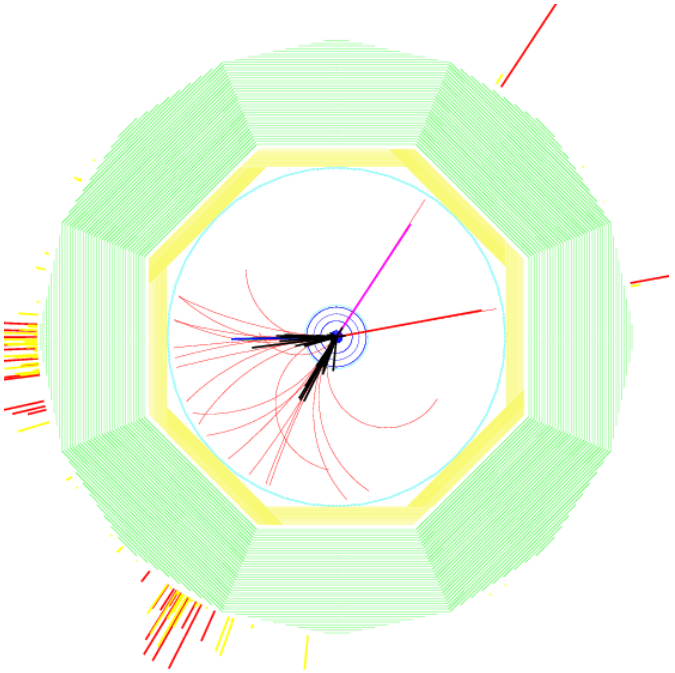


**International Large Detector**
- Standard HEP detector
- TPC as main tracker
- Interchanged with SiD by push and pull principle

# ILD-TPC Requirements

Requirements are driven by benchmark processes, in the case of ILD – TPC the most stringent measurement is the Higgs-recoil measurement:



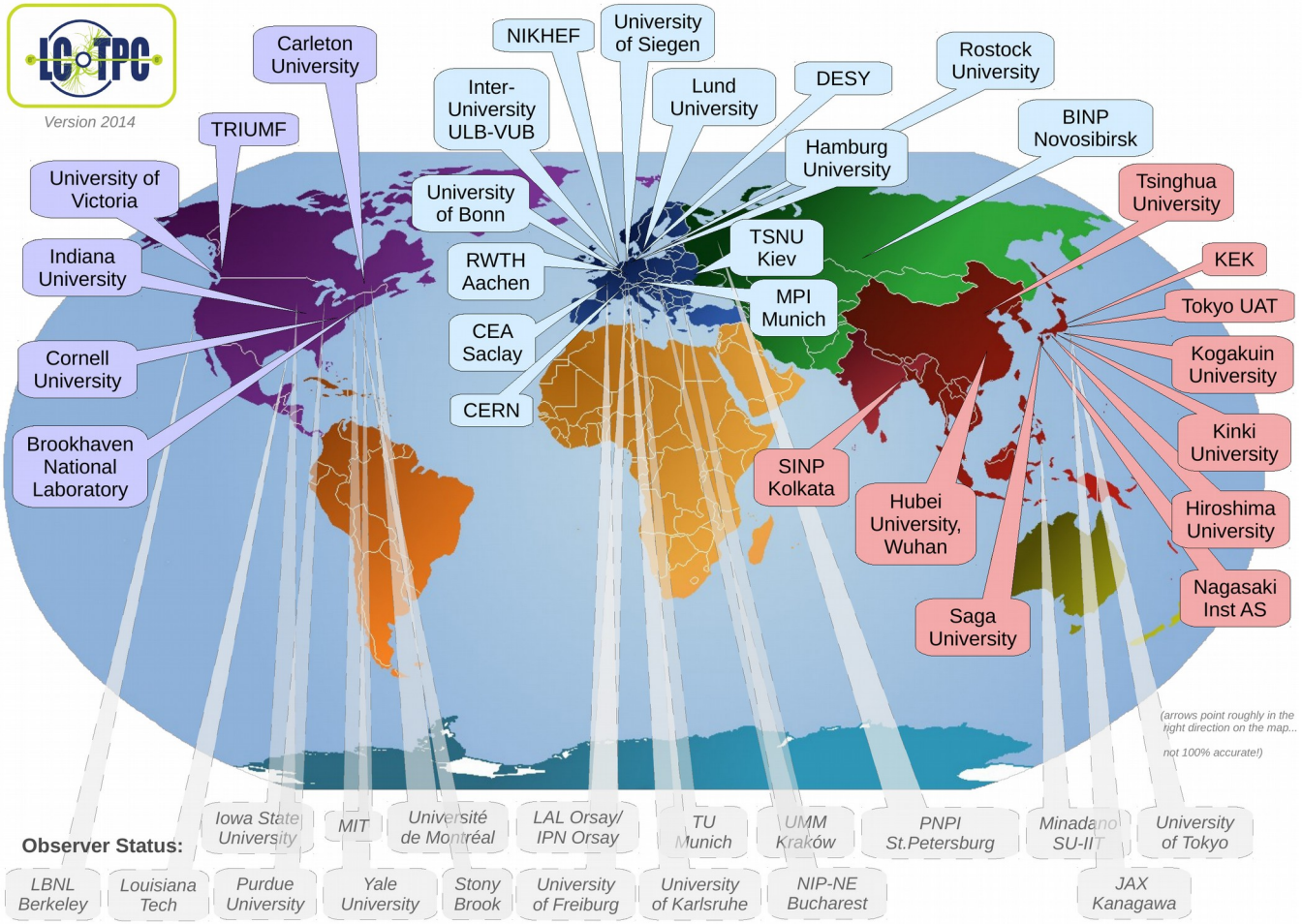
Requirements of TPC from ILC TDR vol. 4

| Parameter | |
|---|---|
| Geometrical parameters | $r_{in}$ 329 mm; $r_{out}$ 1808 mm; z $\pm$ 2350 mm |
| Solid angle coverage | up to $\cos\theta \simeq 0.98$ (10 pad rows) |
| TPC material budget | $\simeq 0.05\ X_0$ including outer fieldcage in $r$ |
| | $< 0.25\ X_0$ for readout endcaps in $z$ |
| Number of pads/timebuckets | $\simeq$ 1-2 $\times 10^6$/1000 per endcap |
| Pad pitch/ no.padrows | $\simeq 1\times$ 6 mm$^2$ for 220 padrows |
| $\sigma_{point}$ in $r\phi$ | $\simeq$ 60 $\mu$m for zero drift, $<$ 100 $\mu$m overall |
| $\sigma_{point}$ in $rz$ | $\simeq 0.4 - 1.4$ mm (for zero – full drift) |
| 2-hit resolution in $r\phi$ | $\simeq 2$ mm |
| 2-hit resolution in $rz$ | $\simeq 6$ mm |
| dE/dx resolution | $\simeq 5$ % |
| Momentum resolution at B=3.5 T | $\delta(1/p_t) \simeq 10^{-4}$/GeV/c (TPC only) |

In addition: very high efficiency for particle of more than 1 GeV.

These requirements can not be fulfilled by conventional wire-based read out. New Micropattern-based readouts have to be applied.

# LCTPC Collaboration




LCTPC-collaboration studies MPGD detectors for the ILD-TPC:
30 Institutes from
12 countries
+ 18 institutes with observer status

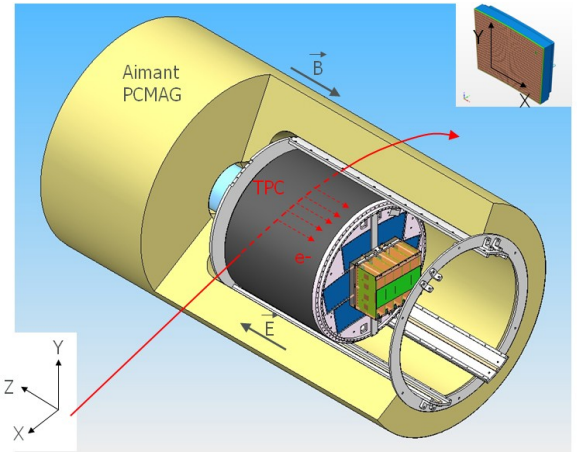
Various gas amplification stages are studied: GEMs, Micromegas, GEMs with double thickness and GridPixes.

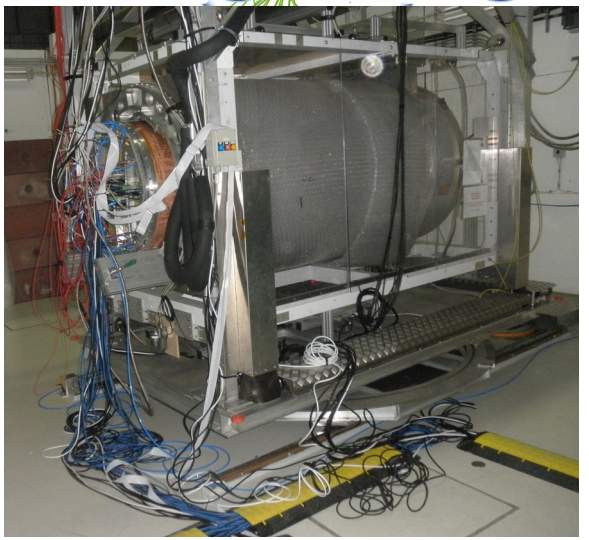
**MPGDs in TPCs**

- Ion backflow can be reduced significantly
- Small pitch of gas amplification regions
  => strong reduction of E×B-effects
- No preference in direction
  => all 2 dim. readout geometries possible

# EUDET Test Facility

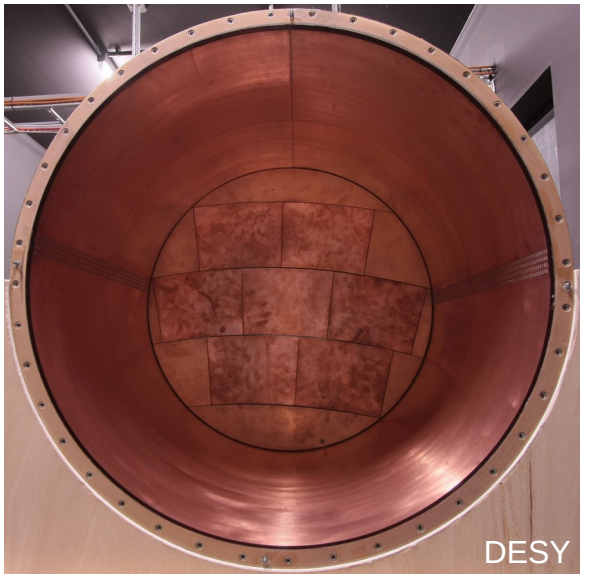
PCMAG: B < 1.2 T, bore diameter: 85 cm
Electron test beam: E = 1- 6 GeV
LP support structure
Beam and cosmic trigger



<u>LP Field Cage Parameter:</u>
length = 61 cm
inner diameter = 72 cm
up to 25 kV at the cathode
=> drift field: E ≈ 350 V/cm
made of composite materials: 1.24 % $X_0$

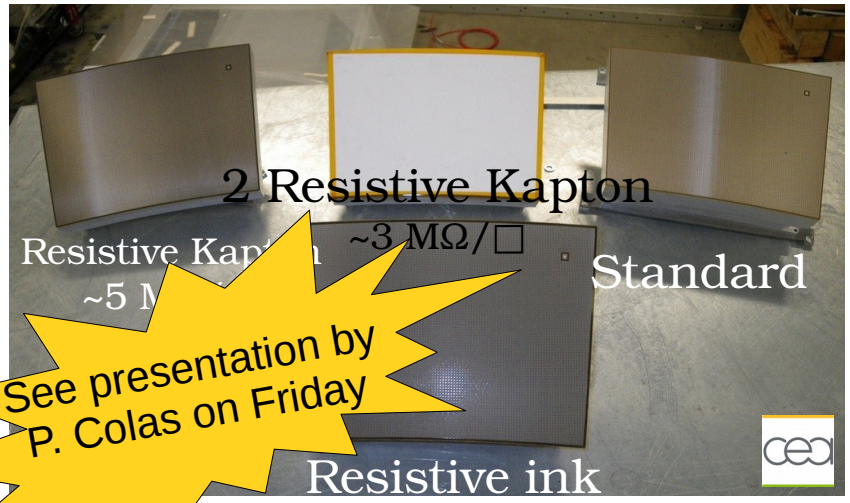

<u>Modular End Plate</u>
first end plate for the LP made from Al
7 module windows
→ size ≈ 22 × 17 $cm^2$




Large Prototype has been built to compare different detector readouts under identical conditions and to address integration issues.

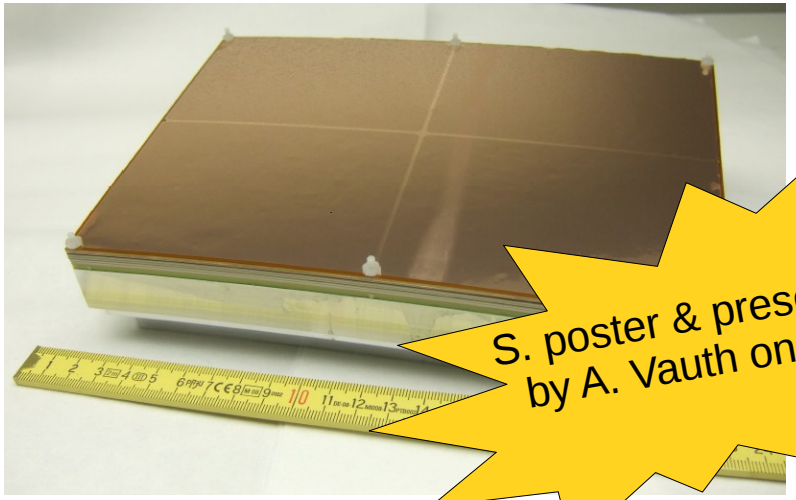
# Other Technologies

Micromegas with resistive layer on pads



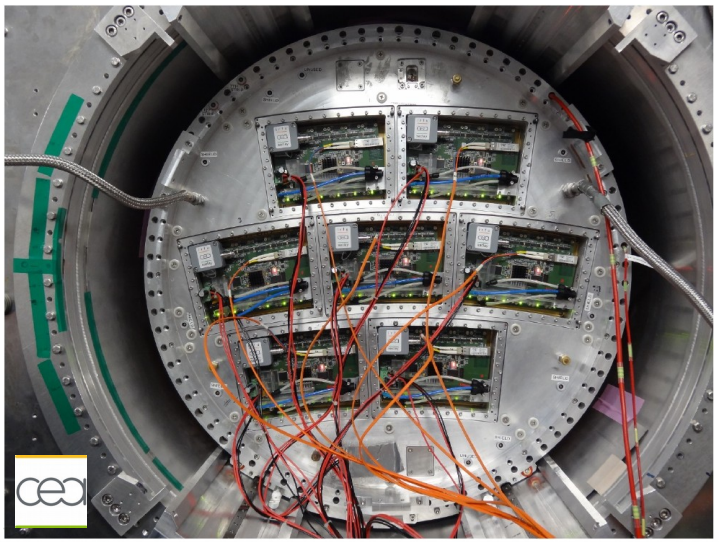

See presentation by P. Colas on Friday

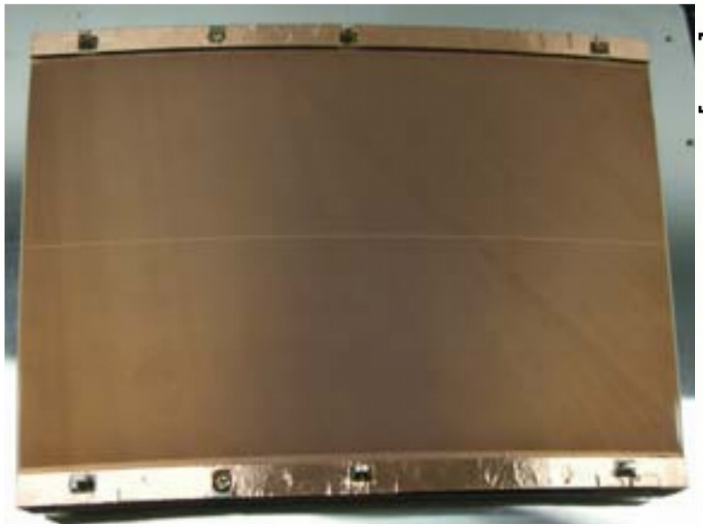
Triple CERN GEMs

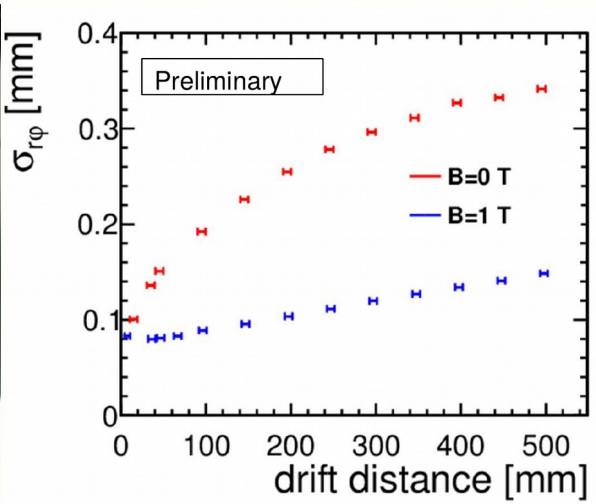


S. poster & presentation by A. Vauth on Friday

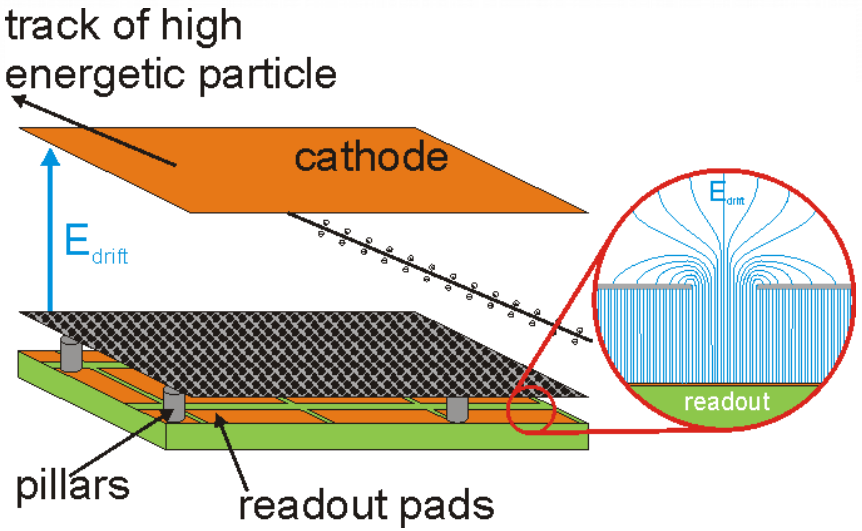
7 MM modules in the endplate





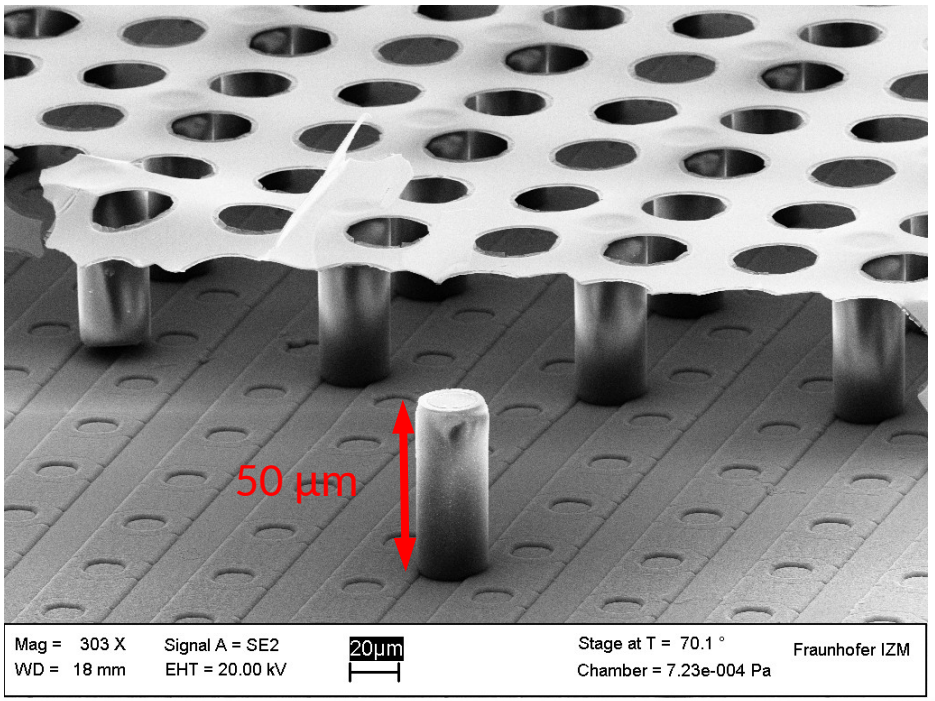


# Improving Micromegas: GridPix




Standard charge collection:
- Pads of several mm²
- Long strips (l~10 cm, pitch ~200 µm)

Instead: Bump bond pads are used as charge collection pads.




Could the spatial resolution of single electrons be improved?

Ar:$CH_4$ 90:10 → $D_t = 208\ \mu m/\sqrt{cm}$

→ $\sigma = 24\ \mu m$

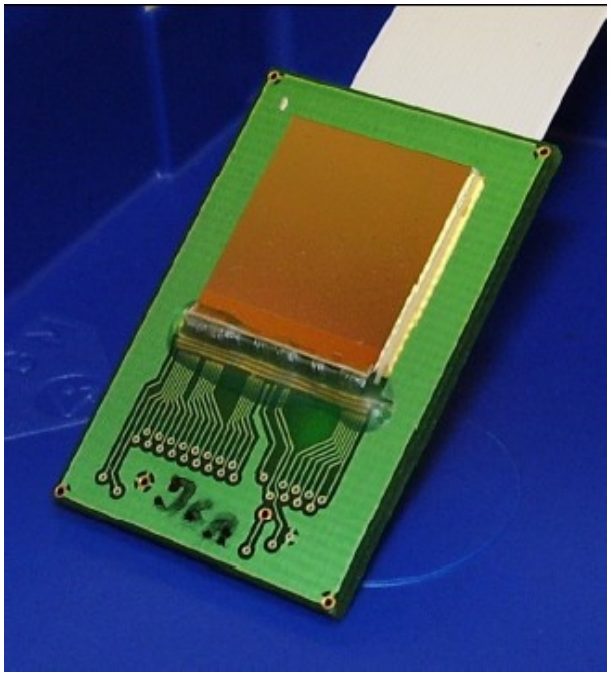
Ar:iButan 95:5 → $D_t = 211\ \mu m/\sqrt{cm}$

→ $\sigma = 24\ \mu m$

Smaller pads/pixels could result in better resolution!

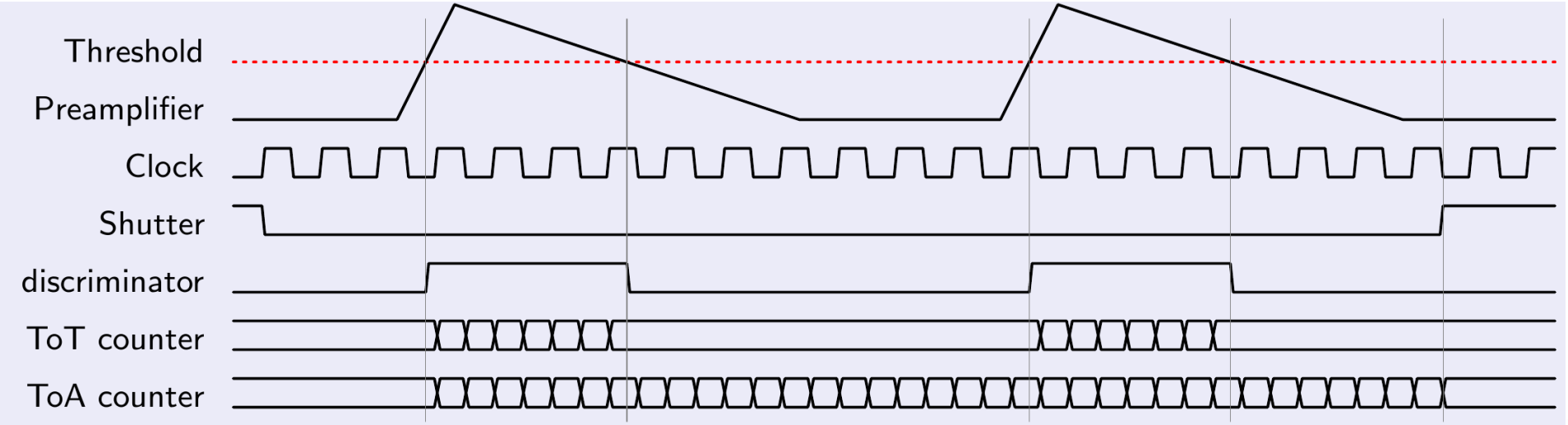
At NIKHEF the GridPix was invented.

# Timepix



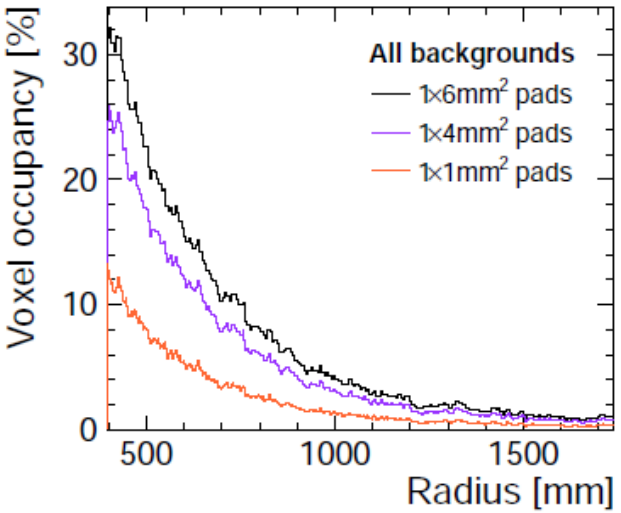
Number of pixels: 256 × 256 pixels
Pixel pitch: 55 × 55 µm²
Chip dimensions: 1.4 × 1.4 cm²
ENC: ~ 90 $e^-$

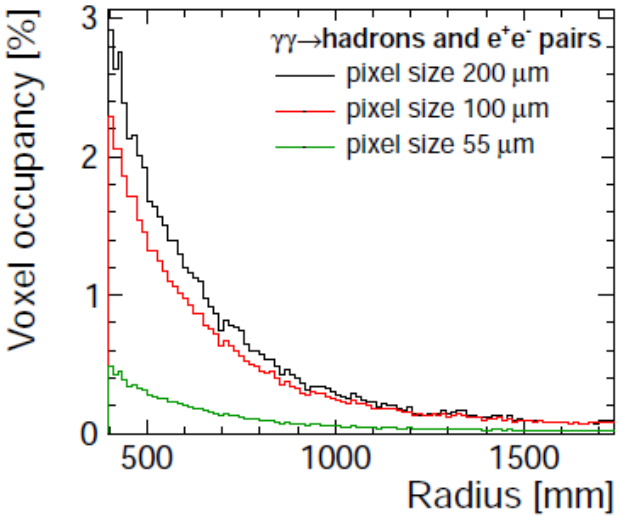
Limitations: no multi-hit capability, charge and time measurement not possible for one pixel.
Each pixel can be set to one of these modes: TOT = time over threshold (charge)
Time between hit and shutter end.



# InGrid Benefits - Challenges

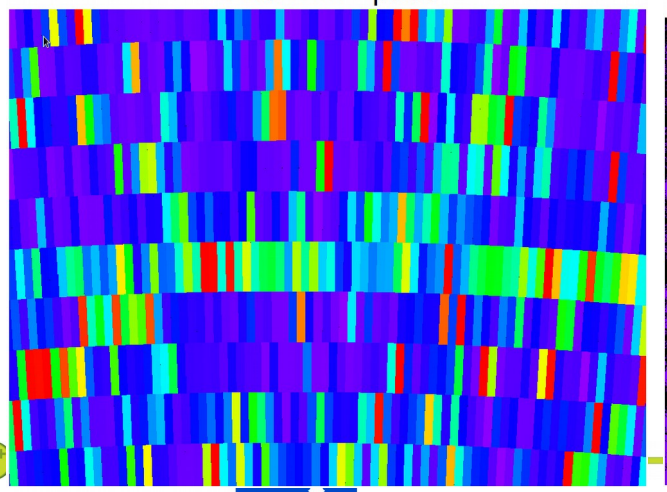
The background ($\gamma\gamma$ → hadrons, $e^+e^-$ → pairs/beam halo μ) is accumulated in the TPC creating a significant occupancy (Simulation for the CLIC detector, M. Killenberg, LCD-Note-2013-005)



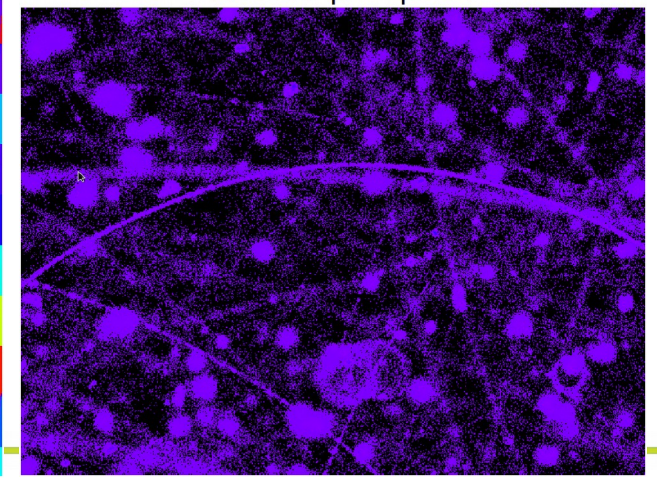




- Lower occupancy → better track finding
- Identification and removal of δ-rays and kink removal
- Improved dE/dx, because of primary $e^-$ counting
- Pad plane and readout electronics fully integrated

1×6 mm² pads



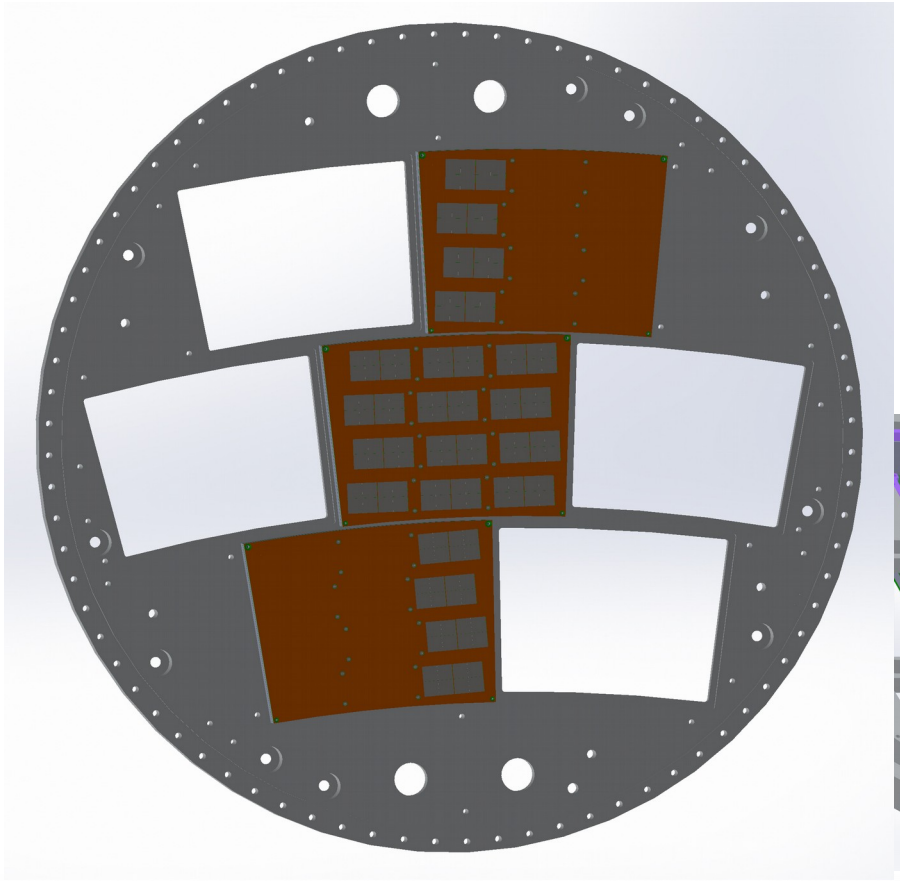
100×100 μm² pixels



To readout the TPC with GridPixes:
~100-120 chips/module
240 module/endcap (10 m²)
→50000-60000 GridPixes

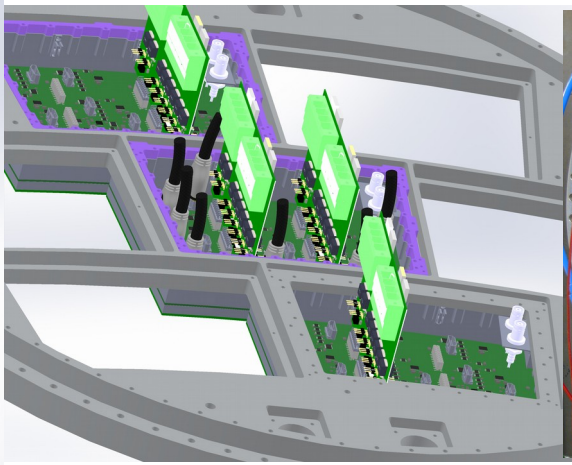
# Envisioned Final Setup

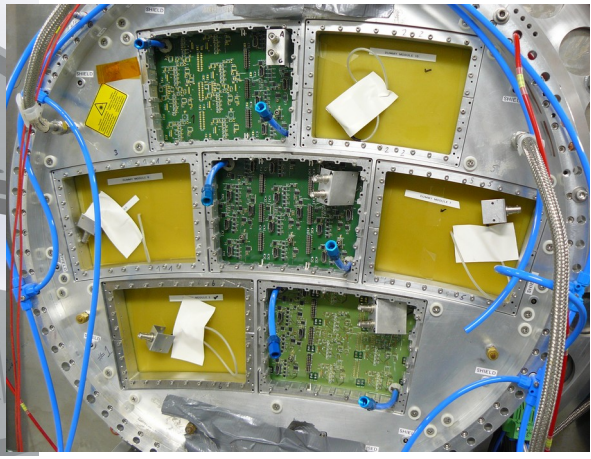
The goal foresaw a LP-module covered completely with GridPixes (~100). This goal could even be surpassed by adding two partially covered modules. In total 160 GridPixes covered an active area of 320 cm²: - central module with 96 chips (coverage 50 %)
- 2 outer modules with 32 chips each



Some challenges:

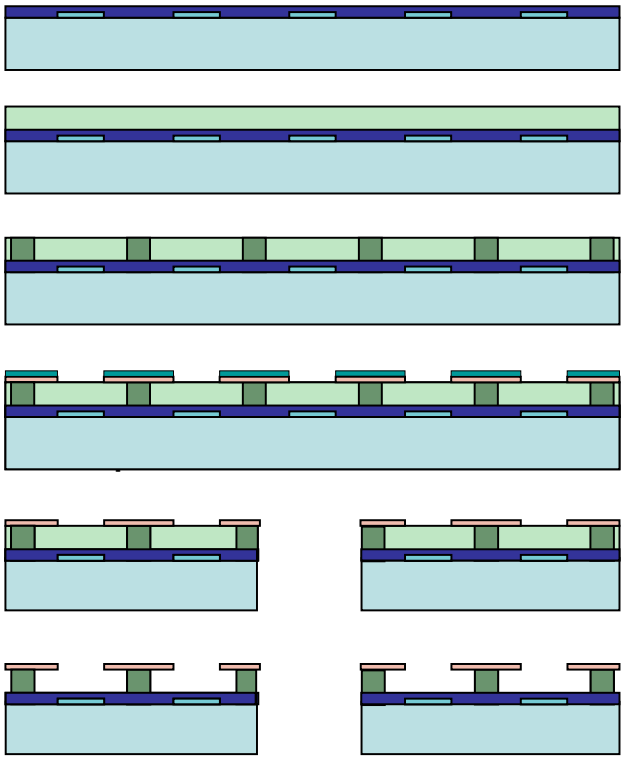
- InGrid production
- Synchronized readout
- Bonding on boards
- LV distribution
- Cooling



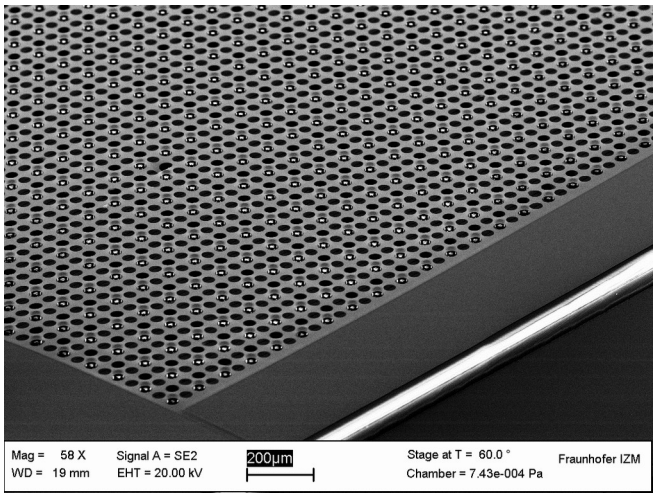


# Wafer-based Production

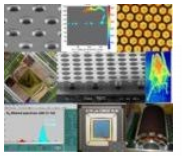
Production at Twente was based on 1 - 9 chips process.
This could not satisfy the increasing demands of R&D projects.
A new production was set up at the Fraunhofer Institut IZM at Berlin.
This process is wafer-based → 1 wafer (107 chips) is processed at a time.



1. Formation of $Si_xN_y$ protection layer
   (to protect chip from discharges)
2. Deposition of SU-8
3. Pillar structure formation
4. Formation of Al grid
5. Dicing of wafer
6. Development of SU-8

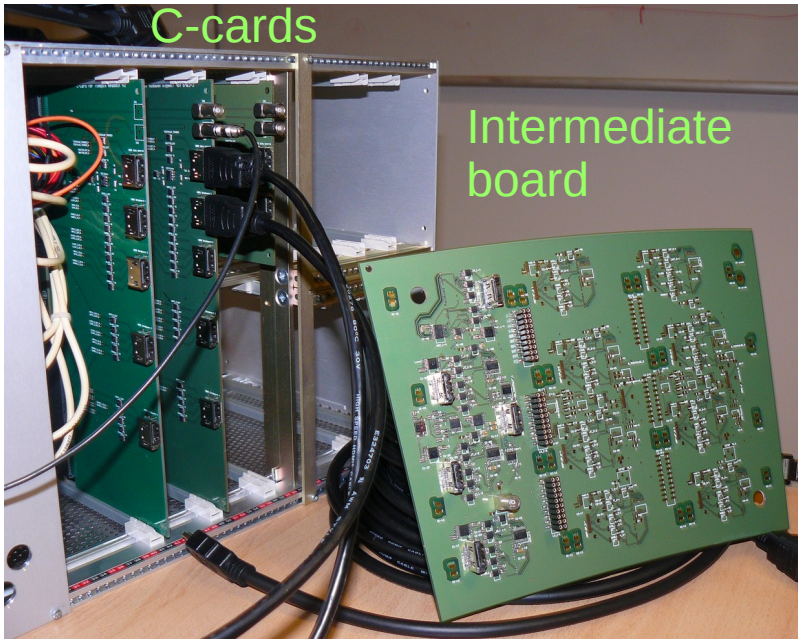


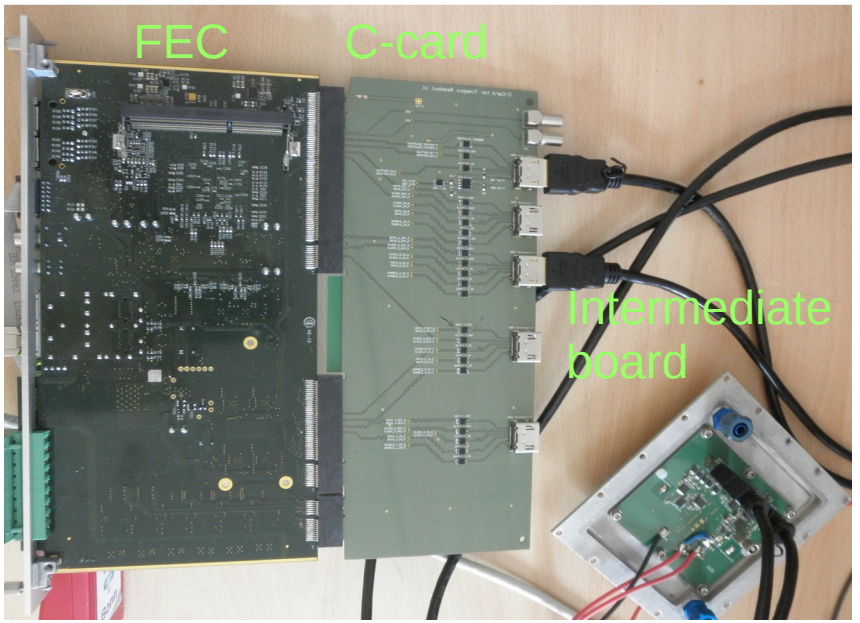
# Readout System



There are several readout systems optimized for different applications available for purchase. We have built one based on the Scalable Readout System of RD51, because it is easy to scale and cheap, if you have the main components already. 🙂

Idea of SRS: produce a flexible readout electronics, which can handle different chips (new FPGA code, chip carrier), which many groups can use.
New C-Card, intermediate board, and chip carriers were designed for Timepix.
Now up to 32 Timepix ASICs can be used per FEC/C-card.

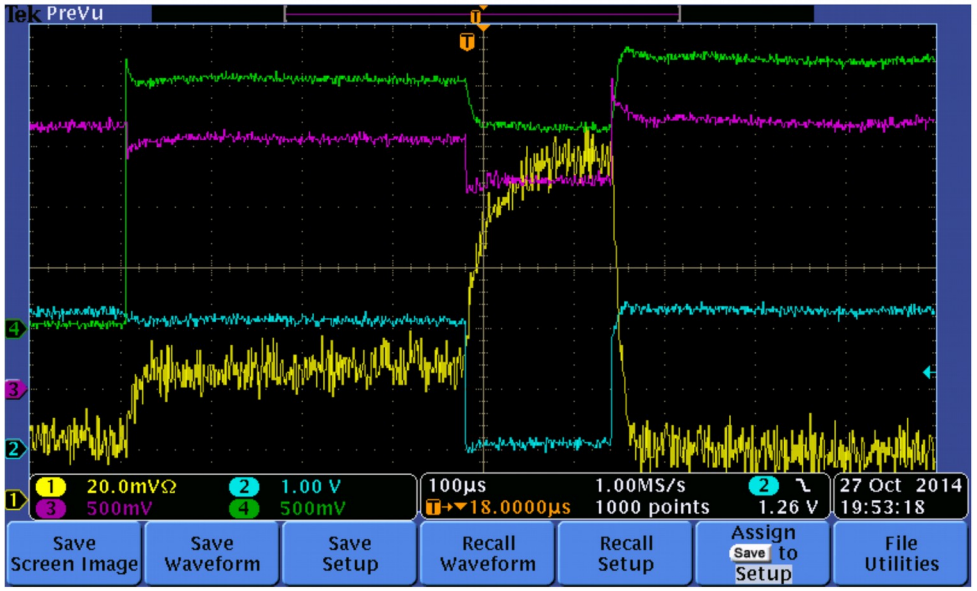


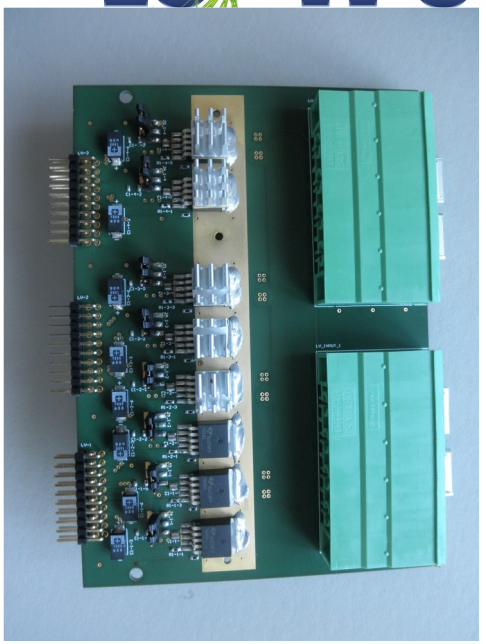

A small-size system using the same FPGA code and most of the hardware can be based on a Virtex6 evaluation board. This is used in CAST.

# LV-Power Supply & Cooling

The power consumption of an Octoboard was carefully studied




Currents of up to 82 A were expected (absolute maximum, when all pixels are in noise)
Voltage drops of 30 % over 15 m cables expected.
=> LV board on detector with LDOs



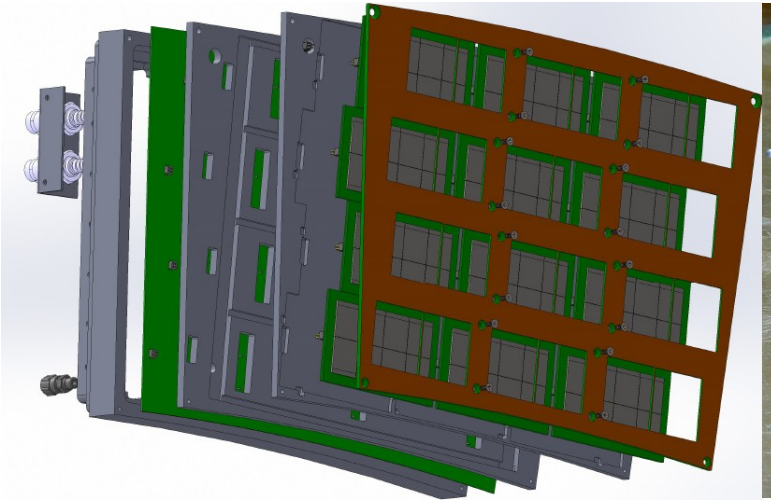
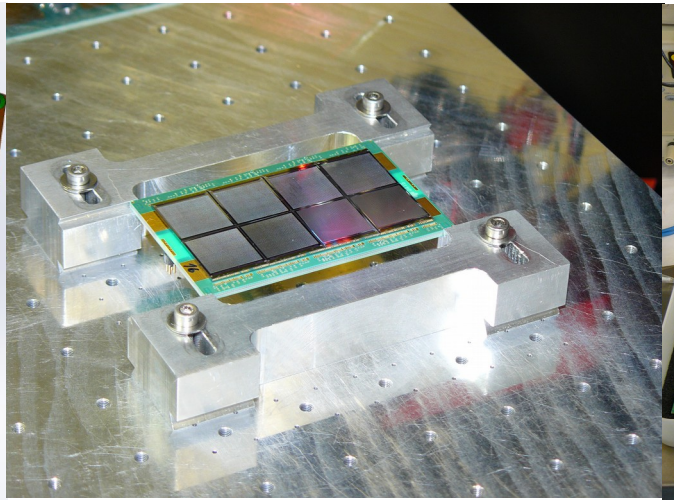
Power consumption of the digital part
Yellow: current going to chip,
lilac: voltage drop over supply line

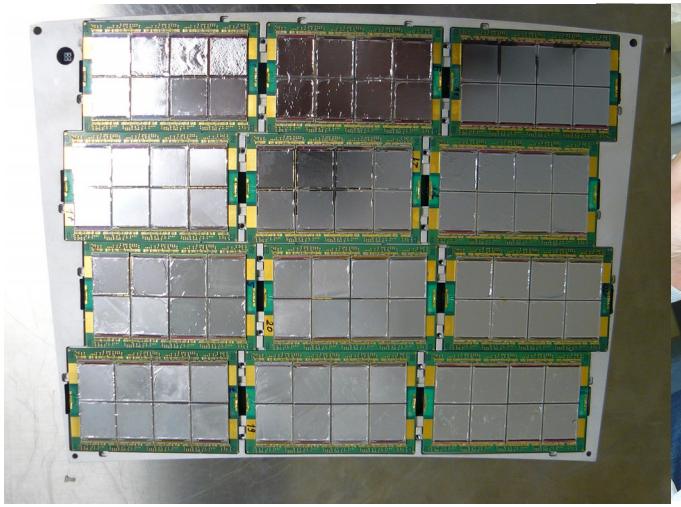
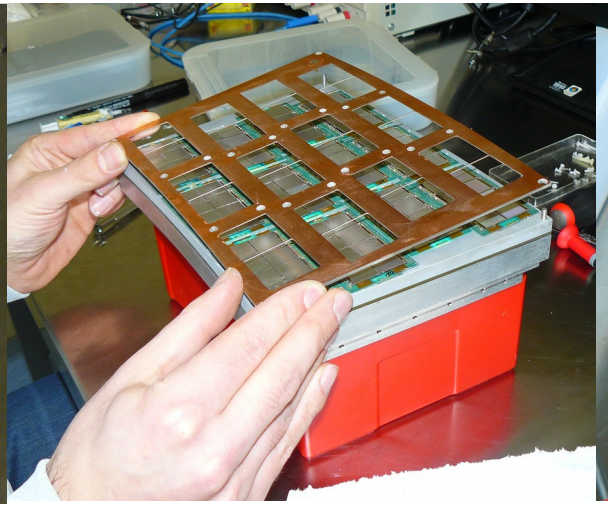
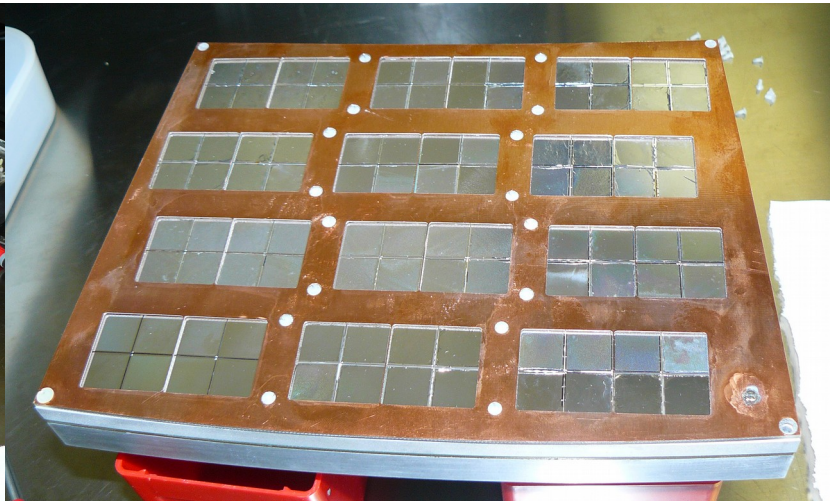
Power supplied by 5 ATX power supplies.

All the dissipated power needs to be cooled:
=> Cooling plate between intermediate board and chip carrier: 2 plates, of which one has pipes engraved, were diffusion welded into one.

Used tab water as coolant.

# Module Production

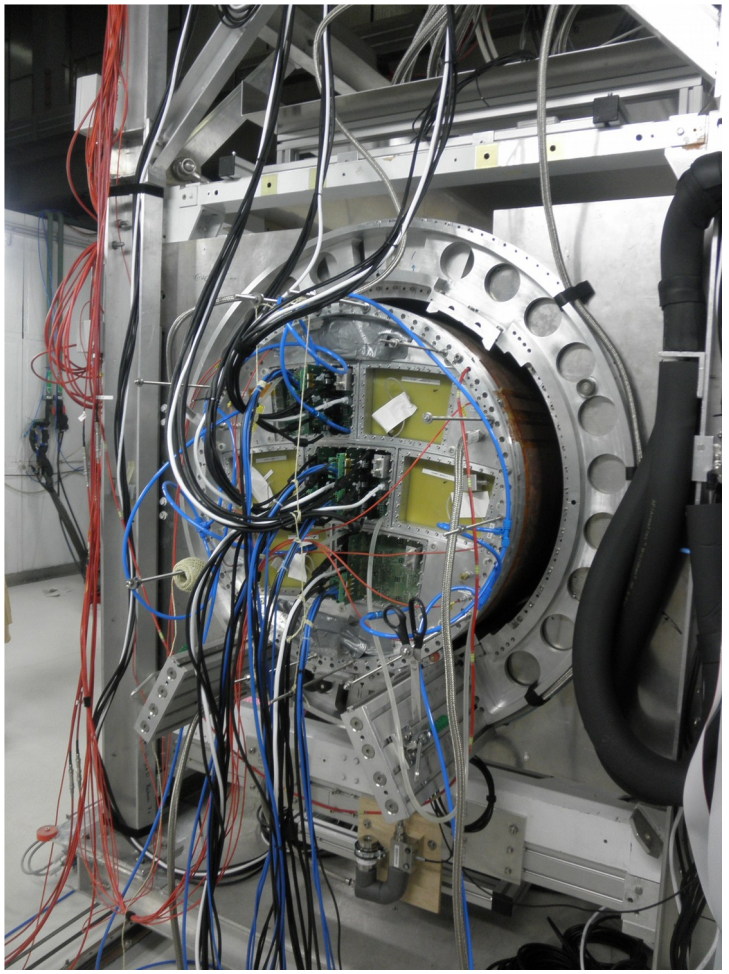




# Test Beam

The test beam was a huge success. A lot of people now think, that a pixel TPC is not a crazy idea anymore, but it is realistic.
During the test beam we collected ~$10^6$ frames at a rate of 4.3-5.1 Hz.

Test beam program:
– Voltage scans (gas gain)
– z-scan
– Momentum scan
– Different angles
– With and without magnetic field (B=1T)
– Two different electrical drift fields

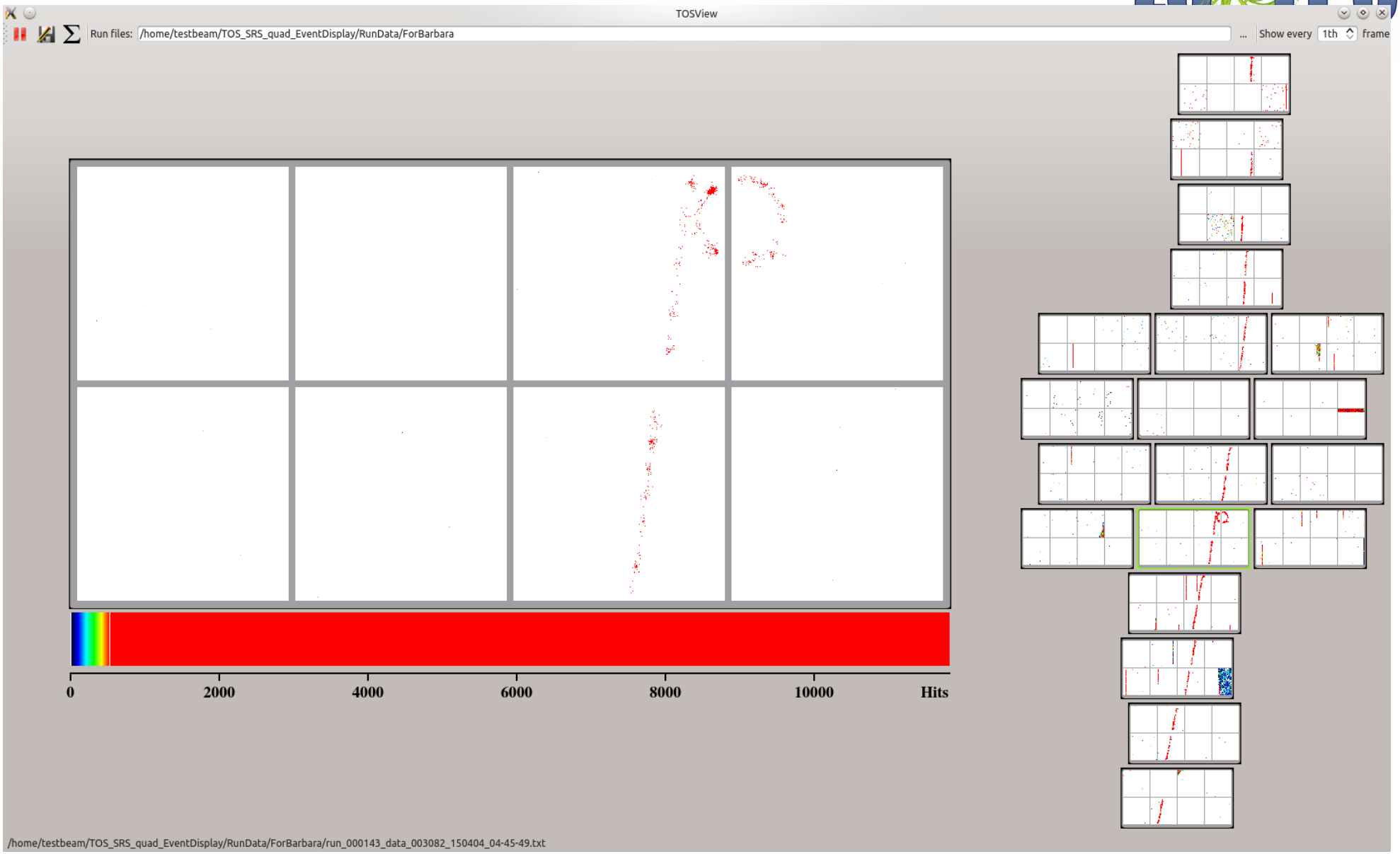
The analysis has started. Some very early results from Michael are already available.



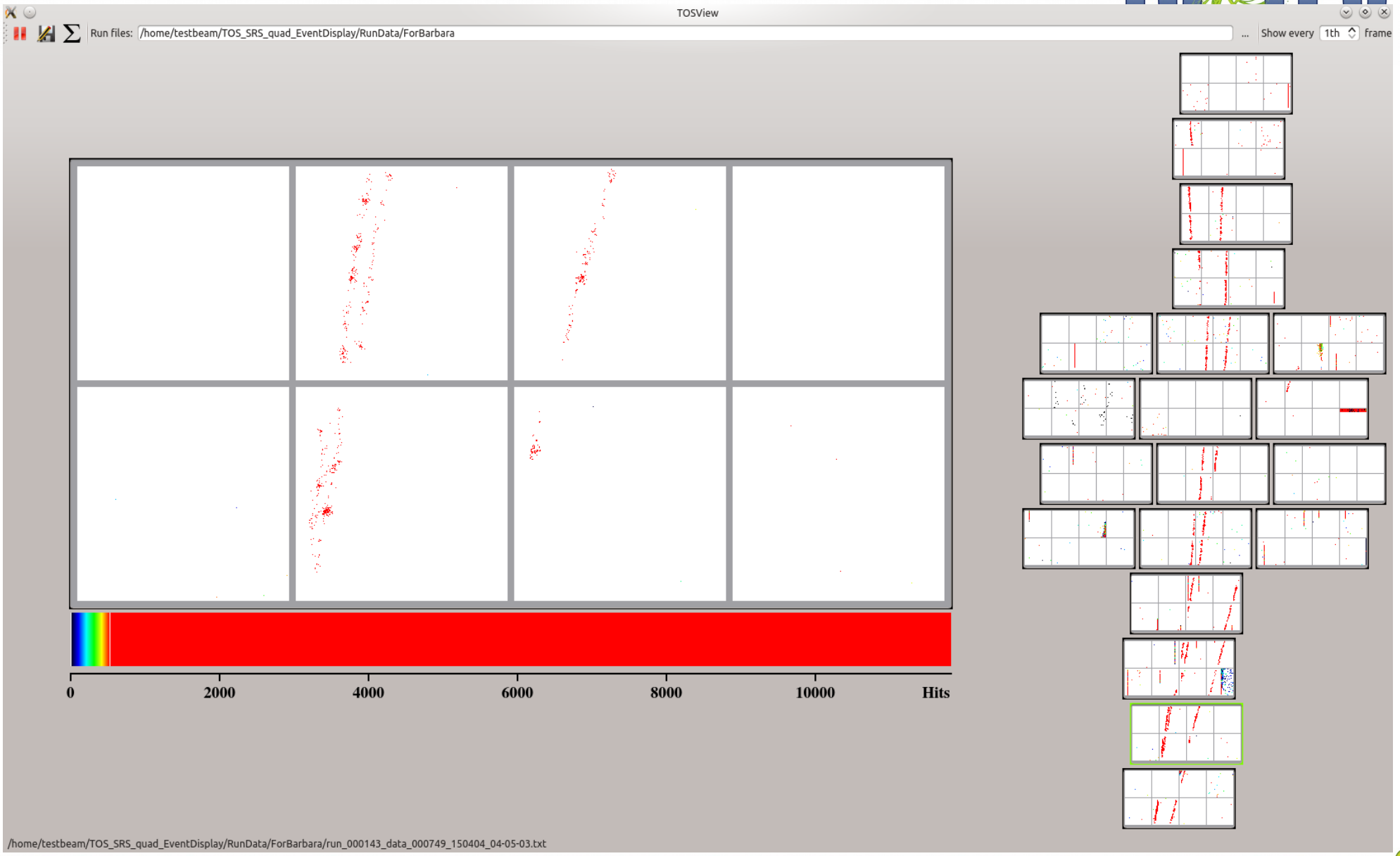
Material budget of 96 chip module (not optimized!)
- metallic frame 4.1 % $X_0$, cooling plate 5.9 % $X_0$
- 2 LV boards 2.5 % X0, 12 Octoboards 2.9 % $X_0$

In total: 18.5 % $X_0$

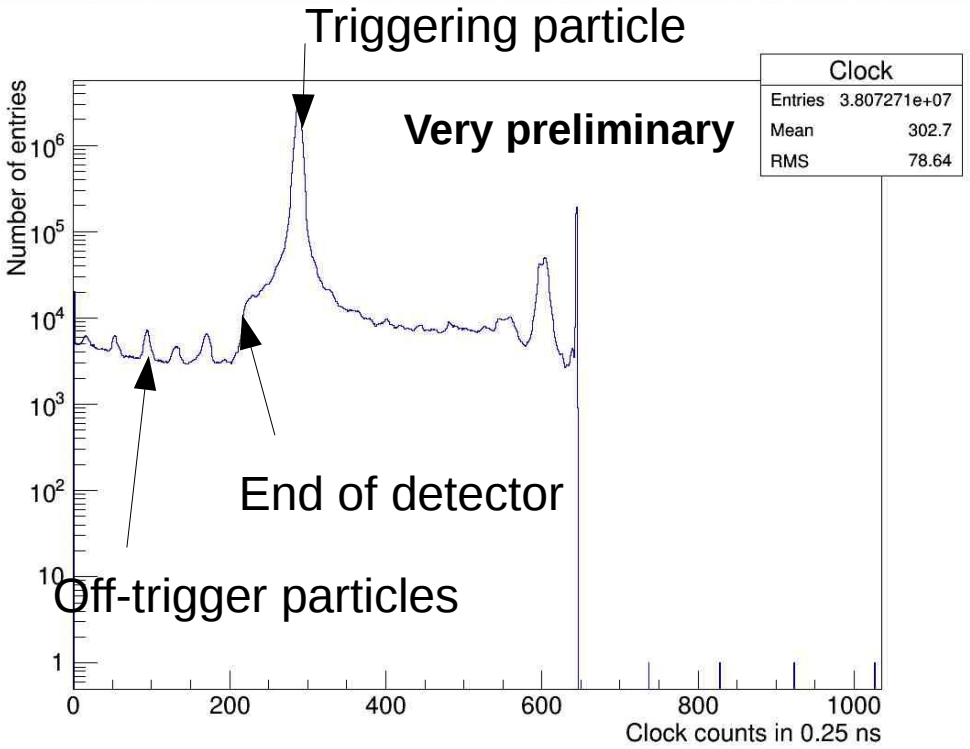
# Online Event Display (I)



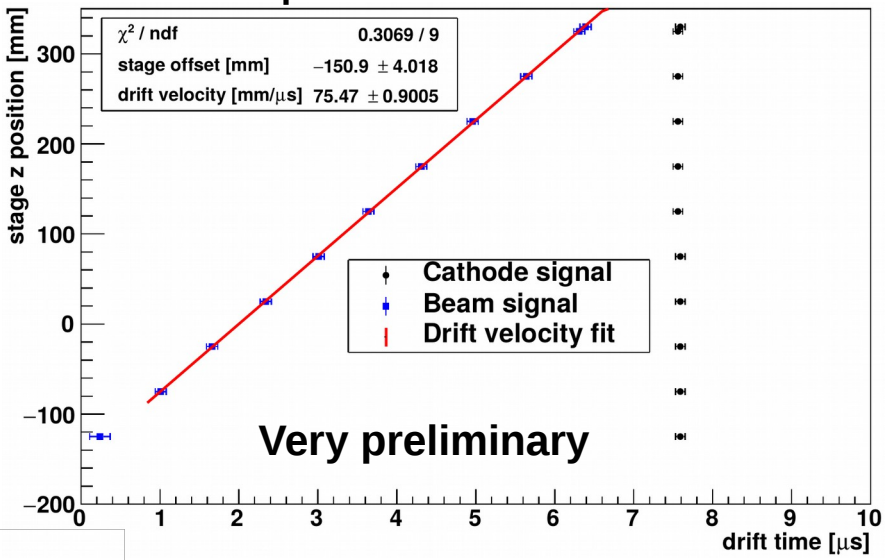
# Online Event Display (II)



# Analysis – Drift Velocity




Drift velocity can be measured for triggering particle, if the beam position is known.
And from the position of the cathode.



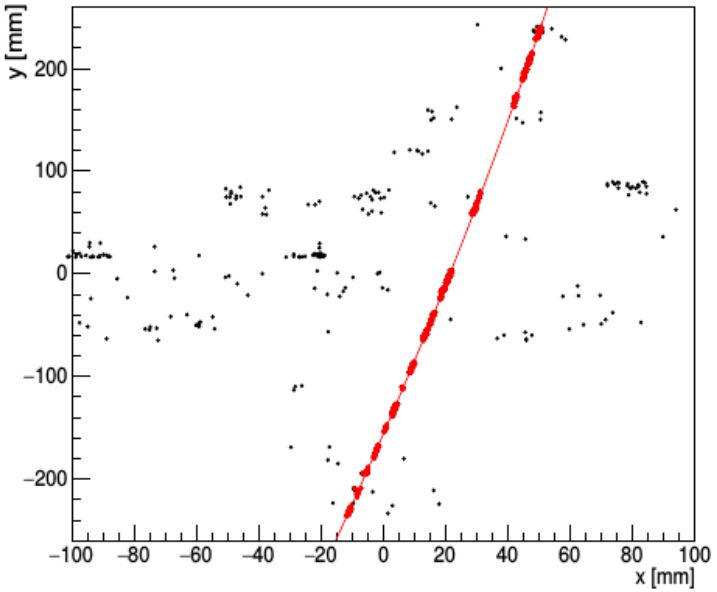

Comparison with simulation:

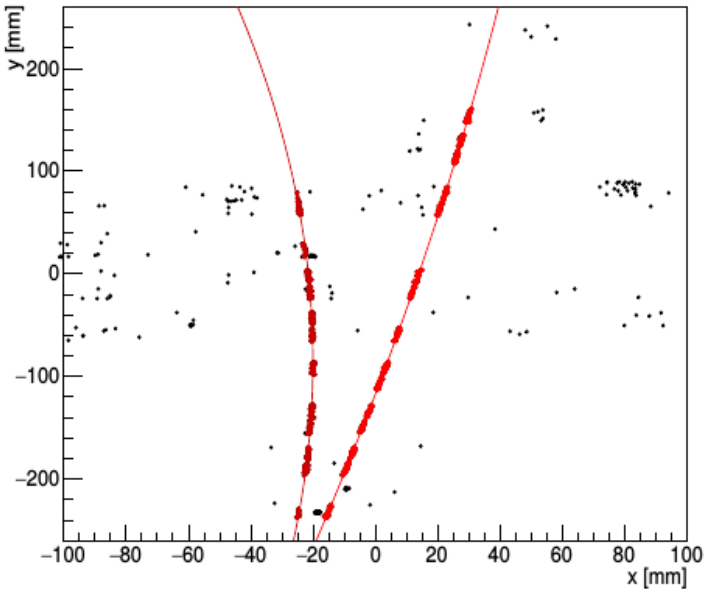
| Condition | Measurement | Simulation |
|---|---|---|
| E=130 V/cm, B= 0T | 5.61±0.02 cm/µs | 5.642 ±0.001 cm/µs |
| E=230 V/cm, B= 0T | 7.67±0.06 cm/µs | 7.650 ±0.002 cm/µs |
| E=230 V/cm, B= 1T | 7.69±0.05 cm/µs | 7.638 ±0.001 cm/µs |

# Track Reconstruction & Analysis

The data is analyzed with MarlinTPC in several steps:

- Cleaning of data (remove noisy chips and pixels)
- Hit finding
- Track finding (various track finders are being tested, most of them are Hough transformation based)
- Selection of clean sample of high energetic tracks (single tracks in event, cuts on angle $\phi$ in pad plane, track position and number of hits per track)
- Analysis

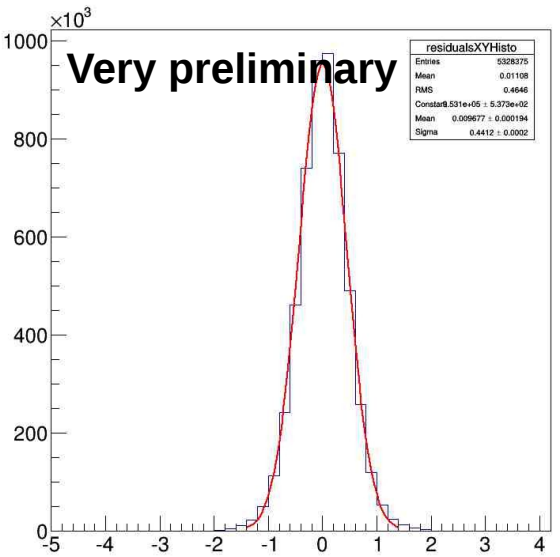


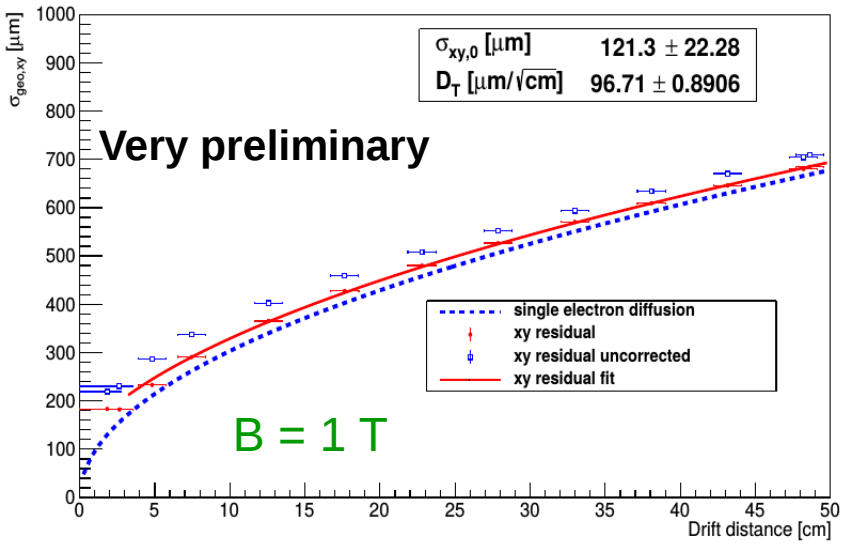



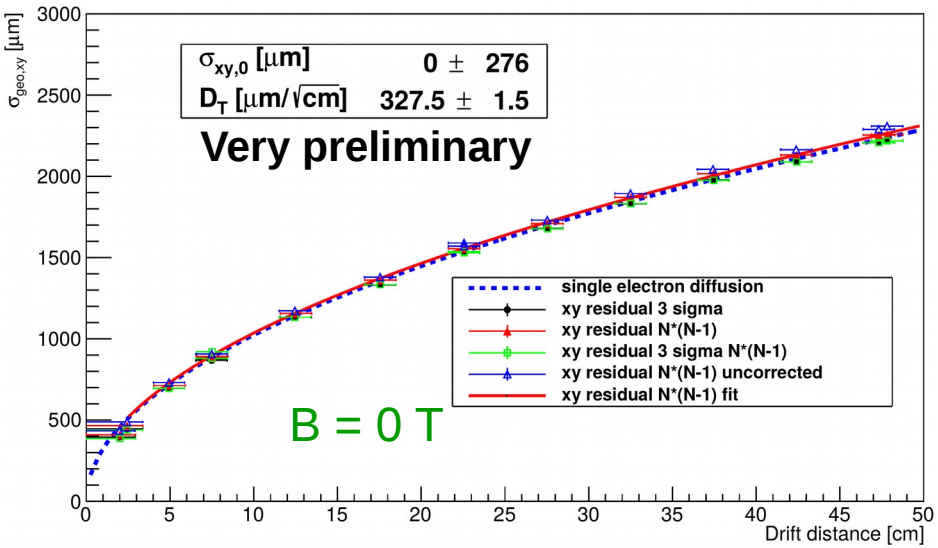
# Spatial Resolution

The spatial resolution is determined by calculating the residuals of single hits to fitted track.
Spatial resolution follows the diffusion of single electrons.

| Condition | Measurement | Simulation |
|---|---|---|
| E = 230 V/cm, B= 0T | 327.5 ± 1.5 µm/√cm | 324 ± 12 µm/√cm |
| E= 230 V/cm, B= 1 T | 96.7 ± 0.9 µm/√cm | 96 ± 5 µm/√cm |



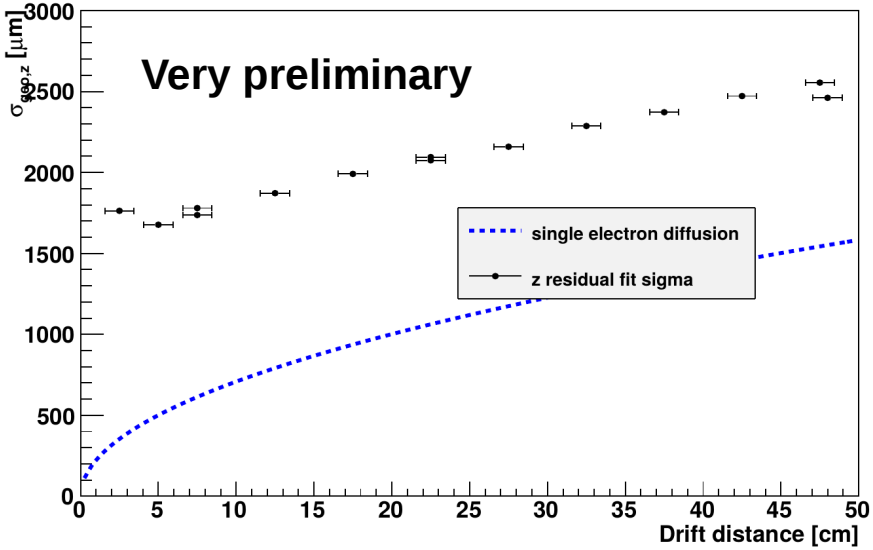



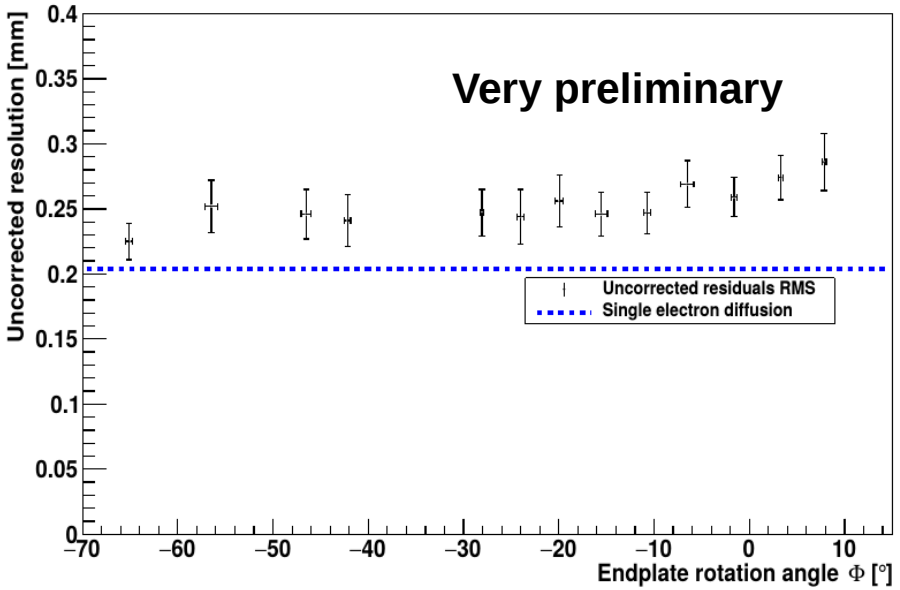



# More Spatial Resolutions

Longitudinal spatial resolution is much worse, because of many degrading effects:

- Time walk effect (partially compensated by fitting only the unaffected side of the residual distribution)
- Electrical field distortions at the border of the GridPixes
- 40 MHz clock for digitization

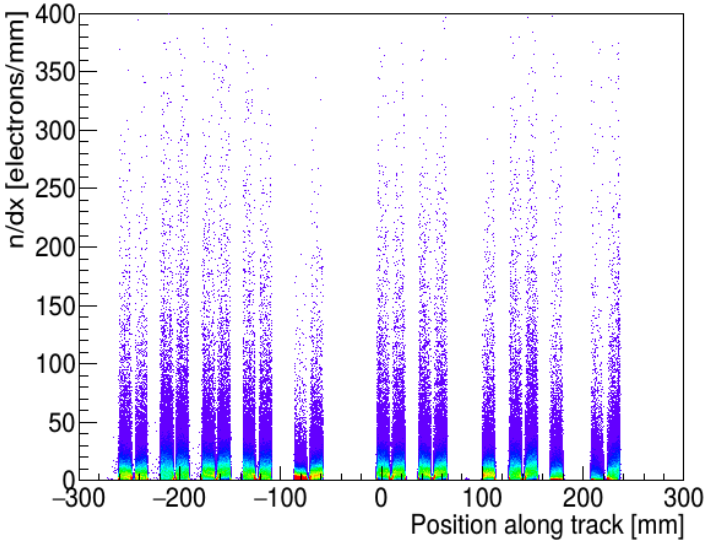


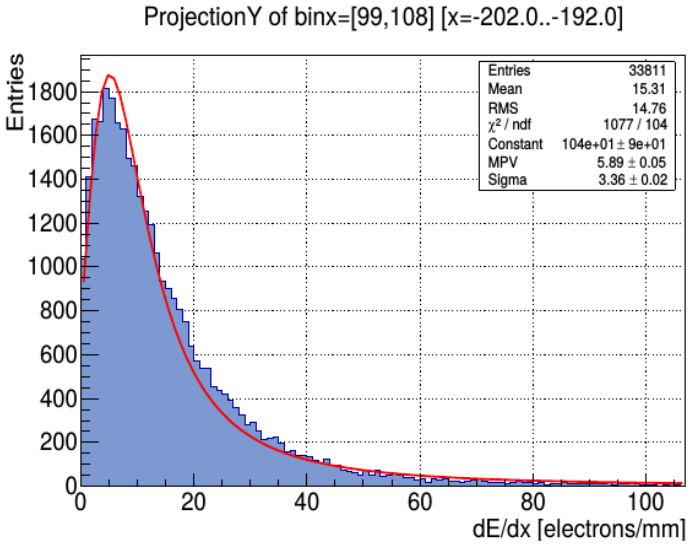



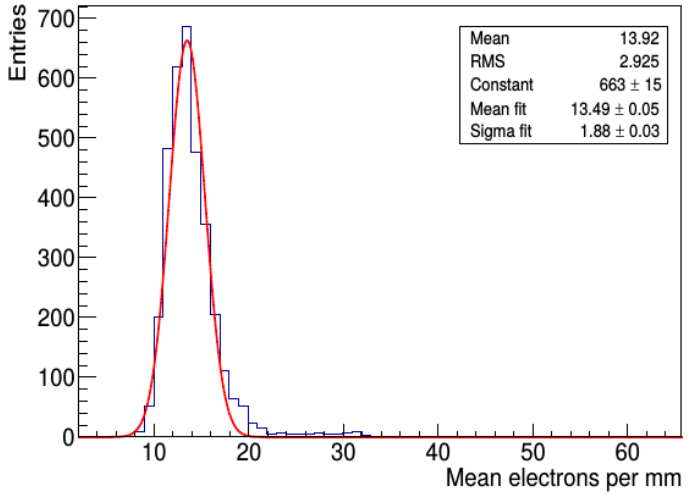

No dependence of transverse spatial resolution on track inclination in the pad plane (turning the TPC)
Error bars represent fluctuations of residuals for tracks

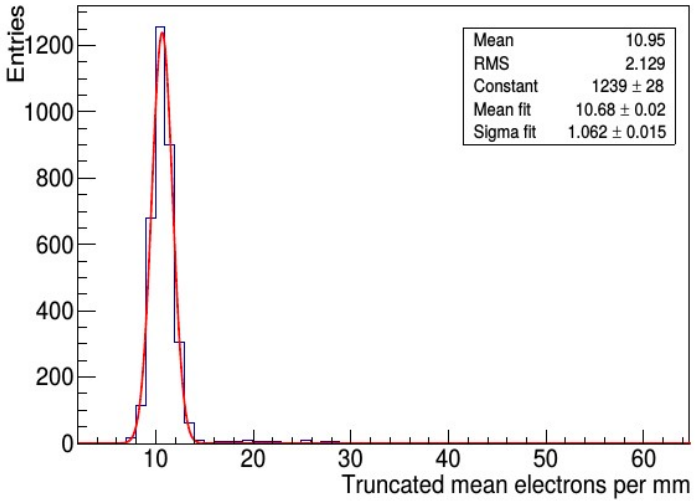
# DE/dx

## Number of electrons per 1 mm long track segment




Extrapolation to ILD:

$r_{TPC} \approx 1.5$ m:

dE/dx = 3.84 %

$r_{GridPix} = 1.01$ m:

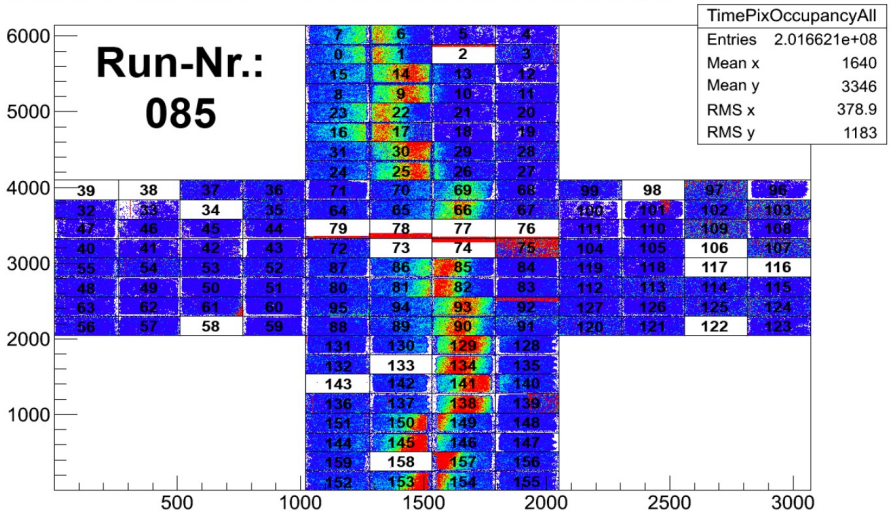
dE/dx = 4.36 %

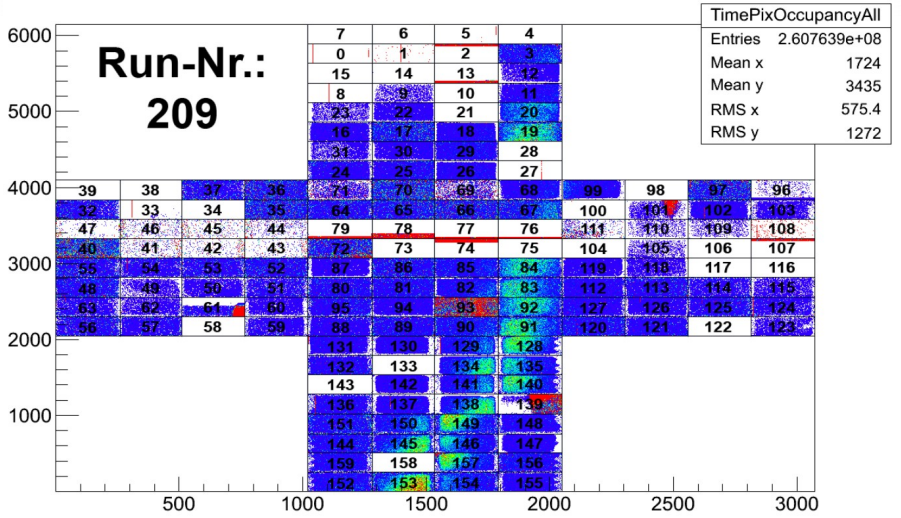
With 31 % inefficiency:

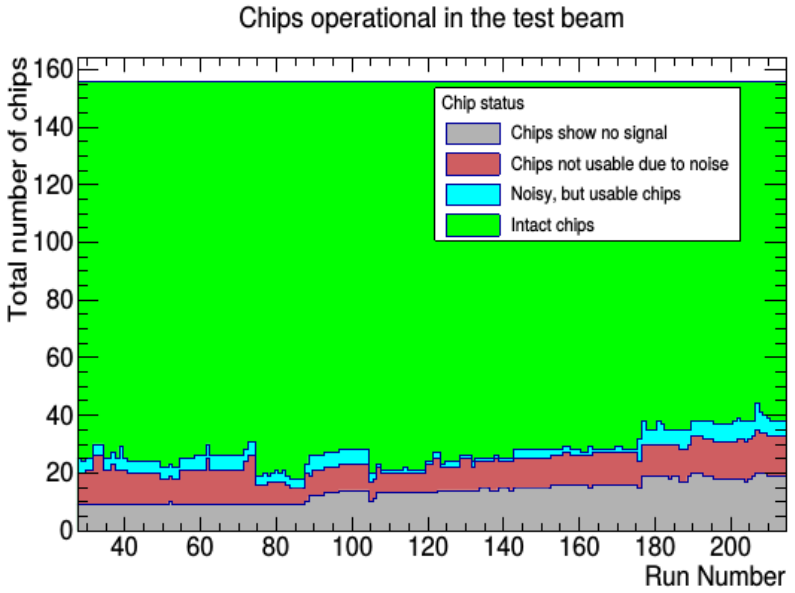
dE/dx = 4.81 / 5.71 %

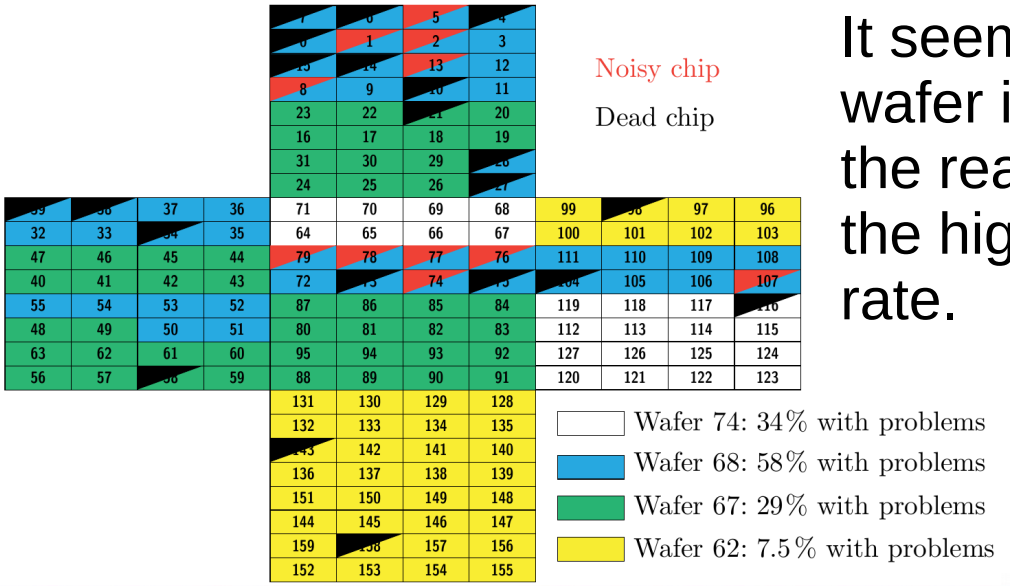
# Serviceability of Chips

Occupancy plots give information on serviceability of chips.



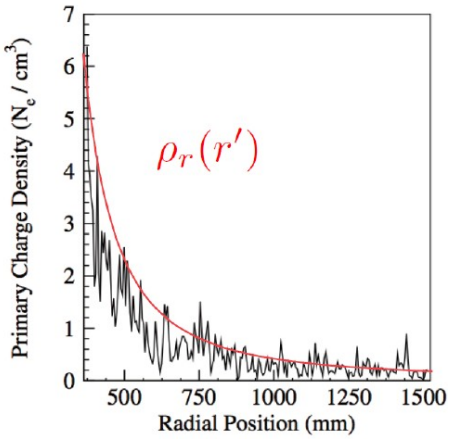



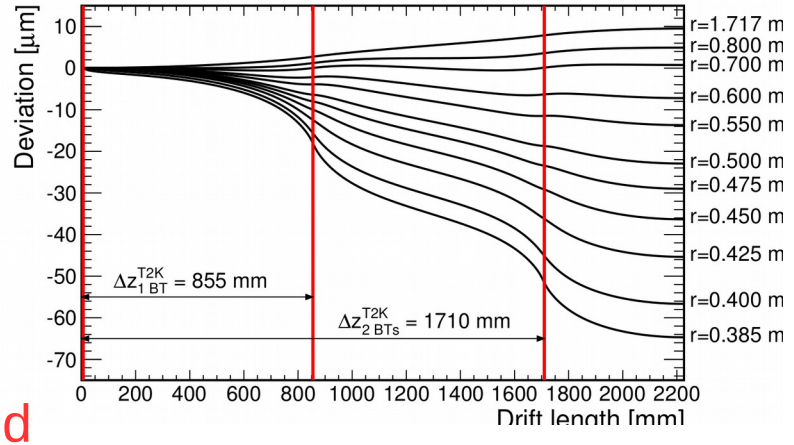

It seems one wafer is mainly the reason for the high failure rate.

# Ion Feedback and Gating

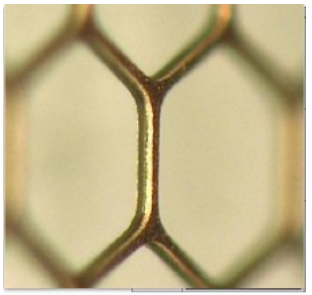
Primary ions create distortions in the electric field which result in O(<1µm) track distortions including a safety margin of estimated BG.

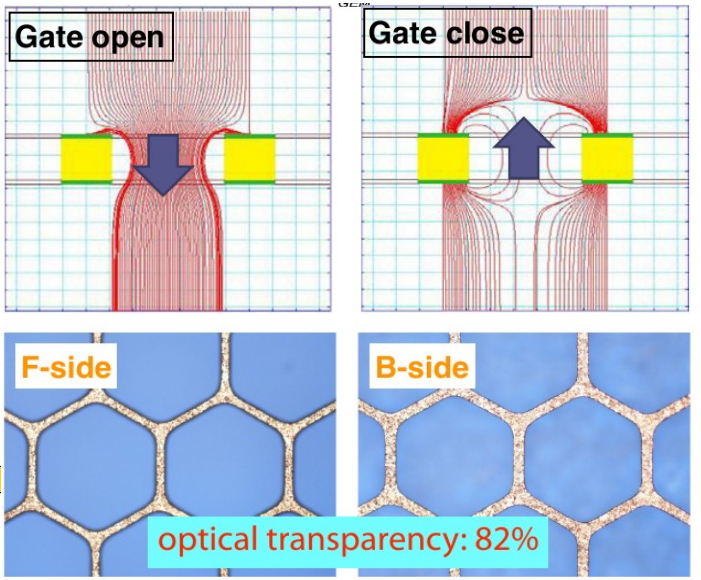



- Machine induced background has 1/r shape
- Ions from gas amplification stage build up discs
- Track distortions are 20 µm per disc without gating device, if IBF is 1/gain
- Total: 60 µm => Gating is needed




- Wire gate is an option
- Alternatively: GEM-gate
- Simulation show:
  Maximum electron transparency is close to optical transparency
- Fujikura Gate-GEM Type 3
  Hexagonal holes: 335 µm pitch, 27/31 µm rim
  Insulator thickness 12.5 µm






See presentation by D. Arai on Thursday

# Summary and Outlook

- To demonstrate the feasibility of covering larger areas (400 cm²) with a highly pixelated readout, 160 GridPixes were mounted on a module of the LP at DESY.
- Wafer-based production was established
- New readout system based on the SRS was developed.
- Detector modules with cooling, LV power supply etc were developed and more than 160 GridPixes were mounted on chip carriers and tested
- Successful operation in test beam in March/April 2015
- Analysis has started, several groups participate

Next steps:

- Adapt readout system to Timepix3; produce InGrid on top of Timepix3
- Improve InGrid technology (other materials, e.g. ceramic pillars)

Acknowledgement:
This is of course the work of many people. In particular, I want to mention Y. Bilevych, who produces the InGrids, and M. Lupberger who developed the readout system and made the first analysis.