

The TOTEM Experiment measures the total pp cross-section with a luminosity-independent method and studies elastic scattering and diffractive phenomena at the LHC energies. Furthermore, TOTEM's physics program aims for a deeper understanding of the proton structure by studying elastic scattering with small momentum transfers and diffractive processes in cooperation with the CMS Experiment. To perform these measurements, TOTEM requires a good acceptance for particles produced at very small angles with respect to the beam. TOTEM's coverage in the pseudo-rapidity near the interaction point spans the range $3.1 \le |\eta| \le 4.7$ and $5.3 \le |\eta| \le 6.5$; this is accomplished by two gas detector telescopes, named T1 and T2. The T1 and the T2 telescopes adopt respectively Cathode Strip Chambers (CSC) and Triple Gas Electron Multiplier(GEM) chambers which are able to detect inelastically produced charged particles. These detectors are complemented by silicon detectors housed in special movable structures embedded in the beam-pipe, called Roman Pots, placed at about 147m and 220m form the interaction point.



In the current TOTEM DAQ architecture, the optical receivers collecting data from detectors (OptoRx) are hosted by the VME boards. In the new TOTEM DAQ architecture, the VME hostboards are replaced by the Scalable Readout System (SRS) components providing faster and cost effective transmission medium. The OptoRx modules are plugged into a custom designed card, named Opto-FEC, that allows the connection with the Front-End Concentrator (FEC) board. Data received from the OptoRx are processed in the FEC and formatted using the User Datagram Protocol (UDP) protocol. Several FECs can be read directly by different PCs implementing point-to-point connection or in an Ethernet switched network architecture. At the present stage the SRU is used as TTC signals receiver and fan-out. In particular the optical signal from the TOTEM TTC system is connected to the SRU. The TTCrx chip on-board provides the LHC Timing, Trigger and Control (TTC) data stream decoding while the Scalable Readout Unit (SRU) FPGA distributes the clock, trigger and fast commands to the Data Trigger Clock and Control (DTCC) links. FEC modules are connected to the SRU DTCC ports via CAT6 Ethernet cables. In addition the SRU module can act as a data concentrator receiving data via DTCC links. This operation mode will be exploited at a later stage in case further processing will be needed on the dataset merged from different FECs.

The legacy TOTEM DAQ can reach up to 1kHz trigger rate in stand alone configuration, such limitation is due to the VME bus bandwidth.





The firmware of the FEC and SRU is mainly developed using the System Verilog integrating hardware description and verification in the same standard language. Although the System Verilog is relatively new and EDA tools supporting it are not fully mature, the language gradually gains attention in the industry thanks to its compactness and syntax structures which translate into more reusable and less error prone code.



In order to take advantage of the System Verilog, the firmware shipped with SRS hardware, has been completely reviewed and created in the new language. The firmware of both the FEC and the SRU consists of two big blocks: System and User units. The System unit provides support for all physical interfaces employed by the FPGA to communicate with external components, i.e. Gigabit Ethernet (GbE), DTCC, I2C, ect. The System unit handles configuration, control and timing signal distribution to the rest of the system, providing some set of services to the User unit. This approach allows potential users of the system to focus only on the deployment of the User unit while adopting the firmware to a specific application. Having the skeleton of the System unit already supporting a whole set of services, that later could be improved gradually by common effort of a whole system users community, lets individuals invest time in design and implementation of processing and preanalysis algorithms that can benefit acceleration from the hardware of the FPGA. The communication between all modules, especially between the System and User units, is provided by standard interfaces of Advanced Microcontroller Bus Architecture(AMBA) family:

The usage of a standard and well documented bus, such as the AMBA one, facilitates development, verification and merging of new modules into the design. Moreover, the adoption of an industrial standard allows one to reuse IP cores, widely available on the market, which speeds up the development stage.

• Advanced High-performance Bus (AHB) — interconnection dedicated for memory-mapped modules

 Advanced eXtensible Interface 4 Stream (AXI4-Stream) — unidirectional interconnection for modules exchanging stream of packets

The verification of the firmware is based on the Universal Verification Methodology (UVM). The Register-Transfer Level (RTL) code of device under test is wrapped in System Verilog classes forming an UVM environment. The environment consists of agents representing different inter-faces. A regular agent is built of driver, sequencer and monitor. The stimulus of the firmware under test is actuated by sequences which communicate with the drivers through the sequencers. Since the System Verilog supports randomization natively (at syntax level), using properly written sequences, test vectors have the chance to cover automatically a wide range of events. A similar result in old-fashioned, hard-coded approach would require thousands of lines of verification code. Moreover, using constraints and distributions, user may guide the testbench to explore different areas of the probability space by looking for possible bugs in the firmware. The coverage indicator allows us to estimate how much a project has been verified. The monitor inside the agents is used to collect traffic generated by the driver and to report it to a scoreboard. The scoreboard is an object that gathers all the stimulus and firmware responses evaluating whether the firmware behaves correctly. The verification code takes advantage of the System Verilog object-oriented constructs, so it can be easily reused and written at the high level of abstraction. For the FEC firmware a common UVM environment has been developed. Addition of a new functionality requires preparation of a specific sequence rather than a whole test-bench. After any modification, the firmware has to pass set of defined tests to be validated for production. Such an approach allows to trace logic, and sometimes also timing, pitfalls at the stage of development where all signals can be easily probed and analysed in the Hardware Description Language (HDL) simulator. It has an undeniable advantage over quite common, on-hardware test approach, in which signal visibility, even with help of logic analyser cores, is limited.



_egend	:		
X	UVM	transaction	

FECs

Smaller			
LDC name host	RU-srs27 192.168.0.127	RU-srs28 192.168.0.128	RU-srs28_2 192.168.0.128
Number of equipments	2	2	2
Number of triggers	24220067	24220050	24220026
Current Trigger rate	78127.203	78130.000	78127.203
Average Trigger rate	71235.469	71235.422	71235.352
Number of sub-events	24220067	24220050	24220026
Sub-event rate	78127	78130	78127
Sub-events recorded	24220062	24220050	24216703
Sub-event recorded rate	78128	78169	77464
Nb. evts w/o HLT decision	0	0	0

The full system has been installed and commissioned at the Interaction Point during August 2015. The system is composed of 16 FEC modules and one SRU.

Every FEC module is equipped with one OptoRx receiving data from 3 full RP detectors containing about 120 VFATs. Up to 4 FECs are read out by a standard PC, running the DATE software from the ALICE Collaboration. The readout PCs stream data to 12 event builder processes running on 5 different storage servers. Each server has a storage capacity of ~70TB and can achieve up to 1GB/s data troughput in write mode. All FECs are connected to the SRU module which distribute the TTC information. The SRU in turn, is connected to the TOTEM TTC network via optical fibre delivering the LHC clock, the orbit, the L1A and the fast commands signals. **The new system is being operated during the TOTEM's special runs, it allows the experiment to reach ~70kHz (on avarage) trigger rate**, which is about 2 order of magnitude higher than the performance of the TOTEM legacy DAQ.