# VMM - An ASIC for Micropattern Detectors


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*on behalf of the ATLAS Muon Collaboration*

# Outline

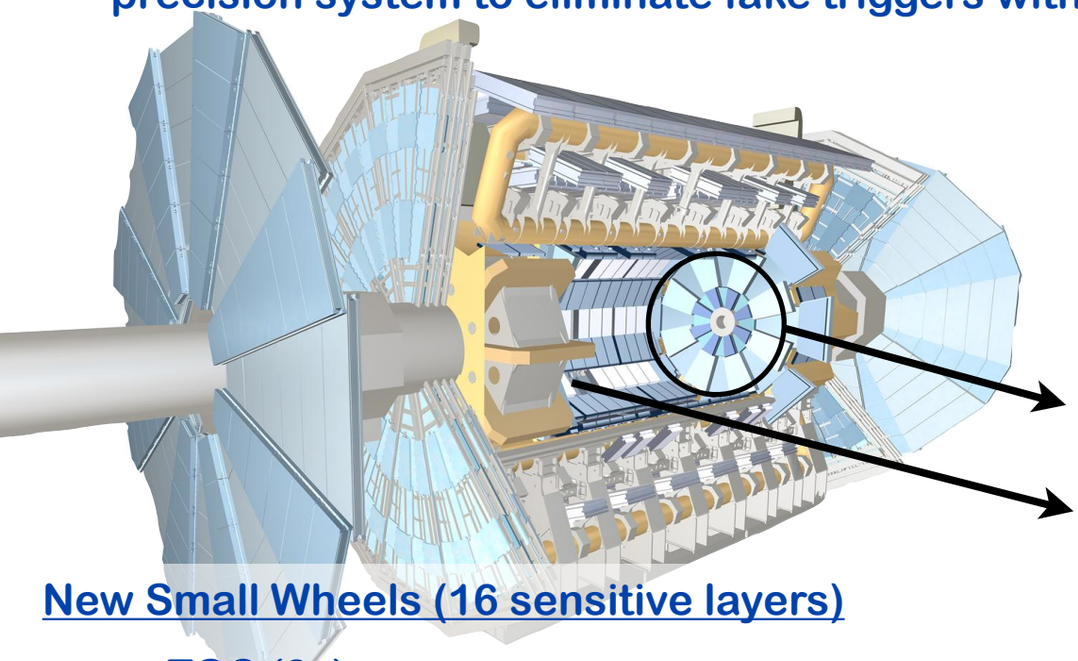


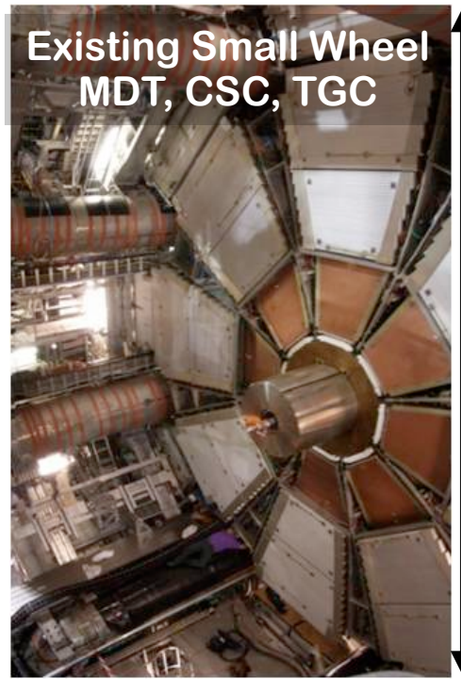
- Motivation and challenges for the electronics development and requirements
  - The ATLAS Upgrade - New Small Wheel(s) - Phase I (2019-2020)
- The first prototype of the VMM ASIC
  - Design, architecture and specifications
  - Testing, noise measurements, functionality
  - Precision and trigger performance with Resistive Micromegas detectors
  - Performance with sTGC detectors
- VMM ASIC evolution - Second Version
  - Digital design and new features implemented
  - Preliminary measurements and developments
  - Issues with the current version and timeline for the next version

# The ATLAS New Small Wheel(s) Upgrade (2019-20)

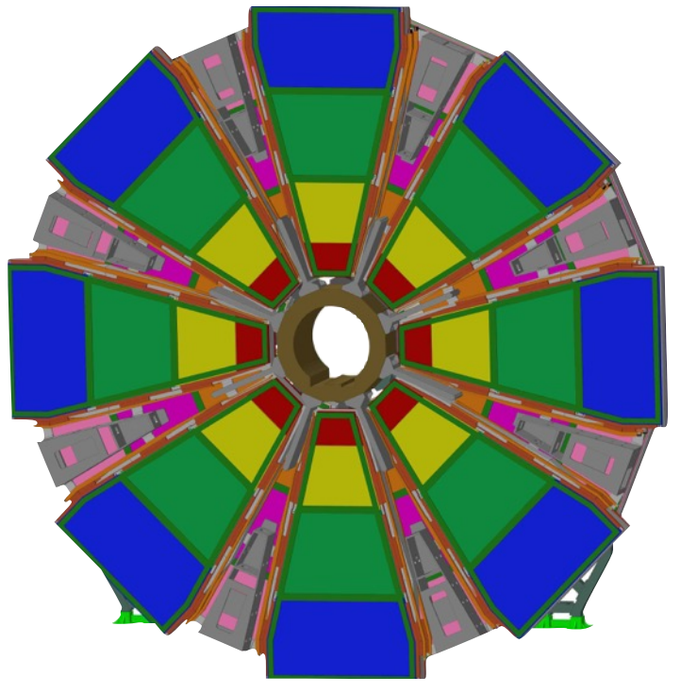


- The ATLAS upgrade is motivated primarily by the pile-up rate expected at high luminosity which will lead to an increased trigger rate. There is a need of replacing the innermost muon station with an efficient trigger and precision system to eliminate fake triggers without loss on physics acceptance.



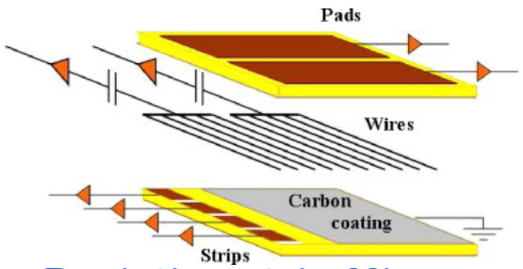



NSW

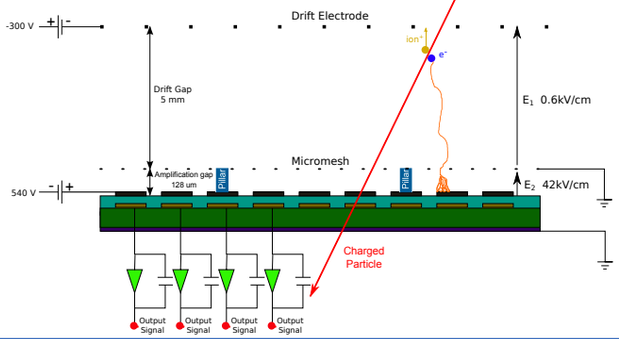


## New Small Wheels (16 sensitive layers)

- **sTGC (8x)**
  (small strip Thin Gap Chambers)




- **Resistive strip Micromegas (8x)**
  (Micromesh Gaseous Structure)




## Front-end Electronics Requirements (need of custom ASIC)

- Another challenge for this Project - More than 2.3 million channels total (2M for Micromegas and 300k for sTGC)
- Operate with both charge polarities
- Sensing element capacitance 10-200pF (sTGC Pad up to 2nF)
- Charge measurements up to 2pC @ < 1fC RMS(6pC for sTGC pads)
- Time measurements ~ 100ns @ < 1ns RMS
- Trigger primitives, complex logic
- Low power, programmable
- Space requirements on the detector

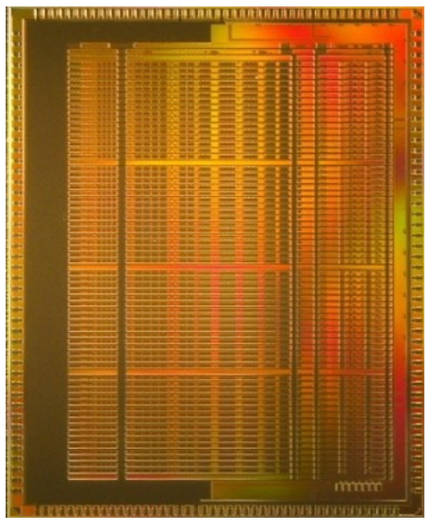
New Small Wheel Technical Design Report: Link
Technical Design Report for the Phase-I Upgrade of the ATLAS TDAQ System: Link

# VMM Front-end ASIC - First Version

**VMM is a data-driven 64-channel front-end ASIC for the read out of the sTGC and Micromegas detectors in the New Small Wheels. Of course it can also be used for other charge interpolated detectors.**

**Developed at Brookhaven National Laboratory**

**Version 1**



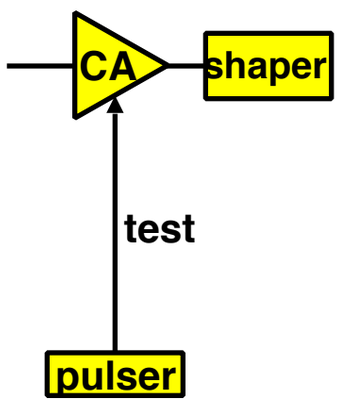
**VMM1 (2012)**

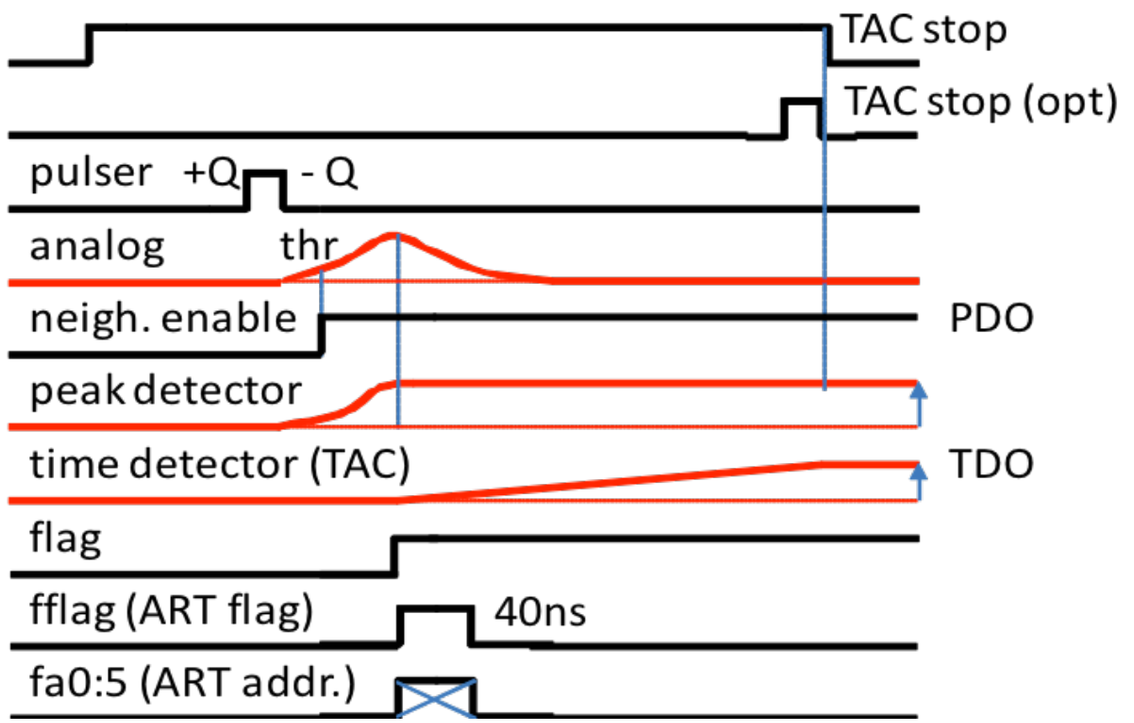
- **IBM CMOS 130nm 1.2V**
- **50 mm²**
- **500k MOSFETs (8k/ch.)**
- **a complex mixed-signal ASIC**
- **2-phase readout**

G. De Geronimo *et al* - ‘’VMM1—An ASIC for Micropattern Detectors”

Nuclear Science, IEEE Transactions on (Volume:60 , Issue: 3 )

# VMM1 Architecture and Specifications

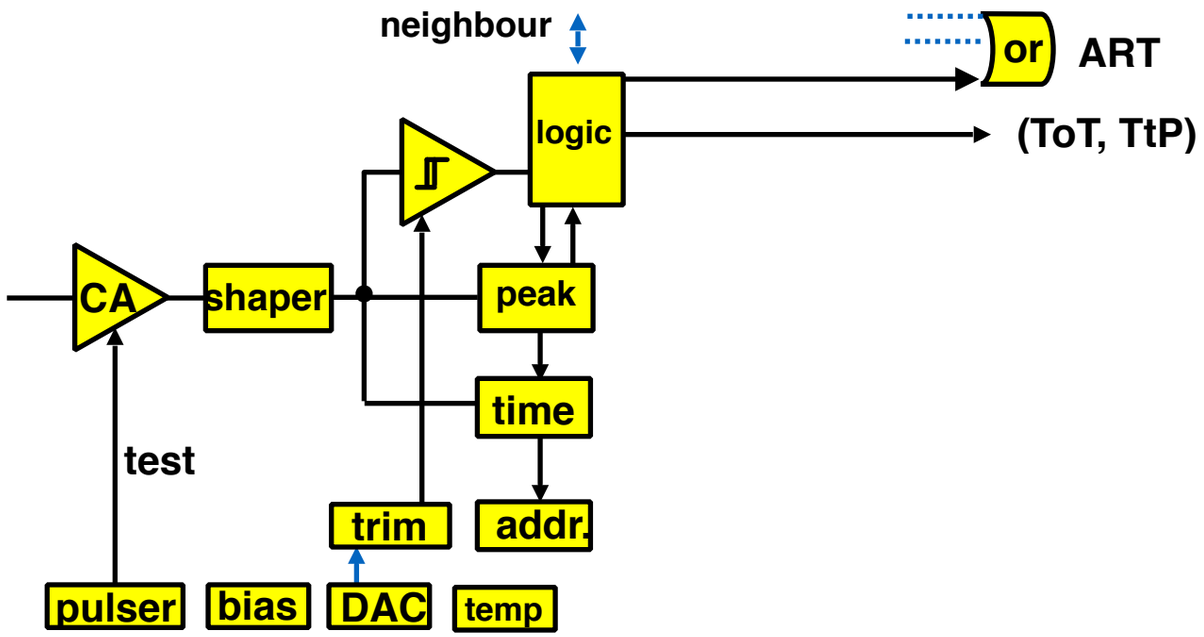


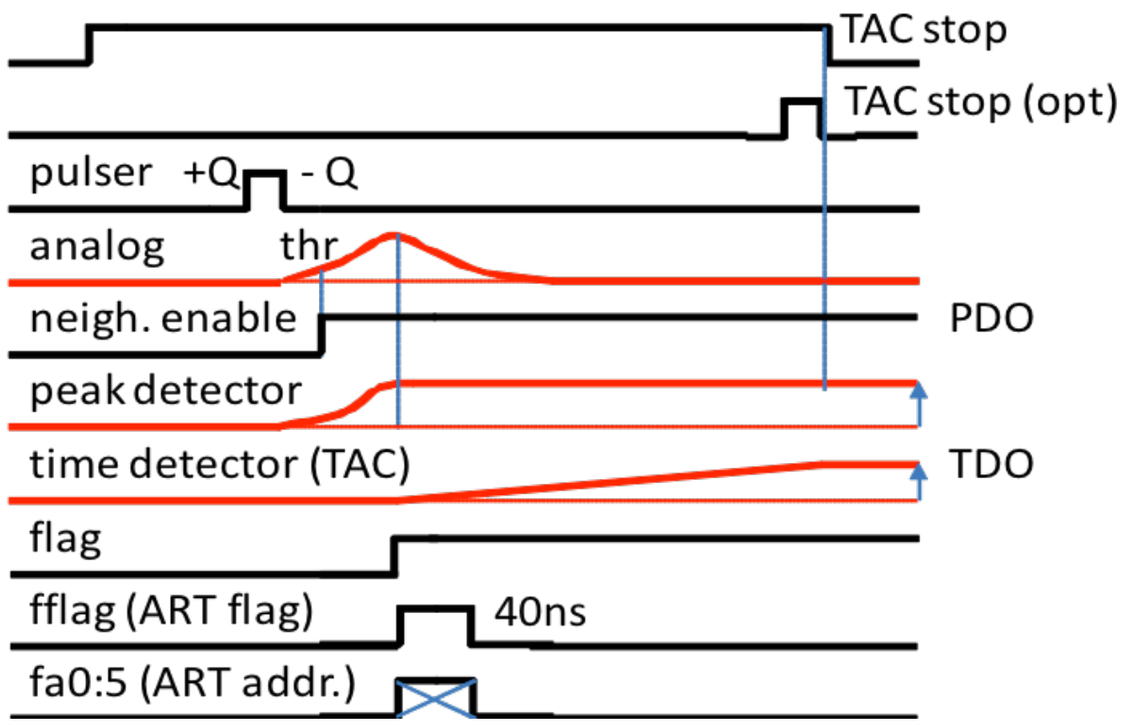




- Charge amplifier: input MOSFET: 10mm, 1.65mA, 18pF with adjustable positive or negative polarity, input capacitance: optimised for 200pF, can operate in a range from sub-pF to 400pF gain: adjustable 0.5, 1, 3, 9 mV/fC (maximum charge 2, 1, 0.33, 0.11 pC )
- Shaper: 3rd order with complex conjugate poles in Delayed Dissipative Feedback (DDF), adjustable peaking time: 25, 50, 100, 200ns

# VMM1 Architecture and Specifications



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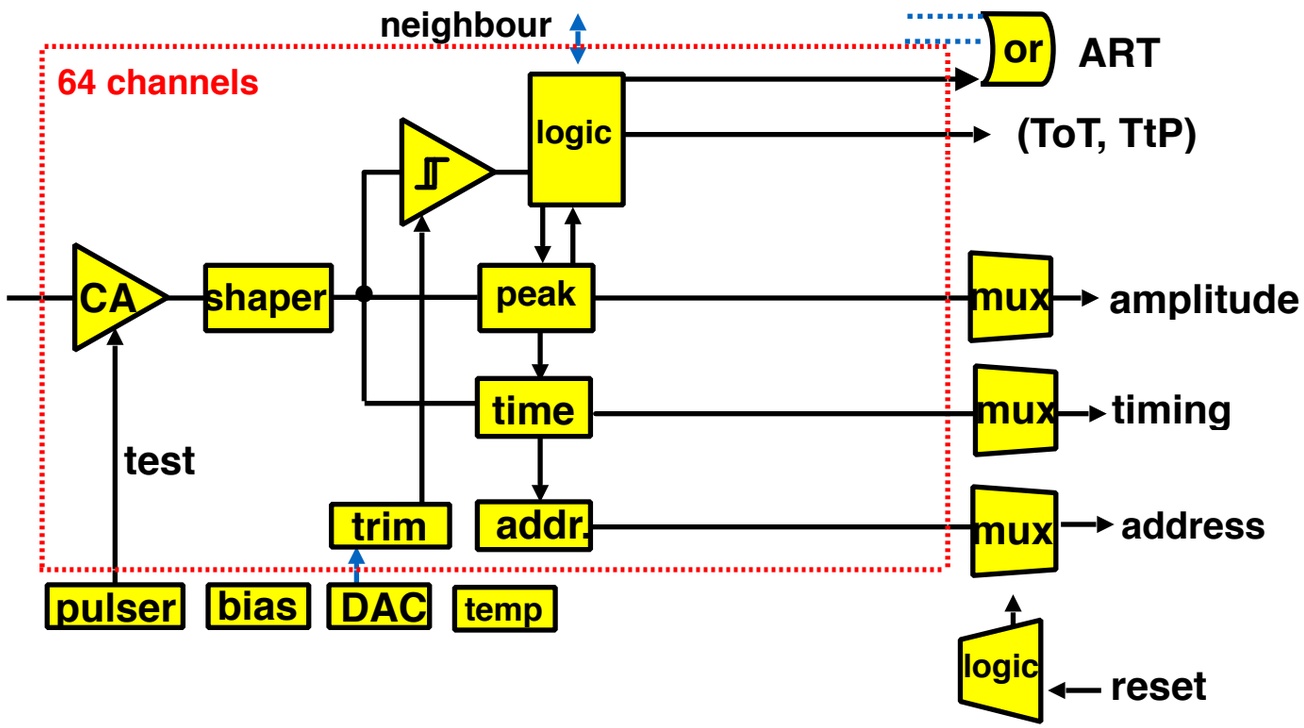
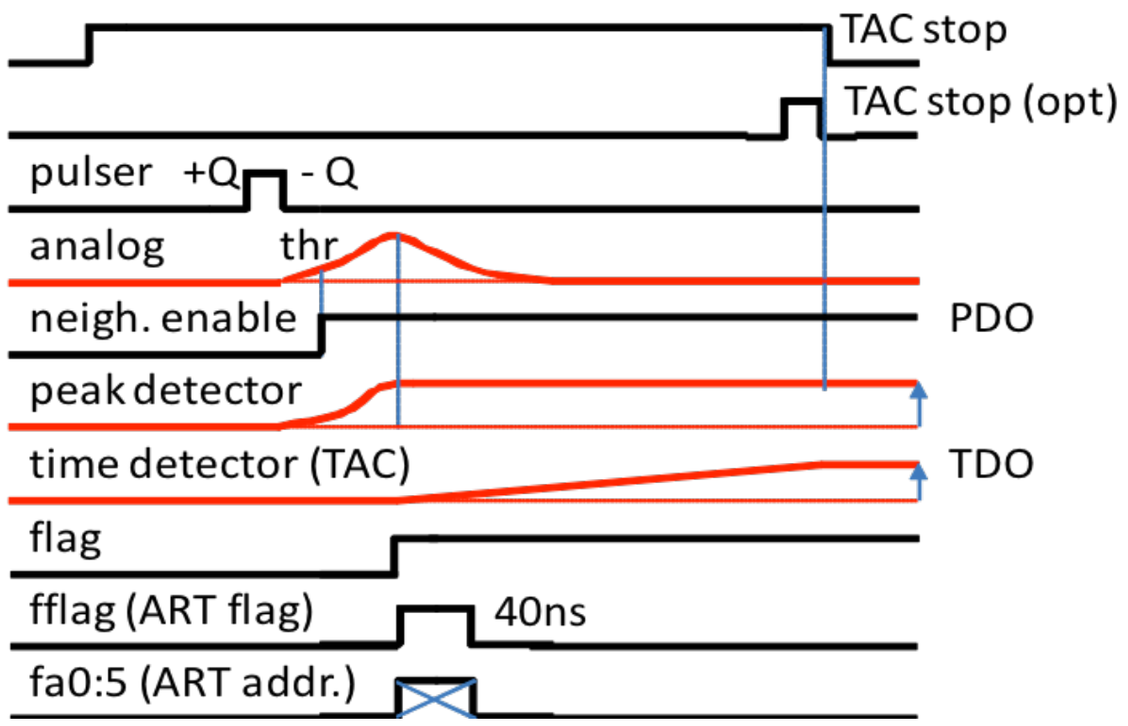
- Shaper: 3rd order with complex conjugate poles in Delayed Dissipative Feedback (DDF), adjustable peaking time: 25, 50, 100, 200ns
- Discriminator: adjustable with 10-bit global DAC, adjustable threshold, channel discrimination adjustment up to 15mV (1mV step), capable of processing sub-hysteresis signals with effective discrimination of ~2mV. This provides neighbour logic for channels but also chip interconnection.
- Peak detector, measurement of the peak amplitude (sub-mV resolution on amplitude measurement)
- Time detector: sub-ns resolution measurement of peak time, low time-walk on peak time measurement with adjustable time-to-amplitude converter (TAC): 125, 250, 500, 1000 ns.
- Logic: direct time-over-threshold or time-to-peak output and Address in Real Time (trigger primitives)

# VMM1 Architecture and Specifications (analog)



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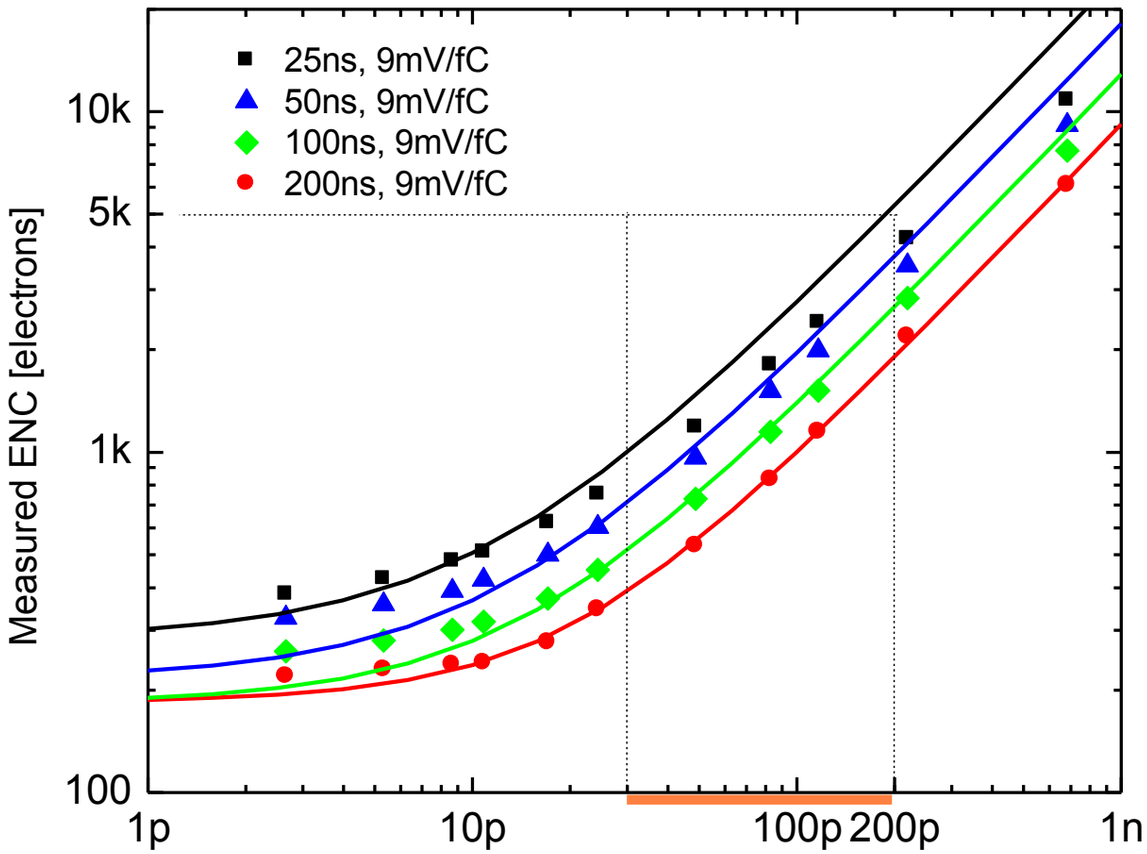
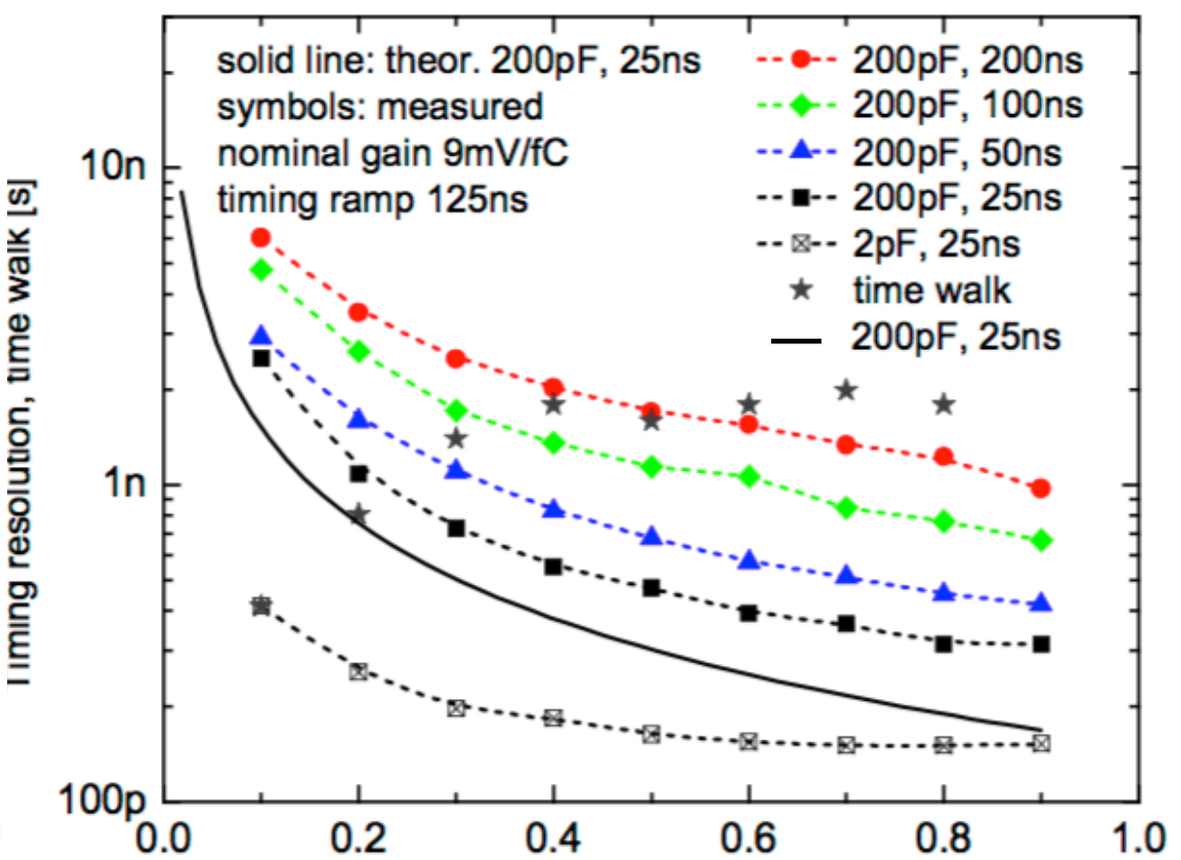
- Time detector: sub-ns resolution measurement of peak time, low time-walk on peak time measurement with adjustable time-to-amplitude converter (TAC): 125, 250, 500, 1000 ns.
- Logic: direct time-over-threshold or time-to-peak output and Address in Real Time (trigger primitives)
- Output: 2 phase readout, PDO and TDO as analog and digital address of the channel
- Monitor Output: Analog pulse, pulser DAQ, threshold (channel, global), temperature, reference voltage.
- PROMPT (courtesy of CERN): export regulations (ITAR) compliance circuit

# Resolution Measurements

## Charge Resolution




## Timing Resolution



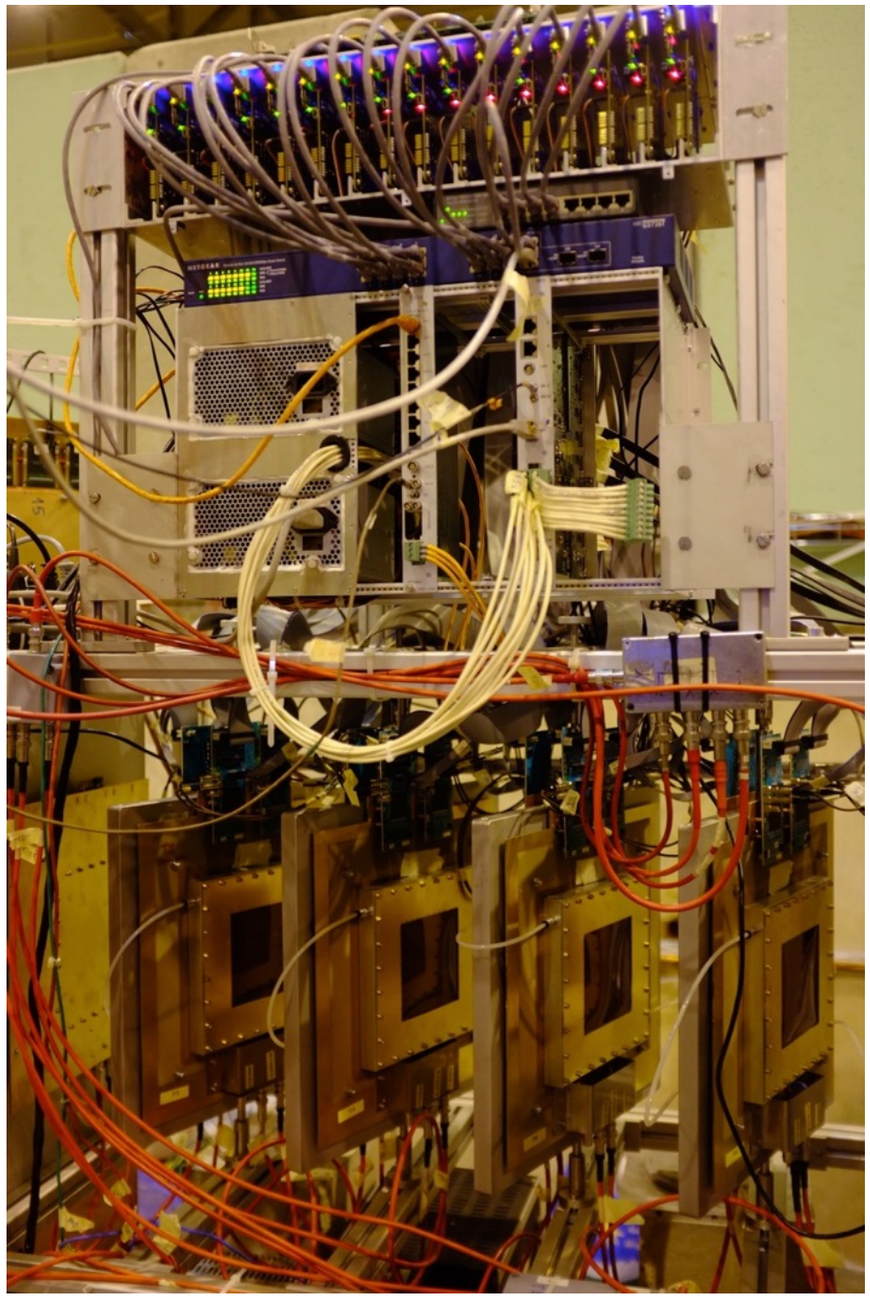

- **charge resolution ENC < 5,000 e- at 25 ns, 200 pF**
- **analog dynamic range $Q_{max}$ / ENC > 12,000 → DDF**
- **timing resolution < 1ns (at peak-detect)**
- **In agreement with the theoretical expectations (solid lines)**

G. De Geronimo *et al* - ‘’VMM1—An ASIC for Micropattern Detectors”

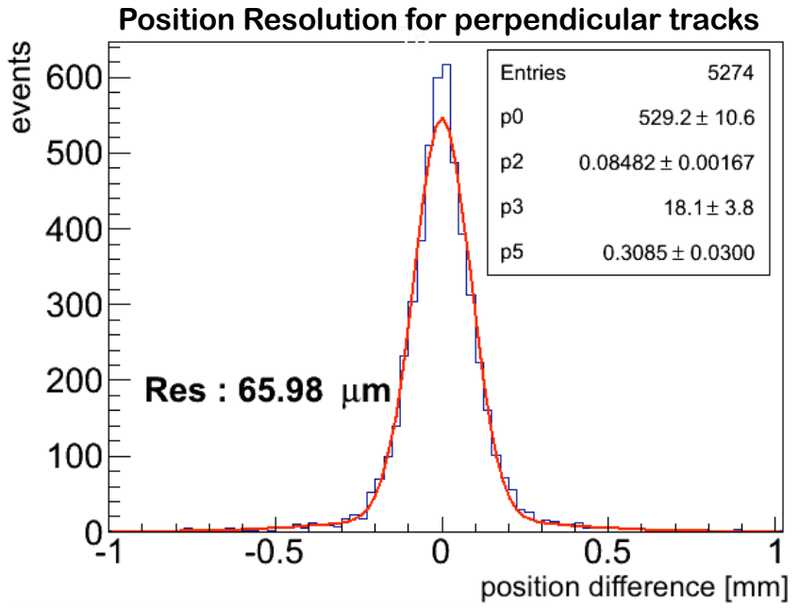
Nuclear Science, IEEE Transactions on (Volume:60 , Issue: 3 )

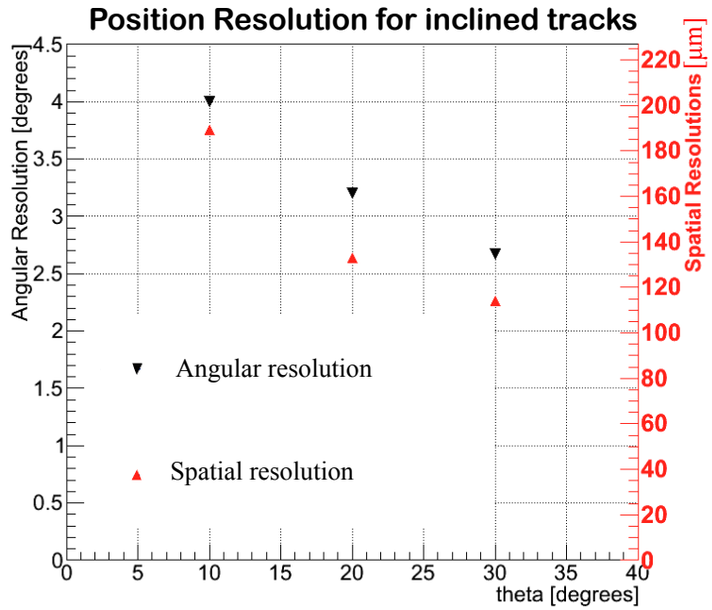
# VMM1 - Testing with Micromegas Detectors

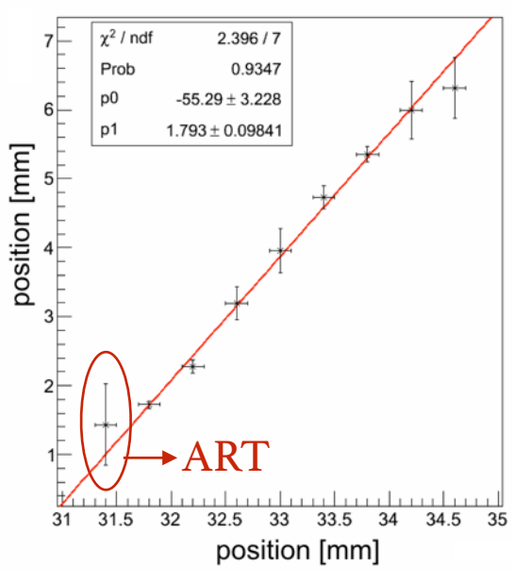


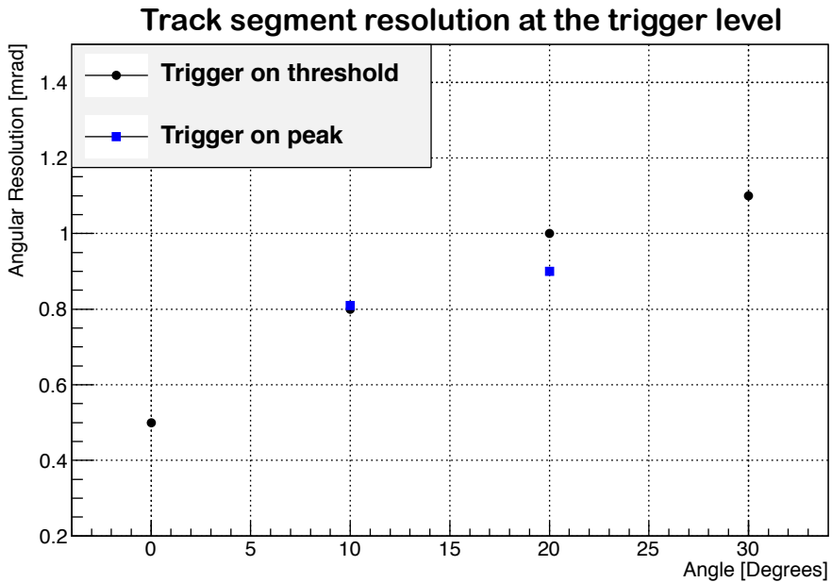


- First prototypes (x16) tested in 2012 test beam successfully[1] with custom readout
- First time testing the Resistive Micromegas as trigger system.
- Low noise (~0.2fC) and good timing gives an excellent position resolution (close to 100μm demonstrated performance[2]) and accurate timing for the μTPC studies.



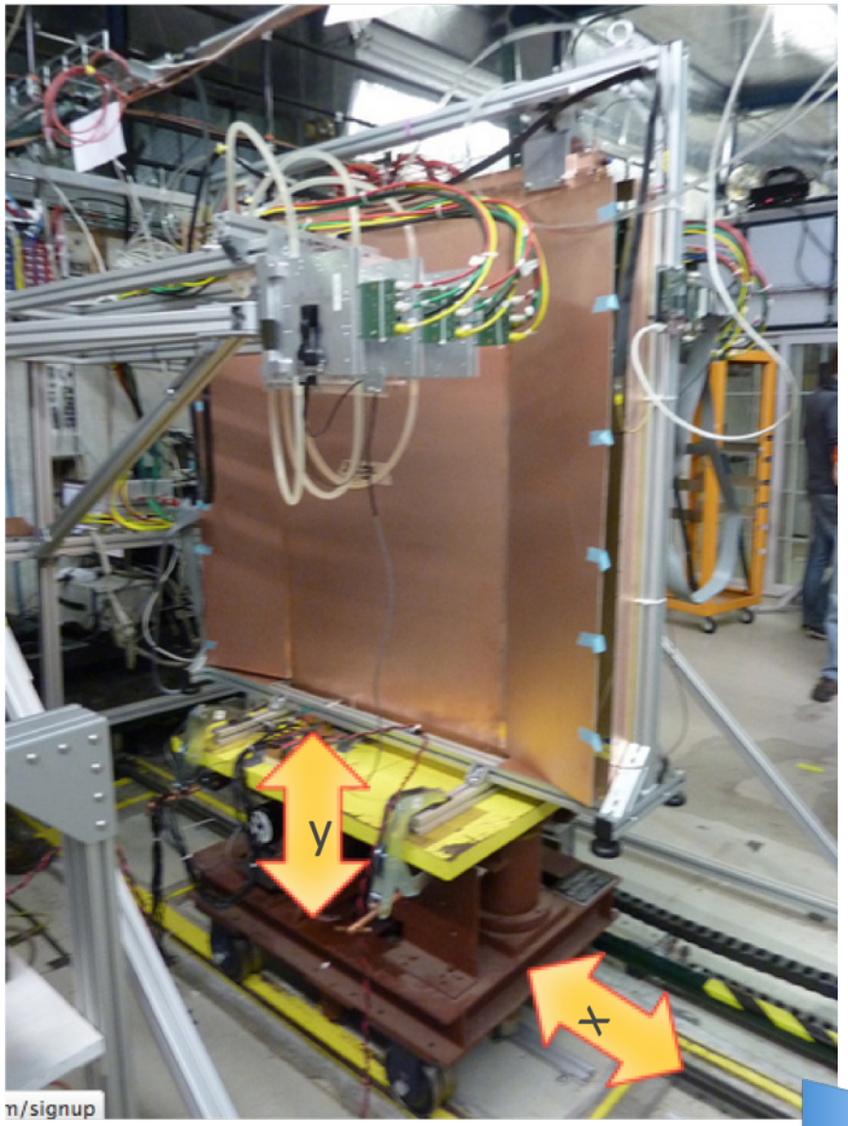




[1]T. Alexopoulos *et al.* - Performance of the First Version of VMM Front-End ASIC with Resistive Micromegas Detectors, ATL-UPGRADE-PUB-2014-001,

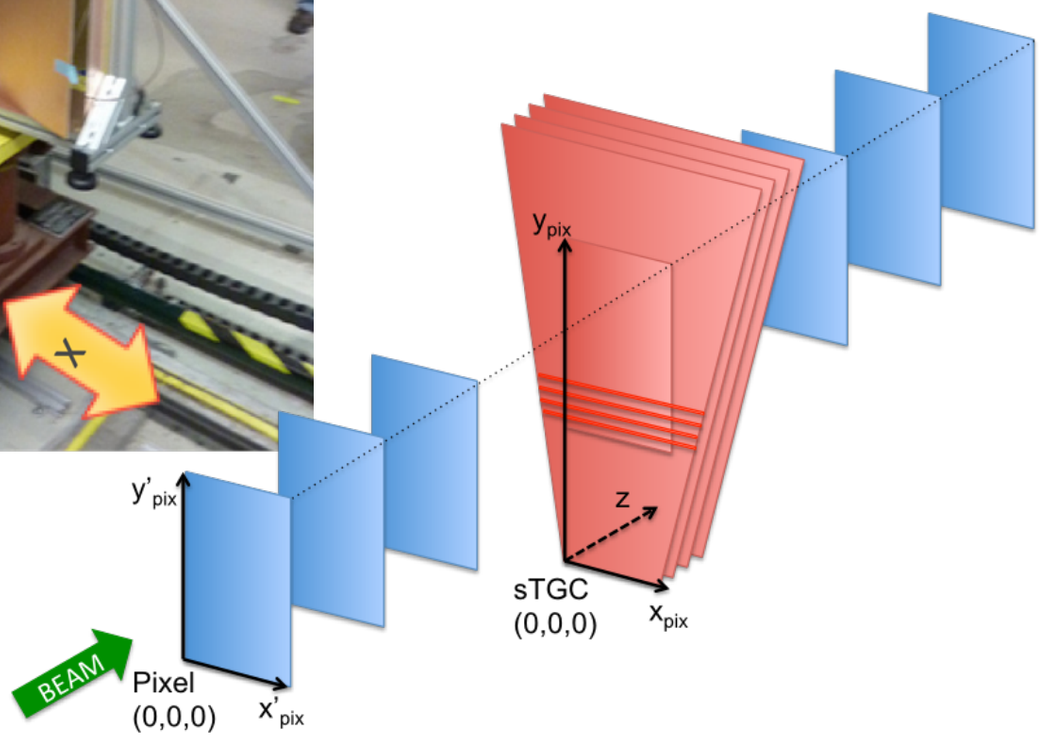
[2]G.Iakovidis - The Micromegas project for the ATLAS upgrade, JINST, C12007 (8),

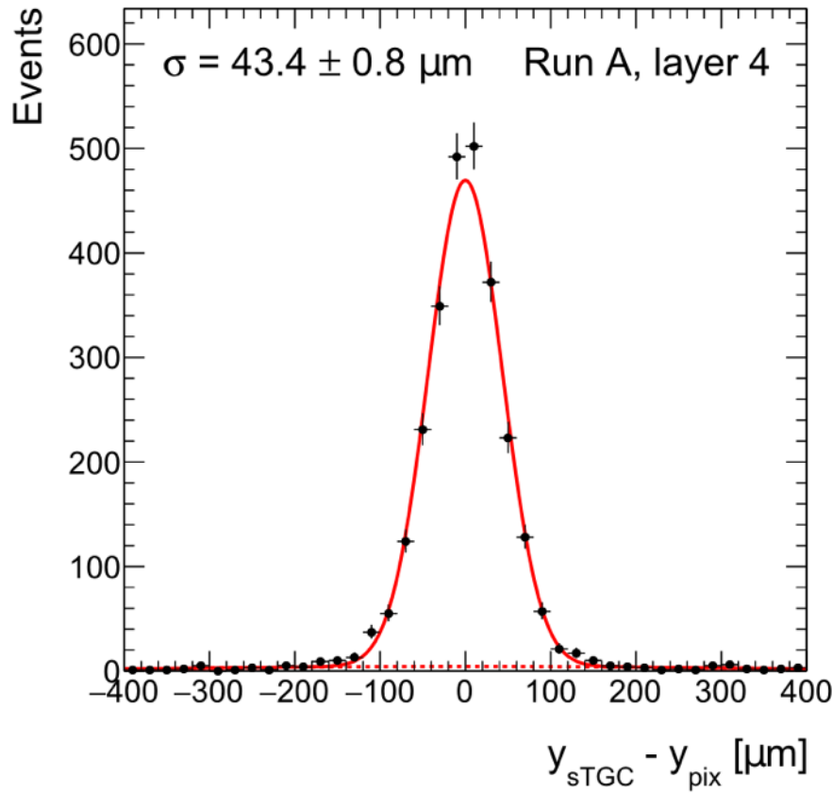
# Testing of sTGC large module with VMM1






- sTGC resolution measurement using a pixel telescope (3 + 3 pixel layers) at Fermilab
- Readout electronics VMM1
- First results of sTGC test beam for runs with sTGC quadruplet + pixel telescope
- Residual widths range from ~50 μm
- Neighbouring logic extensively tested and shows a great advantage



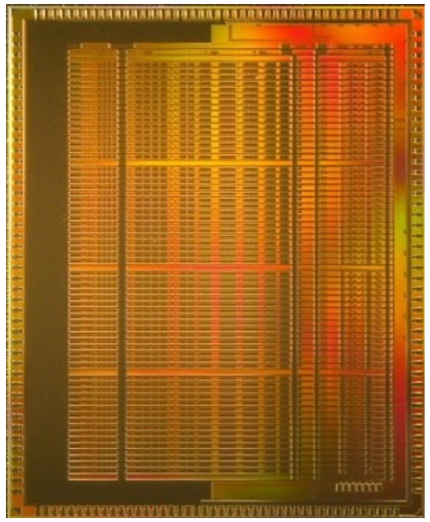

A. Abusleme et al "Performance of a Full-Size Small-Strip Thin Gap Chamber Prototype for the ATLAS New Small Wheel Muon Upgrade", Submitted to NIM: arXiv:1509.06329

# VMM2 - Second Version



**VMM2 is an extremely complex and ambitious ASIC, a planned redesign of VMM1 to bring us closer to the final fully digital VMM - an order of magnitude additional complexity**

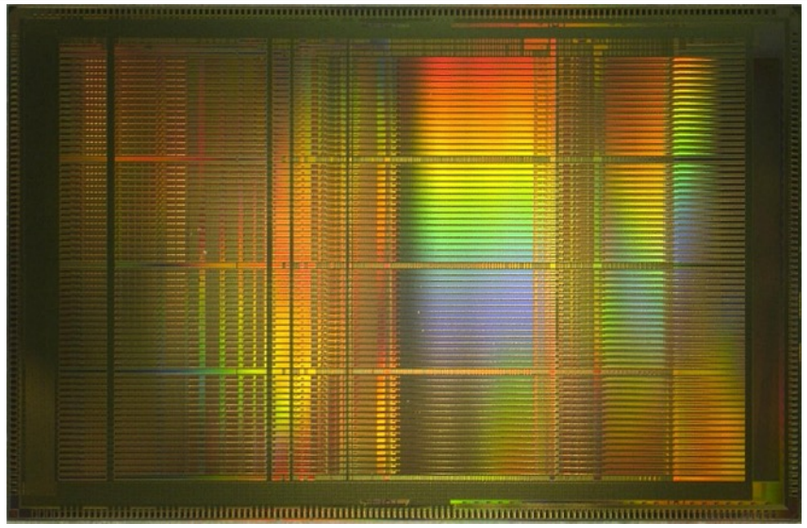
**Version 1**



**VMM1 (2012)**

- 50 mm²
- 500k MOSFETs (8k/ch.)
- a complex mixed-signal ASIC
- 2-phase readout
- extensively tested

**Version 2**



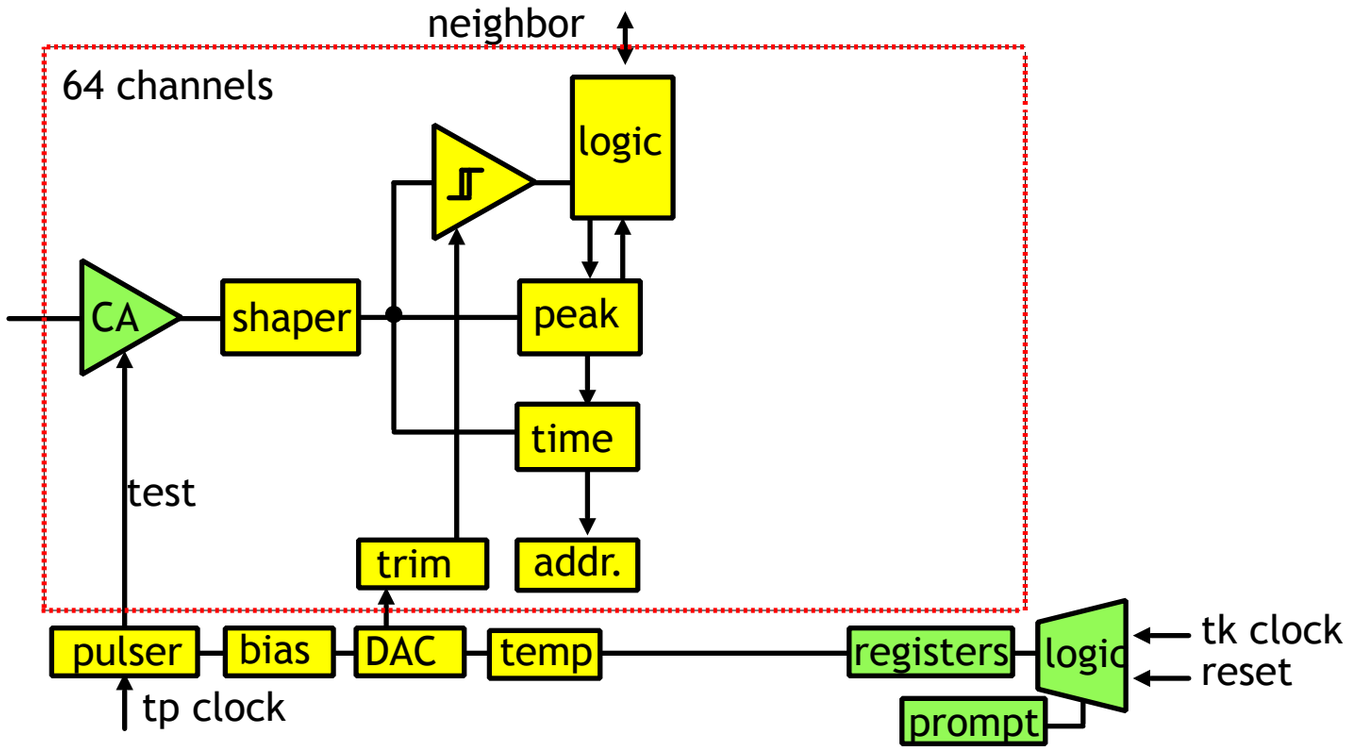
**VMM2 (2014) (currently under testing)**

- 115 mm²
- > 5M MOSFETs (>80k/ch.)
- Deep re-design of VMM1
- Higher functionality and complexity
- continuous fully-digital readout

G. De Geronimo - ''VMM2 - An ASIC for the New Small Wheel''.TWEPP 2014 - Topical Workshop on Electronics for Particle Physics.
https://indico.cern.ch/event/299180/session/4/contribution/45

# VMM2 - Second ASIC prototype in 2014

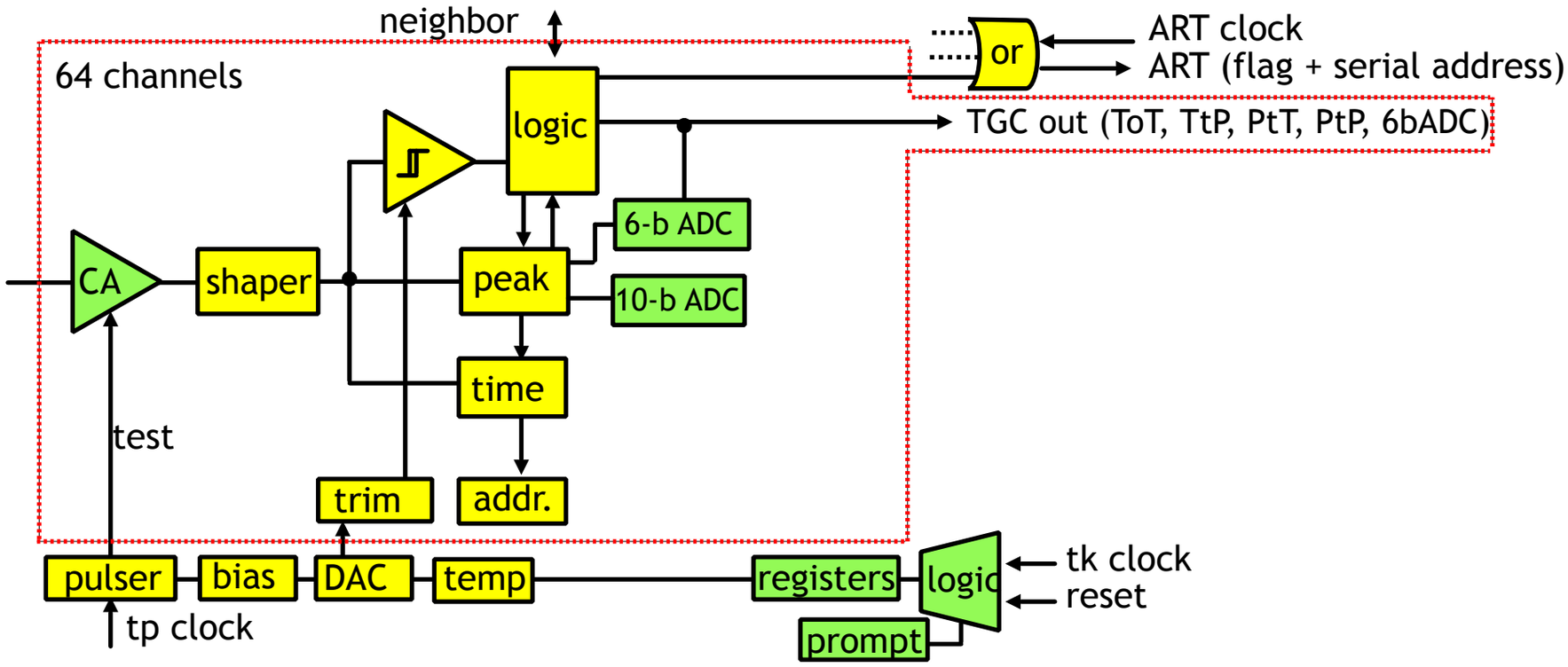





- All the bugs of VMM1 fixed plus additional functionality
- New Configuration logic registers: 80-bit + 24-bit / channel (1616bits)
- Charge amplifier: input transistor: PMOS 180 nm x 20 mm, 2 mA, adjustable gain 0.5, 1, 3, 4.5, 6, 9, 12, 16 mV/fC (max charge 2 to 0.06 pC)

# VMM2 - Second ASIC prototype in 2014



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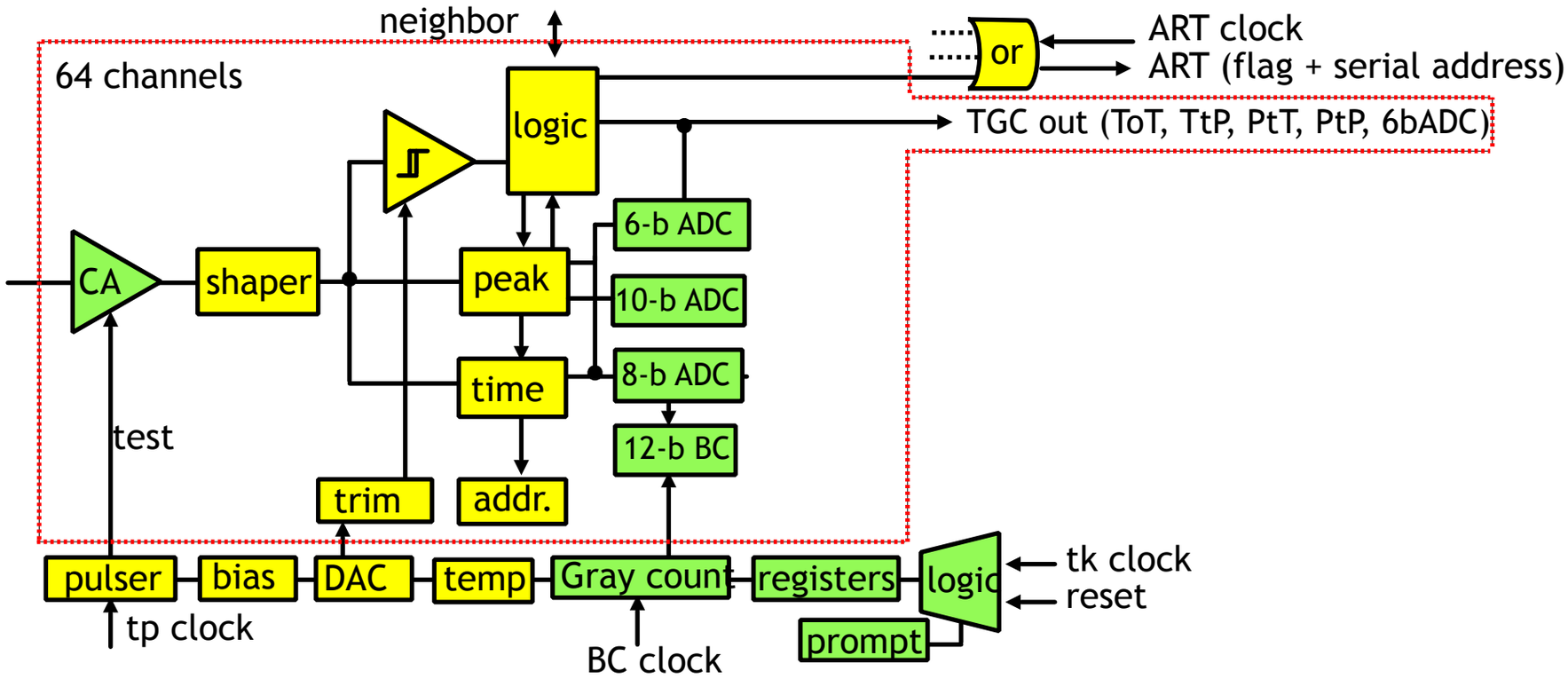
- Peak detector, measurement of the peak amplitude - ADC with current-mode domino architecture 10-bit , 200 ns , sub-mW, for peak amplitude conversion, adjustable conversion time and offset + 6-bit ADC with 25ns conversion time

# VMM2 - Second ASIC prototype in 2014

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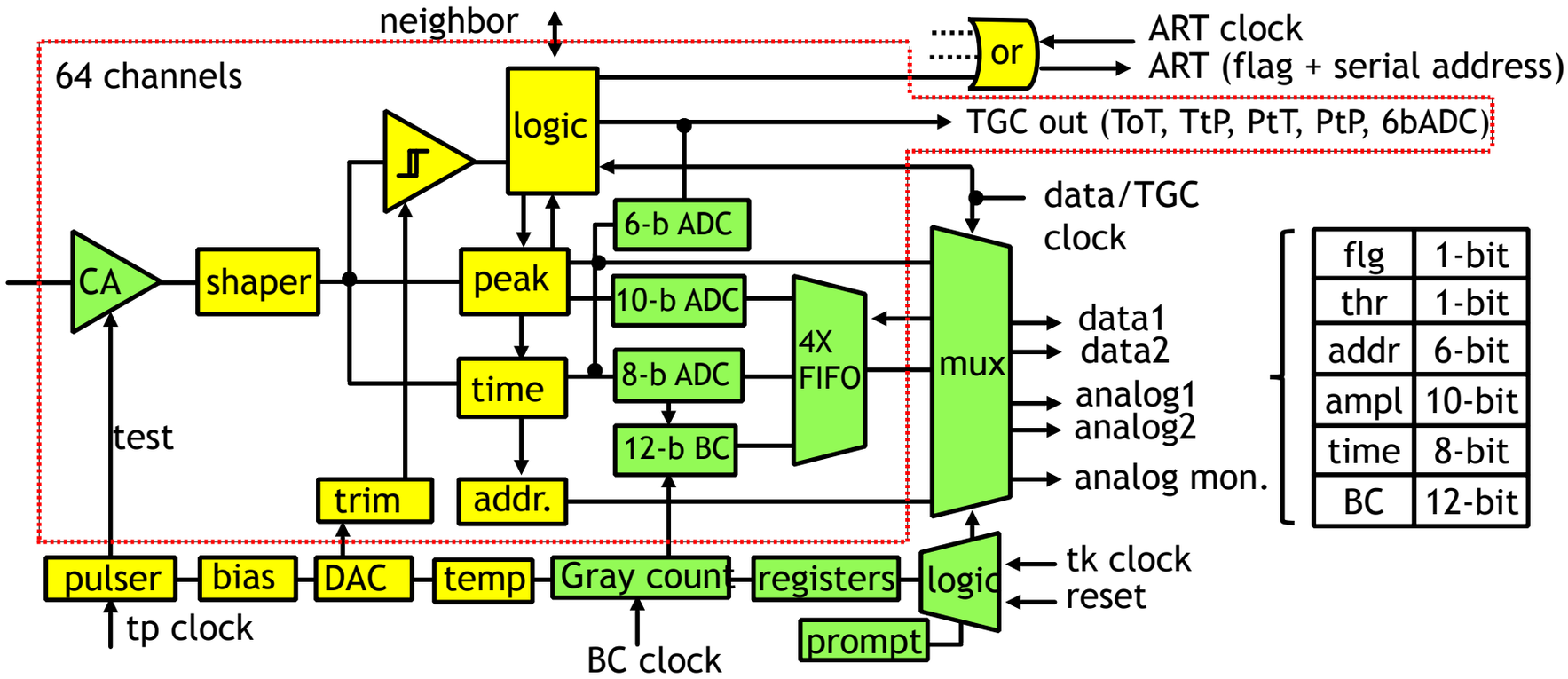
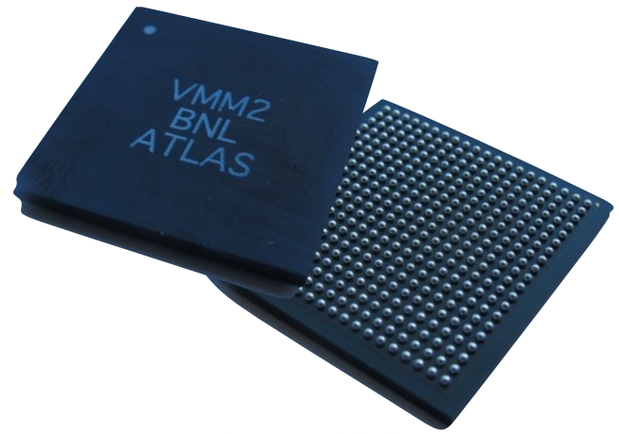
- Peak detector, measurement of the peak amplitude - ADC with current-mode domino architecture 10-bit , 200 ns , sub-mW, for peak amplitude conversion, adjustable conversion time and offset + 6-bit ADC with 25ns conversion time
- Time detector: sub-ns resolution measurement of peak time, 8-bit , 100 ns , same as the 10bit architecture - 12-bit timestamp: - from shared 12-bit Gray-code counter, external BC clock - Complete timing information of 20-bit
- ART: serial output of a flag+ address with a clock reception
- Logic: direct digital output per channel with additional outputs (ToT, TtP, PtT, PtP)

# VMM2 - Second ASIC prototype in 2014 (digital)






| | |
|---|---|
| flg | 1-bit |
| thr | 1-bit |
| addr | 6-bit |
| ampl | 10-bit |
| time | 8-bit |
| BC | 12-bit |




**custom 400-pin**

**21 x 21 mm² BGA**

**1mm pitch**

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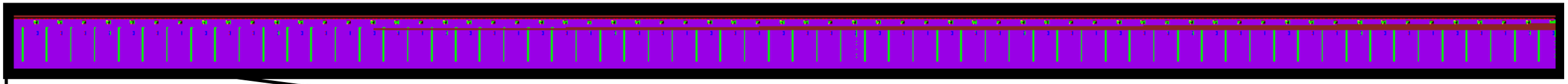
- New Configuration logic registers: 80-bit + 24-bit / channel (1616bits)
- Charge amplifier: input transistor: PMOS 180 nm x 20 mm, 2 mA, adjustable gain 0.5, 1, 3, 4.5, 6, 9, 12, 16 mV/fC (max charge 2 to 0.06 pC)
- Peak detector, measurement of the peak amplitude - ADC with current-mode domino architecture 10-bit , 200 ns , sub-mW, for peak amplitude conversion, adjustable conversion time and offset + 6-bit ADC with 25ns conversion time
- Time detector: sub-ns resolution measurement of peak time, 8-bit , 100 ns , same as the 10bit architecture - 12-bit timestamp: - from shared 12-bit Gray-code counter, external BC clock - Complete timing information of 20-bit
- ART: serial output of a flag+ address with a clock reception
- Logic: direct digital output per channel with additional outputs (ToT, TtP, PtT, PtP)
- 4-deep FIFO: threshold-crossing indicator, 10-bit ADC, 8-bit ADC, 12-bit BC
- Readout: 38bit event continuous self-reset operation fully digital continuous up to 200 MHz (additional to the 2 phase analog mode)
- PROMPT (courtesy of CERN): export regulations (ITAR) compliance circuit

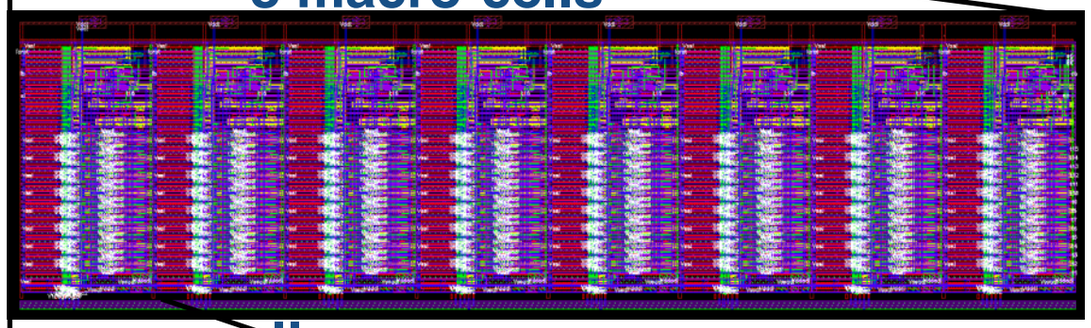
# 10-bit Current-Mode Domino ADC - Functionality



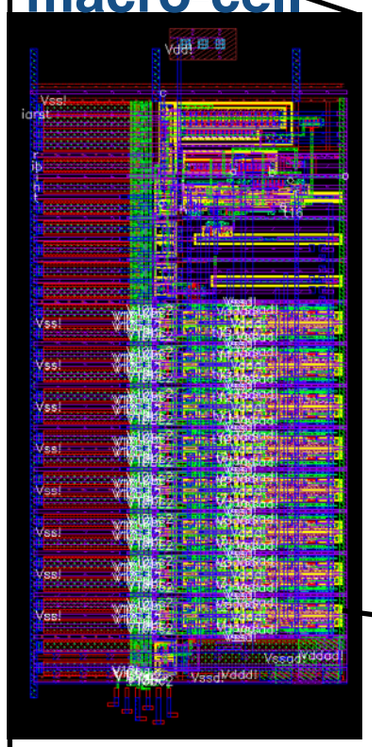
## ADC Cells



8 macro-cells

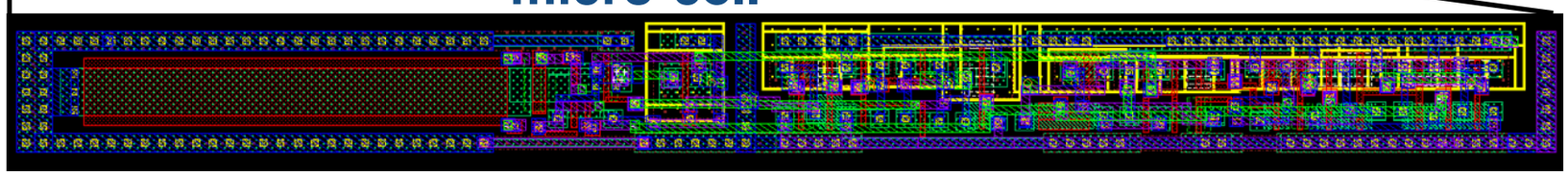


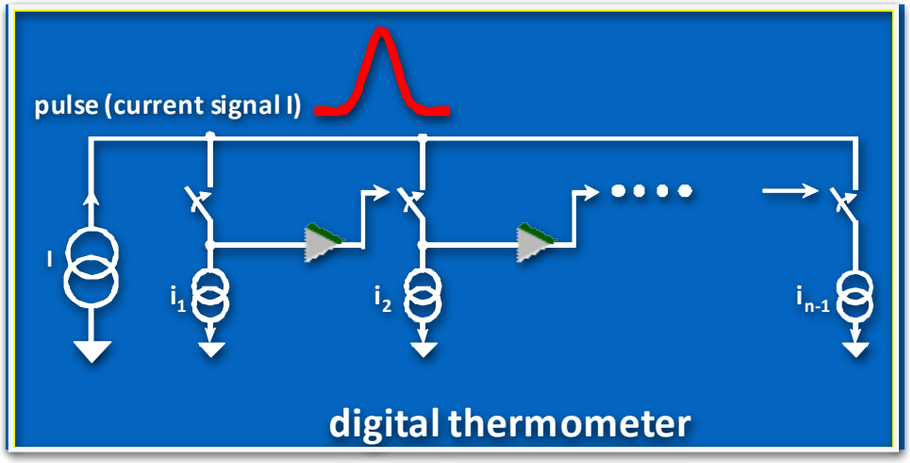
macro-cell



16x micro-cells

micro-cell

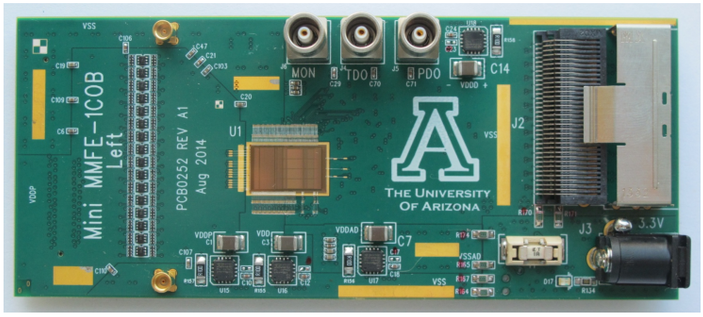





## ADC Core

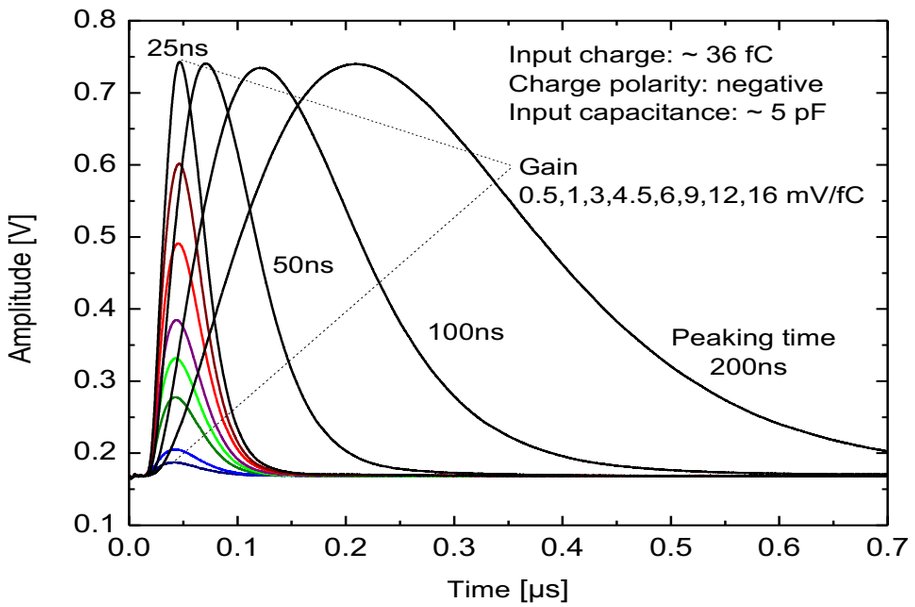
- 1024 shells current sources
- 64 macro-shells, 16 micro-shells each
- resulting current is compared to a current proportional to the peak amplitude
- 2 step mode - First the comparison identifies one of the 64 macro-cells (6 high order bits)
- Then on second step the lower 4 bits are identified

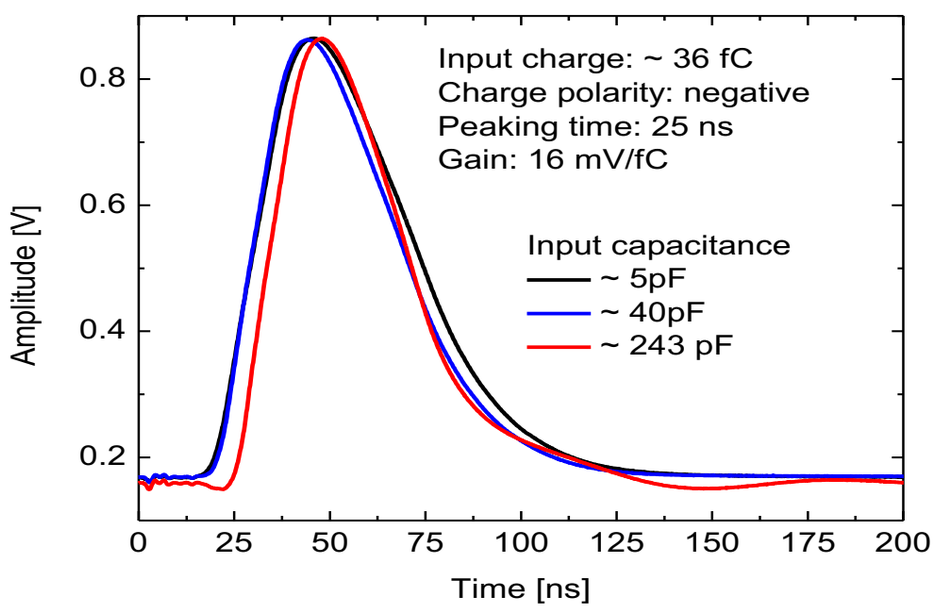
# VMM2 - Preliminary developments and testing

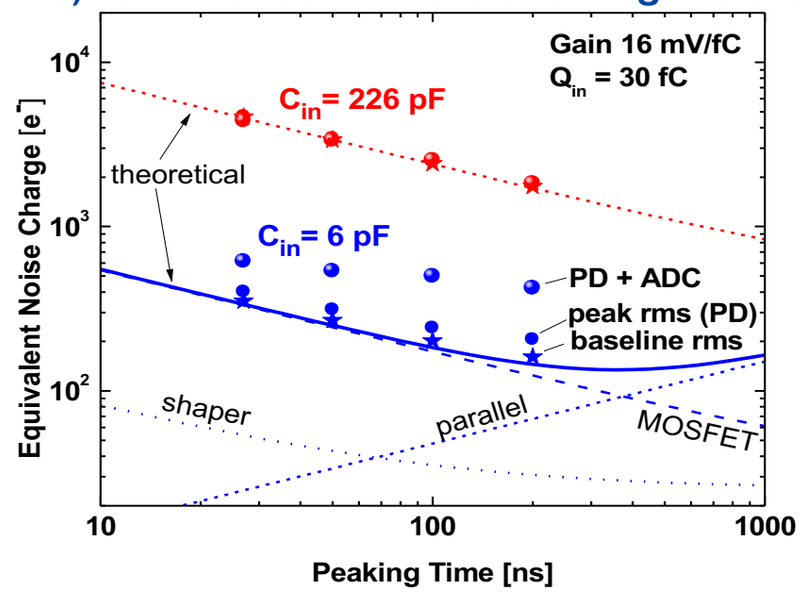


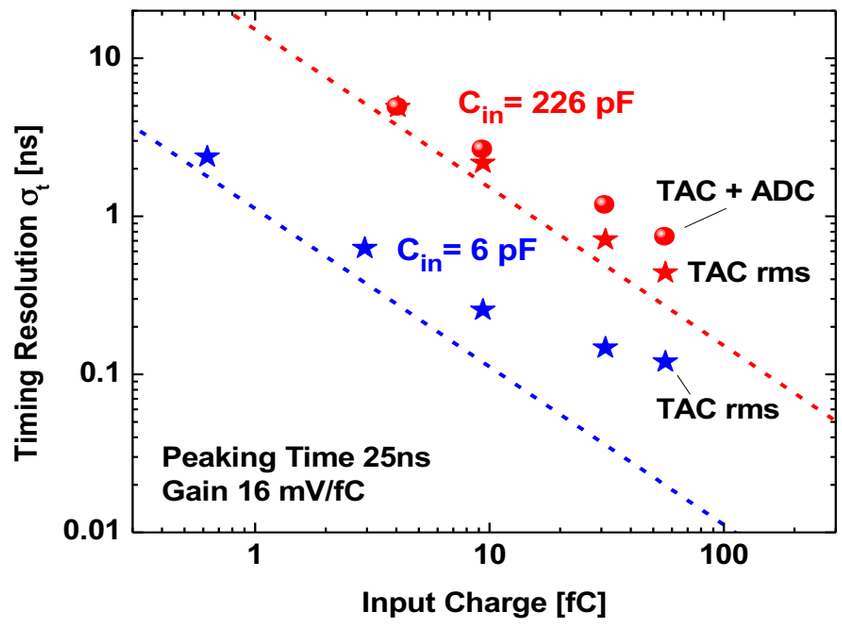



**Several board developments with 1x (ATLAS), 2x (RD-51 SRS), 8x (ATLAS) realised last months allowing the extensive testing**



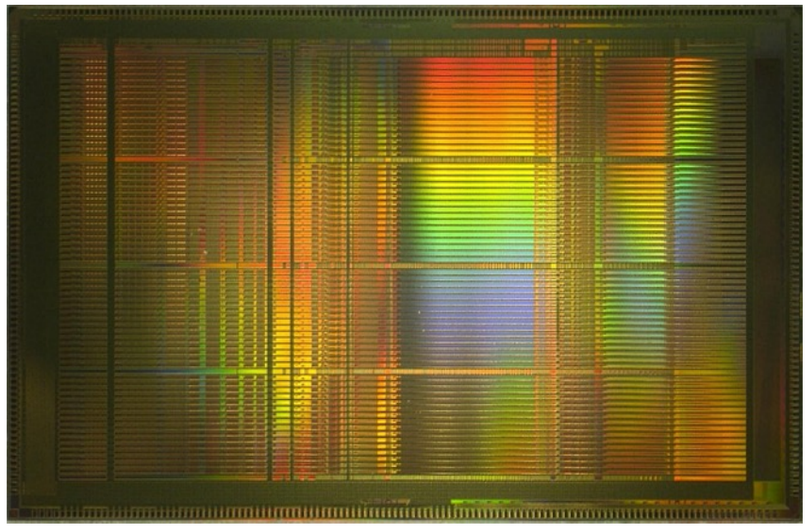



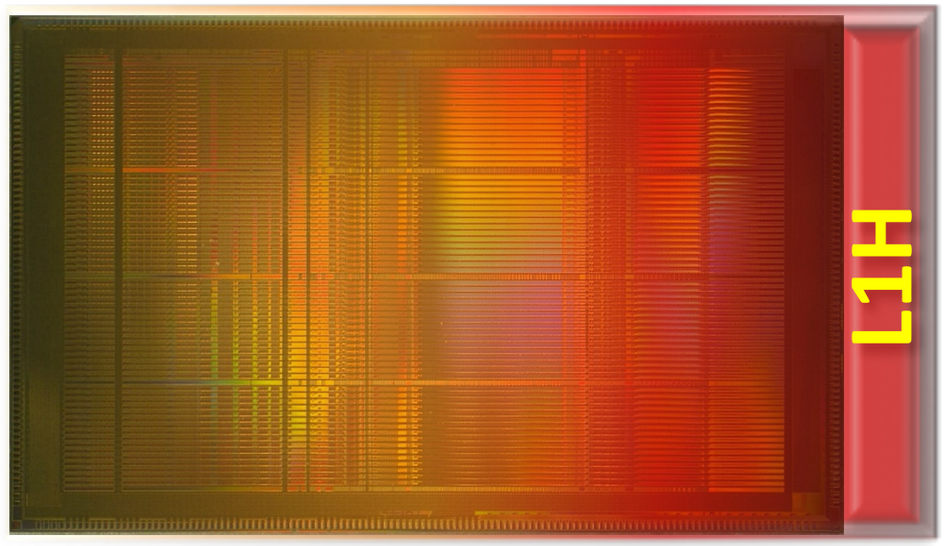



# Towards VMM3 (Submission Dec. 2015)

Version 2



Version 3




**VMM2 - Findings and fixes**

- Tail current in high capacitance detectors signals saturates charge amplifier and introducing a dead-time. (shaper is also affected)
- Locking may appear because of logic in 8-bit, 10-bit ADCs
- Data repetition due to token stuck
- Voltage drop and mismatch in current output of the peak & time detectors
- 6-bit direct output disabled by mistake in logic
- MSB accumulation in ADCs due to parasitics
- Most of the functionality appear to work fine
- All the issues are already understood and fixes are implemented in the VMM3 design

**VMM3 (design in progress - submission - Dec. 2015)**

- 130 mm²
- > 6M MOSFETs
- includes L1 handling and SEU-tolerant logic

Additional, changes, fixes

- Simultaneous direct- and multiplexed-operation
- SLVS I/Os 200mV, +/- 200mV
- input capacitance acceptance up to 2nF
- Trigger acceptance Level 1 handling and additional shared FIFO
- SEU mitigation circuits
- All the bug fixes from VMM2

# Conclusions



- VMM1 was a successful first version
  - ➡ Already a complex version
  - ➡ Many measurements and studies with detectors showed good performance
  - ➡ Very good noise levels for the needs of the ATLAS and not only detectors
- VMM2 is deep redesign of VMM1 that brings us closer to final VMM
  - ➡ Complex design (80k MOSFETs/ch.) with associated risks from the complex control logic
  - ➡ Performance of the novel ADCs and all functionalities under study
  - ➡ All the issues found in testing procedure were simulated and understood, fixes are implemented in the coming version
- VMM3 design is ongoing with additional functionality planned for fall 2015
  - ➡ Hopefully this version will be very close to the final
- Final VMM (probably close to VMM3) is planned for fall of 2016 and as all the previous versions will be under PROMPT (courtesy of CERN): export regulations (ITAR) compliance circuit

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*Thank You*

*Great electronics allow Great Detectors !*