Radiation hardness techniques for the digital parts of the chip pALPIDE

VI Scuola Nazionale
“Rivelatori ed elettronica per Fisica delle Alte Energie, Astrofisica, Applicazioni Spaziali e Fisica Medica”

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Outline

1. ALICE Upgrade Programme
2. ITS Upgrade
3. MAPS (Monolithic Active Pixel Sensors)
4. pALPIDE chip
5. DTU – digital parts development
6. Radiation Hardness techniques

ALICE

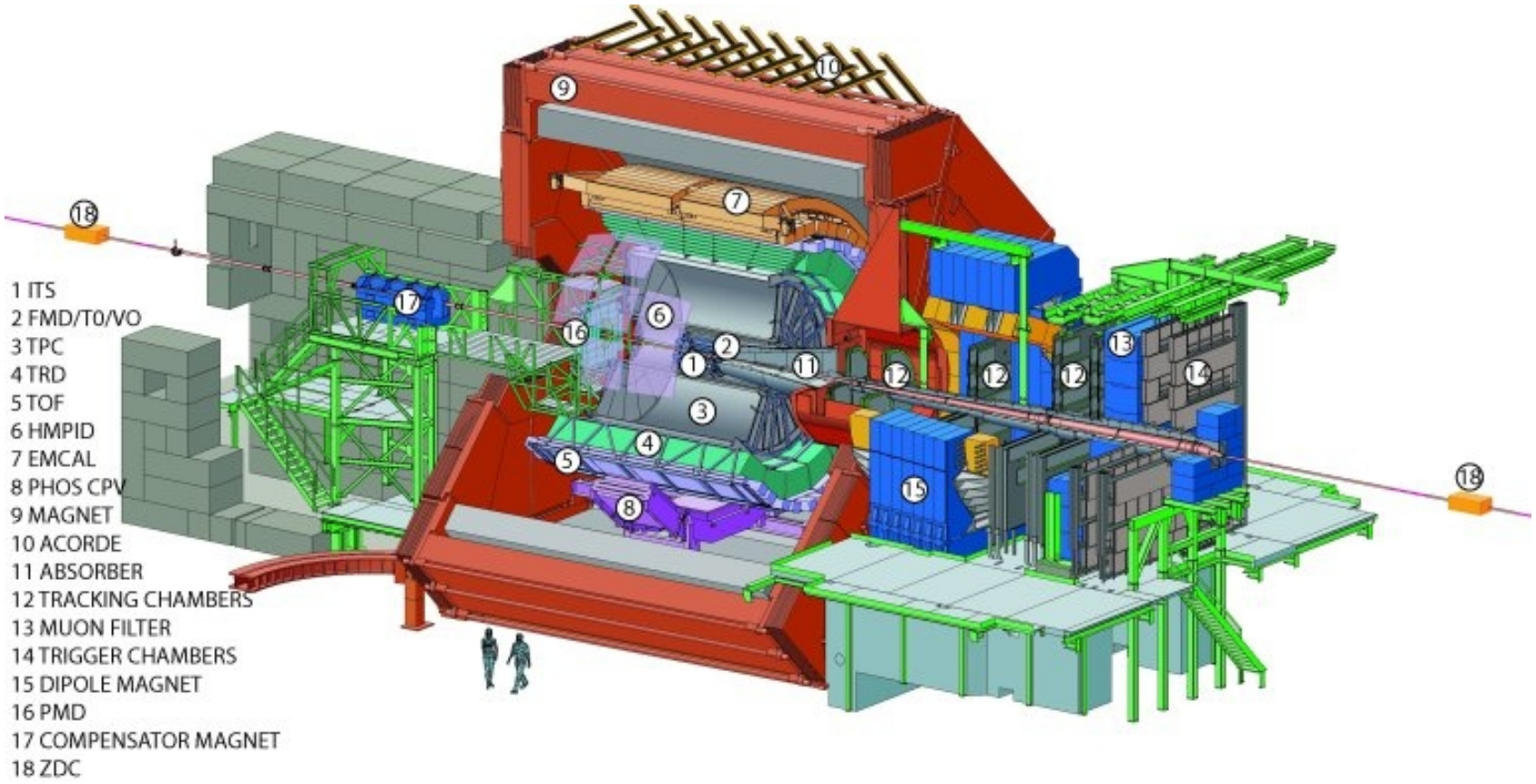
ALICE (**A Large Ion Collider Experiment**) is designed to address the physics of strongly interacting matter, in particular the properties of the **Quark-Gluon Plasma** (**QGP**), using proton-proton, proton-nucleus and nucleus-nucleus collisions at the **CERN LHC**.

The **ALICE apparatus** consists of a

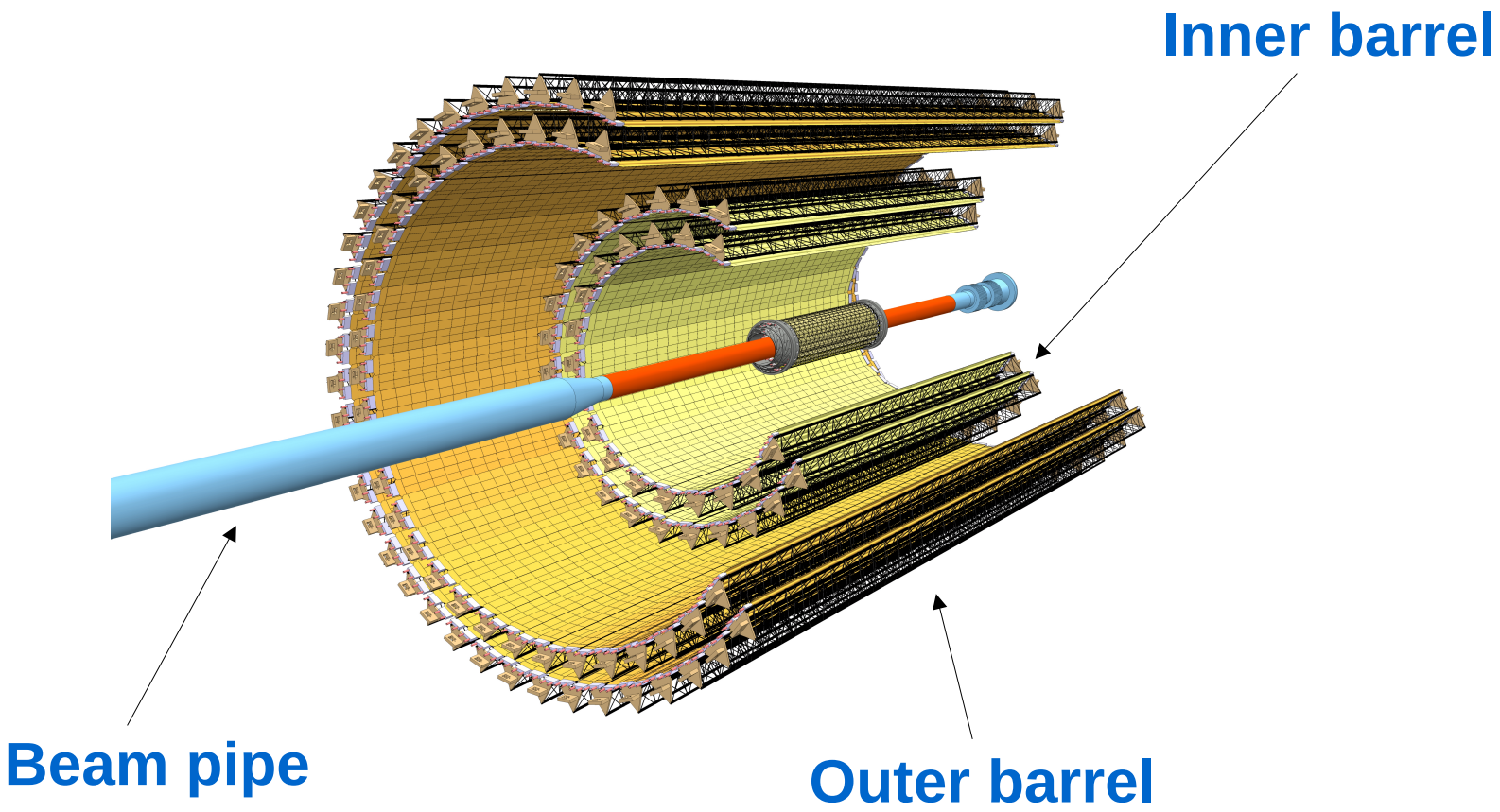
- central barrel
- a forward muon spectrometer
- a set of small detectors for triggering and event characterization.

The apparatus allows for a comprehensive study of **hadrons**, **electrons**, **muons**, **photons** and **jets** produced in **heavy-ion collisions**.

ALICE


1 ITS
2 FMD/T0/V0
3 TPC
4 TRD
5 TOF
6 HMPID
7 EMCAL
8 PHOS CPV
9 MAGNET
10 ACORDE
11 ABSORBER
12 TRACKING CHAMBERS
13 MUON FILTER
14 TRIGGER CHAMBERS
15 DIPOLE MAGNET
16 PMD
17 COMPENSATOR MAGNET
18 ZDC

ITS (Inner Tracking System)



ITS upgrade: key-features

- First detection layer closer to the beam line
  - → inner layer as close as possible (R = 2.2 cm)
  - → smaller beam pipe (R = 1.9 cm)
  - → smaller pixel size (20um x 20um)
- Less material budget
  - → thin sensors, thinner beam pipe (ΔR = 800 um),
  - → **7 layers of Monolithic Active Pixel Sensors (MAPS)**
- Lower power consumption and a highly optimized scheme for the distribution of the electrical power and signals
- Mechanics, cooling and other detector elements improved when compared to the present ITS design.

ITS upgrade: key-features

- High standalone tracking efficiency and resolution
  - → Increase granularity: 6 layers → 7 Layers
  - → Reduced pixel size (20um x 20um)
  - → increase radial extension: 39-430 mm → 22-500 mm
  - → Higher LHC luminosity: 6x1027 cm^{-2} s^{-1} → **Fast readout:** readout of Pb-Pb interactions at >50 kHz and pp up to 1 MHz
- Radiation level:
  - → 700 kRad → 1013 n_{eq}/cm^2 for the full integrated luminosity
- Fast access for yearly maintenance insertion/removal to maintain detector modules during yearly LHC shutdown

Particle sensors

The particle sensors and the associated read-out electronics for **HEP requirements**:

- granularity
- material thickness
- read-out speed
- power consumption
- radiation hardness

Silicon microstrip and **pixel sensors** (based on **CMOS** technology) are at the heart of the majority of particle tracking systems used in particle physics experiments today.

Interface between the sensor and the read-out electronics → typically separate components (**hybrid sensors** = sensors bump-bonded to the CMOS read-out electronics).

MAPS

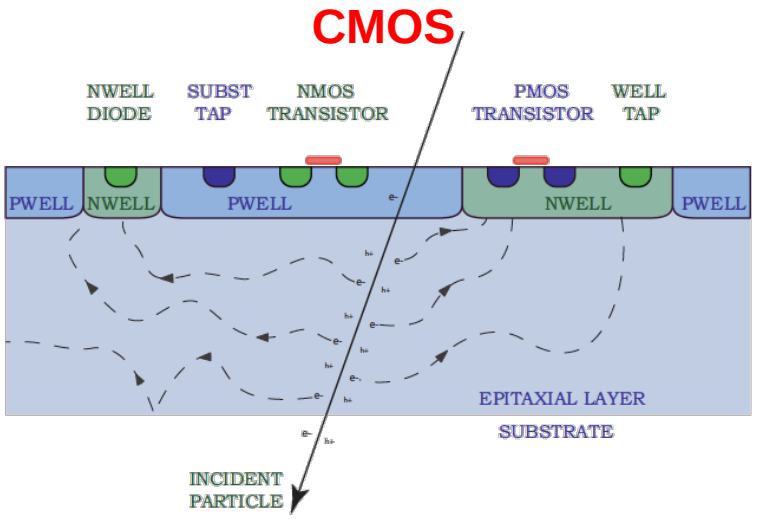
Go beyond technical limitations (higher granularity and less material thickness)

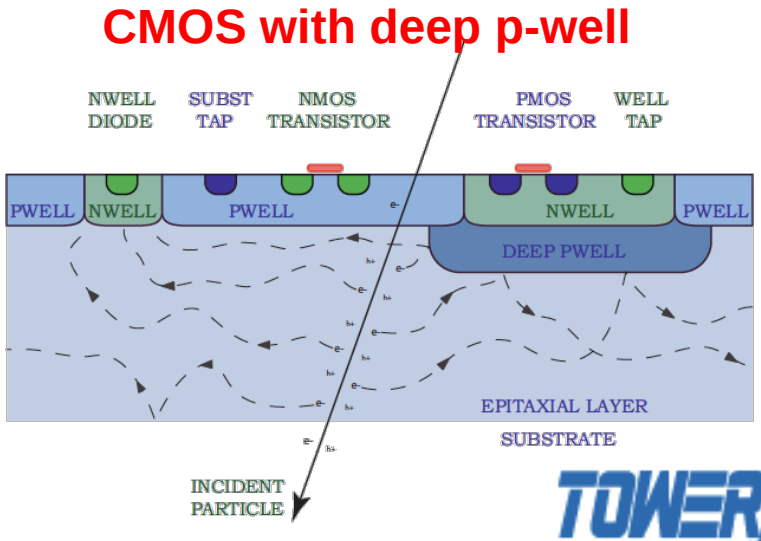
→ **CMOS Monolithic Active Pixels Sensors (MAPS)**

The technology can meet the majority of the requirements of such systems but there are some **limitations**:

- radiation tolerance
- moderate read-out time

Why Tower Jazz 180 nm?





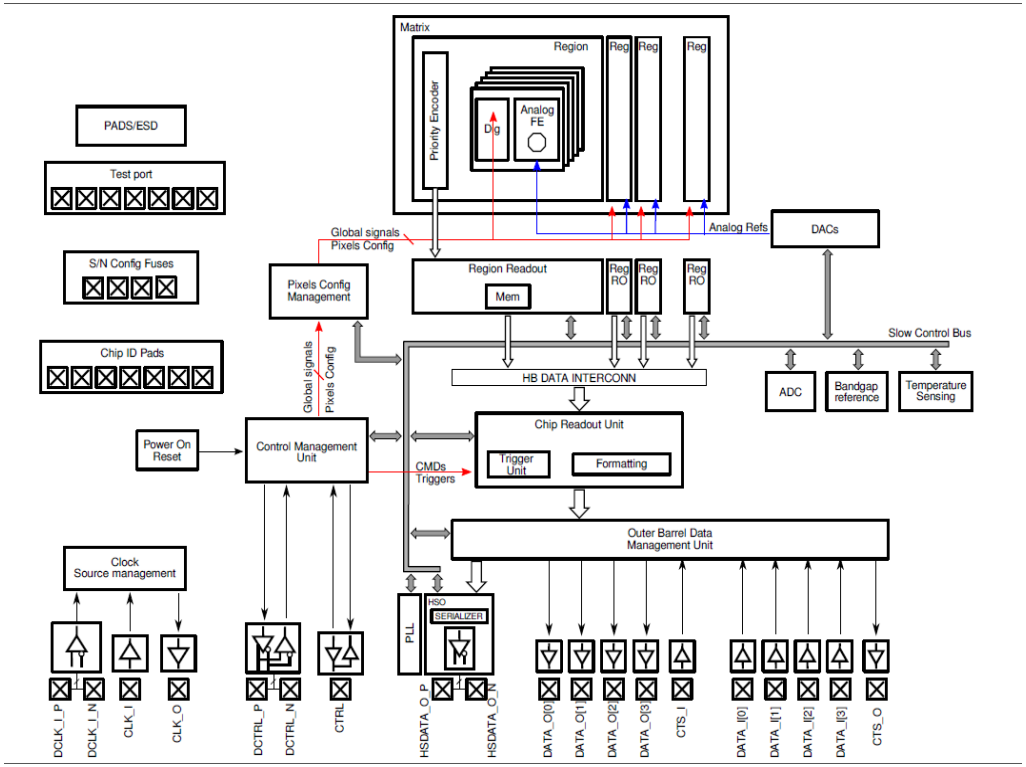
The **0.18 um CMOS** technology by **TowerJazz** has been selected for the implementation of the **Pixel Chip** for all layers of the new ITS.

- Development of monolithic detectors using Tower/Jazz 0.18 um CMOS technology:
- Improved TID resistance due to smaller technology node
- Available with high resistivity (1-5 kΩ·cm) epitaxial layer up to 40 um (substantial depletion at 1-2 V)
- Special quadruple-well available to shield PMOS transistors (allows in-pixel truly CMOS circuitry)

→ Study radiation hardness (TID and SEE)
→ Study/optimize charge collection performance and readout architecture

pALPIDE

pALPIDE (**prototype ALICE Pixel Detector**) is the first small-scale prototype matrix of ALPIDE:



It is designed to address the feasibility of both the analog front-end and the priority encoding scheme.

- It contains a 64-column, 512-row matrix with the ALPIDE front-end in 22um×22um pixels.
- It is read out by a global priority encoder circuit.

DTU

The **Data Transmission Unit (DTU)** provides a fast serial link for the transmission of the data from the pixel chip.

It represents the **unique design for both versions of the internal architecture** (MISTRAL – rolling shutter / pALPIDE ASIC– Priority encoder).

The DTU works in two different environments :

- **Inner Barrel (IB)** : each chip transmits its data over a differential serial line with a line rate of 1.2 Gb/s to a UDC (FPGA-based data concentrator). Data are transmitted over a aluminum over kapton FPC (Flexible Printed Circuit) with a maximum length of 300 mm and then to a micro-coaxial cable over a maximum length of 5 m.

- **Outer Barrel (OB)** : each half module has a master chip which receives the data of 6 chips and send the data over a serial line with a line rate of 400 Mb/s to a UDC. Data are transmitted transmitted over a copper over kapton FPC with a maximum length of 1.5 m, again followed by 5 m of micro-coaxial cable.

DTU

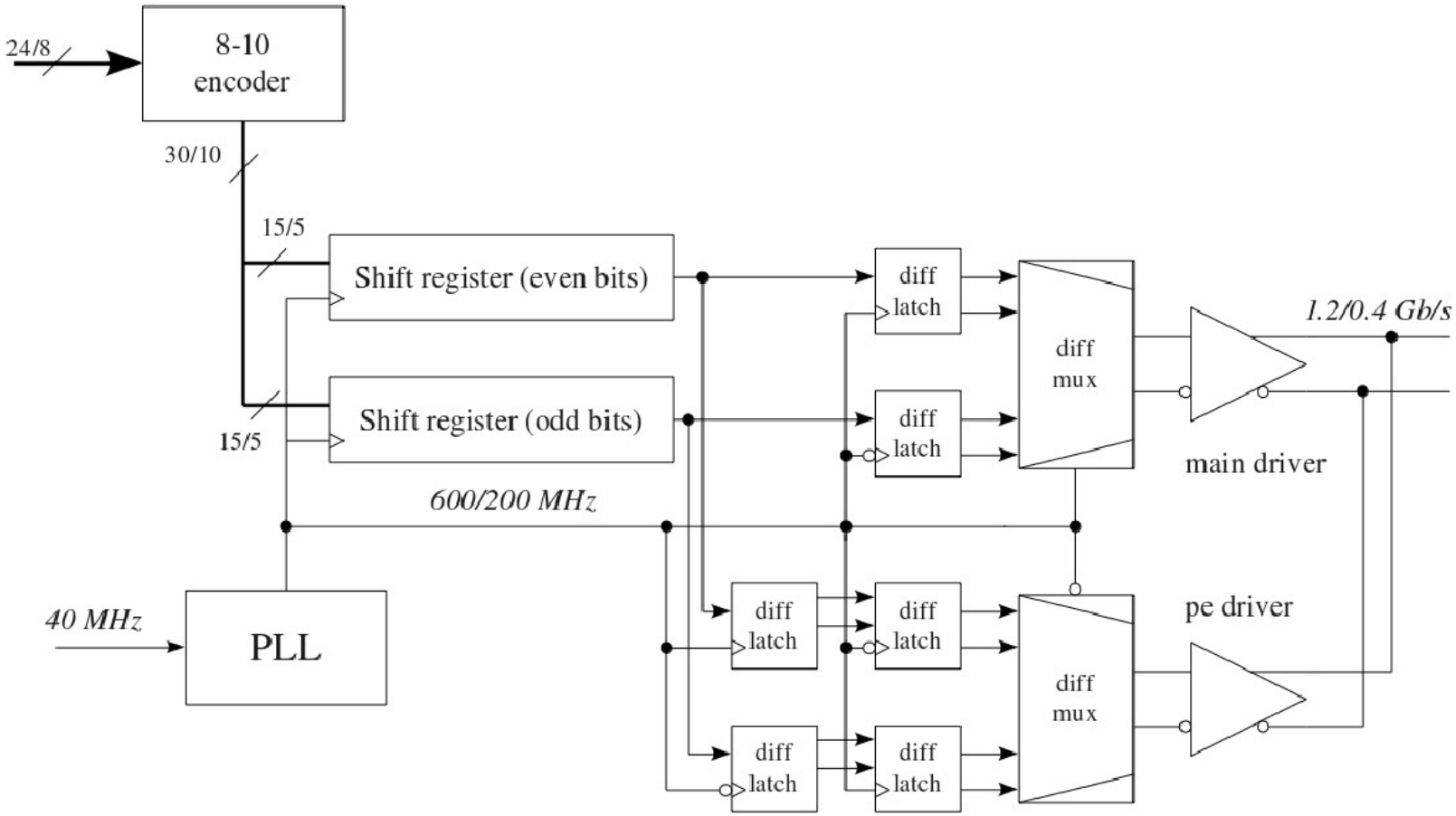
The DTU architecture is based on a **Double Data Rate (DDR)** transmissions scheme.

An **8b/10b-encoder** is connected to two half size **shift registers** (for odd and even bits) which are synchronized on opposite edges of the transmission clock by two differential latches and connected to a main driver via a multiplexer controlled by the transmission clock itself.

A secondary path, equal to the main one but with two extra delay latches drives a second driver in order to provide pre-emphasis. The 600 MHz and the 200 MHz transmission clocks are generated from the 40 MHz system clock via a PLL.

The 1.2 Gb/s line rate, combined with the 8b/10b-encoder gives a data rate of 960 Mb/s for the IB, while the 400 Mb/s line rate gives 320 Mb/s for the OB. Assuming that the input bus is organized in bytes and the clock frequency is 40 MHz, this implies that the number of bytes processed per clock cycle is 3 for the IB and 1 for the OB.

DTU


24/8
8-10
encoder
30/10
15/5
Shift register (even bits)
15/5
Shift register (odd bits)
600/200 MHz
40 MHz
PLL
diff
latch
diff
mux
1.2/0.4 Gb/s
main driver
pe driver

8B/10B encoder

In order to transfer data over a **high-speed link**, in this kind of encoding algorithm the data stream is encoded prior the transmission and then decoded upon reception.

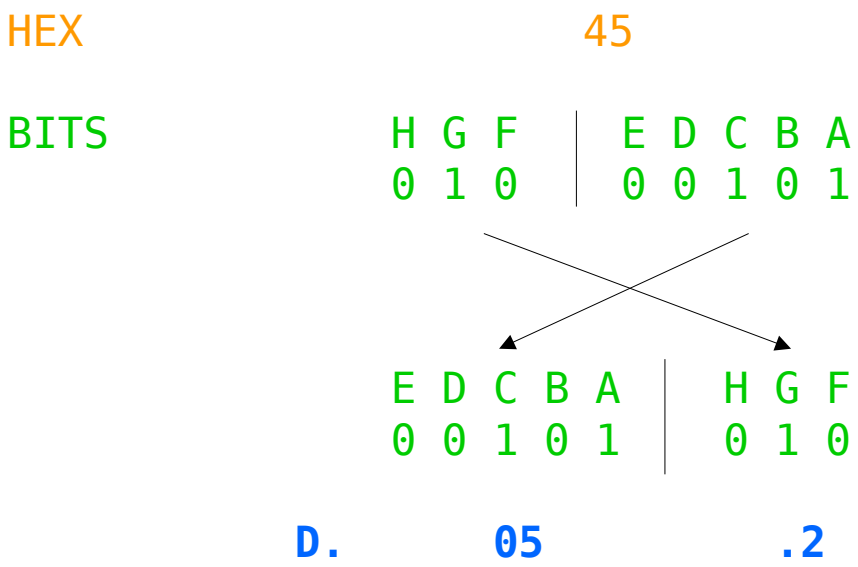
8B/10B encoding maps **1-byte** data into **10-bits** data and its mechanism, in which the difference between the number of ones transmitted and the number of zeros transmitted is always limited to +/-2 and at the end of each symbol, it is either +1 or −1 (this difference is known as the *running disparity*) ensures a DC-balanced transmission.

Since it is **DC-balanced**, the long-term ratio of ones and zeros transmitted is 50%.

The 8B/10B encoding patent (IBM, 1983) is by Al Widmer and Peter Franaszek.

8B/10B encoder

NOTATION

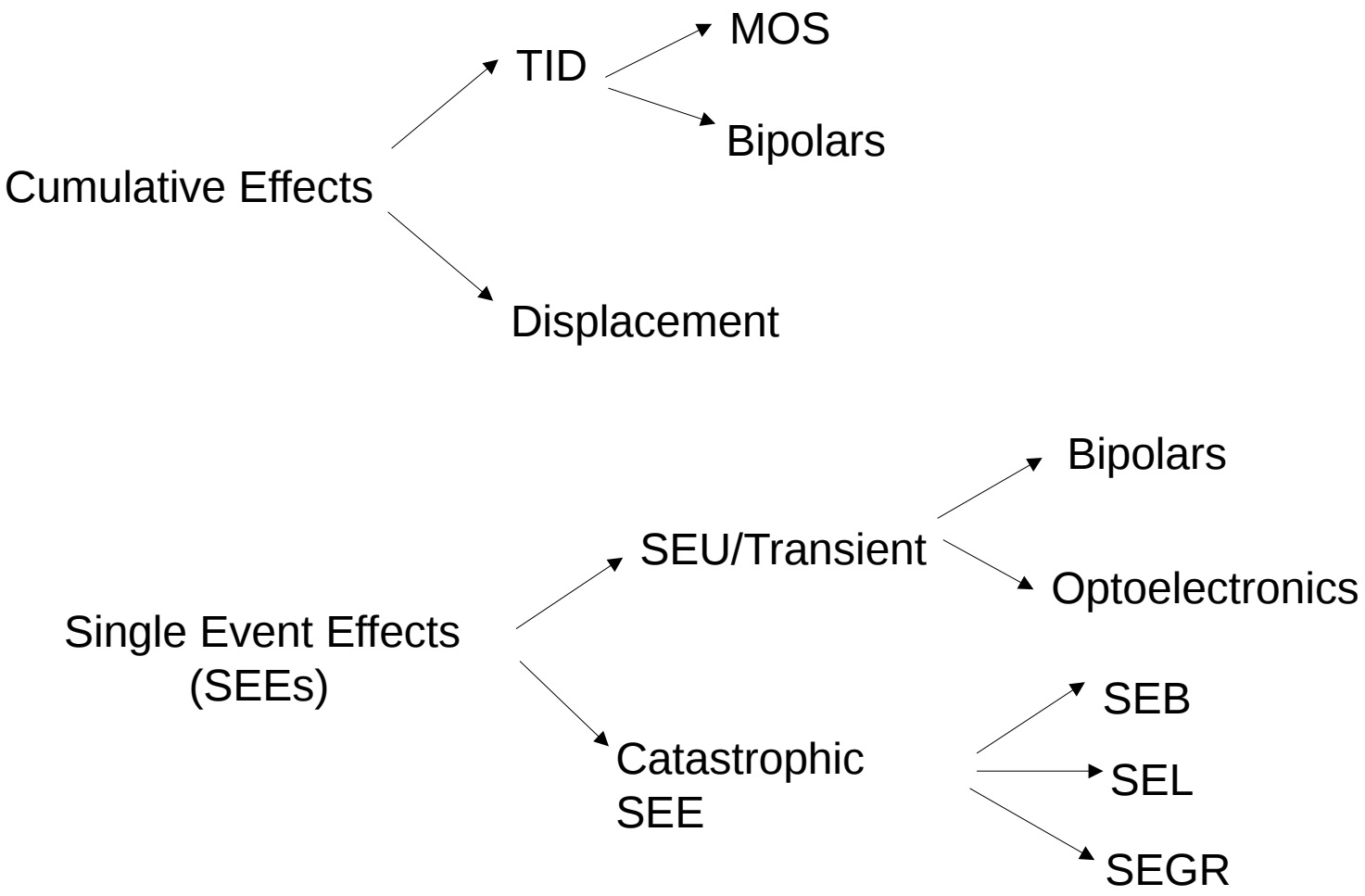


TRANSMISSION ORDER 8B/10B

A B C D E i F G H j
a b c d e i f g h j
1 0 1 0 0 1 0 1 0 1

(Bits I and j based on **running disparity**)

Radiation damages

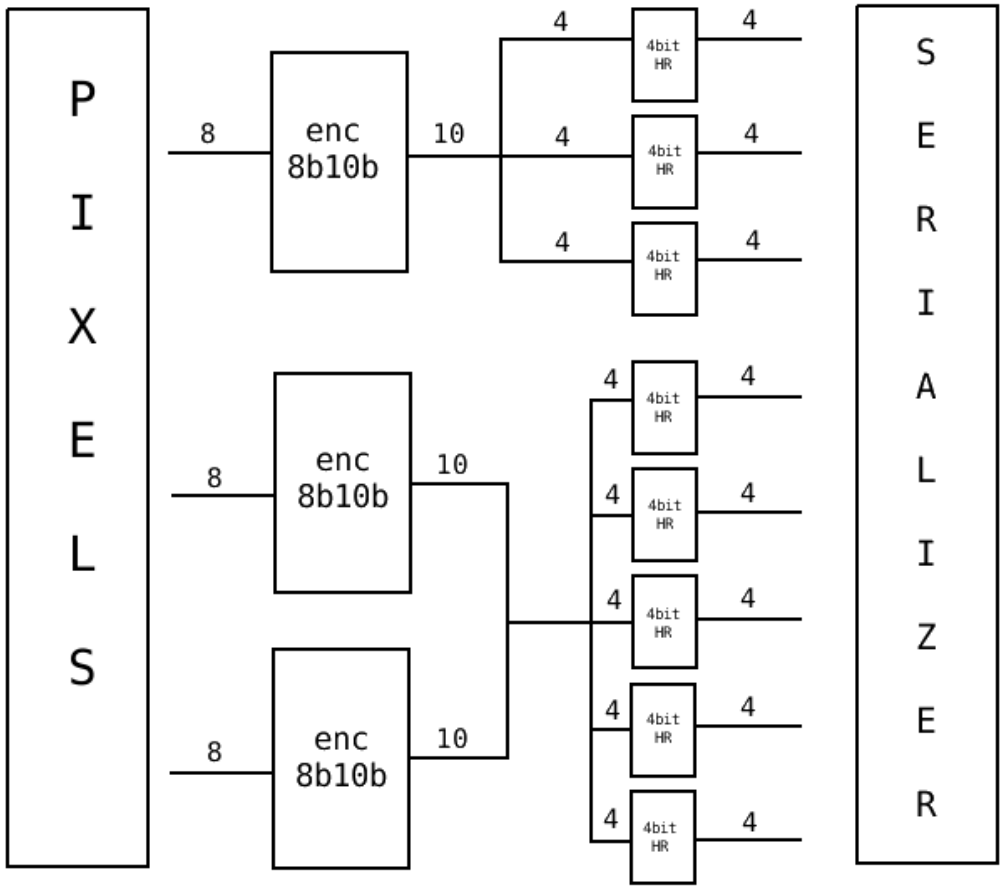


Via F. Faccio scheme

Rad-hard techniques: 8bit/10bit encoder

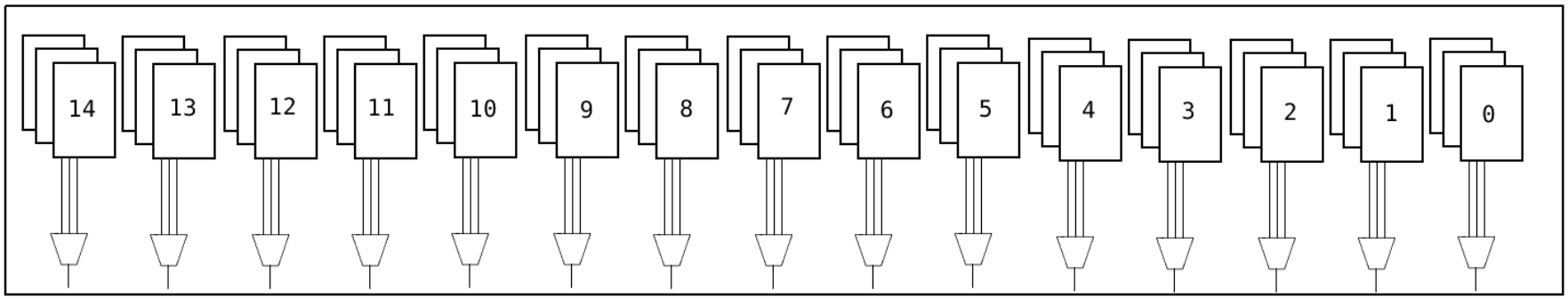
- Digital flow **from VHDL code to final layout** (GDSII for the foundry)
- Need of three 8B/10B encoders (24 input bit, 30 output bits);
- Two different modes:
    - **slow mode (OB)** by using only one encoder
    - **fast mode (IB)** by using all the avaiable encoders
- Use of eight **4-bit Hamming Registers** (G. A. Rinella VHDL models) to permit to choose between the slow mode by using only one encoder and only three Hamming Registers (2 bits are not used) and the fast mode by using three encoders and all the eight Hamming Registers.
- Every Hamming Register is a 4-bit storage register with hamming encoding using **canonical Hamming(7,4) coding**. Single bit flips are synchronously self-corrected. Double bit errors will also be silently processed but a valid correct result is not ensured and their output set to 1111 on reset asserted.

Rad-hard techniques: 8bit/10bit encoder



Rad-hard techniques: serializer

- Two 15-bits registers (one for the odd data and another one for the even data) → 30-bits serializer
- **Triple redudancy** of every flip-flop of the register → 90 flip-flops in total
- One voter for every triple flip-flop
- **Voting mechanism** (if two entries of three are equal, their value is the one chosen)



Chip development

Since end 2011:

- 4 MPWs
- 4 engineering runs

Two internal pixel chip architectures:

- ALPIDE
- MISTRAL.

Small scale prototypes for sensor optimization and radiation tolerance verification.

Full scale prototypes recently fabricated: lab and beam tests ongoing also on:

- irradiated
- thinned (50 um) devices
- thinned devices mounted on flex

Thank You

Backup slides

Pixel chip architecture

MIMOSA (IPHC Strasbourg) – baseline (most mature and advanced)
- Rolling shutter with in-pixel CDS, column-level discriminator, 2 rows parallel RO
- Integration time: 30 us
- Power ≤ 400 mW / cm^2 (ANALOG+DIGITAL)

CHERWELL: Parallel Rolling Shutter (RAL)
- Based on previous development.
- Integration time: ~40 us
- Power < 200 mW / cm^2

EXPLORER: In-pixel discriminator + data driven readout (CERN)
- shaping time ~2 us, readout time ~4 µs;
- Power ~100 mW / cm^2 (ANALOG ONLY)

SENSOR OPTIONS
- collection electrode geometry
- pixel dimensions/shape etc…

READ-OUT OPTIONS
- Priority encoder
- Orthopix
- Parallel rolling shutter

Timeline

2012–2014 R&D

- 2012 evaluation of technologies & prototypes
- 2013 selection of technologies, eng. Design, TDR
- 2014 final design and validation

2015-18 Construction and Installation

- 2015-16 production, construction and test of detector modules
- 2017 assembly and pre-commissioning
- 2018 installation in the cavern