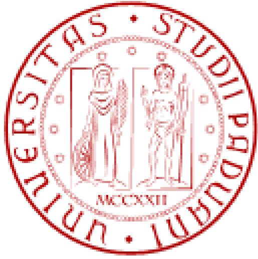

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Radiation vulnerability in 65 nm CMOS I/O transistors after exposure to Grad dose

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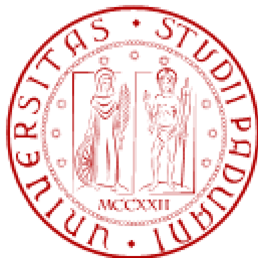


DIPARTIMENTO DI FISICA E ASTRONOMIA 'GALILEO GALILEI'

Outline

- Introduction
- Experiment and devices description
- Results and discussion
- Conclusion

Introduction

- Requirements for electronics implemented in LHC upgrade
  - 1 Grad(SiO_2) target for 10 years after upgrade
  - 65 nm CMOS technology as a strong candidate
- Two commonly used device types for modern CMOS IC:
  - Standard regular threshold voltage MOSFETs (RVT or core MOSFETs)
  - Thick oxide MOSFETs, for I/O or analog applications (I/O transistors)
- Enhanced TID susceptibility in I/O devices has been reported
  - What about the radiation vulnerability of 65 nm I/O transistors at Grad dose?

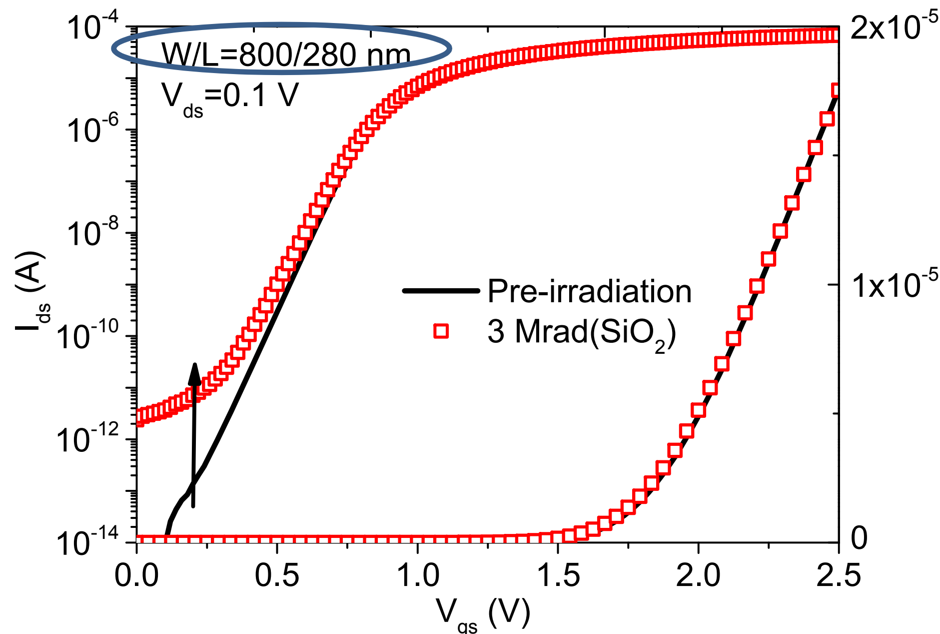
Experiment and devices description

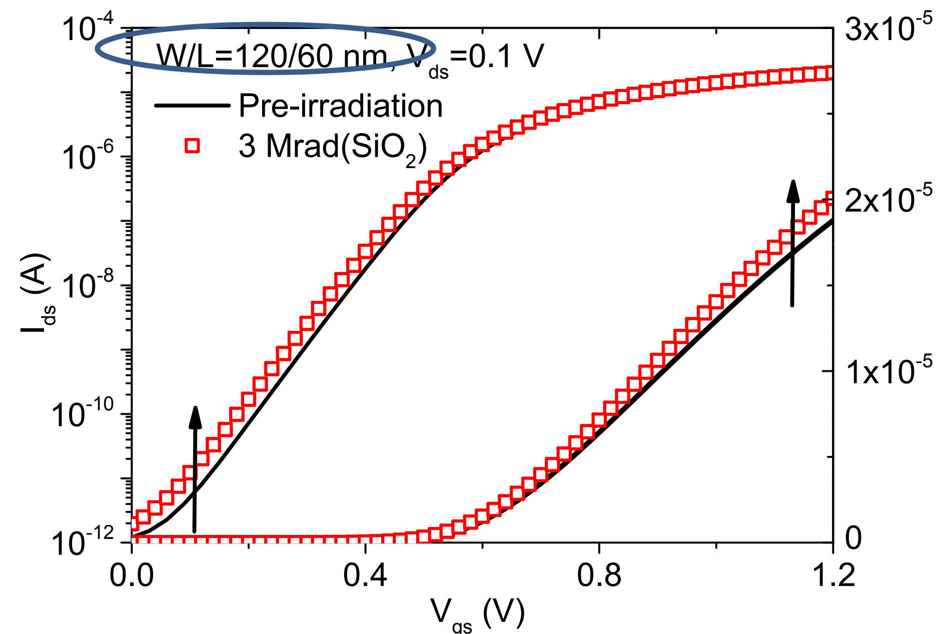
- Bulk devices used in this study
  - I/O nMOS & pMOS transistors in commercial 65 nm technology (~5 nm gate oxide; 2.5 V supply voltage)
  - Core nMOS transistor for comparison (2.5 nm gate oxide; 1.2 V supply voltage)
- Experiment description
  - 10 keV X-ray at INFN- Laboratori Nazionali di Legnaro, Padova
  - 1 krad(SiO_2)/s dose rate, 2 weeks to reach 1 Grad(SiO_2)
  - Bias during irradiaiton:

    1) nMOSFET: V_g=V_{dd}, other terminals grounded

    2) pMOSFET: all terminals grounded

Results and discussion: I/O nMOSFET

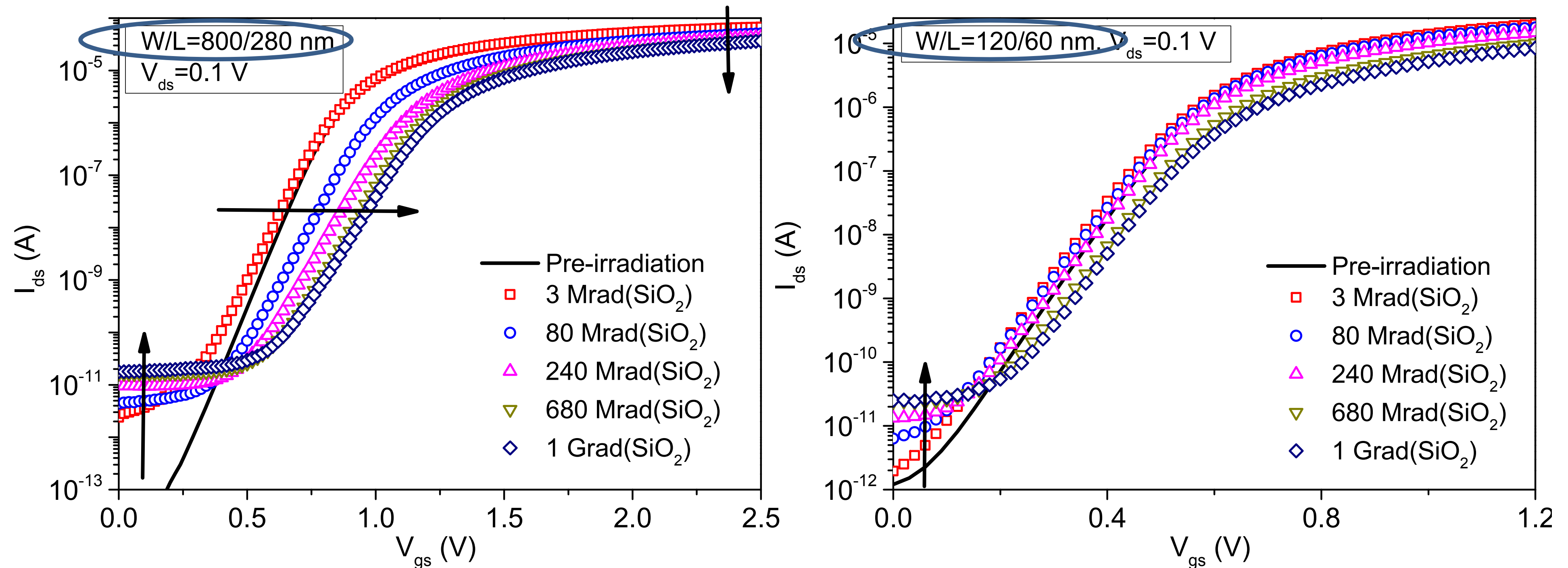




- ***I_{ds}-V_{gs} curves*** of I/O nMOSFET (800/280 nm) and core nMOSFET (120/60 nm) ***before and after 3 Mrad(SiO_2)***.

- Increase in off-state leakage and increase in on-state current were observed, consistent with previous reports at this comparatively low dose range.

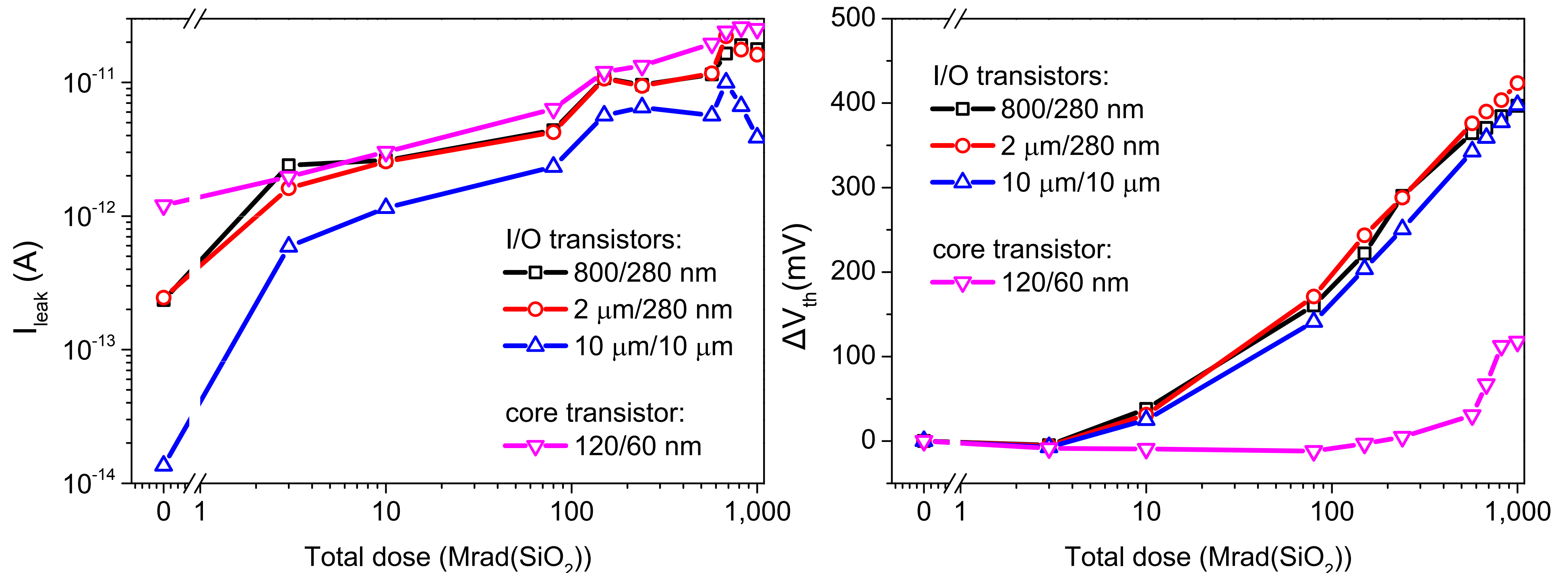
Results and discussion: I/O nMOSFET



- ***I_{ds}-V_{gs} curves*** of I/O nMOSFET (800/280 nm) and core nMOSFET (120/60 nm) ***at doses up to 1 Grad(SiO_2)***.

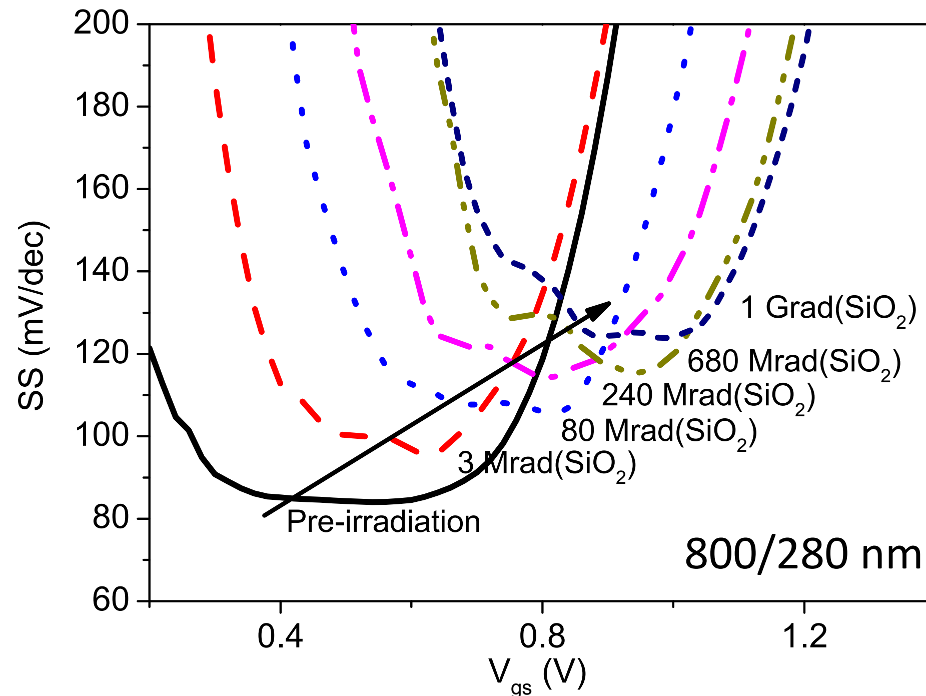
- Stronger degradation was observed in I/O nMOSFET, especially at the threshold voltage shift and drain current decrease.

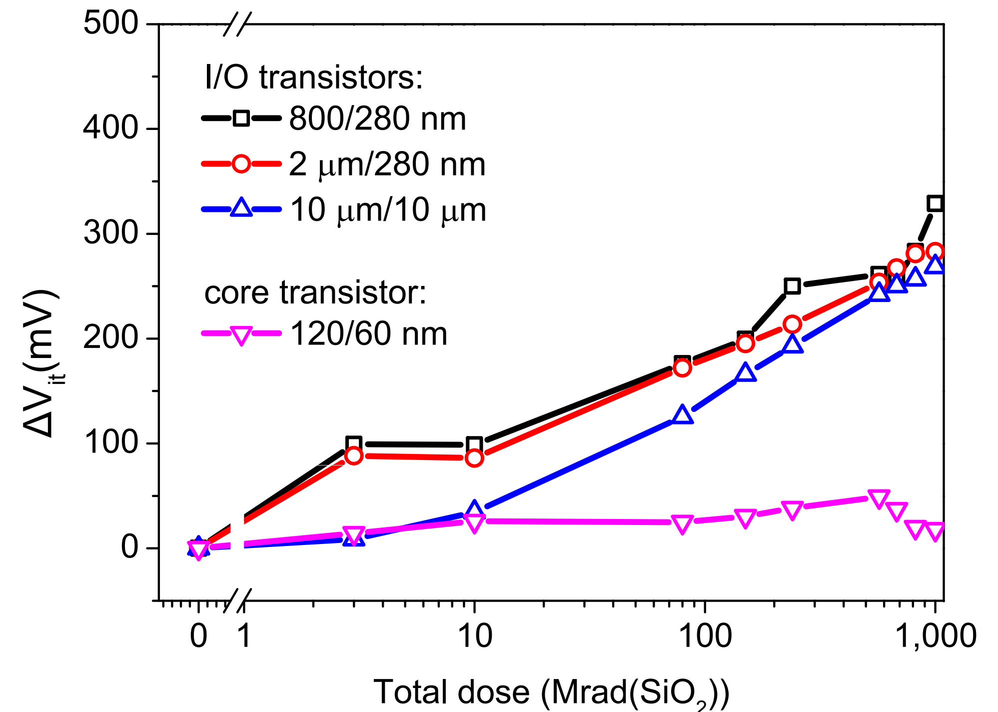
Results and discussion: I/O nMOSFET



- ***Evolution of off-state leakage and threshold voltage shift*** of I/O nMOSFETs and core nMOSFET (120/60 nm) ***with TID up to 1 Grad(SiO_2)***.
- Increase in the off-state leakage is limited even at 1 Grad(SiO_2), indicating a modest charge trapping in STI.
- ΔV_{th} of I/O nMOSFETs shows a negligible dependency on the transistor geometry, indicating the charge trapping in gate oxide.

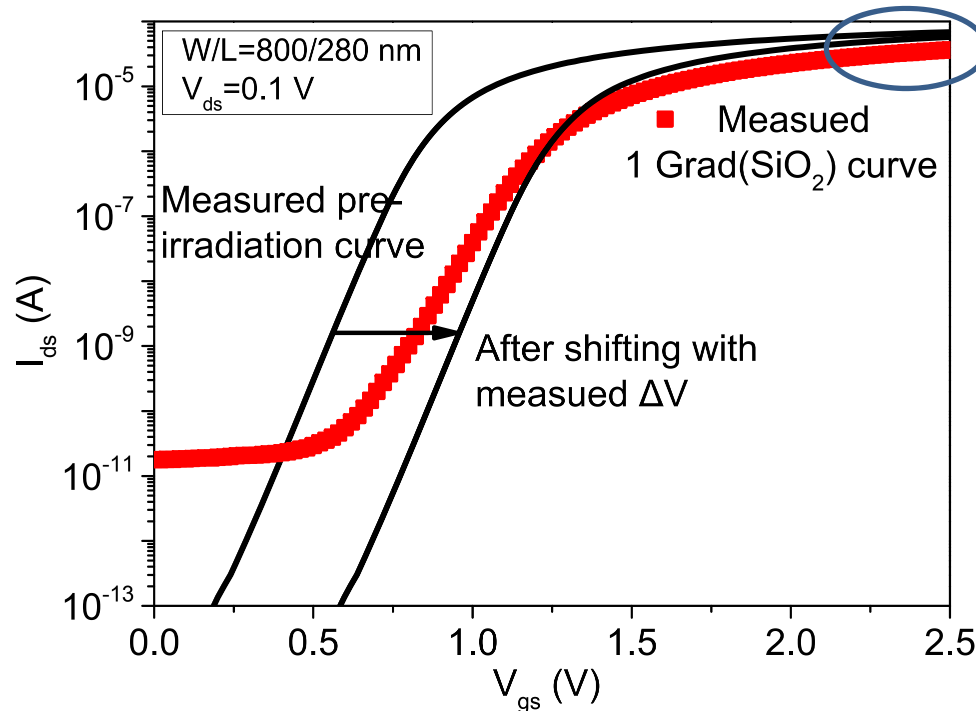
Results and discussion: I/O nMOSFET

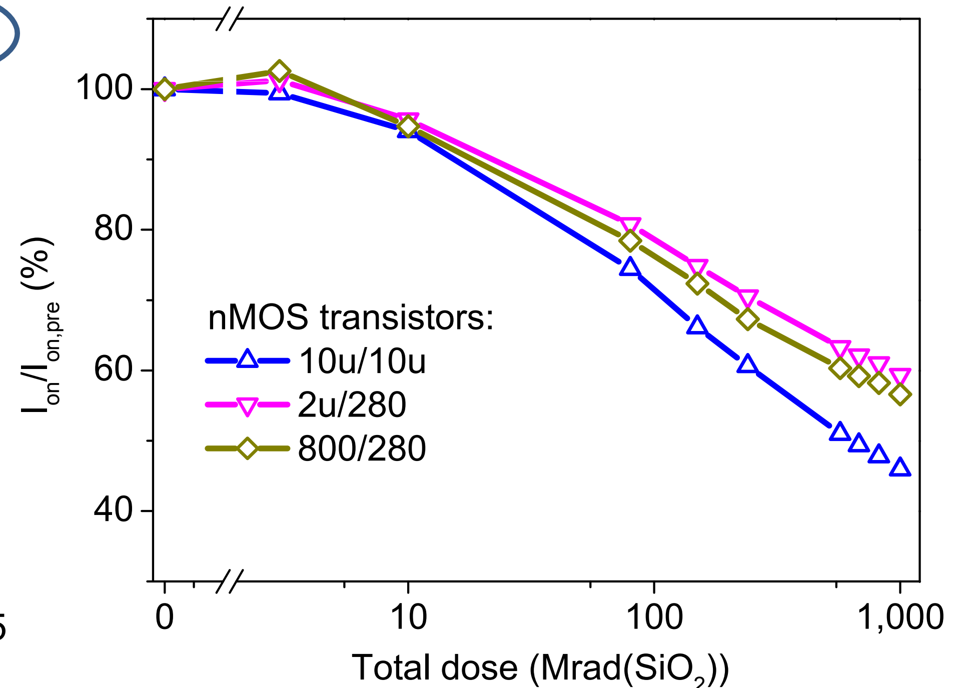




- ***Evolution of Subthreshold-swing (SS) and the relative threshold voltage shift due to the interface traps in gate oxide (ΔV_{it}) of*** I/O nMOSFETs and core nMOSFET (120/60 nm) ***with TID up to 1 Grad(SiO_2)***.
- The charge trapping in gate oxide is comparable to explain the measured degradation in ΔV_{th} (300 v.s. 400 mV).

Results and discussion: I/O nMOSFET

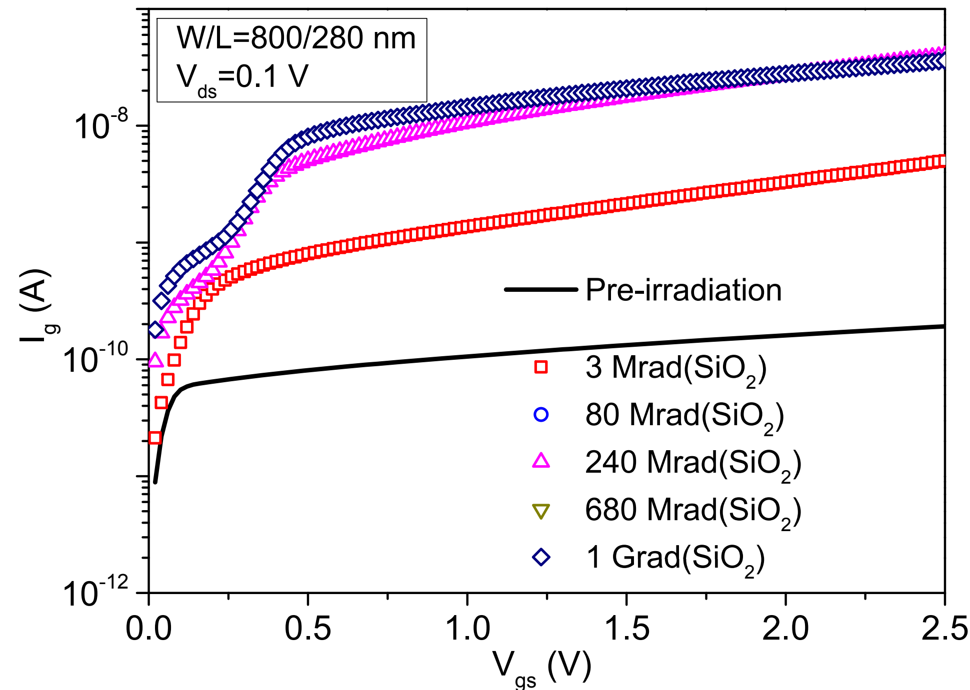




- Through shifting the measured I-V curve with ΔV_{th}, the resulting on-state drain current becomes about 80% of the initial value at 1 Grad(SiO_2).
- The measured on-state drain current is less than 60% at 1 Grad.

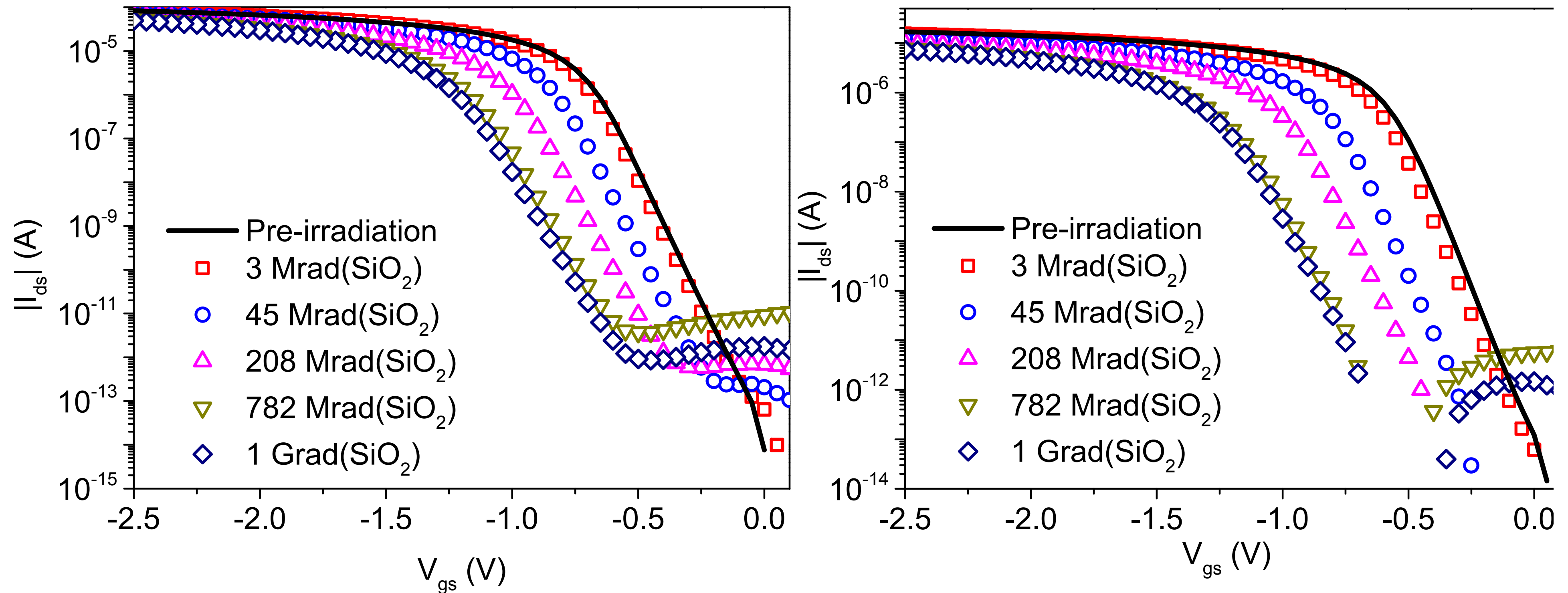
How to explain the severe loss of drain current?

Results and discussion: I/O nMOSFET



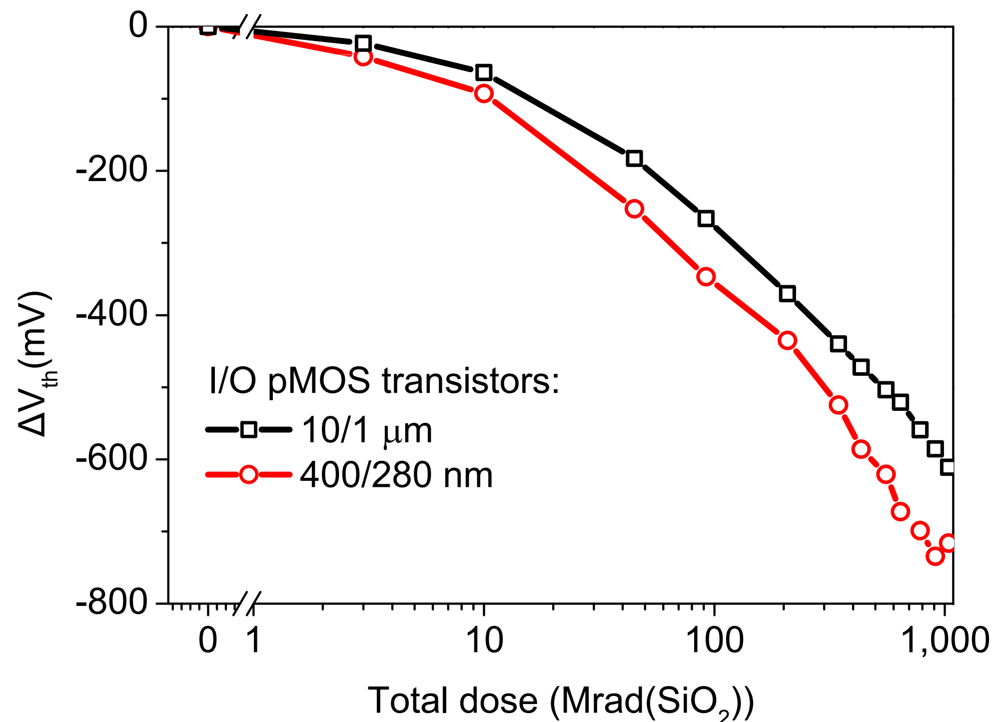
- Gate leakage increase was observed during irradiation, indicating the soft breakdown of gate oxide after exposure to Grad dose.

Results and discussion: I/O pMOSFET



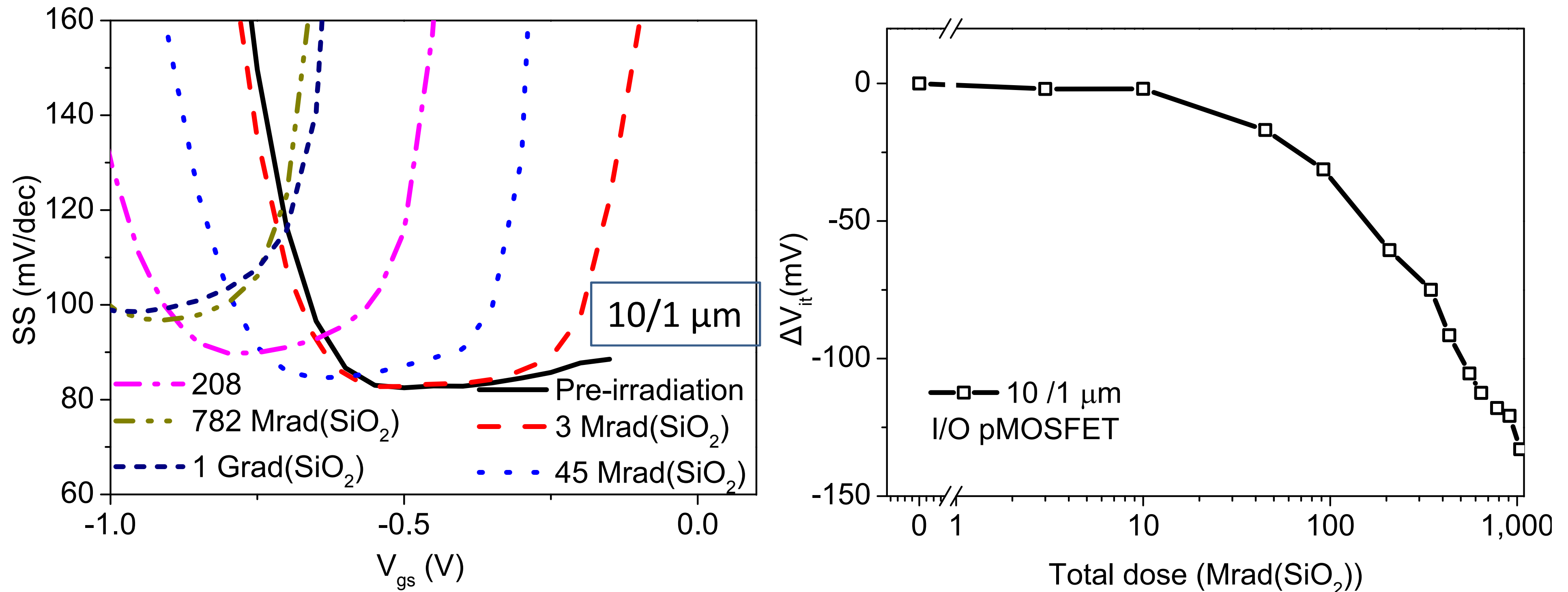
- ***I_{ds}-V_{gs} curves*** of I/O pMOSFETs (10/1 µm) and (400/280 nm) ***at doses up to 1 Grad(SiO_2)***.

Results and discussion: I/O pMOSFET



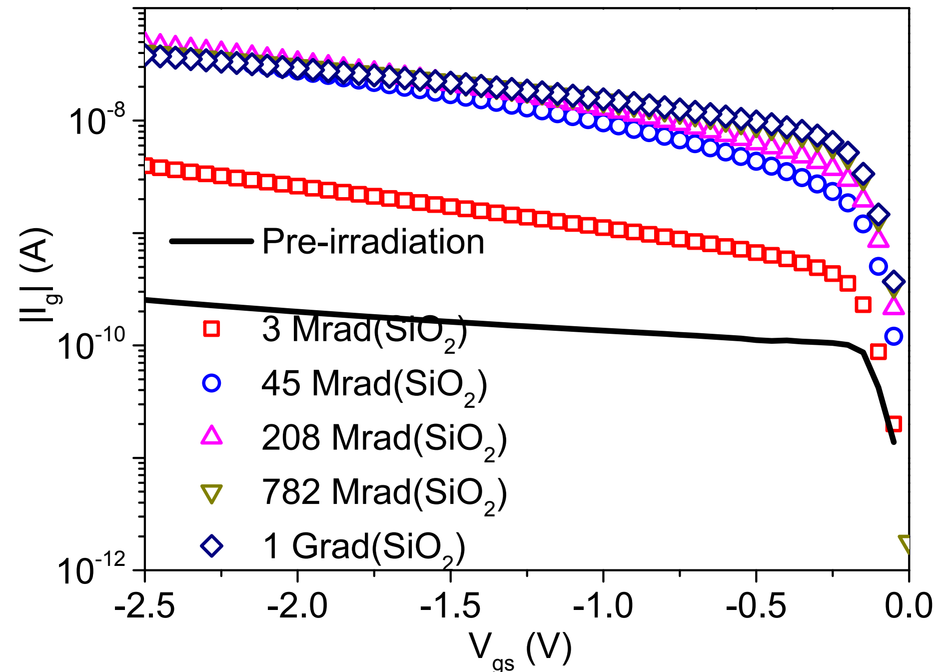
- For pMOS I/O transistors, threshold voltage shift is stronger than that of nMOSFETs.
- A dependency of V_{th} shift on the transistor geometry was observed, indicating the contribution of charge trapping in STI.

Results and discussion: I/O pMOSFET



- An increase in SS was also observed for pMOS I/O transistors, but weaker than that of nMOS transistors.
- Thus, the accumulation of interface traps in gate oxide is not strong enough to explain the characteristics degradation of pMOS transistors (130 v.s. 600 mV).

Results and discussion: I/O pMOSFET



- Similar to nMOS I/O transistors, for pMOSFETs, increase in gate leakage can be observed, indicating the soft breakdown of gate oxide after exposure to Grad dose.

Conclusion

- TID effects in 65 nm CMOS I/O transistors were investigated through 10 keV X-ray exposure;
- Charge trapping in STI contributes to the characteristics degradation for both nMOS and pMOS transistors;
- Charge trapping in the gate oxide, especially the accumulation of interface traps is proved to be existed;
- From the quantitative point of view, apart from the charge trapping in STI and gate oxide, there is the third contribution, which is attributed to the soft breakdown of gate oxide after exposure to Grad dose.

Thanks